TMC2242A/TMC2242B

Digital Half-Band Interpolating/Decimating Filter

12-bit In/16-bit Out, 60 MHz

Features

- TMC2242A and TMC2242B are pin-compatible with TMC2242
- User selectable interpolate gain, -6 dB or 0 dB (2242B)
- 30, 40 and 60 MHz speed grades
- User selectable 2:1 decimation, 1:2 interpolation, and equal-rate filter modes
- Passband ripple < ±0.01 dB
- Stopband rejection 59.4 dB from 0.28 to 0.50 x f_S
- Cascading two TMC2242A or TMC2242B meets CCIR 601 low-pass filter requirement
- Dedicated 12-bit 2's complement input data port and 16-bit output data port with user-selectable rounding from 9 to 16 bits
- Two's complement or offset binary output format
- Built-in limiter prevents overflow
- Single +5 Volt power supply operation
- Small 44-Lead PLCC and 44-Lead MQFP

Applications

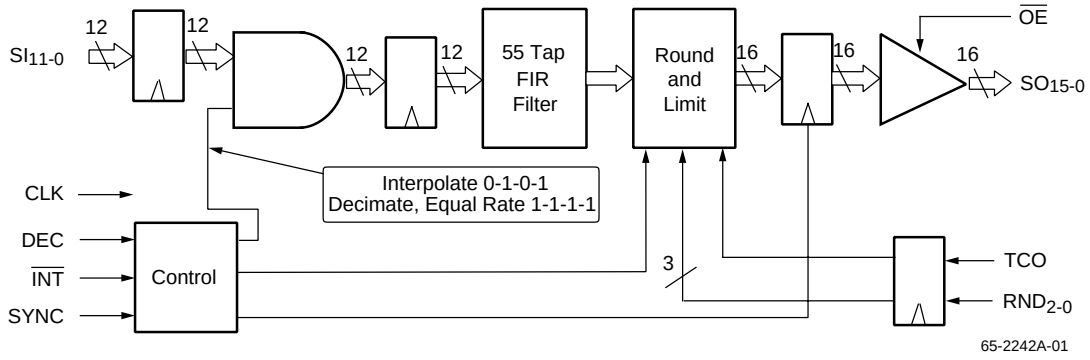
- Low-cost video filtering
- Chrominance bandwidth limiter
- Simple, inexpensive video D/A post-filters
- Reduced cost and complexity for A/D anti-aliasing filters
- High-performance digital low-pass filters
- Digital waveform reconstruction post-filtering
- Telecommunications
- Direct digital synthesis
- Radar

Description

The TMC2242A and TMC2242B are fixed-coefficient linear-phase half-band (low-pass) digital filters. They can be used to halve or double the sampling rate of a digital signal. When used as a decimating post-filter with a double-speed oversampling A/D converter, they greatly reduce the cost and complexity of anti-aliasing filters required ahead of the A/D converter. When used as an interpolating pre-filter with a double-speed oversampling D/A converter, the TMC2242A and TMC2242B significantly reduce the design complexity and production cost of reconstruction filters used on D/A outputs.

The TMC2242A and TMC2242B user selects the mode of operation (decimate, interpolate, or equal-rate) and rounding. The TMC2242A and TMC2242B accept 12-bit 2's complement data at up to 60 MHz and output saturated (overflow-protected) 2's complement or offset binary data rounded to from 9 to 16 bits. Within the speed grade I/O limit, the output sample rate may be 1/2, 1, or 2 times the input sample rate.

Block Diagram



Description (continued)

The filter response is flat to within ±0.01 dB from 0.00 to 0.22 x f_S, with stopband attenuation greater than 59.4 dB from 0.28 x f_S to the Nyquist frequency. The response is 6 dB down at 0.25 x f_S. Symmetric-coefficient filters such as the TMC2242A and TMC2242B have linear phase response. Full compliance with the CCIR-601 standard of 12 dB attenuation at 0.25 x f_S is achieved by cascading two parts.

The TMC2242A and TMC2242B are fabricated on an advanced submicron CMOS process. They are available in a 44-lead J-lead PLCC package. Performance is guaranteed from 0°C to 70°C.

Functional Description

The TMC2242A and TMC2242B implement a fixed-coefficient linear-phase Finite Impulse Response (FIR) filter of 55 effective taps, with special rate-matching input and output structures to facilitate 2:1 decimation and 1:2 interpolation. The faster of either the input or output registers will operate at the guaranteed maximum clock rate (speed grade). The total internal pipeline latency from the input of an impulse to the corresponding output peak (digital group delay) is 34 cycles; the 55-value output response begins after 7 clock cycles and ends after 61 cycles.

To perform interpolation, the chip slows the effective input register clock rate to half the output rate. It internally inserts zeroes between the incoming data samples to "pad" the input data rate to match the output rate.

To perform decimation, the chip sets the output register clock rate to half of the input rate. One output is then obtained for every two inputs.

For interpolation, the user should bring SYNC HIGH for at least one clock cycle, returning it LOW with the first desired input data value. When interpolating, the chip will then continue to accept a new data input on each alternate rising edge of the clock. When decimating, the chip will present one output value for every two clock cycles. The user may leave SYNC LOW or toggle it once per rising clock edge, with equivalent performance.

The output data format is two's complement if TCO is HIGH, inverted offset binary if LOW. The user can tailor the output data word width to his/her system requirements using the Rounding control. As shown in Table 4, the output is half-LSB rounded to the resolution selected by the value of $RND_{2\text{-}0}$. The asynchronous three-state output enable control simplifies connection to a data bus with other drivers.

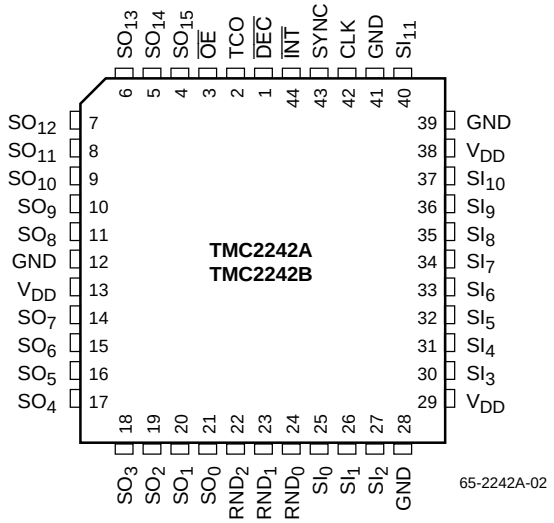
Table 1. Operating Modes

$\overline{DEC}$	$\overline{INT}$	TMC2242A	TMC2242B
0	0	Equal Rate	Interpolate (0 dB)
0	1	Decimate	Decimate
1	0	Interpolate (-6 dB)	Interpolate (-6 dB)[1]
1	1	Equal Rate	Equal Rate

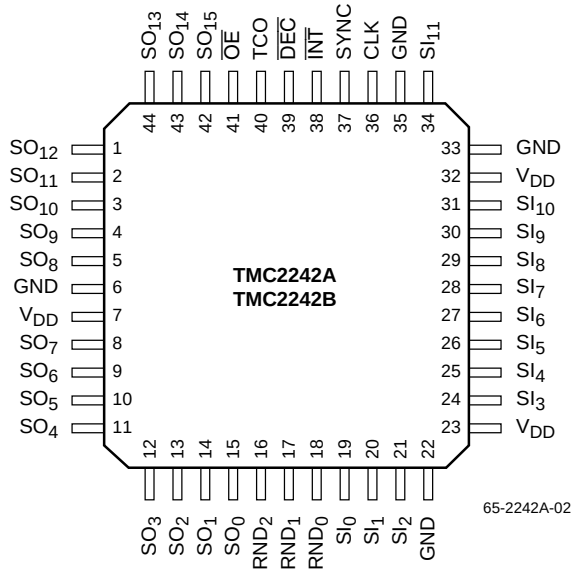
Note:

1. With 15-bit overflow protection. All other modes on both parts limit to 16 bits.

Pin Assignments



44 Lead PLCC



44 Lead MQFP

Pin Descriptions

Pin Name	Pin Number PLCC	Pin Number MQFP	Pin Function Description
Timing Controls			
$\overline{INT}$	44	38	**Interpolate.** When $\overline{INT}$ is LOW and $\overline{DEC}$ is HIGH, the input data register runs at 1/2 the CLK rate and zeros are inserted in the data stream between valid input values, reducing gain by 6dB. The TMC2242A and TMC2242B interpolate and output results at the full CLK rate.
$\overline{DEC}$	1	39	**Decimate.** When $\overline{DEC}$ is LOW and $\overline{INT}$ is HIGH, the input data register runs at the full CLK rate. In this mode, the TMC2242A and TMC2242B decimate and output results at 1/2 the CLK rate. When $\overline{INT}$ = $\overline{DEC}$, the TMC2242A is in equal rate mode. When both $\overline{INT}$ and $\overline{DEC}$ are HIGH, the TMC2242B is likewise in equal-rate mode, but when both $\overline{INT}$ and $\overline{DEC}$ are LOW, the TMC2242B interpolates with unity gain. In equal-rate mode, the input and output sample rates equal the chip clock rate.
SYNC	43	37	**Synchronization.** Incoming data are synchronized by holding SYNC HIGH on CLK N–1 and LOW on CLK N when the first input data word is present on SI_{11-0}. If $\overline{DEC}$ = $\overline{INT}$=1 (equal rate mode), SYNC is inactive. SYNC may be held LOW until resynchronization is desired, or it may be toggled at 1/2 the CLK rate.
CLK	42	36	**Clock.** The TMC2242A and TMC2242B operate from a single master clock. All internal registers, except the output register in decimation mode, are strobed on the rising edge of CLK. All timing parameters are referenced to the rising edge of CLK.
Data Inputs			
SI_{11-0}	40, 37-30, 27-25	34, 31-24, 21-19	**Input Data Port.** A 12-bit 2's-complement input word is registered by the rising edge of CLK. In Interpolate Mode, SI_{11-0} is registered on every other CLK (synchronized by SYNC). SI_{11} is the MSB.
Data Outputs			
SO_{15-0}	4-11, 14-21	42-44, 1-5, 8-15	**Output Data Port.** A 16-bit 2's-complement output result is available after the rising edge of CLK. In Decimate Mode, SO_{15-0} is registered on every other CLK (synchronized by SYNC). SO_{15-0} is rounded according to the state of RND_{2-0}. SO_{15} is the MSB. The limiter circuitry ensures that for internal overflow, a valid full-scale output (7FFF or 8000) will be generated. With the TMC2242B in interpolate mode with -6dB gain, limits are 3FFF and C000 (TCO=1).
Output Controls			
$\overline{OE}$	3	41	**Output Enable.** When LOW, SO_{15-0} are enabled. When HIGH, SO_{15-0} are in a high-impedance state. $\overline{OE}$ is asynchronous with respect to CLK.
TCO	2	40	**Output Format.** When TCO is HIGH, output data are in signed 2's-complement format. When LOW, the output is inverted offset binary.
RND_{2-0}	22-24	16-18	**Rounding Select.** These inputs set the position of the effective LSB of the output result. Outputs below the rounding bit are zeroed (Table 4).
Power			
V_{DD}	13,29, 38	7, 23, 32	**Supply Voltage.** +5 Volt power inputs. These should come from the same power source and be decoupled to GND.
GND	12,28, 39,41	6, 22, 33, 35	**Ground.** Ground inputs should be connected to the system digital ground plane.

Absolute Maximum Ratings

(beyond which the device may be damaged)[1]

Parameter	Conditions	Min	Max	Units
Supply Voltage		-0.5	7.0	V
Input Voltage		-0.5	V_{DD} + 0.5	V
Output Applied Voltage[2]		-0.5	V_{DD} + 0.5	V
Externally Forced Current[3,4]		-3.0	+6.0	mA
Short Circuit Duration	Single output in HIGH state to ground		1	sec
Operating Temperature (Case)		-20	110	°C
Junction Temperature			140	°C
Lead Soldering Temperature	10 seconds		300	°C
Storage Temperature		-65	150	°C

Notes:

1. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Conditions	Min	Nom	Max	Units
V_{DD}	Power Supply Voltage		4.75	5.0	5.25	V
f_{CLK}	Clock frequency	TMC2242A, B			30	MHz
		TMC2242A-1,B-1			40	MHz
		TMC2242A-2,B-2			60	MHz
t_{PWH}	CLK pulse width, HIGH		6			ns
t_{PWL}	CLK pulse width, LOW		6			ns
t_S	Input Data Set-up Time		6			ns
t_H	Input Data Hold Time		1			ns
V_{IH}	Input Voltage, Logic HIGH		2.0			V
V_{IL}	Input Voltage, Logic LOW				0.8	V
I_{OH}	Output Current, Logic HIGH				-2.0	mA
I_{OL}	Output Current, Logic LOW				4.0	mA
T_A	Ambient Temperature, Still Air		0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I_{DD}	Total Power Supply Current	V_{DD} = Max, C_{LOAD}=25pF, f_{CLK}=Max				
		TMC2242A,B			150	mA
		TMC2242A-1,B-1			195	mA
		TMC2242A-2,B-2			290	mA
I_{DDU}	Power Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH, f_{CLK}=Max				
		TMC2242A,B			120	mA
		TMC2242A-1,B-1			155	mA
		TMC2242A-2,B-2			230	mA
I_{DDQ}	Power Supply Current, Quiescent	V_{DD} = Max, CLK = LOW			5	mA
C_{PIN}	I/O Pin Capacitance			5		pF
I_{IH}	Input Current, HIGH	V_{DD} = Max, V_{IN} = V_{DD}			±10	µA
I_{IL}	Input Current, LOW	V_{DD} = Max, V_{IN} = 0 V			±10	µA
I_{OZH}	Leakage Current, HIGH	$\overline{OE}$ = HIGH, V_{OUT} = V_{DD}			±10	µA
I_{OZL}	Leakage Current, LOW	$\overline{OE}$ = HIGH, V_{OUT} = 0 V			±10	µA
I_{OS}	Short-Circuit Current	V_{DD} = Max, Output = HIGH, one pin to ground, one second duration max.	-20		-80	mA
V_{OH}	Output Voltage, HIGH	SO15-0, I_{OH} = Max	2.4			V
V_{OL}	Output Voltage, LOW	SO15-0, I_{OL} = Max			0.4	V

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t_{DO}	Output Delay Time	C_{LOAD} = 25 pF			15	ns
t_{HO}	Output Hold Time	C_{LOAD} = 25 pF	2.5			ns
t_{ENA}	Output Enable Time	C_{LOAD} = 0 pF			12	ns
t_{DIS}	Output Disable Time	C_{LOAD} = 0 pF			12	ns

Table 2. Impulse Response

Hex	Decimal Equivalent	
FFF2	-0.000875473	start & end
0000	0.0	
0017	0.001390457	
0000	0.0	
FFDB	-0.002265930	
0000	0.0	
0039	0.003501892	
0000	0.0	
FFA8	-0.006366836	
0000	0.0	
007D	0.007621765	
0000	0.0	
FF51	-0.01071167	
0000	0.0	
00F3	0.01483154	
0000	0.0	
FEB5	-0.02018738	
0000	0.0	
01CA	0.02796364	
0000	0.0	
FD79	-0.03949928	
0000	0.0	
03CD	0.05937767	
0000	0.0	
F95E	-0.1036148	
0000	0.0	
145B	0.3180542	
2010	0.5009766	center

Input = 0, 0, 0, …, 0, 400h, 0, …, 0, 0, 0
$\overline{INT}$ = $\overline{DEC}$ = TCO = 1

Table 3. Step Response

Input	$\overline{INT}$=1 $\overline{DEC}$=1 TCO=0	$\overline{INT}$=1 $\overline{DEC}$=1 TCO=1	$\overline{INT}$=0 $\overline{DEC}$=1 TCO=1	$\overline{INT}$=1 $\overline{DEC}$=0 TCO=1	
400	xx	xx	xx	xx	
400 ... 400	xx ... 3FE7	xx ... 4018	xx ... 2008	xx ... 4018	DC Gain
400 000 ... 000	3FE7 3FE7 ... 3B90	4018 4018 ... 446F	2010 2008 ... 245F	4018 4018 ... 446F	Max Ringing
000	3B90	446F	2010	446F	
000	4FEB	3014	1004	1004	
000	6FFB	1004	0000	1004	
000 ... 000	8456 ... 7FFF	FBA9 ... 0000	FBA9 ... 0000	FBA9 ... 0000	Min Ringing Steady State

Table 4a. Input Data Format

-2^0	2^{-1}	2^{-2}	…	2^{-10}	2^{-11}

Table 4b. Output Data Formats and Bit Weighting for TCO = 1

Interpolation Mode (TMC2242A and TMC2242B when $\overline{INT}$ = 0 and $\overline{DEC}$ = 1)

-2^{1}	2^{0}	2^{-1}	…	2^{6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}

Decimation, Equal Rate Modes (and TMC2242B in unity gain interpolate mode with $\overline{INT}$ = $\overline{DEC}$ = 0)

-2^{0}	2^{-1}	2^{-2}	…	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}

Rounded LSBs as a function of RND_{2-0}

												RND_{2-0}
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5}	SO_{4}	SO_{3}	SO_{2}	SO_{1}	SO_{0r}	000
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5}	SO_{4}	SO_{3}	SO_{2}	SO_{1r}	0	001
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5}	SO_{4}	SO_{3}	SO_{2r}	0	0	010
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5}	SO_{4}	SO_{3r}	0	0	0	011
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5}	SO_{4r}	0	0	0	0	100
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6}	SO_{5r}	0	0	0	0	0	101
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7}	SO_{6r}	0	0	0	0	0	0	110
SO_{15}	SO_{14}	SO_{13}	…	SO_{8}	SO_{7r}	0	0	0	0	0	0	0	111

Notes:

1. A leading minus sign denotes the two's complement sign bit.
2. When TCO=0, the most significant bit of the output is positive instead of negative.
3. In all operating modes except $\overline{INT}$ = 0 and $\overline{DEC}$ = 1, the gain is approximately unity. When $\overline{INT}$ = 0 and $\overline{DEC}$ = 1, the output gain is -6 dB.
4. The "r" indicates that the trailing significant output bit has been rounded to the nearest 1/2 LSB. (Internally, the chip adds 1 to the next lower bit, to allow the user to obtain a properly rounded output)

Table 5. TMC2242A Steady-State Output Values and Limiter Triggers (L) versus Input Data

Input	$\overline{INT}$ = 1 or $\overline{DEC}$ = 0		$\overline{INT}$ = 0 and $\overline{DEC}$ = 1		Interpretation
	TCO = 0	TCO = 1	TCO = 0	TCO = 1	
7FF	0000 (L)	7FFF (L)	3FF7 / 3FE7	4008 / 4018	+ full-scale
400	3FE7	4018	5FF7 / 5FEF	2008 / 2010	+1/2 scale
001	7FEF	0010	7FF7	0008	+1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	8007	FFF8	-1 LSB
C00	C017	BFE8	A007 / A00F	DFF8 / DFF0	-1/2 scale
801	FFFF (L)	8000 (L)	C007 / C017	BFF8 / BFE8	- full-scale

Table 6. TMC2242B Steady-State Output Values and Limiter Triggers (L) versus Input Data

Interpolation Modes

Input	$\overline{INT}$ = 0 and $\overline{DEC}$ = 0		$\overline{INT}$ = 0 and $\overline{DEC}$ = 1		Interpretation
	TCO = 0	TCO = 1	TCO = 0	TCO = 1	
7FF	0000 (L)	7FFF (L)	4000 (L)	3FFF (L)	+ full-scale
400	3FEF / 3FDF	4010 / 4020	5FF7 / 5FEF	2008 / 2010	+1/2 scale
001	7FEF	0010	7FF7	0008	+1 LSB
000	7FFF	0000	7FFF	0000	Zero
FFF	800F	FFF0	8007	FFF8	-1 LSB
C00	C00F / C01F	BFF0 / BFE0	A007 / A00F	DFF8 / DFF0	-1/2 scale
801	FFFF	8000 (L)	BFFF	C000 (L)	- full-scale

Decimation and Equal-Rate Modes

Input	$\overline{INT}$ = 1		Interpretation
	TCO = 0	TCO = 1	
7FF	0000 (L)	7FFF (L)	+ full-scale
400	3FE7	4018	+1/2 scale
001	7FEF	0010	+1 LSB
000	7FFF	0000	Zero
FFF	800F	FFF0	-1 LSB
C00	C017	BFE8	-1/2 scale
801	FFFF (L)	8000 (L)	- full-scale

Performance Curves

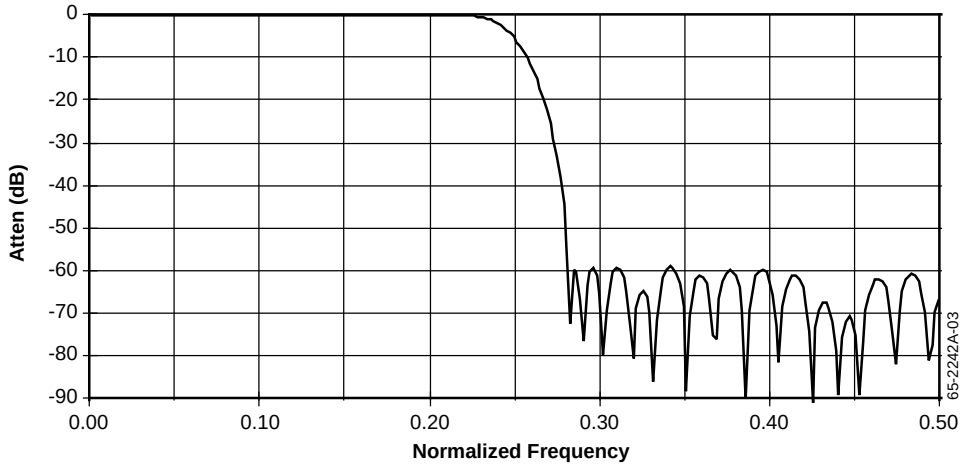


Figure 1. Frequency Response

Performance Curves (continued)

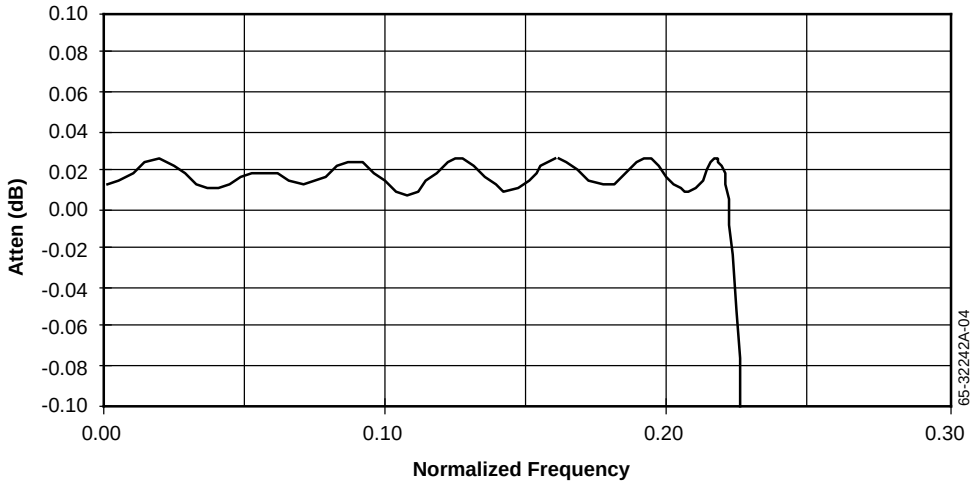


Figure 2. Passband Ripple Response

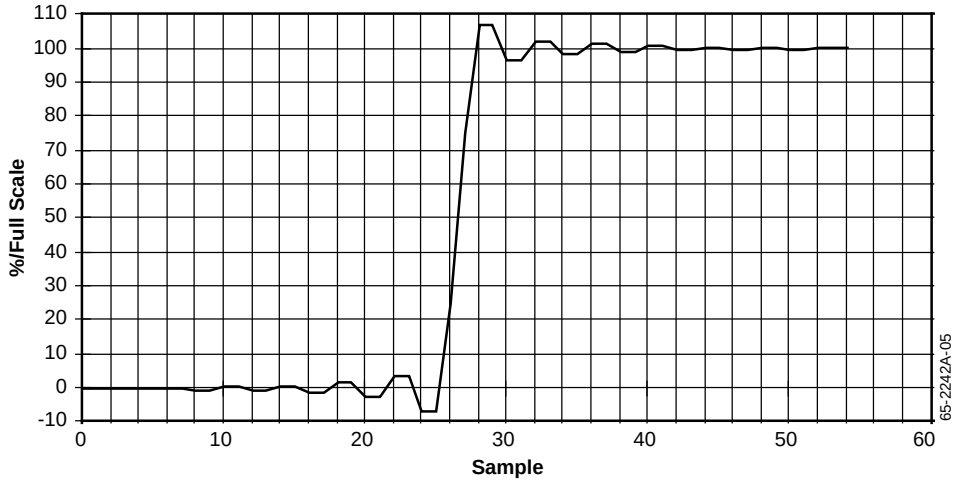


Figure 3. Step Response

Equivalent Circuits

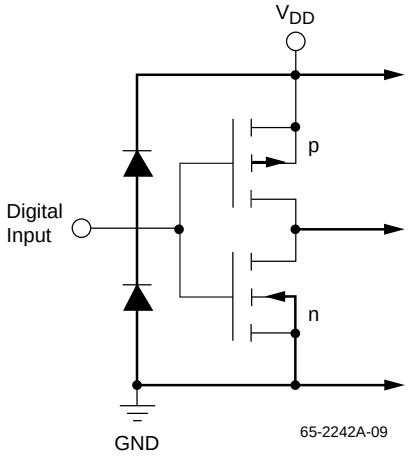


Figure 7. Equivalent Digital Input Circuit

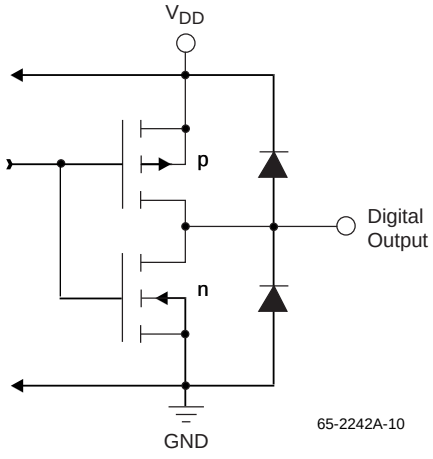
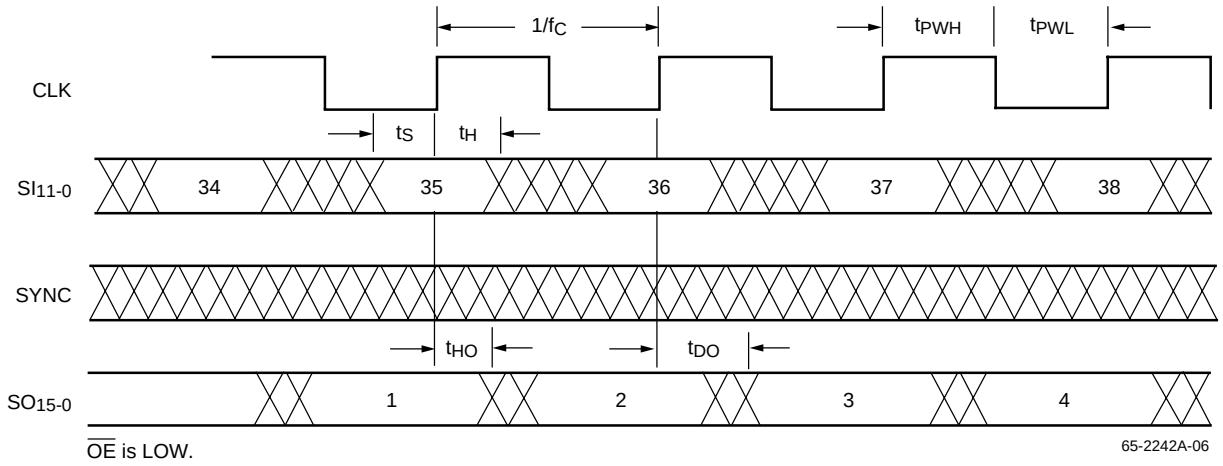


Figure 8. Equivalent Digital Output Circuit

Timing Diagrams



Note: Values at SO_{15-0} are impulse response centers (peaks) corresponding to same-numbered inputs.

Figure 4. Equal Rate Mode

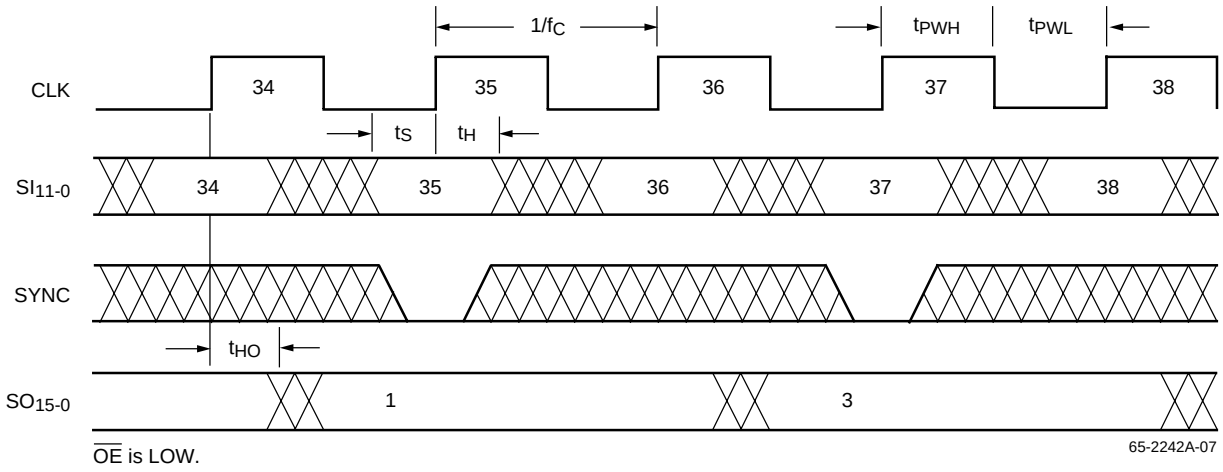


Figure 5. Decimate Mode

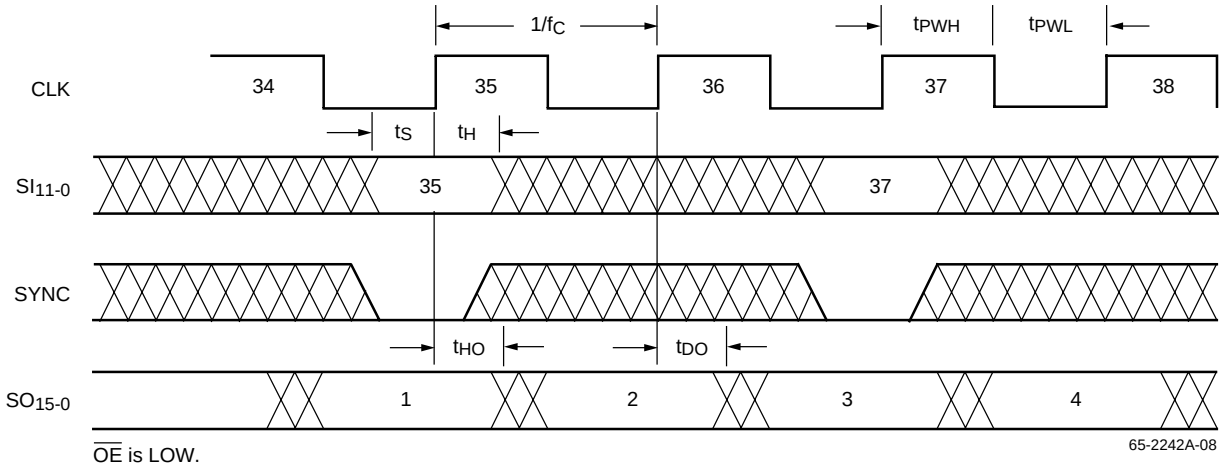


Figure 6. Interpolate Mode

Timing Diagrams (continued)

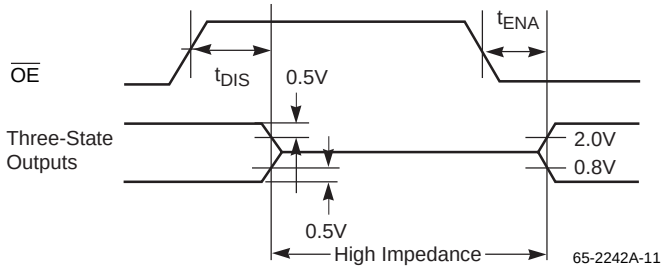


Figure 9. Threshold Levels for Three State Measurements

Applications Discussion

The TMC2242A and TMC2242B are well-suited for filtering digitized composite NTSC or PAL video. In Figure 10, the TMC1175A 8-bit video A/D converter outputs, D_{7-0}, are connected to the TMC2242B inputs, SI_{11-4}, respectively (grounding SI_{3-0}). The RND_{2-0} controls are set to 111 for a 9-bit rounded decimated output on SO_{15-7}.

In Figure 11, the TMC2242B drives a fast D/A converter to reconstruct analog composite video. The TMC3003 10-bit digital-to-analog converter inputs, D_{9-0} are connected to the TMC2242B outputs SO_{15-6}, respectively. The TMC2242B RND_{2-0} controls are set to 110 for rounded 10-bit interpolation operation.

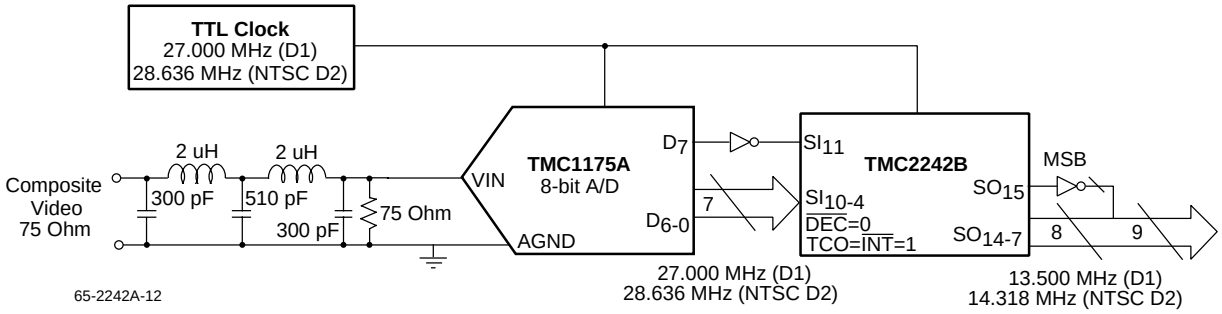
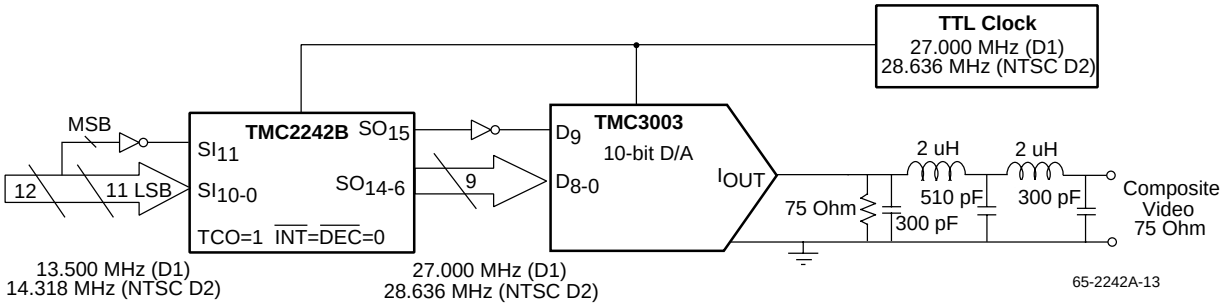


Figure 10. Decimating Oversampled Video With a Low Cost 8-bit A/D



Note: Data buses are unsigned binarys; TMC2242 input is two's complement.

Figure 11. Interpolating Digital Video Signals before Reconstruction

Notes:

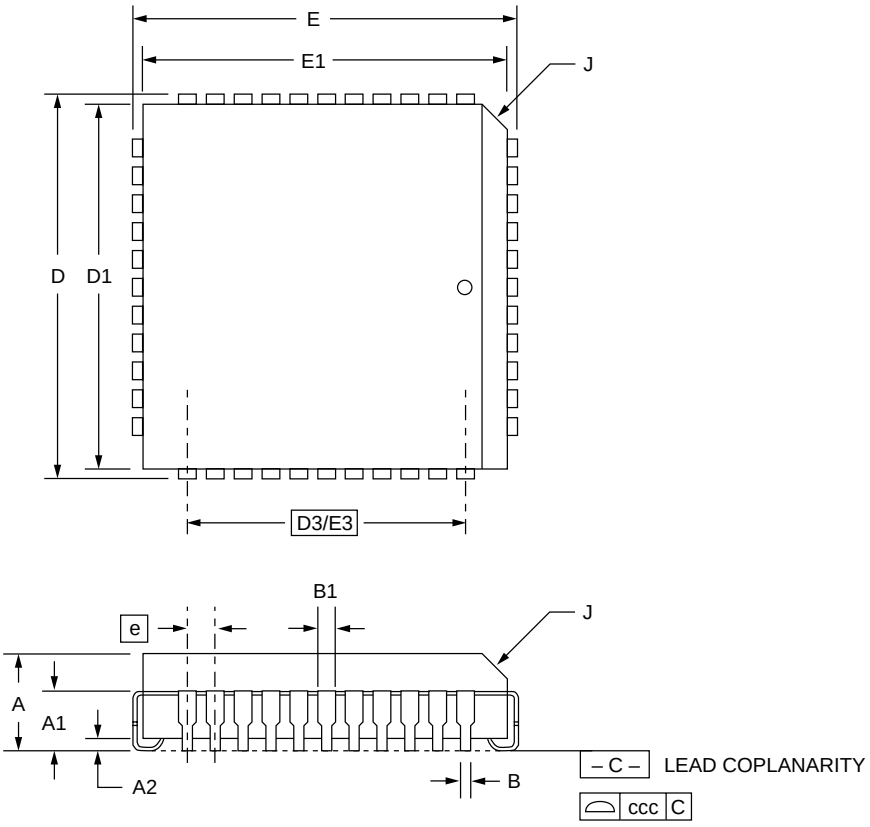
Notes:

Mechanical Dimensions – 44-Pin PLCC Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.685	.695	17.40	17.65	
D1/E1	.650	.656	16.51	16.66	3
D3/E3	.500 BSC		12.7 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.056	1.07	1.42	2
ND/NE	11		11		
N	44		44		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982
2. Corner and edge chamfer (J) = 45°
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm)

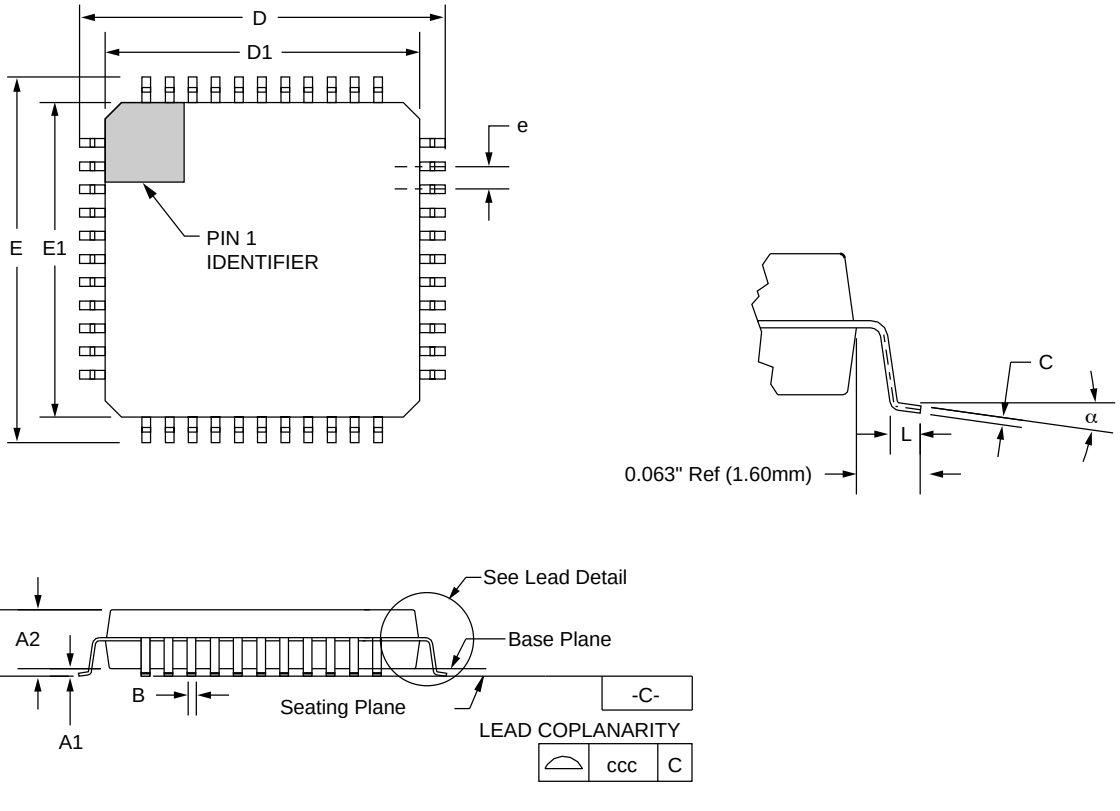


Mechanical Dimensions – 44-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.077	.093	1.95	2.35	
A1	.000	.010	.00	.25	
A2	.077	.083	1.95	2.11	
B	.012	.018	.30	.46	7
C	.005	.009	.13	.23	
D/E	.510	.530	12.95	13.45	
D1/E1	.390	.398	9.90	10.10	2
e	.032 BSC		.81 BSC		
L	.026	.037	.66	.94	6
N	44		44		4
ND	11		11		5
α	0°	7°	0°	7°	
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Dimensions "D1" and "E1" do not include mold protrusion.
3. Pin 1 identifier is optional.
4. Dimension N: number of terminals.
5. Dimension ND: Number of terminals per package edge.
6. "L" is the length of terminal for soldering to a substrate.
7. "B" includes lead finish thickness.



44 Lead Metric Quad Flat Pack (MQFP) – 3.2mm Footprint Rev 1.0 11/28/95

Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2242AR2C	0°C to 70°C	30 MHz	Commercial	44-Lead PLCC	2242AR2C
TMC2242AR2C1	0°C to 70°C	40 MHz	Commercial	44-Lead PLCC	2242AR2C1
TMC2242AR2C2	0°C to 70°C	60 MHz	Commercial	44-Lead PLCC	2242AR2C2
TMC2242BR2C	0°C to 70°C	30 MHz	Commercial	44-Lead PLCC	2242BR2C
TMC2242BR2C1	0°C to 70°C	40 MHz	Commercial	44-Lead PLCC	2242BR2C1
TMC2242BR2C2	0°C to 70°C	60 MHz	Commercial	44-Lead PLCC	2242BR2C2
TMC2242AKTC	0°C to 70°C	30 MHz	Commercial	44-Lead MQFP	2242AKTC
TMC2242AKTC1	0°C to 70°C	40 MHz	Commercial	44-Lead MQFP	2242AKTC1
TMC2242AKTC2	0°C to 70°C	60 MHz	Commercial	44-Lead MQFP	2242AKTC2
TMC2242BKTC	0°C to 70°C	30 MHz	Commercial	44-Lead MQFP	2242BKTC
TMC2242BKTC1	0°C to 70°C	40 MHz	Commercial	44-Lead MQFP	2242BKTC1
TMC2242BKTC2	0°C to 70°C	60 MHz	Commercial	44-Lead MQFP	2242BKTC2