

TMC2272A

Digital Colorspace Converter

36 Bit Color, 50 MHz

Features

- 50 MHz (20ns) pipelined throughput
- 3 Simultaneous 12-bit input and output channels (64 Giga { 2^{36} } colors)
- Two's complement inputs and outputs
- Overflow headroom available in lower resolution
- 10-bit user-defined coefficients
- TTL compatible input and output signals
- Full precision internal calculation
- Output rounding
- On-board coefficient memory
- Submicron CMOS process

Applications

- Translation between component color standards (RGB, YIQ, YUV, etc.)
- Broadcast composite color encoding and decoding (all standards)
- Broadcast composite color standards conversion and transcoding
- Camera tube and monitor phosphor colorimetry correction
- White balancing and color-temperature conversion
- Image capture, processing and storage
- Color matching between systems, cameras and monitors
- Three-dimensional perspective translation

Description

A 50-MHz, three-channel, 36 bit (three 12-bit components) colorspace converter and color corrector, the TMC2272A uses 9 parallel multipliers to process high-resolution imagery in real time.

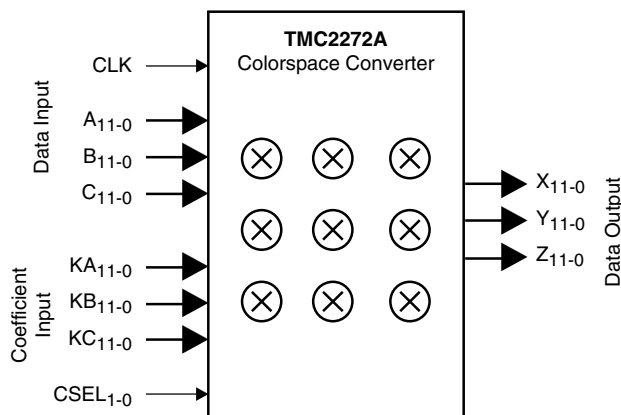
The TMC2272A also operates at any slower clock rate and with any smaller data path width, allowing it to handle all broadcast and consumer camera, frame-grabber, encoder/decoder, recorder and monitor applications as well as most electronic imaging applications.

A complete set of three 12-bit samples is processed on every clock cycle, with a five-cycle pipeline latency. Full 23-bit (for each of three components) internal precision is provided

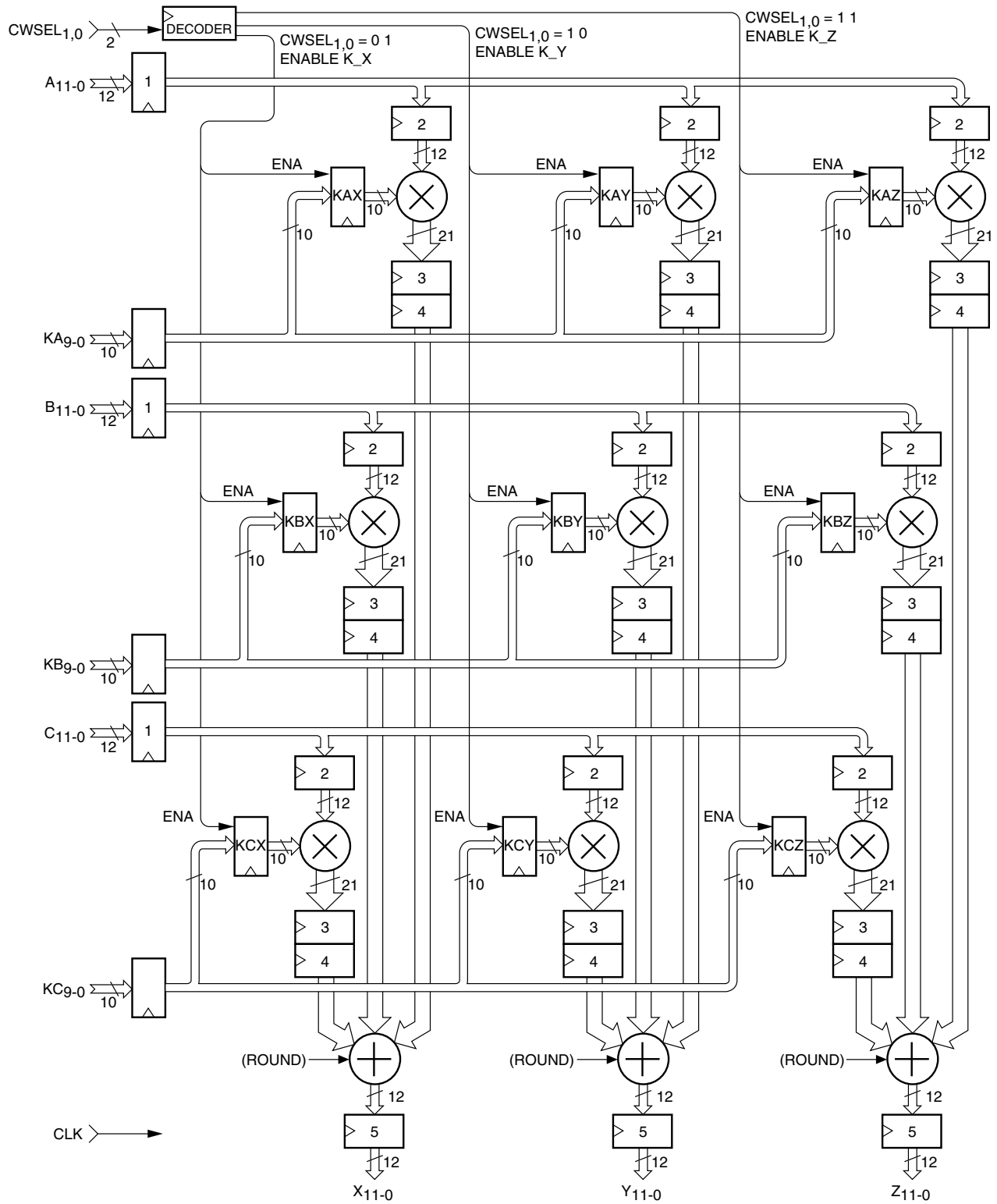
with 10-bit user-defined coefficients. The coefficients may be varied dynamically, with three new coefficients loaded every clock cycle. (The full set of nine can be replaced in three clock cycles.) Rounding to 12 bits per component is performed only at the final output. This allows full accuracy with correct rounding and overflow headroom for applications that require less than 12 bits per component.

The TMC2272A is fabricated in a submicron CMOS process and performance is guaranteed over the full operating temperature range. It is available in a 120-pin Plastic Pin Grid Array (PPGA) package, 120-pin Ceramic Pin Grid Array (CPGA), 120-pin MQFP to PGA package, and 120-pin Plastic Quad FlatPack (PQFP) in three speed grades.

Logic Symbol



Block Diagram



Functional Description

The TMC2272A is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product). With a 50MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A₁₁₋₀, B₁₁₋₀, C₁₁₋₀) accept 12-bit two's complement integer data, which is also the format for the output ports (X₁₁₋₀, Y₁₁₋₀, Z₁₁₋₀). Other format and path width options are discussed in the numeric format and overflow section. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. Table 2 details the bit weighting.

Full precision is maintained throughout the TMC2272A. Each output is accurately rounded to 12 bits from the 23 bits entering the final adder.

Signal Definitions

A(n), B(n), C(n)

Indicates the data word presented to that input port during the specified clock rising edge (n). Applies to input ports A₁₁₋₀, B₁₁₋₀, and C₁₁₋₀.

KAX(n) thru KCZ(n)

Indicates coefficient value stored in the specified one of the nine onboard coefficient registers KAX through KCZ, input during or before the specified clock rising edge (n).

X(n), Y(n), Z(n)

Indicates data available at that output port t_{DO} after the specified clock rising edge (n). Applies to output ports X₁₁₋₀, Y₁₁₋₀, and Z₁₁₋₀.

The TMC2272A utilizes six input and output ports to realize a "triple dot product", in which each output is the sum of all three input words, multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words rounded to 12-bits are then available every clock cycle. See the Applications Discussion regarding encoded video standard conversion matrices.

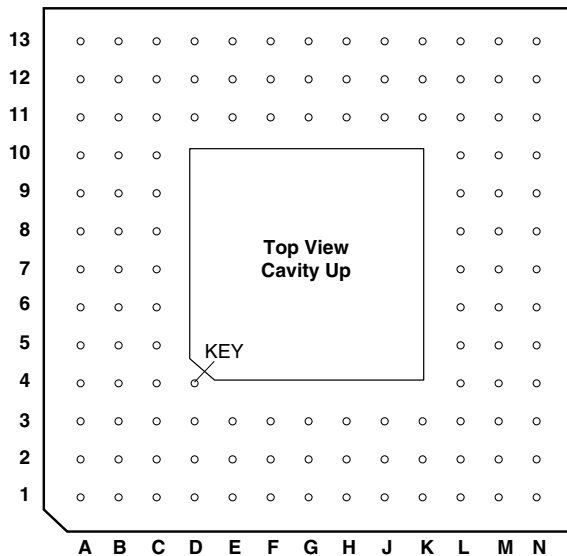
$$X(5)=A(1)KAX(1)+B(1)KBX(1)+C(1)KCX(1)$$

$$Y(5)=A(1)KAY(1)+B(1)KBY(1)+C(1)KCY(1)$$

$$Z(5)=A(1)KAZ(1)+B(1)KBZ(1)+C(1)KCZ(1)$$

Pin Assignments

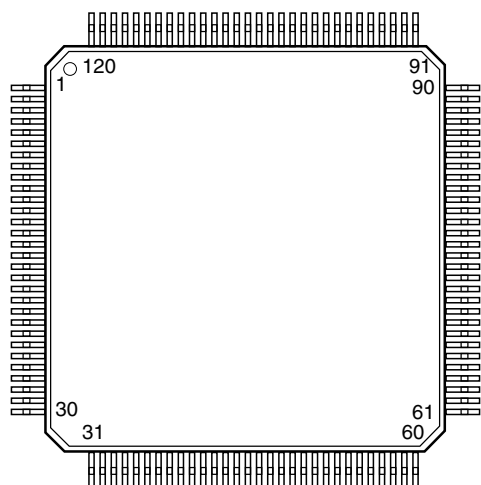
120 Pin Plastic Pin Grid Array, H5 Package, 120 Pin Ceramic Pin Grid Array, G1 Package, and 120 Pin MQFP to PPGA, H6 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	X ₇	C5	GND	G11	A ₃	L10	KB ₈
A2	X ₉	C6	C ₁₀	G12	A ₂	L11	KA ₁
A3	X ₁₀	C7	GND	G13	A ₄	L12	KA ₅
A4	GND	C8	VDD	H1	Y ₄	L13	KA ₆
A5	C ₁₁	C9	C ₀	H2	Y ₀	M1	Z ₂
A6	C ₈	C10	B ₈	H3	VDD	M2	Z ₇
A7	C ₇	C11	B ₅	H11	GND	M3	Z ₉
A8	C ₅	C12	B ₃	H12	A ₀	M4	Z ₁₁
A9	C ₃	C13	B ₁	H13	A ₁	M5	KC ₂
A10	C ₁	D1	Y ₁₁	J1	Y ₁	M6	KC ₄
A11	B ₁₀	D2	X ₀	J2	Y ₂	M7	KC ₆
A12	B ₇	D3	X ₃	J3	GND	M8	KC ₉
A13	B ₄	D11	CLK	J11	KA ₈	M9	KB ₂
B1	X ₄	D12	B ₀	J12	CWSEL ₁	M10	KB ₅
B2	X ₅	D13	A ₁₀	J13	CWSEL ₀	M11	KB ₉
B3	X ₈	E1	Y ₉	K1	Y ₃	M12	KA ₂
B4	X ₁₁	E2	Y ₁₀	K2	Z ₀	M13	KA ₃
B5	GND	E3	GND	K3	Z ₃	N1	Z ₅
B6	C ₉	E11	A ₁₁	K11	KA ₄	N2	Z ₈
B7	C ₆	E12	A ₉	K12	KA ₇	N3	Z ₁₀
B8	C ₄	E13	A ₈	K13	KA ₉	N4	KC ₁
B9	C ₂	F1	Y ₇	L1	Z ₁	N5	KC ₃
B10	B ₁₁	F2	Y ₈	L2	Z ₄	N6	KC ₅
B11	B ₉	F3	VDD	L3	Z ₆	N7	KC ₇
B12	B ₆	F11	A ₇	L4	GND	N8	KC ₈
B13	B ₂	F12	A ₆	L5	KC ₀	N9	KB ₁
C1	X ₁	F13	A ₅	L6	GND	N10	KB ₃
C2	X ₂	G1	Y ₅	L7	VDD	N11	KB ₆
C3	X ₆	G2	Y ₆	L8	KB ₀	N12	KB ₇
C4	VDD	G3	GND	L9	KB ₄	N13	KA ₀

Pin Assignments (continued)

120 Pin Metric Quad Flat Pack (MQFP), KE Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	X6	31	Z6	61	KA1	91	B5
2	X5	32	Z7	62	KA2	92	B6
3	X4	33	Z8	63	KA3	93	B7
4	X3	34	GND	64	KA4	94	B8
5	X2	35	Z9	65	KA5	95	B9
6	X1	36	Z10	66	KA6	96	B10
7	X0	37	Z11	67	KA7	97	B11
8	GND	38	KC0	68	KA8	98	C0
9	Y11	39	KC1	69	KA9	99	C1
10	Y10	40	KC2	70	CWSEL ₁	100	C2
11	Y9	41	KC3	71	CWSEL ₀	101	C3
12	VDD	42	GND	72	GND	102	VDD
13	Y8	43	KC4	73	A0	103	C4
14	Y7	44	KC5	74	A1	104	C5
15	Y6	45	KC6	75	A2	105	C6
16	GND	46	VDD	76	A3	106	GND
17	Y5	47	KC7	77	A4	107	C7
18	Y4	48	KC8	78	A5	108	C8
19	Y0	49	KC9	79	A6	109	C9
20	VDD	50	KB0	80	A7	110	C10
21	Y1	51	KB1	81	A8	111	C11
22	Y2	52	KB2	82	A9	112	GND
23	Y3	53	KB3	83	A10	113	GND
24	GND	54	KB4	84	A11	114	GND
25	Z0	55	KB5	85	B0	115	X11
26	Z1	56	KB6	86	B1	116	X10
27	Z2	57	KB7	87	B2	117	X9
28	Z3	58	KB8	88	CLK	118	VDD
29	Z4	59	KB9	89	B3	119	X8
30	Z5	60	KA0	90	B4	120	X7

Pin Descriptions

Pin Name	CPGA/PPGA/MPGA Pin Number	KE Pin Number	Pin Function Description
Power			
V _{DD}	F3, H3, L7, C8, C4	12, 20, 46, 102, 118	Supply Voltage. The TMC2272A operates from a single +5V supply. All pins must be connected.
GND	E3, G3, J3, L4, L6, H11, C7, C5, A4, B5	8, 16, 24, 34, 42, 72, 106, 112, 113, 114	Ground
Clock			
CLK	D11	88	System Clock. The TMC2272A operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.
Controls			
CWSEL _{1,0}	J12, J13	70, 71	Coefficient Write Select. This input selects which three of the 9 coefficient registers, if any, will be updated on the next clock cycle from the KA ₉₋₀ , KB ₉₋₀ , AND KC ₉₋₀ inputs. See Table 4 and the Functional Block Diagram.

Pin Descriptions (continued)

Pin Name	CPGA/PPGA/ MPGA Pin Number	KE Pin Number	Pin Function Description
Inputs			
A ₁₁₋₀	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12	84, 83, 82, 81, 80, 79, 78, 77, 76, 75, 74, 73	Data Input A. This is one of three 12-bit wide data input ports.
B ₁₁₋₀	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12	97, 96, 95, 94, 93, 92, 91, 90, 89, 87, 86, 85	Data Input B. This is one of three 12-bit wide data input ports.
C ₁₁₋₀	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9	111, 110, 109, 108, 107, 105, 104, 103, 101, 100, 99, 98	Data Input C. This is one of three 12-bit wide data input ports.
KA ₉₋₀	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13	69, 68, 67, 66, 65, 64, 63, 62, 61, 60	Coefficient Input KAX, KAY, or KAZ. These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select (CWSEL ₁₋₀) on the next clock. See Table 1 and the Functional Block Diagram.
KB ₉₋₀	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8	59, 58, 57, 56, 55, 54, 53, 52, 51, 50	Coefficient Input KBX, KBY, OR KBZ. These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select (CWSEL ₁₋₀) on the next clock. See Table 1 and the Functional Block Diagram.
KC ₉₋₀	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5	49, 48, 47, 45, 44, 43, 41, 40, 39, 38	Coefficient Input KCX, KCY, OR KCZ. These are the 10-bit wide coefficient input ports. The value at each of these three inputs will update one coefficient register as selected by the coefficient write select (CWSEL ₁₋₀) on the next clock. See Table 1 and the Functional Block Diagram.
Outputs			
X ₁₁₋₀	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2	115, 116, 117, 119, 120, 1, 2, 3, 4, 5, 6, 7	Output X. These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t _{DO} after every clock rising edge.
Y ₁₁₋₀	D1, E2, E1, F2, F1, G2, G1, H1, K1, J2, J1, H2	9, 10, 11, 13, 14, 15, 17, 18, 23, 22, 21, 19	Output Y. These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t _{DO} after every clock rising edge.
Z ₁₁₋₀	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2	37, 36, 35, 33, 32, 31, 30, 29, 28, 27, 26, 25	Output Z. These are the data outputs. Data are available at the 12-bit registered Output Ports X,Y and Z t _{DO} after every clock rising edge.

Table 1. Coefficient Loading

		CWSEL _{1,0}			
		00	01	10	11
Input	KA ₉₋₀	Hold All	Load KAX	Load KAY	Load KAZ
Input	KB ₉₋₀	Hold All	Load KBX	Load KBY	Load KBZ
Input	KC ₉₋₀	Hold All	Load KCX	Load KCY	Load KCZ

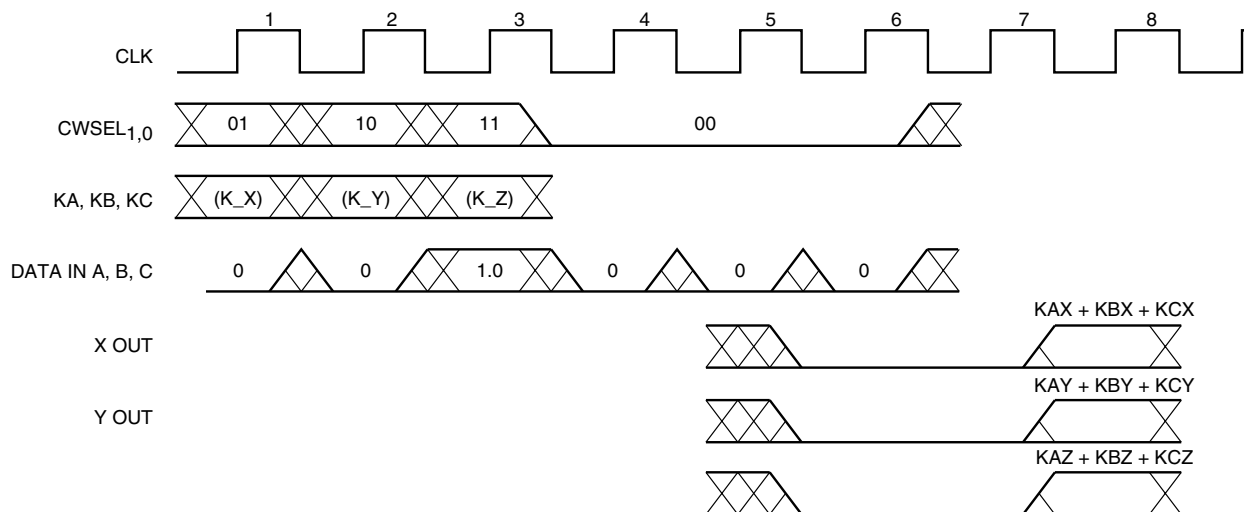


Figure 1. Impulse Response

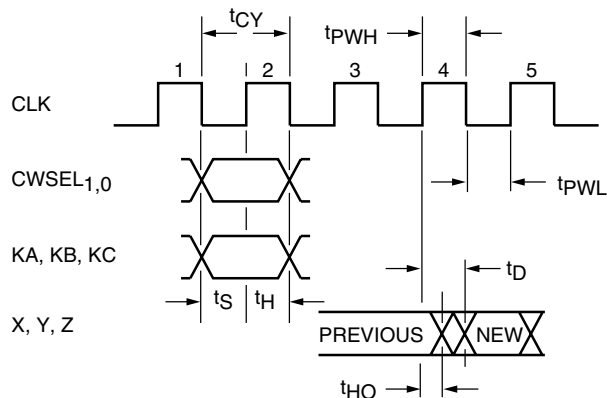


Figure 2. Input/Output Timing

Numeric Format and Overflow

Table 2 shows the binary weightings of the input and output ports of the TMC2272A. Although the internal sums of products could grow to 23 bits, the outputs X, Y, and Z are rounded to yield 12-bit integer words. Thus the output format is identical to the input data format. Bit weighting is easily adjusted by applying the same scaling correction factor to both input and output data words.

As shown in Table 2, the TMC2272A’s matched input and output data formats accommodate 0dB (unity) gain. Therefore the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific translation performed to ensure that no overflow occurs.

Use with Fewer than 12 Bits

The TMC2272A can be configured to provide several format and overflow options when used in systems with fewer than 12 bits of resolution. An 8-bit system will be used as an example, however these concepts apply to any other word width.

The most apparent mode of operation is to left justify the incoming data and to ground the unused input LSBs. However, the outputs will still be rounded to the least significant bit of the TMC2272A, having little if any effect on the top 8 bits actually used. Because the TMC2272A carries out all calculations to full precision, the preferred mode of operation is to right justify and sign extend the data as shown in Figure 3. Since all the LSBs are used, the desired output will be rounded correctly, and overflow will be accommodated by bits 7 through 10.

The TMC2272A may also be used in unsigned binary 8-bit systems as shown in Figure 4. Bits 11 through 8 will handle overflow.

In all applications, a digital zero (ground) should be connected to all unused inputs.

Table 2. Bit Weightings for Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	\bullet	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	
Inputs																							
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Σ										
Coefficients KA, KB, KC													$-K_9$	Σ	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Internal Sum	$-X_{20}$	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	Σ	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	
Outputs																							
X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	Σ										

A minus sign indicates a two's complement sign bit.

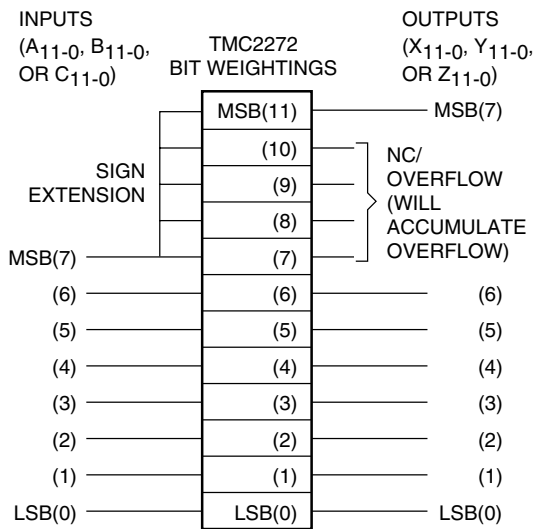


Figure 3. Two's Complement 8-bit Application

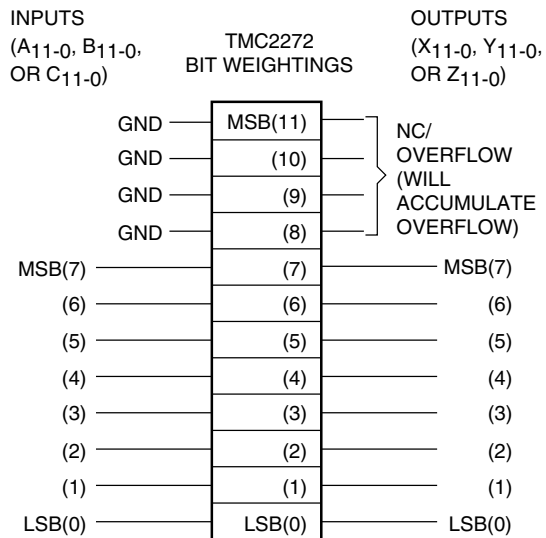


Figure 4. Binary 8-bit Application

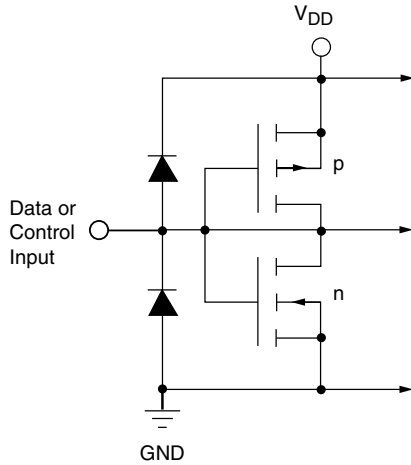


Figure 5. Equivalent Digital Input Circuit

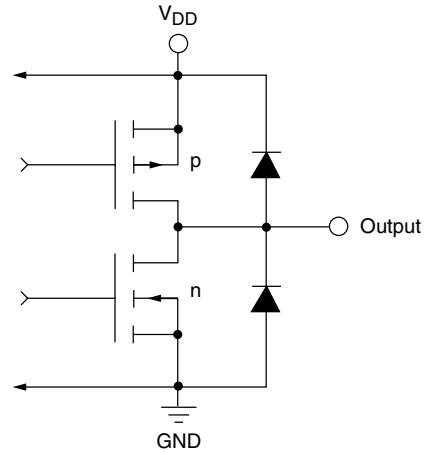


Figure 6. Equivalent Digital Output Circuit

Absolute Maximum Ratings (beyond which the device may be damaged)¹

Parameter	Min	Typ	Max	Unit
Supply Voltage	-0.5		7.0	V
Input Voltage	-0.5		$V_{DD} + 0.5$	V
Applied Voltage ²	-0.5		$V_{DD} + 0.5$	V
Externally Forced Current ^{3,4}	-3.0		6.0	mA
Short Circuit Duration (single output in HIGH state to ground)			1	sec
Operating, Ambient Temperature	-20		110	°C
Junction Temperature			140	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature (10 seconds)			300	°C

Notes:

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied. Performance and reliability are guaranteed only if Operating Conditions are not exceeded.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Min	Nom	Max	Units
V _{DD}	Power Supply Voltage	4.75	5.0	5.25	V
f _{CLK}	Clock Frequency	TMC2272A		30	MHz
		TMC2272A-2		40	MHz
		TMC2272A-3		50	MHz
t _{PWH}	CLK pulse width, HIGH	6			ns
t _{PWL}	CLK pulse width, LOW	8			ns
t _S	Input Data Setup Time	6			ns
t _H	Input Data Hold Time	2			ns
V _{IH}	Input Voltage, Logic HIGH	2.0			V
V _{IL}	Input Voltage, Logic LOW			0.8	V
I _{OH}	Output Current, Logic HIGH			-2.0	mA
I _{OL}	Output Current, Logic LOW			4.0	mA
T _A	Ambient Temperature, Still Air	0		70	°C

Electrical Characteristics

Parameter		Conditions	Min	Typ	Max	Units
I _{DD}	Total Power Supply Current	V _{DD} = Max, C _{LOAD} = 25pF, f _{CLK} = Max				
		TMC2272A			125	mA
		TMC2272A-2			140	mA
		TMC2272A-3			155	mA
I _{DDU}	Power Supply Current, Unloaded	V _{DD} = Max, f _{CLK} =Max				
		TMC2272A			120	mA
		TMC2272A-2			135	mA
		TMC2272A-3			150	mA
I _{DDQ}	Power Supply Current, Quiescent	V _{DD} = Max, CLK = LOW			12	mA
C _{PIN}	I/O Pin Capacitance		5			pF
I _{IH}	Input Current, HIGH ¹	V _{DD} = Max, V _{IN} = V _{DD}			±5	μA
I _{IL}	Input Current, LOW ¹	V _{DD} = Max, V _{IN} = 0 V			±5	μA
I _{OZH}	Hi-Z Output Leakage Current, Output HIGH ²	V _{DD} = Max, V _{IN} = V _{DD}			±10	μA
I _{OZL}	Hi-Z Output Leakage Current, Output LOW ²	V _{DD} = Max, V _{IN} = 0 V			±10	μA
I _{OS}	Short-Circuit Current		-20		-80	mA
V _{OH}	Output Voltage, HIGH	I _{OH} = Max, V _{DD} = Min	2.4			V
V _{OL}	Output Voltage, LOW	I _{OL} = Max, V _{DD} = Min			0.4	V

Notes:

1. Except pins XC₁₁₋₀, YC₁₁₋₈.
2. Pins XC₁₁₋₀, YC₁₁₋₈.

Switching Characteristics

Parameter		Conditions	Min	Typ	Max	Units
t _{DO}	Output Delay Time	C _{LOAD} = 25 pF			15	ns
t _{HO}	Output Hold Time	C _{LOAD} = 25 pF	3			ns

Applications Discussion

The TMC2272A can convert between any two three-coordinate colorspace with the selection of the proper coefficients. Sets of coefficients for some popular colorspace conversions are presented below.

By concatenating coefficient matrices of single transformations, the user can program the TMC2272A to perform compound transforms efficiently. For example, given an RGB input, correction of the relative values of R and B, for

color temperature, conversion to YIQ, modification of contrast by changing Y, and conversion back to RGB can be performed as quickly and easily as any simple transformation. To calculate the final set of coefficients from the coefficients of the individual transformations, the procedure in Figure 7 (concatenation) is used. If more than two matrices are to be combined, the result from the concatenation of the first two matrices is concatenated with the third. If more matrices must be incorporated in the final function, the last step is repeated.

$$\begin{vmatrix} A & B & C \\ D & E & F \\ G & H & I \end{vmatrix} = \begin{vmatrix} J & K & L \\ M & N & O \\ P & Q & R \end{vmatrix} = \begin{vmatrix} AJ + BM + CP & AK + BN + CQ & AL + BO + CR \\ DJ + EM + FP & DK + EN + FQ & DL + EO + FR \\ GJ + HM + IP & GK + HN + IQ & GL + HO + IR \end{vmatrix}$$

Figure 7. Concatenation

Converting from GBR to YC_BC_R

With the right coefficients, two external NOT gates, and an external 4-bit half-adder, the TMC2272A can convert video data from 8-bit full-scale (e.g. VGA) GBR components to 10-bit YC_BC_R components.

Table 3. 10-bit component formats and inclusive ranges.

Color Space Term	Range	Format
Y Luminance	64-940	magnitude
Y' Y - 64	0-876	magnitude
C _B Color difference, Blue	64-960	magnitude
U' C _B - 512	±448	2's comp
C _R Color difference, Red	64-960	magnitude
V' C _R - 512	±448	2's comp
GBR Green, Blue, Red components	0-255	magnitude, 8-bits

The analog defining equations for 1 Volt luminance and ±0.5 Volt color difference components are:

$$Y = +0.5870(G) + 0.1140(B) + 0.2990(R)$$

$$B - Y = -0.3313(G) + 0.5000(B) - 0.1687(R)$$

$$R - Y = -0.4187(G) - 0.0813(B) + 0.5000(R)$$

To translate these equations into the digital domain, note that the ranges of R, G, and B are 0 to 255 instead of 0 to 1, the range of Y is 64 to 940 instead of 0 to 1, and the ranges of U and V are 64 to 960 instead of +/-0.5:

$$Y = (876/255)(0.587(G)+0.114(B)+0.299(R))+64 = 2.01652(G)+0.39162(B)+1.02715(R)+64$$

$$C_B = (896/255)(0.3313(G)+0.5(B)-0.1687(R))+512 = -1.16397(G)+1.75686(B)-0.59289(R)+512$$

$$C_R = (896/255)(-0.4187(G)-0.0813(B)+0.5(R))+512 = -1.47115(G)-0.28571(B)+1.75686(B)+512$$

Let Y'=Y-64, U'=C_B-512, and V'=C_R-512. The TMC2272A will compute Y', U', and V'. Adding 64 (040_h) externally to Y' will then yield Y, whereas inverting the most significant bits of U' and V', U'⁹ and V'⁹, will yield C_B and C_R, respectively. Multiplying the equations immediately above by 128 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

128 (Y')	=	258 (G) 102	+50 (B) 032	+131 (R) 083	dec. hex
128 (U')	=	-149 (G) 36B	+225 (B) 0E1	-76 (R) 3B4	dec hex
128I (V')	=	-188 (G) 344	-37 (B) 3DB	+225 (R) 0E1	dec. hex

If the TMC2272A input data alignment for 8-bit GBR is:

0	0	G7	G6	G5	G4	G3	G2	G1	G0	0	0
0	0	B7	B6	B5	B4	B3	B2	B1	B0	0	0
0	0	R7	R6	R5	R4	R3	R2	R1	R0	0	0

then the output data alignment for 10-bit Y'U'V' is:

0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U9	U9	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
V9	V9	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The factors of 4 in the input data format and 128 in the equations are absorbed by the internal 9-bit (factor of 512) right-shifting of the emerging results.

At the output of the TMC2272A, invert the most significant bits, U9 and V9, of the chrominance components, and add 1 at Y6 of the luminance to obtain the true CCIR Rec. 601 values.

Converting from GBR to 8-bit Full-Scale YUV

With the right coefficients and two external NOT gates, the TMC2272A can convert video data from 8-bit full-scale (e.g. VGA) GBR components to 8-bit full-scale YUV components.

Table 4. 8-bit component formats and inclusive ranges:

Color Space Term	Range	Format
Y Luminance	0-255	magnitude
U Color difference, Blue	128 to -127	2's comp
U' U + 128	0-255	magnitude
V Color difference, Red	128 to -127	2's comp
V' V + 128	0-255	magnitude
G,B,R Green, Blue, Red components	0-255	magnitude

As in the previous RGB to YC_BC_R case, begin with the defining equations, but without the range compensation factors of 255/876 and 255/896:

$$Y = 0.5870 (G) + 0.1140 (B) + 0.2990 (R)$$

$$U = -0.3313 (G) + 0.5000 (B) - 0.1687 (R)$$

$$V = -0.4187 (G) - 0.0813 (B) + 0.5000 (R)$$

The TMC2272A will compute Y, U, and V directly, whereas inverting the most significant bits of U and V, U7 and V7 will yield U' and V', respectively. Multiplying the equations immediately above by 512 and rounding each coefficient to the nearest integer yields the recommended set of coefficients for GBR to YUV conversion.

512 (Y)	=		301 (G)	+	58 (B)	+	153 (R)	dec.
			12D		03A		099	hex
512 (U)	=	-	170 (G)	+	256 (B)	-	86 (R)	dec.
			356		100		3AA	hex
512 (V)	=	-	214 (G)	-	42 (B)	+	256 (R)	dec.
			32A		3D6		100	hex

If the TMC2272A input data alignment for 8-bit GBR is:

0	0	0	0	G7	G6	G5	G4	G3	G2	G1	G0
0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

then the output data alignment for 8-bit YUV is:

0	0	0	0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U7	U7	U7	U7	U7	U6	U5	U4	U3	U2	U1	U0
V7	V7	V7	V7	V7	V6	V5	V4	V3	V2	V1	V0

where the quintupled U9 and V9 sign bits denote two's complement sign extensions. The factor of 512 in the equations above is absorbed by the internal 9-bit right shift of each emerging result.

At the output of the TMC2272A, invert the most significant bits, U7 and V7, of the chrominance components, to obtain the 8-bit offset format.

Converting From YC_BC_R to GBR

Following the notation employed earlier, the TMC2272A will be used to convert data in Y'U'V' format into GBR format.

Since Y' = 876, U' = V' = 0, and G = B = R = 255 for saturated white output, every Y' coefficient will be 225/876 = 0.29110. The full analog matrix for Y'U'V' to GBR conversion is:

$$G = 0.29110 (Y') - 0.09794 (U') - 0.20324 (V')$$

$$B = 0.29110 (Y') + 0.50431 (U')$$

$$R = 0.29110 (Y') + 0.39901 (V')$$

Since the largest element is just over 0.5 and the largest permissible coefficient is 511, multiply all elements of the matrix by 512 to obtain the values to load into the TMC2272A.

$$G = \begin{matrix} 149 (Y') & - & 50 (U') & - & 04 (V') \\ 095 & & 3CE & & 398 \end{matrix} \quad \begin{matrix} \text{dec.} \\ \text{hex} \end{matrix}$$

$$B = \begin{matrix} 149 (Y') & + & 258 (U') \\ 095 & & 100 \end{matrix} \quad \begin{matrix} \text{dec.} \\ \text{hex} \end{matrix}$$

$$R = \begin{matrix} 149 (Y') & + & 204 (V') \\ 095 & & 0CC \end{matrix} \quad \begin{matrix} \text{dec.} \\ \text{hex} \end{matrix}$$

Decrease the incoming luminance at the input to the TMC2272A by 64 by adding 1's at positions Y9, Y8, Y7, and Y6. Invert U9 and V9 and their sign extensions, to accommodate CCIR Rec. 601 data. Instead of reducing Y by 64, an alternate is to reduce each of the G, B, and R outputs by (255) (64 / 876) = 19.

For the Y'U'V' to RGB conversion, the TMC2272A input data alignment for 10-bit Y'U'V' is:

0	0	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
U9	U9	U9	U8	U7	U6	U5	U4	U3	U2	U1	U0
V9	V9	V9	V8	V7	V6	V5	V4	V3	V2	V1	V0

where the tripled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272A output data alignment for 8-bit GBR is then:

0	0	0	0	G7	G6	G5	G4	G3	G2	G1	G0
0	0	0	0	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	R7	R6	R5	R4	R3	R2	R1	R0

Converting From 8-bit Full Scale YUV to GBR

Following the notation employed earlier, the TMC2272A will be used to convert data in 8-bit YUV format into 8-bit GBR format.

Since $Y = 256$, $U = V = 0$, and $G = B = R = 255$ for saturated white output, every Y coefficient will be $255 / 255 = 1.0$. The full matrix for YUV to GBR conversion is:

$$G = 1.0 (Y) \quad -0.3443 (U) \quad -0.7142 (V)$$

$$B = 1.0 (Y) \quad +1.7727 (U)$$

$$R = 1.0 (Y) \quad +1.3965 (V)$$

Since the largest element is over 1.0 and the largest permissible coefficient is 511, multiply all elements of the matrix by 256 to obtain the values to load into the TMC2272A:

$$G = \begin{matrix} 256 (Y') & - 88 (U') & - 83 (V') & \text{dec.} \\ 100 & 3A8 & 349 & \text{hex} \end{matrix}$$

$$B = \begin{matrix} 256 (Y') & + 454 (U') & & \text{dec.} \\ 100 & 1C6 & & \text{hex} \end{matrix}$$

$$R = \begin{matrix} 256 (Y') & + 359 (V') & & \text{dec.} \\ 100 & 167 & & \text{hex} \end{matrix}$$

For the YUV to RGB conversion, the TMC2272A input data alignment for 10-bit Y'U'V' is:

```
0  Y9 Y8 Y7 Y6 Y5 Y4 Y3 Y2 Y1 Y0 0
U9 U9 U8 U7 U6 U4 U4 U3 U2 U1 U0 0
V9 V9 V8 V7 V6 V5 V4 V3 V2 V1 V0 0
```

where the doubled U9 and V9 sign bits denote two's complement sign extensions. The TMC2272A output data alignment for 8-bit GBR is then:

```
0  0  0  0  G7 G6 G5 G4 G3 G2 G1 G0
0  0  0  0  B7 B6 B5 B4 B3 B2 B1 B0
0  0  0  0  R7 R6 R5 R4 R3 R2 R1 R0
```

Note that the inputs have to be doubled because the coefficient gain is 256, whereas the internal gain is $1 / 512$, for a net gain of $1/2$.

Table 5. Summary of Colorspace Conversion Coefficients

Conversion	KAX	KAY	KAZ	KBX	KBY	KBZ	KCX	KCY	KCZ
RGB to YUV	099	3AA	100	12D	356	32A	03A	100	3D6
RGB to $Y_{C_B}C_R$	083	3B4	0E1	102	36B	344	032	0E1	3DB
YUV to RGB	100	100	100	000	3A8	1C6	167	349	000
$Y_{C_B}C_R$ to RGB	149	149	149	000	3CE	102	0CC	398	000

Table 6. Conversion Port Assignments and Alignments

Port	AIN	BIN	CIN	XOUT	YOUT	ZOUT
RGB to YUV	R_{7-0}	G_{7-0}	B_{7-0}	Y_{7-0}	$U_{7-0}(e)$	$V_{7-0}(e)$
RGB to $Y_{C_B}C_R$	R_{7-0}	G_{7-0}	B_{7-0}	Y_{9-0}	$U_{9-0}(e)$	$V_{9-0}(e)$
YUV to RGB	$Y_{8-1}(e)$	$U_{8-1}(e)$	$V_{8-1}(e)$	R_{7-0}	G_{7-0}	B_{7-0}
$Y_{C_B}C_R$ to RGB	Y_{9-0}	$C_{B9-0}(e)$	$C_{R9-0}(e)$	R_{7-0}	G_{7-0}	B_{7-0}

Where X_{Y-0} denotes right-justified, (e) denotes sign extension, and X_{Y-1} denotes shifted one bit leftward from a right-justified position.

HSV (HSI) Format Conversions

HSV (or HSI) refers to Hue (color), Saturation (vividness), and Value (intensity or brightness), quantities which are directly related to the human perception of light and color. The V (or I) levels are simply the Y (or luminance) levels. Hue and Saturation are derived from the R-Y and B-Y color difference values of a signal.

HSV Calculations:

$$\text{Value (V)} = \text{Intensity (I)} = Y$$

$$\text{Hue (H)} = \text{Arctan} (B-Y/R-Y)$$

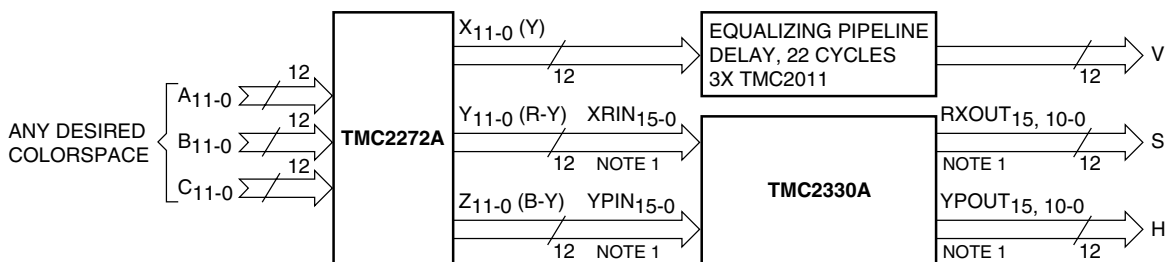
$$\text{Saturation (S)} = \sqrt{(R-Y)^2 + (B-Y)^2}$$

$$R-Y = S * \cos(H)$$

$$B-Y = S * \sin(H)$$

One may use two 64Kx8 ROM look-up-tables to calculate Hue and Saturation from R-Y and B-Y in an 8-bit system. However, the finite size of this LUT may limit performance, especially if the TMC2272A's full precision is used. The TMC2330A, developed to translate between rectangular and polar coordinates, can perform the trigonometric transformations to 16 bit precision at 50MHz. These calculations are the same as required in HSV calculations. A 4 Gigabyte x 32 bit LUT can achieve the same accuracy and precision as the TMC2330A, if it is programmed correctly.

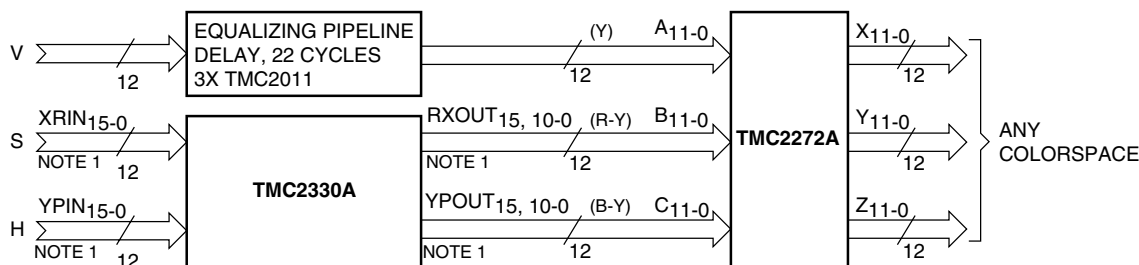
To convert between Y, R-Y, B-Y and HSV, the TMC2272A isn't needed at all; simply use the TMC2330A. To convert between HSV and any other format, use the TMC2330A to translate between HSV and Y, R-Y, B-Y, and use the TMC2272A to translate between Y, R-Y, B-Y and the other format. See Figures 8 and 9.



Notes:

1. Connect TMC2272A MSBs (Bits 11) to TMC2330A MSBs (Bits 15) and also to TMC2330A Bits 14-11. Connect TMC2272A LSBs (Bits 10-0) to TMC2330A LSBs (Bits 10-0). TMC2330A output bits 14-11 are overflow.
2. TMC2272A Y₁₁₋₀ outputs should not be confused with the designation “Y” used to signify the intensity components. The assignment of components to TMC2272A inputs and outputs may be altered through the selection of appropriate coefficients.

Figure 8. Conversion to HSV



Notes:

1. Connect input MSBs (Bits 11) to TMC2330A MSBs (Bits 15) and also to TMC2330A Bits 14-11. Connect input LSBs (Bits 10-0) to TMC2330A LSBs (Bits 10-0).
2. TMC2272A Y₁₁₋₀ outputs should not be confused with the designation “Y” used for an intensity component. Component assignment depends on the coefficient used.

Figure 9. Conversion from HSV

Input Interpolation/Output Decimation and Filtering

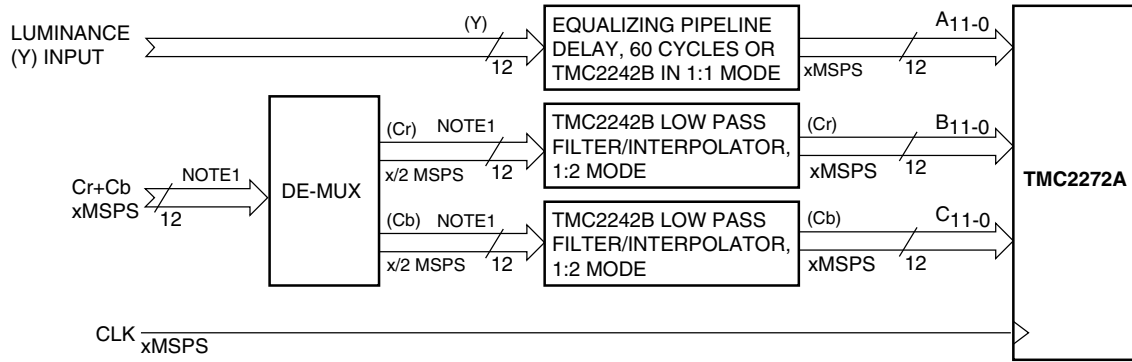
In some applications the two color-difference signals (R-Y/B-Y or Cr/Cb, for example) are transmitted at one-half the rate of the luminance (Y) signal. These two color-difference signals are often multiplexed to one signal which is at the same sample rate as the luminance signal.

In many applications, if the color difference signals are already band-limited, it is satisfactory to use the same color difference sample for each two luminance samples. Little improvement is obtained with a simple averaging ((A+B)/2) interpolation filter. If the color difference signal is not band-limited, either of these two methods may yield unsatisfactory results due to aliasing. In this case, a Fairchild TMC2242B digital low-pass (half-band) interpolating filter will correctly band-limit each color difference signal as it is interpolated. See Figure 10.

The same methods are used to decimate the color difference outputs. Simple decimation by removing every other sample of color information may yield unsatisfactory results due to aliasing. This is a problem because the color difference signals have not been transformed with the higher-bandwidth luminance signals and therefore have higher bandwidths than they had before the transform. The best performance is

obtained by using a precise low-pass (half-band) decimation filter such as the TMC2242B to remove aliasing components. See Figure 11.

The TMC2242B is a bi-directional, selectable rate filter/interpolator/decimator.



Notes:

1. Width of input paths will vary with source.
2. See TMC2242B Datasheet for further information.

Figure 10. Input Interpolation and Filtering

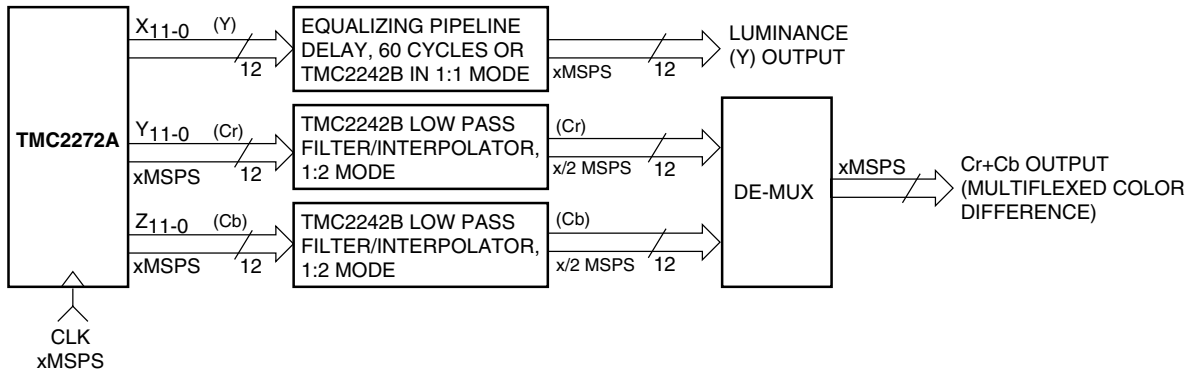


Figure 11. Output Decimation and Filtering

Related Products

- TMC1175 8 bit 40 Msp/s A/D Converter
- TMC2301 Image Resampling Sequencer
- TMC2302A Image Manipulation Sequencer
- TMC2249A Video Mixer
- TMC2242B Half-Band Filter
- TMC2330A Coordinate Transformer

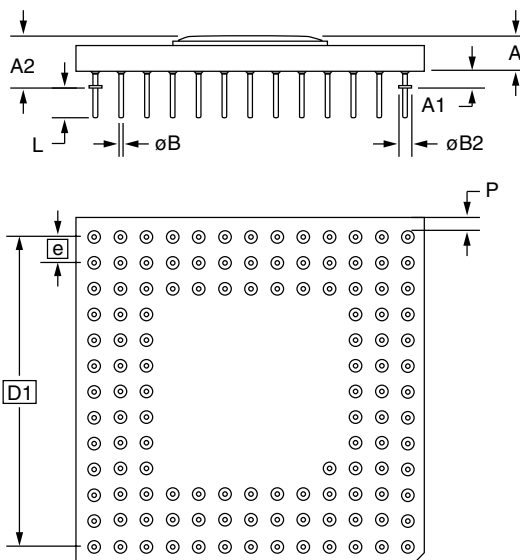
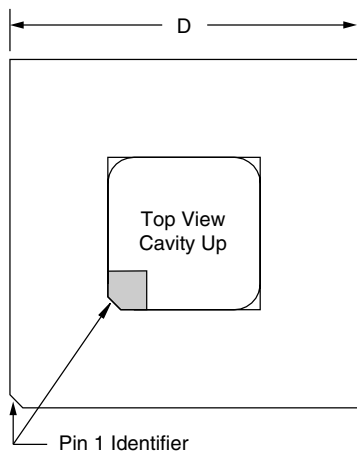
Mechanical Dimensions

120-Lead CPGA Package Outline

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



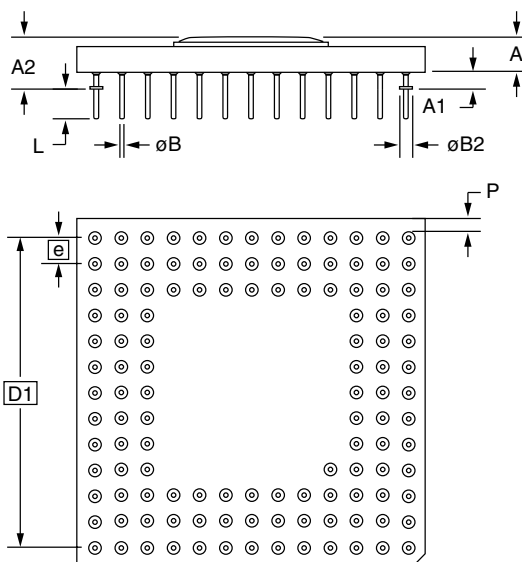
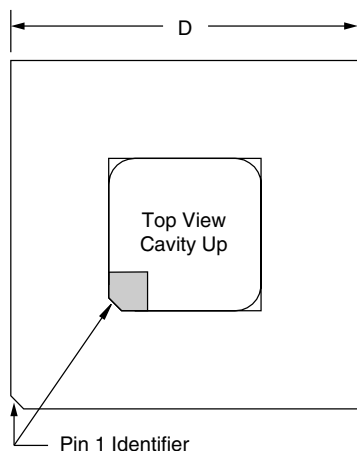
Mechanical Dimensions

120-Lead PPGA Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.340	1.380	33.27	35.05	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
L1	.170	.190	4.31	4.83	
M	13		13		3
N	120		120		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



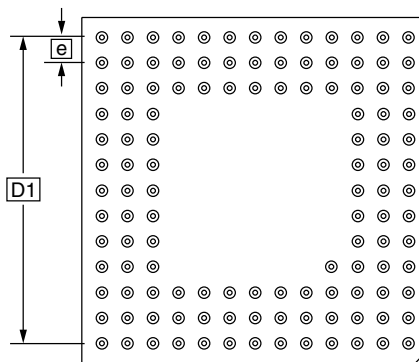
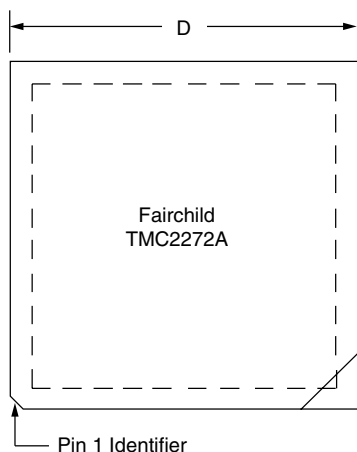
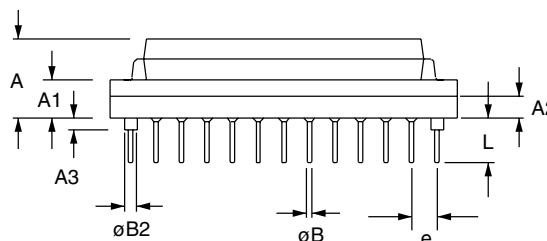
Mechanical Dimensions

120-Lead Metric Quad Flat Package to Pin Grid Array Package (MPGA)

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.309	.311	7.85	7.90	
A1	.145	.155	3.68	3.94	
A2	.080	.090	2.03	2.29	
A3	.050 TYP.		1.27 TYP.		
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.355	1.365	34.42	34.67	SQ
D1	1.200 BSC		30.48 BSC		
e	.100 BSC		2.54 BSC		
L	.175	.185	4.45	4.70	
M	13		13		3
N	120		120		4

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.



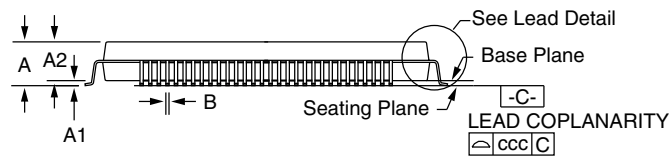
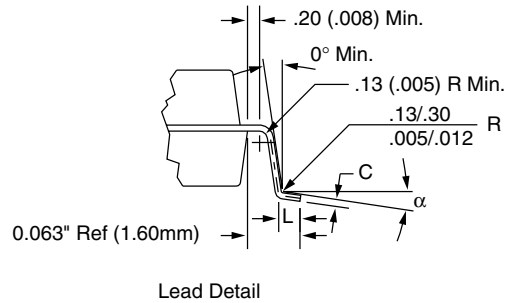
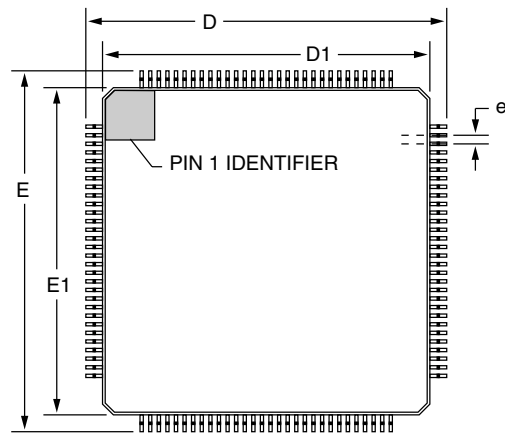
Mechanical Dimensions

120-Lead MQFP Package

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.154	—	3.92	
A1	.010	—	.25	—	
A2	.125	.144	3.17	3.67	
B	.012	.018	.30	.45	3, 5
C	.005	.009	.13	.23	5
D/E	1.219	1.238	30.95	31.45	
D1/E1	1.098	1.106	27.90	28.10	
e	.0315 BSC		.80 BSC		
L	.026	.037	.65	.95	4
N	120		120		
ND	30		30		
α	0°	7°	0°	7°	
ccc	—	.004	—	.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Controlling dimension is millimeters.
3. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be .08mm (.003in.) maximum in excess of the "B" dimension. Dambar cannot be located on the lower radius or the foot.
4. "L" is the length of terminal for soldering to a substrate.
5. "B" & "C" includes lead finish thickness.



Ordering Information

Product Number	Temperature Range	Speed Grade	Screening	Package	Package Marking
TMC2272AG1C	0°C to 70°C	30 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2272AG1C
TMC2272AG1C2	0°C to 70°C	40 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2272AG1C2
TMC2272AG1C3	0°C to 70°C	50 MHz	Commercial	120 Pin Ceramic Pin Grid Array	2272AG1C3
TMC2272AH5C	0°C to 70°C	30 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C
TMC2272AH5C2	0°C to 70°C	40 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C2
TMC2272AH5C3	0°C to 70°C	50 MHz	Commercial	120 Pin Plastic Pin Grid Array	2272AH5C3
TMC2272AH6C	0°C to 70°C	30 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2272AH6C2	0°C to 70°C	40 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2272AH6C3	0°C to 70°C	50 MHz	Commercial	120 Lead Metric Quad Flatpack to Pin Grid Array	N/A
TMC2272AKEC	0°C to 70°C	30 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC
TMC2272AKEC2	0°C to 70°C	40 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC2
TMC2272AKEC3	0°C to 70°C	50 MHz	Commercial	120 Lead Plastic Quad Flatpack	2272AKEC3

LIFE SUPPORT POLICY

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.