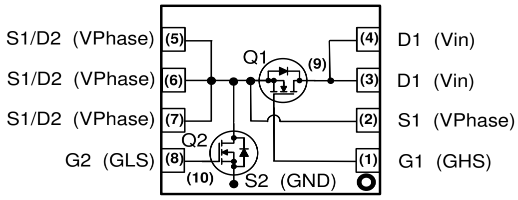
Power Block

Features

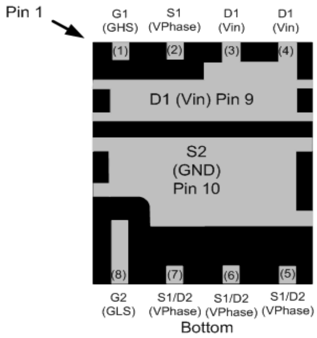
- Dual asymmetric N-channel OptiMOS™5 MOSFET
- Logic level (4.5V rated)
- Optimized for high performance buck converters
- Qualified according to JEDEC[1)] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product Summary

		Q1	Q2	
V_{DS}		25	25	V
$R_{DS(on),max}$	V_{GS}=10 V	3	0.8	mΩ
	V_{GS}=4.5 V	4	1.1	
I_D		50	50	A



Top view



Bottom View

Type	Package	Marking
BSG0811ND	PG-TISON8-4	0811ND

Maximum ratings, at T_j=25 °C, unless otherwise specified [2)]

Parameter	Symbol	Conditions	Value		Unit
			Q1	Q2	
Continuous drain current	I_D	T_C=70 °C, V_{GS}=10 V	50	50	A
		T_C=70 °C, V_{GS}=4.5 V	50	50	
		T_A=25 °C, V_{GS}=4.5 V[3)]	31	50	
		T_A=25 °C, V_{GS}=4.5 V[4)]	19	41	
Pulsed drain current	$I_{D,pulse}$	T_C=70 °C	160	160	
Avalanche energy, single pulse	E_{AS}	Q1: I_D=10 A, Q2: I_D=20 A, R_{GS}=25 Ω	30	160	mJ
Gate source voltage	V_{GS}		±16		V
Power dissipation	P_{tot}	T_A=25 °C[3)]	6.25	6.25	W
		T_A=25 °C[4)]	2.5	2.5	
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

1) J-STD20 and JESD22

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	

Thermal characteristics

Parameter		Symbol	Conditions	min.	typ.	max.	Unit
Thermal resistance, junction - case	Q1	R_{thJC}		-	-	4.3	K/W
	Q2			-	-	1.8	
Thermal resistance, junction - ambient[2]	Q1	R_{thJA}	application specific board[3]	-	-	20	
	Q2						
	Q1		6 cm^2 cooling area[4]	-	-	50	
	Q2						

Electrical characteristics, at T_j=25 °C, unless otherwise specified

Static characteristics

Parameter		Symbol	Conditions	min.	typ.	max.	Unit
Drain-source breakdown voltage	Q1	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	25 [6]	-	-	V
	Q2						
Gate threshold voltage	Q1	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250 µA	1.2	1.6	2	
	Q2						
Zero gate voltage drain current	Q1	I_{DSS}	V_{DS}=25 V, V_{GS}=0 V, T_j=25 °C	-	-	1	µA
	Q2						
	Q1		V_{DS}=25 V, V_{GS}=0 V, T_j=150 °C	-	-	100	
	Q2						
Gate-source leakage current	Q1	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	-	100	nA
	Q2						
Drain-source on-state resistance	Q1	$R_{DS(on)}$	V_{GS}=4.5 V, I_D=20 A	-	3.2	4.0	mΩ
	Q2			-	0.9	1.1	
	Q1		V_{GS}=10 V, I_D=20 A	-	2.4	3.0	
	Q2			-	0.7	0.8	
Gate resistance	Q1	R_G		-	0.7	1.2	Ω
	Q2			-	0.7	1.2	
Transconductance	Q1	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=20 A	46	93	-	S
	Q2			90	180	-	

[2] Only one of both transistors active

[3] 8 Layers copper 70µm thickness. PCB in still air.

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Dynamic characteristics							
Input capacitance	Q1	C_{iss}	V_{GS}=0 V, V_{DS}= 12 V, f=1 MHz	-	780	1100	pF
	Q2			-	2700	3700	
Output capacitance	Q1	C_{oss}		-	390	520	
	Q2			-	1400	1900	
Reverse transfer capacitance	Q1	C_{rss}		-	38	-	
	Q2			-	130	-	
Turn-on delay time	Q1	$t_{d(on)}$	V_{IN}=12 V, V_{DRV}=5 V, F_{SW}=500 KHz, I_{OUT}=30 A [5]	-	4.3		ns
	Q2			-	5.6	-	
Rise time	Q1	t_r		-	4.7	-	
	Q2			-	4.3	-	
Turn-off delay time	Q1	$t_{d(off)}$		-	4.3	-	
	Q2			-	8.8	-	
Fall time	Q1	t_f		-	1.4	-	
	Q2			-	2.6	-	
Gate Charge Characteristics							
Gate to source charge	Q1	Q_{gs}	V_{DD}=12 V, I_D=30 A, V_{GS}=0 to 4.5 V	-	2.0	-	nC
Gate to drain charge		Q_{gd}		-	1.4	-	
Gate charge total		Q_g		-	5.6	8.4	
Gate plateau voltage		$V_{plateau}$		-	2.6	-	V
Gate to source charge	Q2	Q_{gs}		-	6.4	-	nC
Gate to drain charge		Q_{gd}		-	4.7	-	
Gate charge total		Q_g		-	20	29	
Gate plateau voltage		$V_{plateau}$		-	2.3	-	V
Output charge	Q1	Q_{oss}	V_{DD}=12 V, V_{GS}=0 V	-	8	-	nC
	Q2			-	27	-	

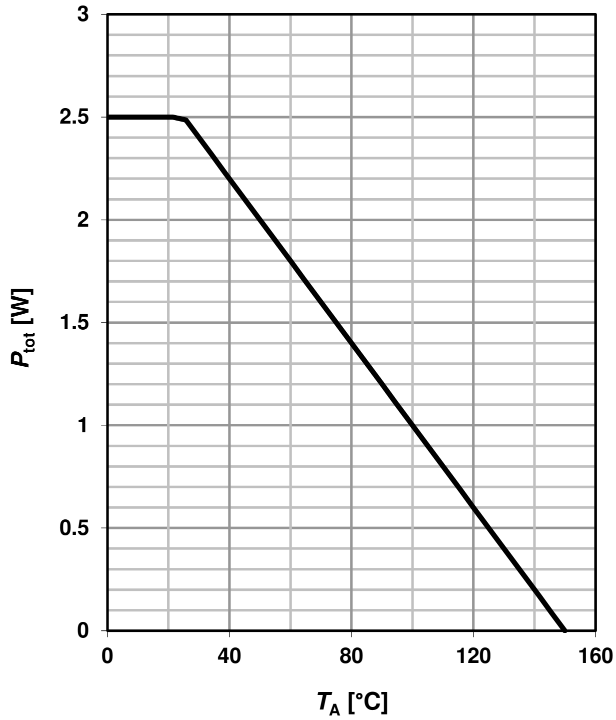
[5] For more information see application note n° TBD

[6] The device can withstand a pulse of not more than 30 V for a duration of up to 2 ns at a frequency of 600 kHz with maximum buck converter input voltage V_{IN}=16 V.

Parameter		Symbol	Conditions	Values			Unit
				min.	typ.	max.	
Reverse Diode							
Diode continuous forward current	Q1	I_S	T_C=25 °C	-	-	29	A
	Q2			-	-	50	
Diode pulse current	Q1	$I_{S,pulse}$		-	-	160	
	Q2			-	-	160	
Diode forward voltage	Q1	V_{SD}	V_{GS}=0 V, I_F=20 A, T_j=25 °C	-	0.84	1	V
	Q2			-	0.77	1	
Reverse recovery charge	Q1	Q_{rr}	V_R=12 V, I_F=I_S, di_F/dt=100 A/µs	-	10	-	nC
	Q2			-	20	-	

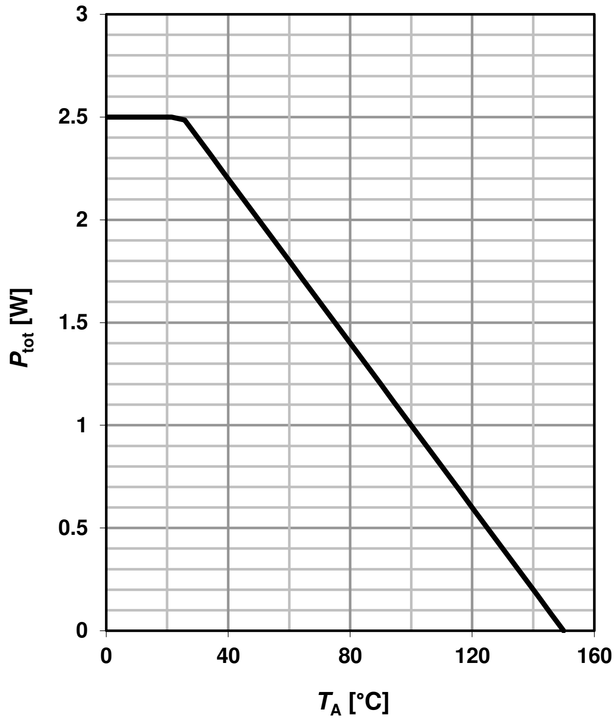
1 Power dissipation (Q1)

P_{tot}=f(T_A)[4)]



2 Power dissipation (Q2)

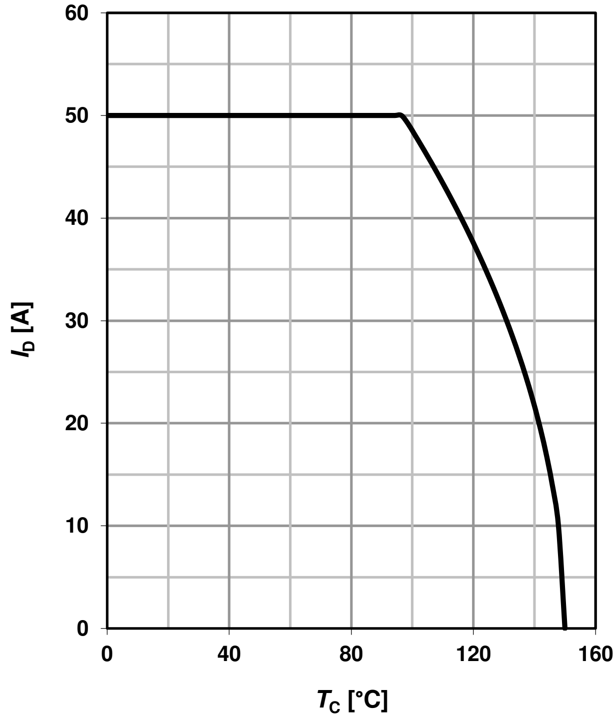
P_{tot}=f(T_A)[4)]



3 Drain current (Q1)

I_D=f(T_C)

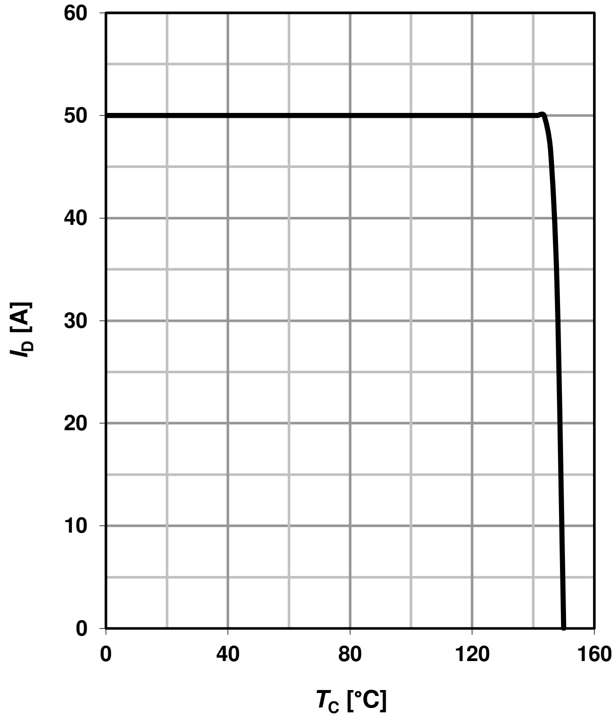
parameter: V_{GS}≥10 V



4 Drain current (Q2)

I_D=f(T_C)

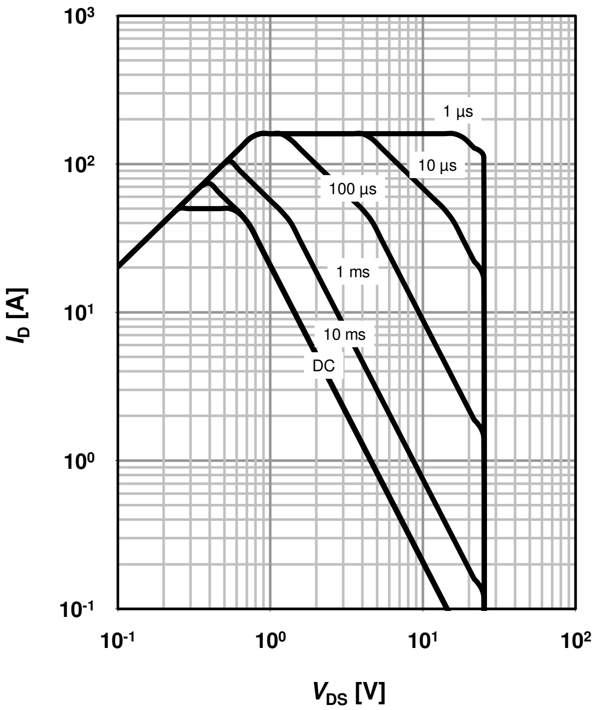
parameter: V_{GS}≥10 V



5 Safe operating area (Q1)

I_D=f(V_{DS}); T_C=25 °C; D=0

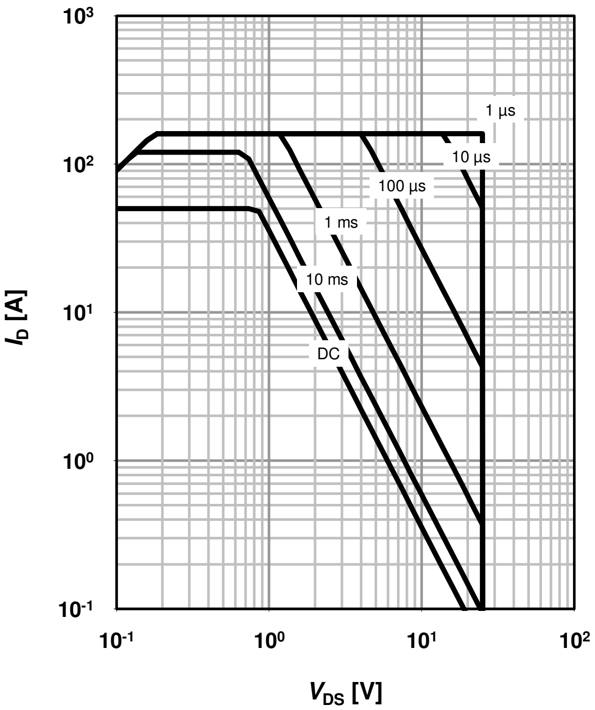
parameter: t_p



6 Safe operating area (Q2)

I_D=f(V_{DS}); T_C=25 °C; D=0

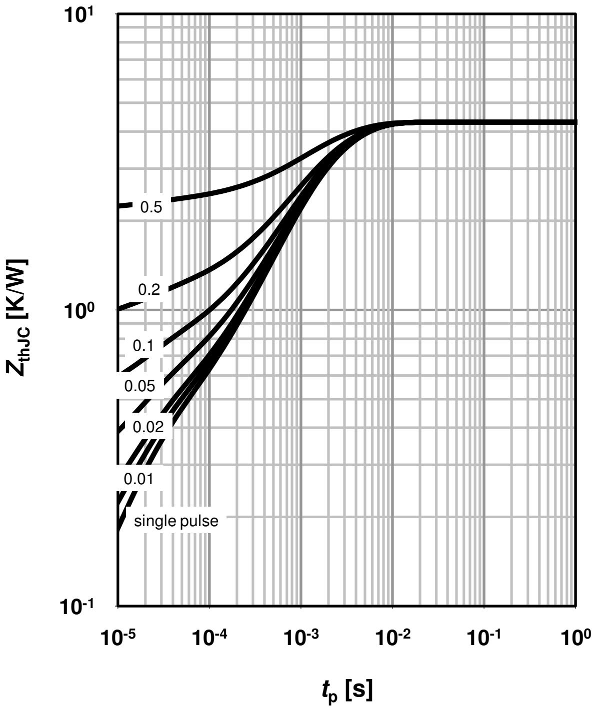
parameter: t_p



7 Max. transient thermal impedance (Q1)

Z_{thJC}=f(t_p)

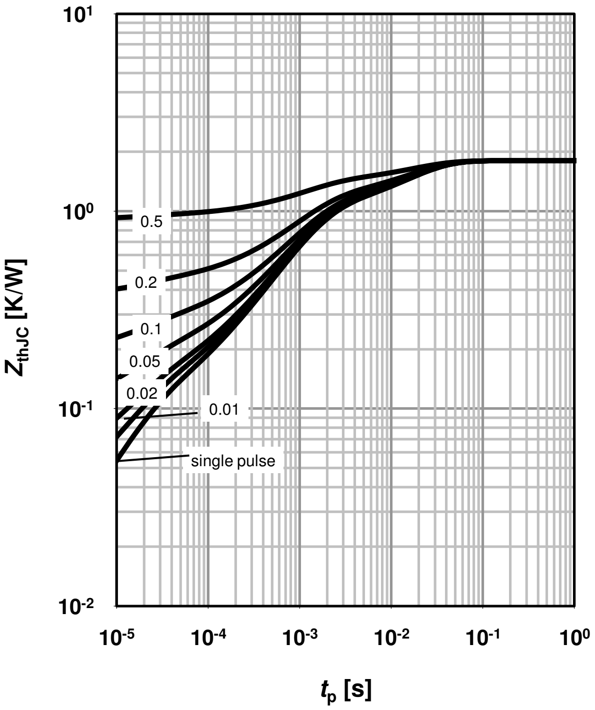
parameter: D=t_p/T



8 Max. transient thermal impedance (Q2)

Z_{thJC}=f(t_p)

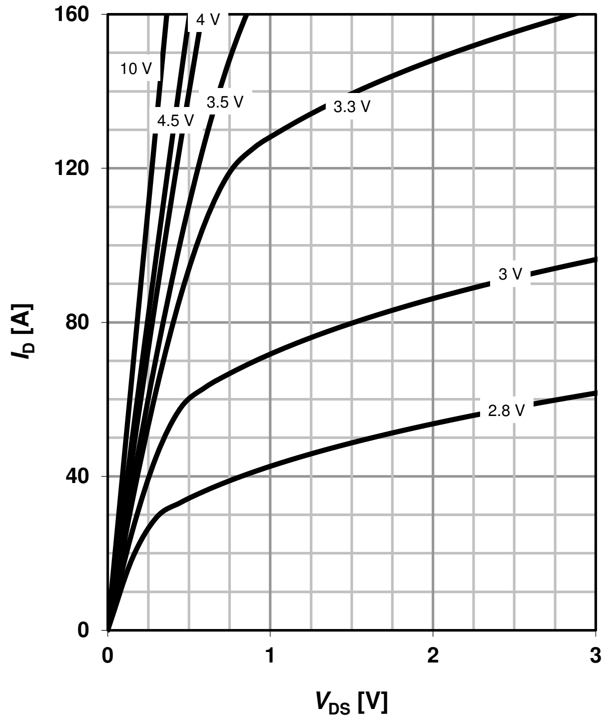
parameter: D=t_p/T



9 Typ. output characteristics (Q1)

I_D=f(V_{DS}); T_j=25 °C

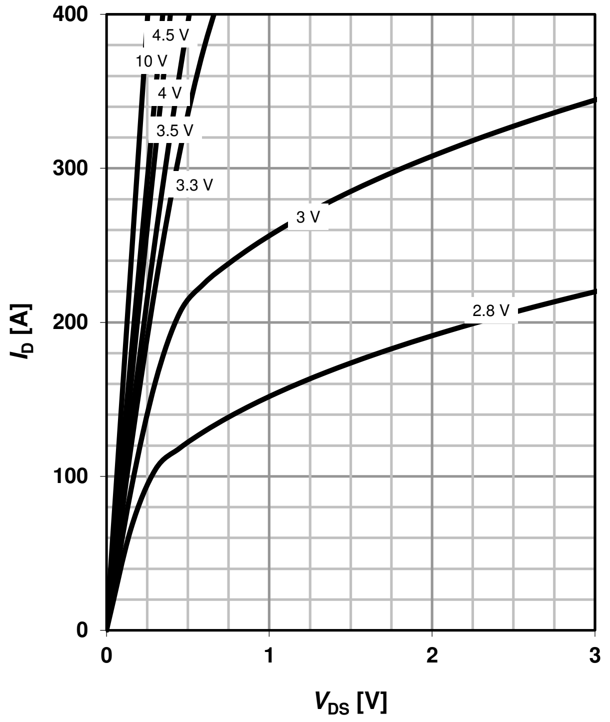
parameter: V_{GS}



10 Typ. output characteristics (Q2)

I_D=f(V_{DS}); T_j=25 °C

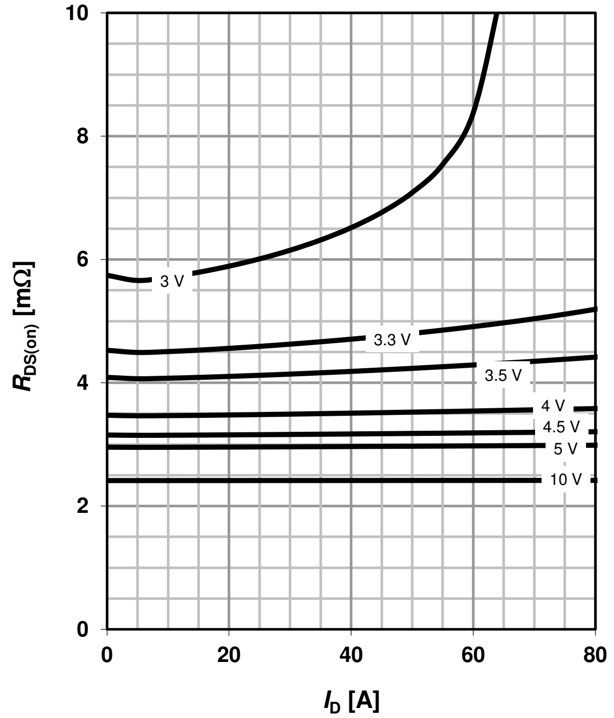
parameter: V_{GS}



11 Typ. drain-source on resistance (Q1)

$R_{DS(on)}$=f(I_D); T_j=25 °C

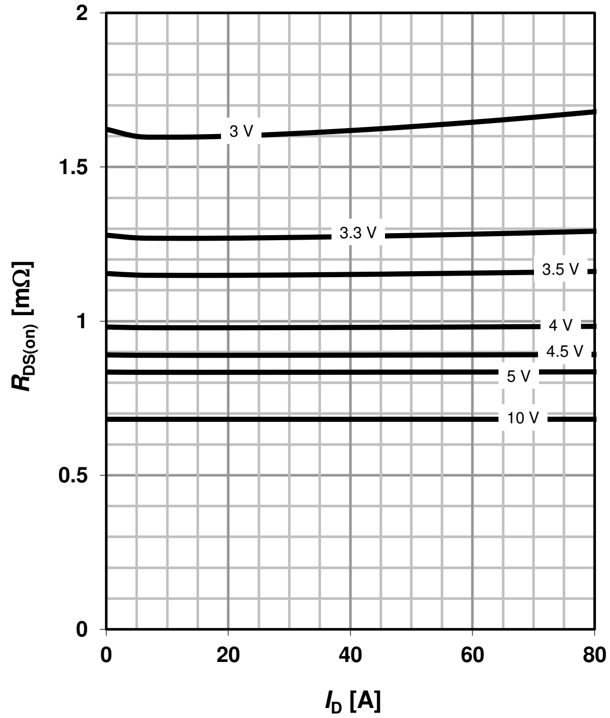
parameter: V_{GS}



12 Typ. drain-source on resistance (Q2)

$R_{DS(on)}$=f(I_D); T_j=25 °C

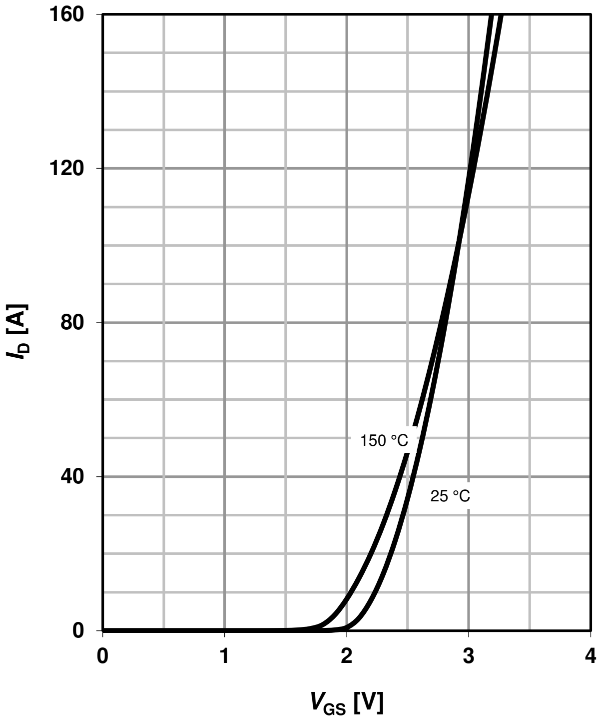
parameter: V_{GS}



13 Typ. transfer characteristics (Q1)

I_D=f(V_{GS}); |V_{DS} |>2 | I_D| $R_{DS(on)max}$

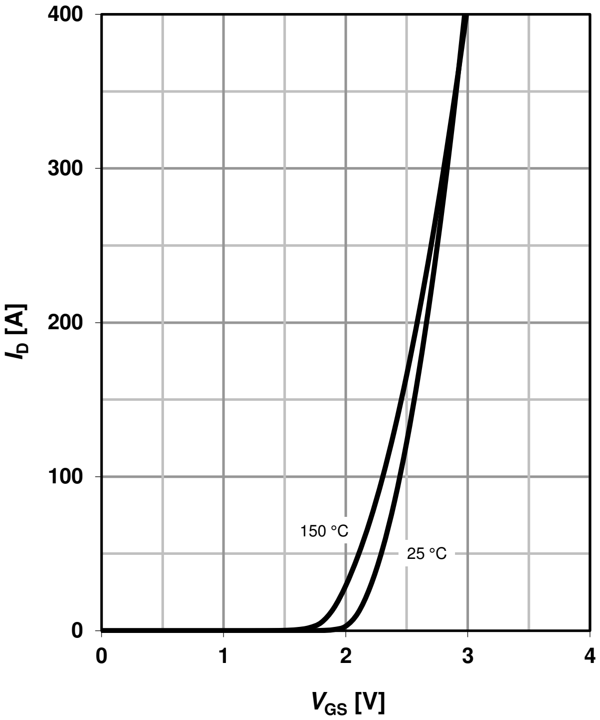
parameter: T_j



14 Typ. transfer characteristics (Q2)

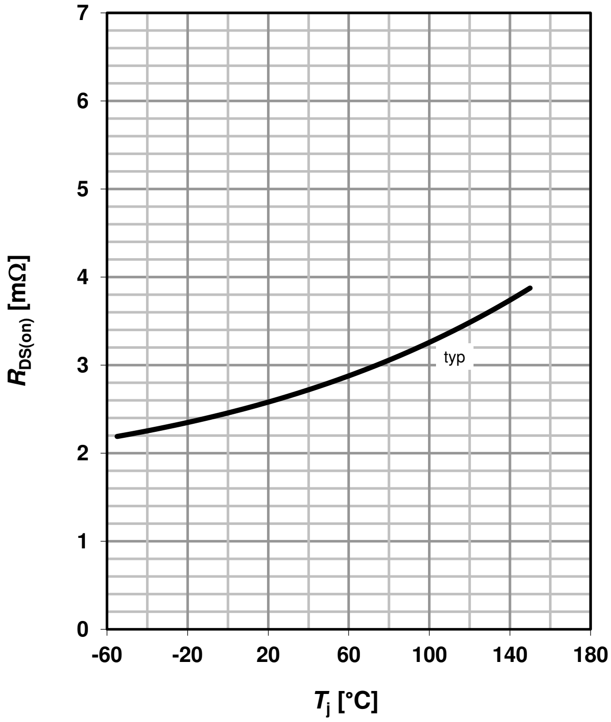
I_D=f(V_{GS}); /V_{DS} |>2 | I_D/ $R_{DS(on)max}$

parameter: T_j



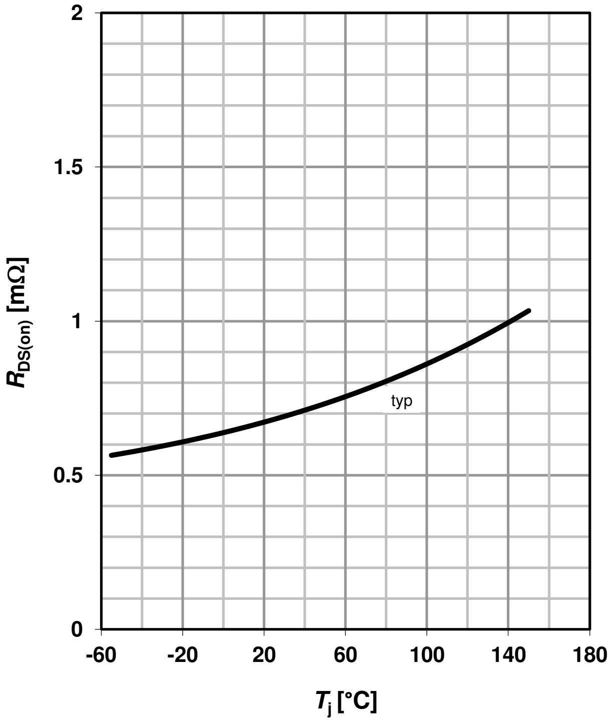
15 Drain-source on-state resistance (Q1)

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



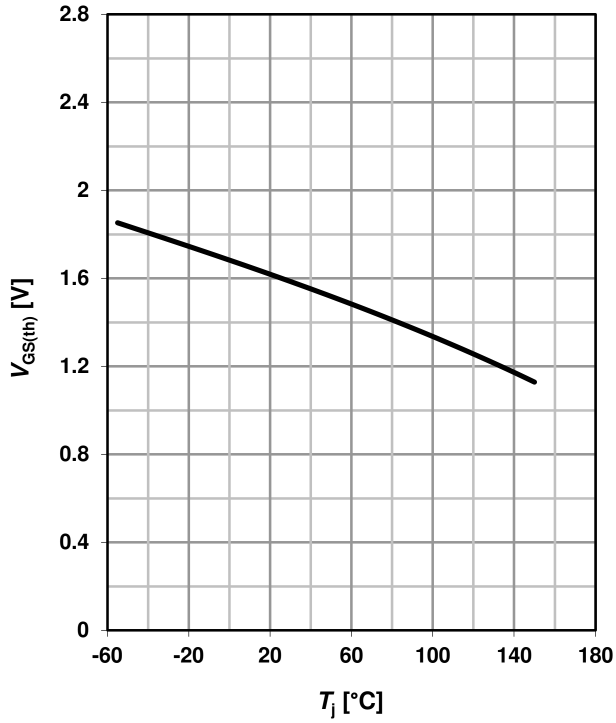
16 Drain-source on-state resistance (Q2)

$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V



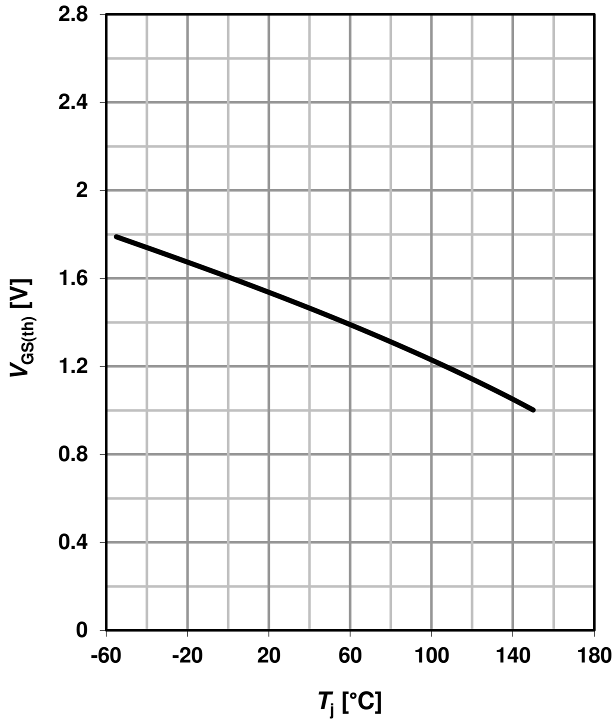
17 Typ. gate threshold voltage (Q1)

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



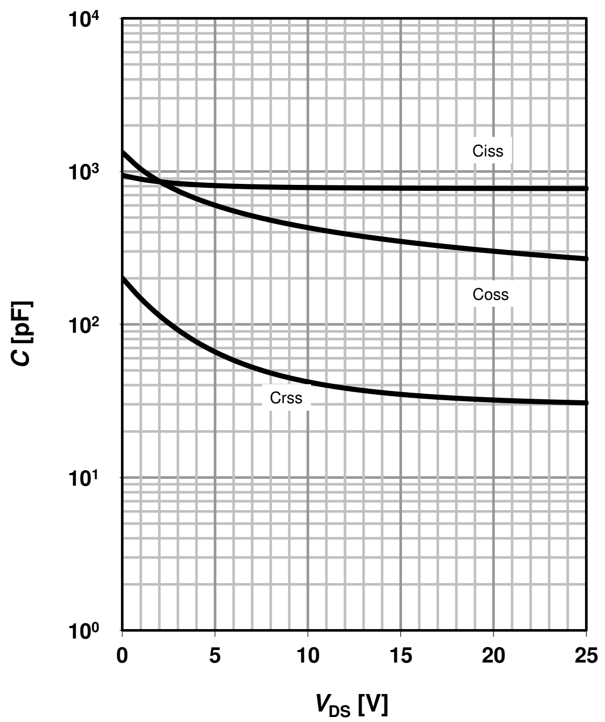
18 Typ. gate threshold voltage (Q2)

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}; I_D=250 µA



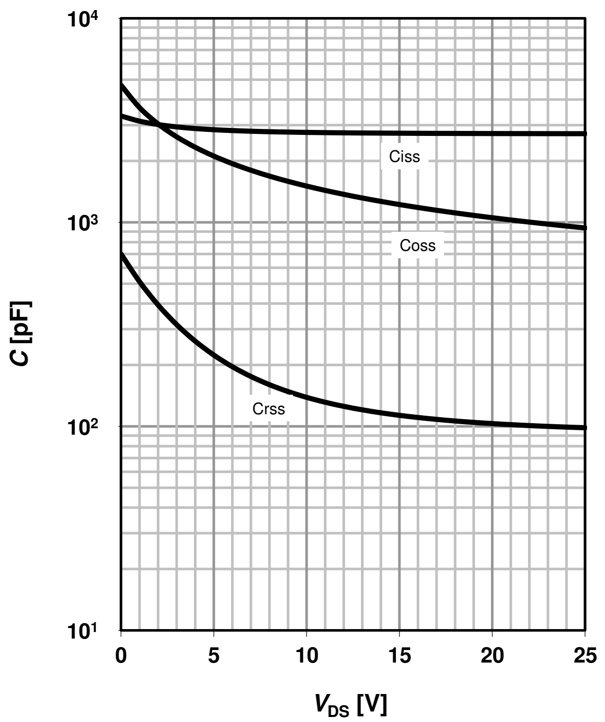
19 Typ. capacitances (Q1)

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



20 Typ. capacitances (Q2)

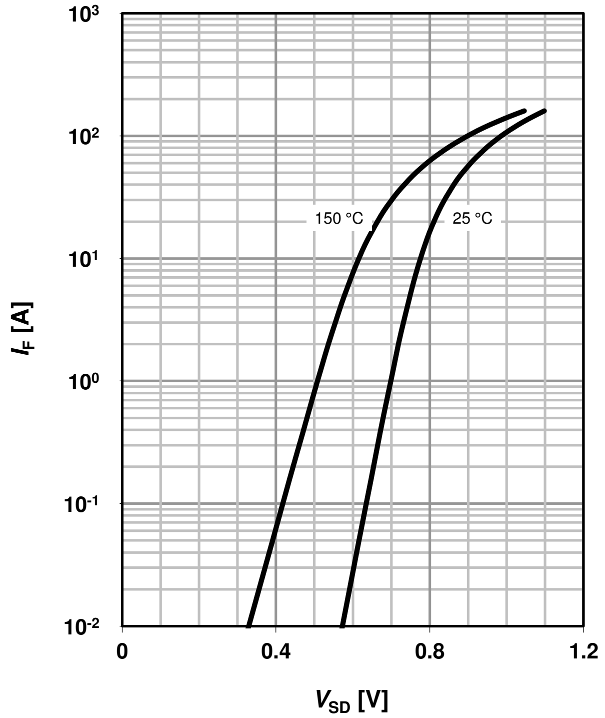
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



21 Forward characteristics of reverse diode (Q1)

I_F=f(V_{SD})

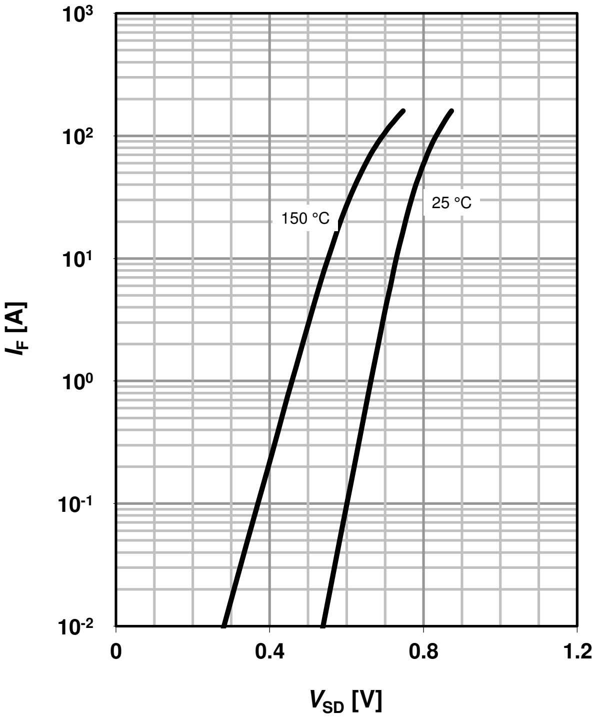
parameter: T_j



22 Forward characteristics of reverse diode (Q2)

I_F=f(V_{SD})

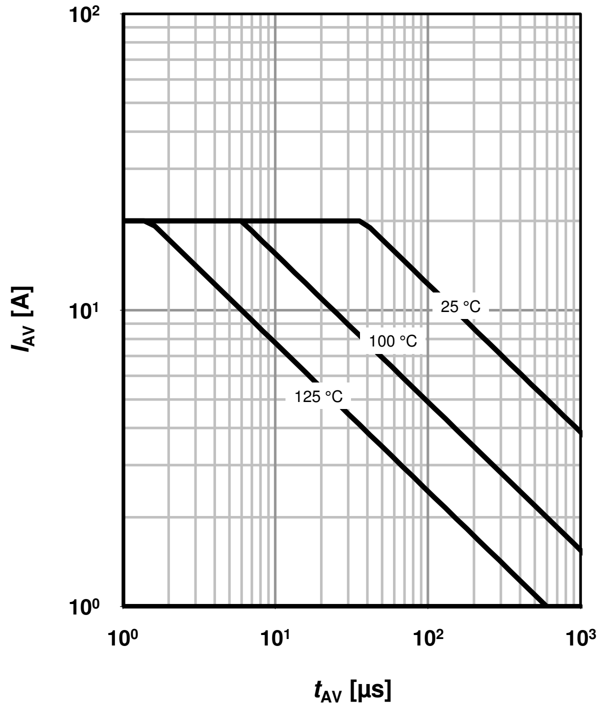
parameter: T_j



23 Avalanche characteristics (Q1)

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

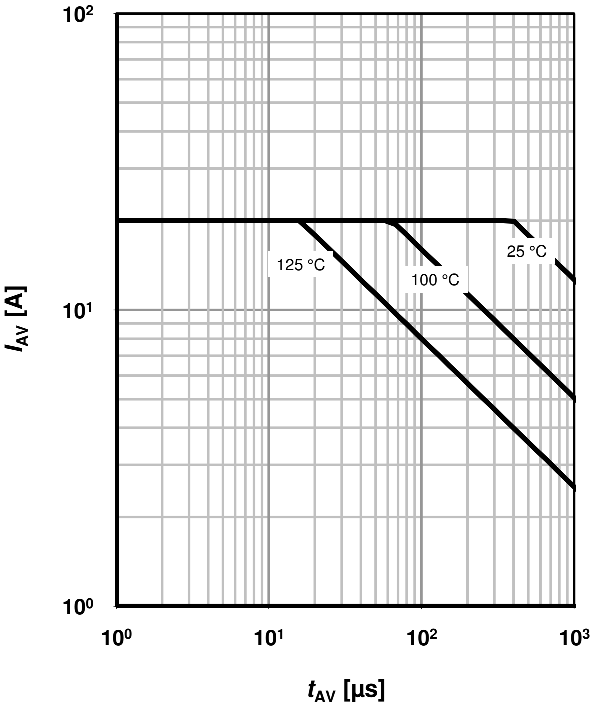
parameter: $T_{j(start)}$



24 Avalanche characteristics (Q2)

I_{AS}=f(t_{AV}); R_{GS}=25 Ω

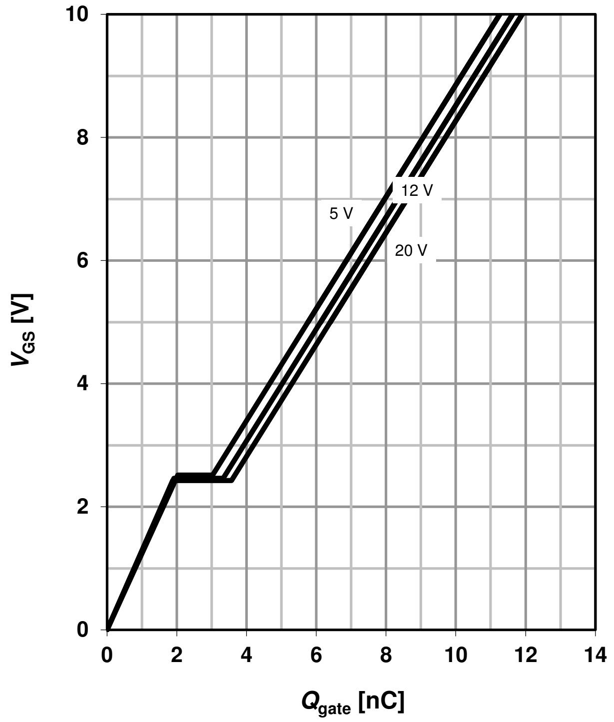
parameter: $T_{j(start)}$



25 Typ. gate charge (Q1)

V_{GS}=f(Q_{gate}); I_D=20 A pulsed

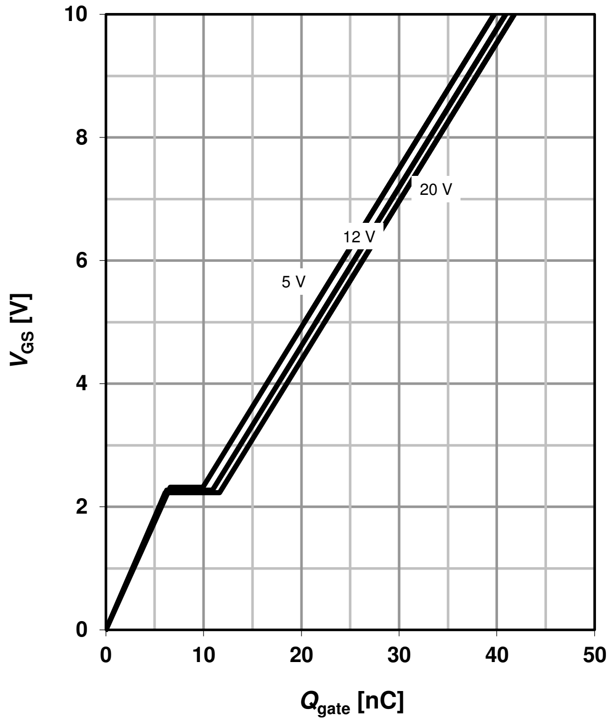
parameter: V_{DD}



26 Typ. gate charge (Q2)

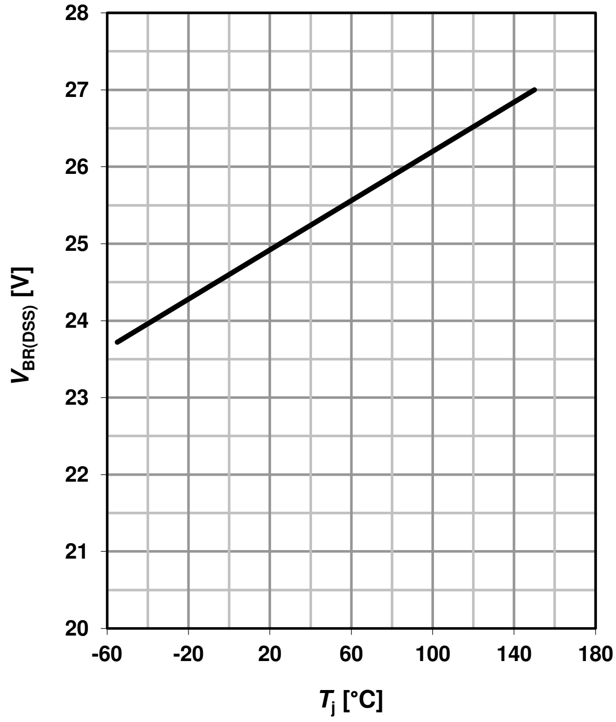
V_{GS}=f(Q_{gate}); I_D=20 A pulsed

parameter: V_{DD}



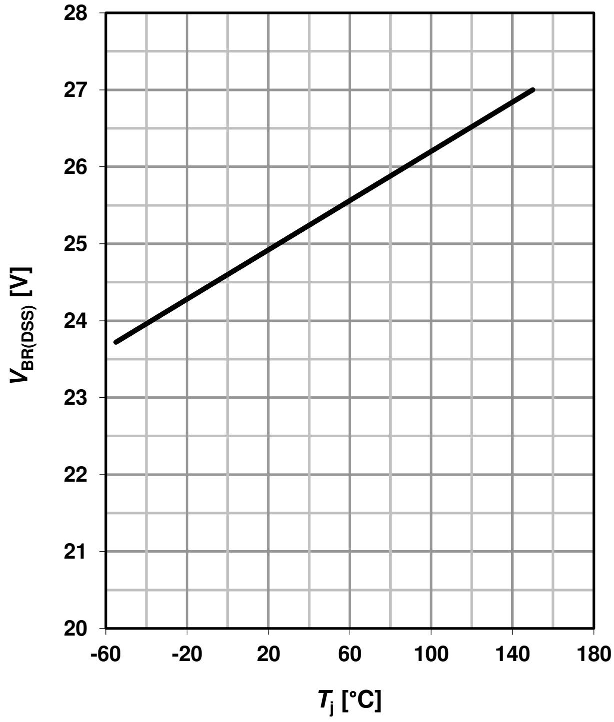
27 Drain-source breakdown voltage (Q1)

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



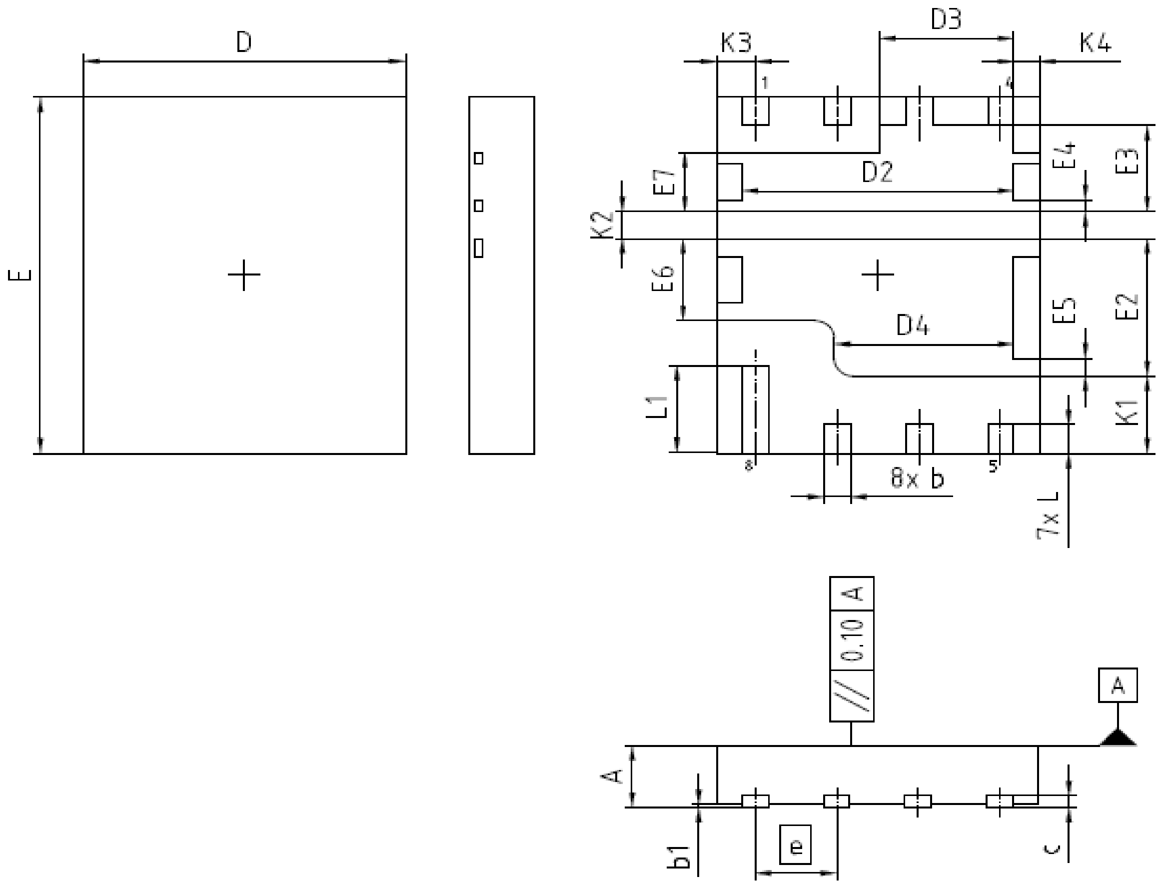
28 Drain-source breakdown voltage (Q2)

$V_{BR(DSS)}$=f(T_j); I_D=1 mA



Package Outline

PG-TISON8-4

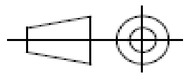


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.15	0.035	0.045
b	0.31	0.51	0.012	0.020
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	4.90	5.10	0.193	0.201
D2	4.12	4.32	0.162	0.170
D3	1.99	2.19	0.078	0.086
D4	2.69	2.89	0.106	0.114
E	5.90	6.10	0.232	0.240
E2	2.22	2.42	0.087	0.095
E3	1.35	1.55	0.053	0.061
E4	0.10	0.30	0.004	0.012
E5	0.20	0.40	0.008	0.016
E6	1.29	1.49	0.051	0.059
E7	0.90	1.10	0.035	0.043
e	1.27 (BSC)		0.05 (BSC)	
N	8		8	
L	0.38	0.58	0.015	0.023
L1	1.38	1.58	0.054	0.062
K1	1.20	1.40	0.047	0.055
K2	0.35	0.55	0.014	0.022
K3	0.50	0.70	0.020	0.028
K4	0.29	0.49	0.011	0.019

DOCUMENT NO.
Z8B00176527

SCALE 0 2.5 5mm

EUROPEAN PROJECTION

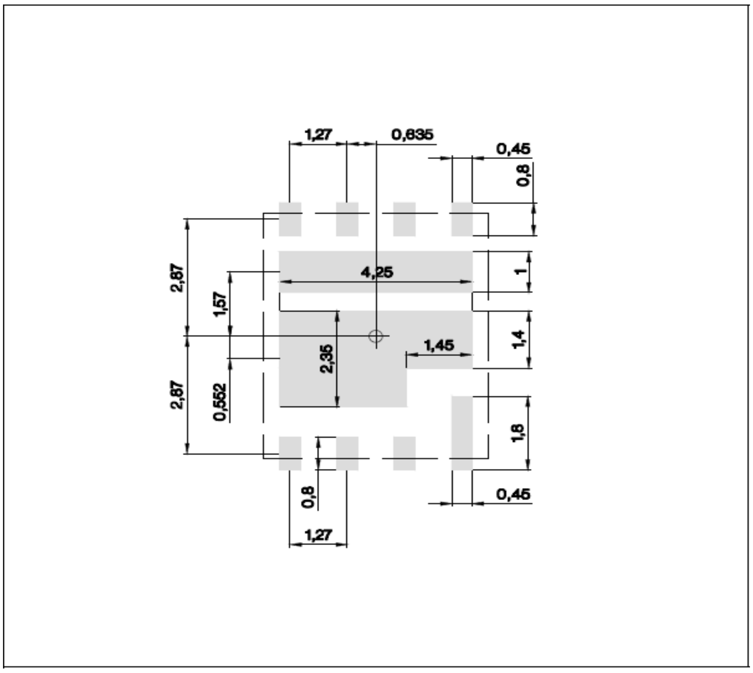


ISSUE DATE
13-03-2015

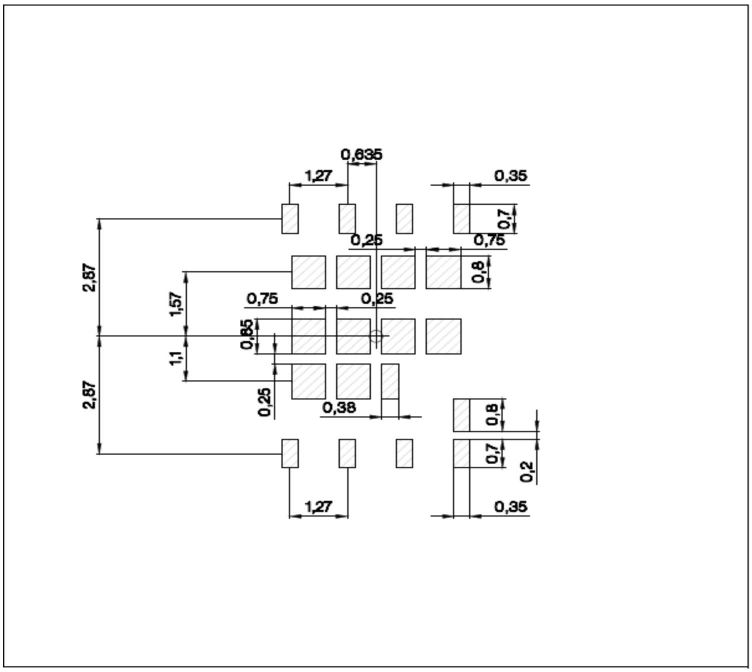
REVISION
01

Boardpads & Apertures

PG-TISON8-4



copper



stencil apertures

All the dimensions in mm

Revision History

BSG0811ND

Revision: 2016-03-24, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-03-17	Release of final version
2.1	2016-03-24	Update package drawing

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Published by
Infineon Technologies AG
81726 München, Germany

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.