

Features

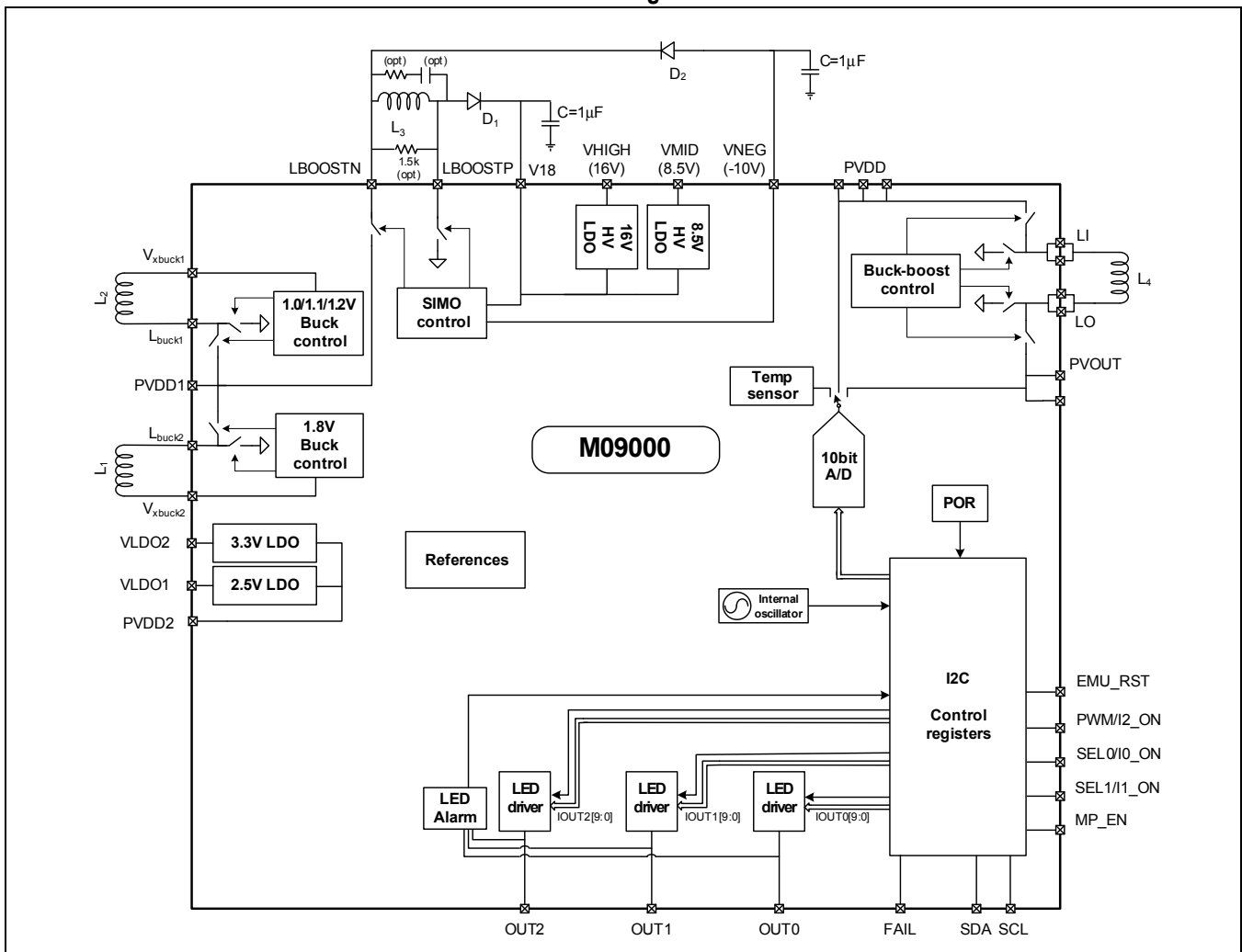
- Three programmable 1.2A common anode LED/laser drivers with integrated buck-boost converter and PWM current control
- 1.8 V and 1.0/1.1/1.2/1.8 V Buck converters capable of 300 mA current loads
- 2.5 V (30 mA) and 3.3 V (150 mA) LDO regulators
- Accurate DMD supply generators (+16 V/8.5 V and -10 V)
- Monitor and fault protection features
- I²C interface

Applications

- Portable video projector systems

The M09000 is a highly integrated, high efficiency driver and power management IC designed for embedded DLP pico projectors. It provides three programmable LED/laser drivers with integrated buck-boost converter, power management functionalities, including high voltage generators for DMD. All of these functions are supported while operating from a single Li-Ion cell.

Block Diagram



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Ordering Information

Part Number	Package	Case Operating Temperature
M09000-14	5x5 mm 40-pin QFN	-40 °C to +85 °C
* The letter "G" designator after the part number indicates that the device is RoHS compliant.		

Revision History

Revision	Level	Date	Description
V2	Release	July 2015	Updated registers.
D (V1)	Release	December 2012	Silicon updated to version -14. Changed typical LED Driver current accuracy in Table 1-3 . Changed typical Undervoltage Lockout in Table 1-4 . Changed ADC Offset Error, Slope Error and Full Scale in Table 1-5 . Changed LDO operating voltage in Table 1-7 and Table 1-8 . Changed Vih specification in Table 1-11 .
C (V1P)	Preliminary	July 2012	Updated register section.
B (V2A)	Advance	March 2012	Changed the Operating Voltage from a minimum of 3.15 to 2.6 and a maximum of 4.3 to 5.25. This change is reflected in Table 1-2 , Table 1-7 , Table 1-8 and Table 1-9 . Changed Pin 11 from GND to PVDDM (V _{DD} Supply). This is reflected in Figure 2-1 and Table 2-1 .
A (V1A)	Advance	February 2012	Initial release.

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1.0 Electrical Characteristics

1.1 Absolute Maximum Ratings

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
PVDDX	3.7 V supplies	—	-0.4	—	+5.5	V
PVOUT	Buck-boost DC-DC converter output	—	-0.4	—	+5.5	V
IOUT0, IOUT1, IOUT2	Output pins for driving LED	—	-0.4	—	+5.5	V
LI, LO	External inductor pins for DC-DC converter	—	-0.4	—	+5.5	V
T _{JCTN}	Junction Temperature	1	-40	—	+125	°C
T _{STG}	Storage Temperature	—	-65	—	+150	°C
V18, VHIGH, VMID	Positive DMD outputs	—	-0.4	—	+19.8	V
VNEG	Negative DMD output	—	-12.0	—	+0.4	V
LBOOSTP	Positive side of inductor for DMD	—	-0.4	—	+19.8	V
LBOOSTN	Negative side of inductor for DMD	—	-12	—	+5.5	V
LBUCK1, LBUCK2	Inductor pins for buck converters 1 & 2	—	-0.4	—	+5.5	V
VXBUCK1	Output of buck converter 1	—	-0.4	—	+5.5	V
VXBUCK2	Output of buck converter 2	—	-0.4	—	+2.0	V
VLDO1, VLDO2	LDO regulator output 1 & 2	—	-0.4	—	+5.5	V
SCL, SDA	I ² C interface	—	-0.4	—	+5.0	V
FAIL, EMU_RST	Fault signal output and EMU reset pins	—	-0.4	—	+5.5	V
PWM, SEL0, SEL1	Strobe input and PWM input pins	—	-0.4	—	+5.5	V
MP_EN	Enable pin	—	-0.4	—	+5.5	V
NOTES:						
1. $\theta_{JC} = 16.4$ °C/W.						

1.2 Operating Conditions

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Table 1-2. Operating Conditions

Parameter	Notes	Minimum	Typical	Maximum	Units
PVDDD, PVDD1, PVDDM	1	2.7	3.7	5.25	V
Disable current (EN=L)	—	—	1	25	μA
Active current (EN=H)	2	—	2	—	mA

NOTES:

- All features will be functional down to 3.15 V.
- No current drawn by high voltage supplies, buck regulators, LDOs or LEDs. Exclude power dissipation of I^2C .

1.3 LED Driver Characteristics

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{\text{CASE}} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

Table 1-3. LED Driver Characteristics

Parameter	Notes	Minimum	Typical	Maximum	Units
Output current	1	—	—	1.2	A
Current accuracy	2	—	+/-3.6	—	%
Current step	3	—	1073	—	μA
Current turn-on time	4	—	30	40	μs
Current ripple	—	-2	—	2	%
Current overshoot	—	—	—	10	%
Driver impedance	5	—	100	—	$\text{m}\Omega$
PWM input frequency	—	4.5	12.5	20	kHz
PWM resolution	—	—	—	8	bits
PWM time out	6	140	200	540	μs

NOTES:

- At PVDDD=3.3 V. 1A for PVDDD=3.15 V. Limited by buck boost converter.
- Part to part variation measured at room temperature @ 300 mA.
- Scale DAC set to maximum scale (3Fh).
- PVOUT transitioning from 2.5 V to 3.5 V, $I_{\text{OUT}}=1\text{A}$, 10-90%. Limited by DC-DC converter slewing.
- $I_{\text{out}}=500\text{ mA}$. Impedance can be lowered at the expense of accuracy.
- Time out is $2T_{\text{ck}}+40\text{ }\mu\text{s}$.

1.4 Buck-Boost DC-DC Converter

Typical values: Ta=25 °C, PVDDX=3.7 V.

Min and Max values: T_{CASE} = -40 °C to +85 °C, PVDDX = 2.7 V to 5.25 V.

Table 1-4. Buck-Boost DC-DC Converter

Parameter	Notes	Minimum	Typical	Maximum	Units
Output voltage	1	2	—	4.6	V
Overvoltage protection	2	—	5.2	—	V
Input under voltage lock-out	—	—	3.14	—	V
Current limiter range	3	0.2	—	6.4	A
Current limiter accuracy	4	-25	—	+25	%
Soft start time	—	—	1	—	msec

NOTES:

- PVDDD=3.15 V, I_{out}=1.2A. Output under voltage alarm set at 1.5 V.
- Programmable 4.6 V, 4.8 V, 5.0 V (default), 5.2 V.
- Programmable.
- Valid in the range of 1 A to 6.4 A.

1.5 Monitor ADC Specifications

Typical values: Ta=25 °C, PVDDX=3.7 V.

Min and Max values: T_{CASE} = -40 °C to +85 °C, PVDDX = 2.7 V to 5.25 V.

Table 1-5. Monitor ADC Specifications

Parameter	Notes	Minimum	Typical	Maximum	Units
Resolution	—	—	—	10	bits
Full scale input	—	4.9	5.27	5.6	V
Step size	—	—	5.17	—	mV
Offset error	—	—	29	—	mV
Conversion rate	1	—	4	—	ksps

NOTES:

- ADC is interleaved between temp sensor, VBAT and PVOUT in this order conversion initiated by SELX change: will require 750 μsec to complete all 3 conversion

1.6 DMD Power

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

Table 1-6. DMD Power

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{HIGH}	DMD VHIGHigh voltage (pin 37)	—	15.68	16	16.32	V
I_{HIGH}	Allowable output current to maintain VHIGHigh regulation and ripple	—	—	—	4	mA
V_{MID}	DMD VMID voltage (pin 36), register 09h[3] = 0b	—	8.33	8.5	8.67	V
	DMD VMID voltage (pin 36), register 09h[3] = 1b	1		5		
I_{MID}	Allowable output current to maintain VMID regulation and ripple	—	—	—	3	mA
V_{NEG}	DMD VNEG voltage (pin 39)	—	-10.2	-10	-9.8	V
I_{NEG}	Allowable output current to maintain VNEG regulation and ripple	—	—	—	4	mA
IBAT	Typical current draw from battery	2	—	9.5	—	mA
T_1	EN=H → EMU_RST=H	3	100	120	240	msec
T_2	$V_{MID}=H$ → V_{HIGH}, V_{NEG} start	3	3.2	8	11	msec
T_3	V_{HIGH}, V_{NEG} start turn-off → V_{MID} start turn-off	3	8	10	12	msec
T_4	V_{MID} start turn-off → EMU_RST=L	3	150	180	300	msec
Ripple	VHIGH, VMID, VNEG IOU=4 mA, PVDD=3.7, COUT=1 μ F	—	—	—	200	mV
Line regulation	$V_{HIGH}, V_{MID}, V_{NEG}$	—	—	—	20	mV/V
Load regulation	VHIGH, VMID, VNEG IOU=0 → 4 mA, PVDD=3.7, COUT=1 μ F	—	—	—	15	V/A
NOTES:						
1. V_{HIGH} and V_{NEG} disabled at register 2Eh[0] = 1b and 2Eh[2] = 1b.						
2. Current draw for a given load depends on external component selected (inductor ESR and diode leakage).						
3. Programmable through registers 0x0Bh and 0x0Ch.						

1.7 3.3 V LDO Regulator (VLDO2)

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 3.7\text{ V}$ to 5.25 V .

Table 1-7. 3.3 V LDO Regulator (VLDO2)

Parameter	Notes	Minimum	Typical	Maximum	Units
Operating voltage	—	3.7		5.25	V
Turn-on time	—	—	—	5	msec
LDO mode minimum operating voltage	1	—	3.4	3.6	V
Regulated voltage in LDO mode	1	3.25	3.3	3.36	V
High side switch resistance $PVDD2 < 3.4\text{ V}$	1	—	—	1	Ω
Current load	—	—		150	mA
Load regulation	—	—	10	30	mV
Line regulation	1	—	—	0.8	%

NOTES:

- The maximum VLDO2 voltage will be limited by the battery voltage and the switch resistance.

1.8 2.5 V LDO Regulator (VLDO1)

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.8\text{ V}$ to 5.25 V .

Table 1-8. 2.5 V LDO Regulator (VLDO1)

Parameter	Notes	Minimum	Typical	Maximum	Units
Operating voltage	—	2.8	3.7	5.25	V
Turn-on time	—	—	—	5	msec
Output voltage	—	2.38	2.5	2.62	V
Current load	—	—		30	mA
Load regulation	—	—	10	30	mV
Line regulation	—	—	—	0.8	%

1.9 Buck Regulators (VXBUCK1/2)

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

Table 1-9. Buck regulators (VXBUCK1/2)

Parameter	Notes	Minimum	Typical	Maximum	Units
Operating voltage	—	2.7	3.7	5.25	V
Turn-on time	—	—	—	5	msec
Output voltage ripple (1.2/1.8 V regulator)	—	—	2	—	%
Output voltage (1.2 V regulator)	—	1.14	1.2	1.26	V
Current load (1.2 V regulator)	—	—	—	300	mA
Output voltage (1.8 V regulator)	—	1.71	1.8	1.89	V
Current load (1.8 V regulator) ¹	—	—	—	300	mA

1.10 Internal Temperature Sensor

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

Table 1-10. Internal Temperature Sensor

Parameter	Notes	Minimum	Typical	Maximum	Units
Range	—	—	-40 to 155	—	$^\circ\text{C}$
Overtemperature alarm with default setting (register programmable at 0x18)	—	113	120	128	$^\circ\text{C}$
Temperature step	—	—	0.45	—	$^\circ\text{C}$
Absolute accuracy	1	—	+/-8	—	$^\circ\text{C}$

NOTES:

1. After system calibration at room temperature (one point calibration).

1.11 CMOS Pin Characteristics

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

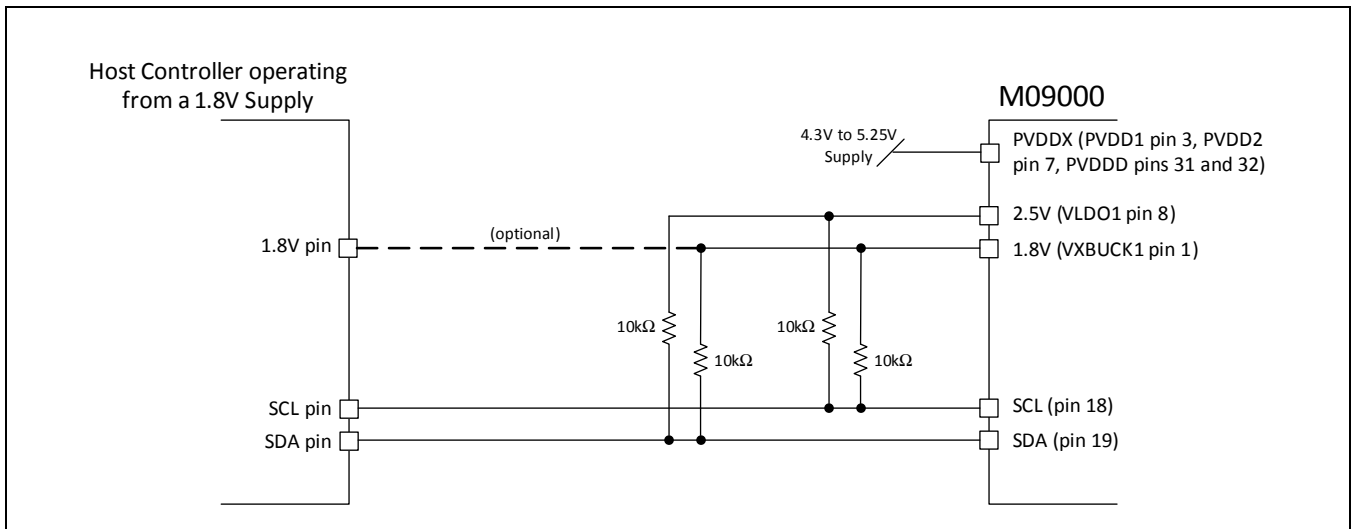
Table 1-11. CMOS Pins Characteristics

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
V_{IH}	High level input voltage, pins SDA and SCL for $PVDDX \leq 4.3\text{V}$	1	1.65	—	3.63	V
	High level input voltage, pins SDA and SCL for $4.3\text{V} < PVDDX \leq 5.25\text{V}$	1,2	1.83	—		
	High level input voltage, for input pins other than SDA and SCL and for $PVDDX \leq 4.3\text{V}$	1	1.5	—		
	High level input voltage, for input pins other than SDA and SCL and for $4.3\text{V} < PVDDX \leq 5.25\text{V}$	1,2	1.61	—		
V_{IL}	Low level input voltage	—	0	—	0.4	V
V_{OL}	Low level output voltage	3	0	—	0.4	V
V_{OH}	High level output voltage	4	—	—	3.63	V

NOTES:

1. Digital pins are 3.3 V (+/-10%) tolerant if battery voltage is higher than 3.15 V.
2. See Figure 1-1 for recommended pull-up configuration for $PVDDX > 4.3\text{V}$.
3. SDA/FAULT, $I_{out}=3\text{ mA}$
4. Open drain output.

Figure 1-1. I2C Pull-up for PVDDX from 4.3V to 5.25V



1.12 I²C Timing Specifications^{1,2}

Typical values: $T_a=25\text{ }^\circ\text{C}$, $PVDDX=3.7\text{ V}$.

Min and Max values: $T_{CASE} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $PVDDX = 2.7\text{ V}$ to 5.25 V .

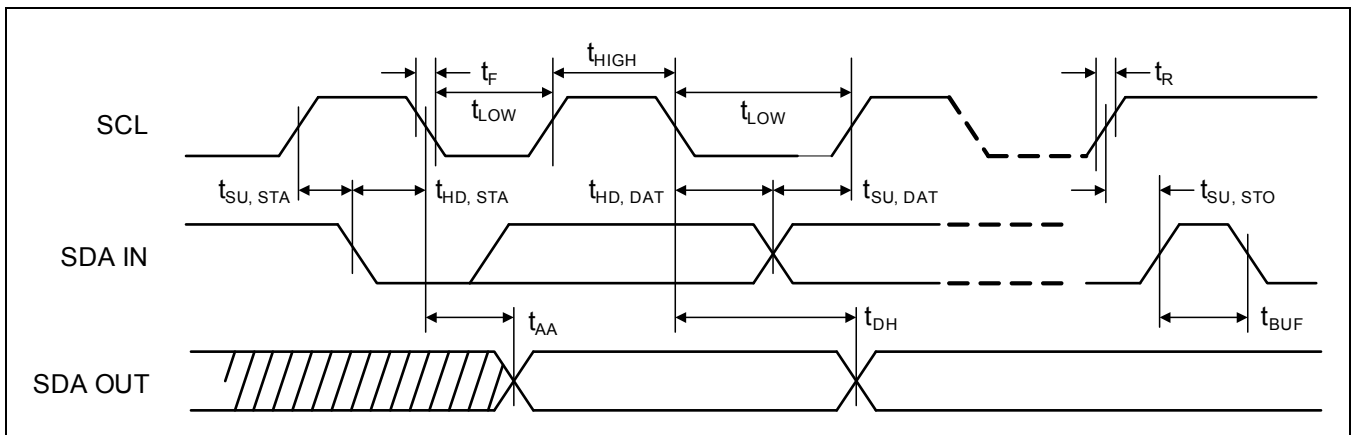
Table 1-12. I²C Timing Specifications

Symbol	Parameter	Notes	Minimum	Typical	Maximum	Units
f_{SCL_MASTER}	Clock Frequency, SCL_M		—	—	400	kHz
t_{LOW}	Clock Pulse Width Low		160	—	—	ns
t_{HIGH}	Clock Pulse Width High		60	—	—	ns
t_{AA}	Clock Low to Data Out Valid		0	—	70	ns
$t_{HD,STA}$	Start Hold Time		160	—	—	ns
$t_{SU,STA}$	Start Set-up Time		160	—	—	ns
$t_{HD,DAT}$	Data In Hold Time		0	—	—	ns
$t_{SU,DAT}$	Data In Set-up Time		10	—	—	ns
$R_{PULL-UP}$	Outputs (SDA,FAULT) internal pull-up resistor value to PVDD2	2	—	250	—	k Ω
$t_{SU,STO}$	Stop Set-up Time		160	—	—	ns
t_{DH}	Data Out Hold Time		5	—	—	ns

NOTES:

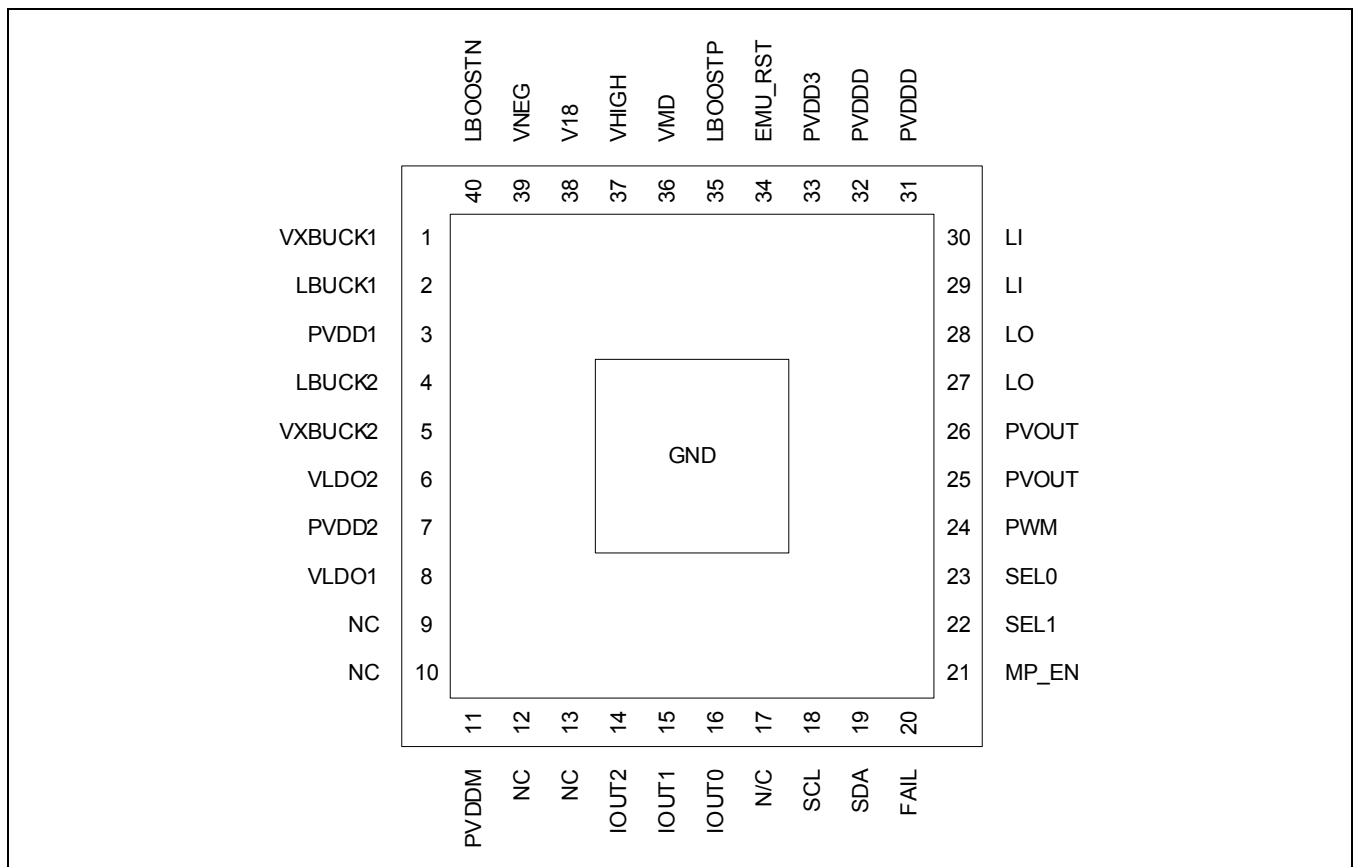
1. Guaranteed by design and characterization.
2. 4.7 k Ω should be added externally to the proper termination voltage for $PVDDX < 4.3\text{V}$. See Figure 1-2 for $PVDDX \geq 4.3\text{V}$.

Figure 1-2. I²C Timing Diagram



2.0 Pin Descriptions and Package Outline Drawings

Figure 2-1. M09000 Pinout Diagram



2.1 Pin Descriptions

Table 2-1. Pin Descriptions

Pin#	Name	Comment	Type	Description
1	VXBUCK1		A	VX buck converter 1 (1.0/1.1/1.2/1.8 V)
2	LBUCK1		A	Inductor for buck converter 1
3	PVDD1		P	Buck converters V_{DD}
4	LBUCK2		A	Inductor for buck converter 2
5	VXBUCK2		A	VX buck converter 2 (1.8 V)
6	VLDO2		P	LDO regulator output 2 (3.3 V)
7	PVDD2		P	Analog V_{DD}
8	VLDO1		P	LDO regulator output 1 (2.5 V)
9	NC		—	No connect
10	NC		—	No connect
11	PVDDM		P	Auxiliary supply
12	NC		—	No connect
13	NC		—	No connect
14	IOUT2		A	LED Current output 2. Add 100 k Ω to ground at this pin.
15	IOUT1		A	LED Current output 1. Add 100 k Ω to ground at this pin.
16	IOUT0		A	LED Current output 0. Add 100 k Ω to ground at this pin.
17	NC		I	Not connected
18	SCL	CMOS	I	I ² C clock
19	SDA	CMOS (PU)/Open collector	I/O	I ² C data
20	FAIL	Open collector (PU)	O	Fault signal (active low)
21	MP_EN	CMOS (PD)	I	Enable
22	SEL1	CMOS (PD)	I	Strobe input
23	SEL0	CMOS (PD)	I	Strobe input
24	PWM	CMOS (PD)	I	PWM input (for DLP systems)
25	PVOUT		P	DC-DC converter output (LEDs anode)
26	PVOUT		P	DC-DC converter output (LEDs anode)
27	LO		A	Inductor output (LED driver)
28	LO		A	Inductor output (LED driver)
29	LI		A	Inductor input (LED driver)
30	LI		A	Inductor input (LED driver)
31	PVDDD		P	Driver V_{DD} (3.2-4.2 V)

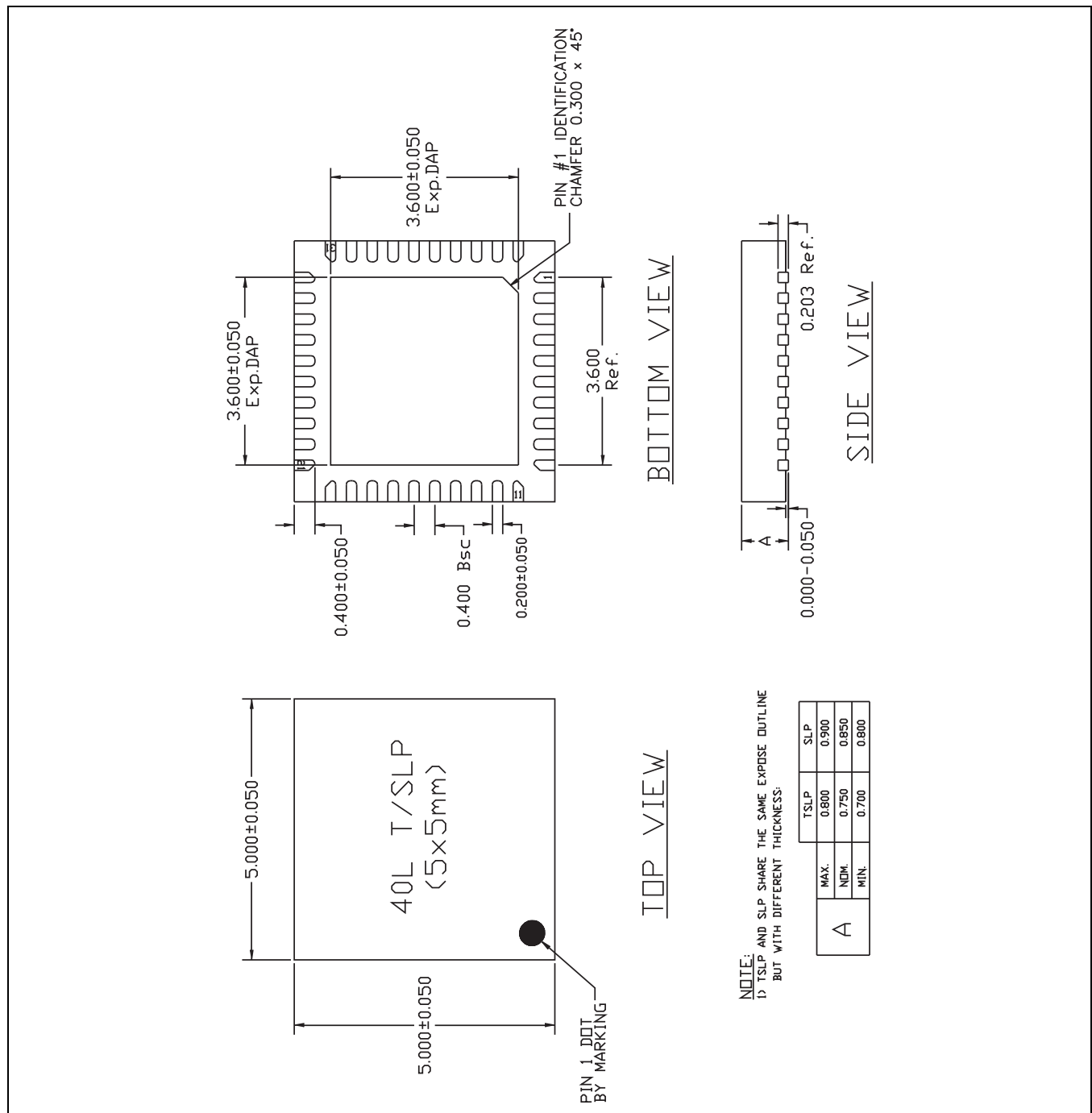
Table 2-1. Pin Descriptions

Pin#	Name	Comment	Type	Description
32	PVDDD		P	Driver V _{DD} (3.2-4.2 V)
33	PVDD3		P	Digital V _{DD}
34	EMU_RST	Open collector	O	EMU Reset (VHIGH,VMID,VNEG ready)
35	LBOOSTP		A	Positive side of inductor
36	VMID		A	+8.5 V output regulated voltage
37	VHIGH		A	+16 V output regulated voltage
38	V18		A	+18 V intermediate output voltage (from boost)
39	VNEG		A	-10 V output regulated voltage
40	LBOOSTN		A	Negative side of inductor

2.2 Package Information

The M09000 is packaged in a 5x5 mm 40pin QFN package with 0.4 mm pin pitch.

Figure 2-2. Package Information



3.0 Functional Description

The M09000 is a highly integrated LED/laser driver and PMIC for projection display applications.

The driver portion consists of three 10-bit LED drivers and a buck-boost converter to generate the voltage necessary to bias the common anode voltage for the LEDs. The DC-DC converter can operate from a Li-Ion battery (2.7-4.3 V).

The part is capable of generating the DMD power supplies and includes 2 buck converters: 1.0/1.1/1.2/1.8 V programmable and 1.8 V, and 2 LDO regulators: 2.5 V and 3.3 V.

Monitor functionality and safety features are integrated as well.

The M09000 can be controlled via the I²C interface.

3.1 User Configurable Registers

The M09000 is controlled by 49 user configurable registers in address locations 0x00 through 0x2E and registers 0x3A and 0x3B. The registers are described in the last section of this data sheet.

At power-up all registers will be set to their default value and the M09000 outputs will be disabled. To make the M09000 outputs active the MP_EN pin must be pulled high and the registers in [Chapter 3](#) below must have the appropriate values written to them through the I²C port on the M09000.

Each time the MP_EN pin goes low the registers will be cleared and reset to their default value. When MP_EN is returned to a high state these registers must be rewritten before the M09000 will be reactivated.

It is not necessary to write all 48 registers. If the default setting of a register is acceptable then it does not need to be written.

Below is a basic register configuration to enable all the outputs.

Table 3-1. First Step Basic Register Configuration (all other registers may be left at their default value)

Name	Address	Recommended Setting	Description
SOFT_RESET	0X30h	00h	After power up and MP_EN=HI, then write AAh (self resetting)
INPUT_CNTL	0x0E	27h	Configure inputs and assign LED outputs
OUTPUT_CNTLx	0x10, 0x11, 0x12	34h	Recommended LED driver configuration.
IOUTx_LSB	0x13[5:0]	00xxxxxb	Two least significant bits of output current setting
IOUTx_MSB	0x14, 0x15, 0x16	xxh	Eight most significant bits of output current setting.

Table 3-1. First Step Basic Register Configuration (all other registers may be left at their default value)

Name	Address	Recommended Setting	Description
HEADROOM_0, HEADROOM_1	0x19[3:0], 0x19[7:4], 0x1A[3:0]	0110b 1001b 1011b	Output headroom for 0 to 0.4A Output headroom for 0.4A to 0.8A Output headroom for 0.8A to 1.2A
BUCKBOOST_USR0	0x1B	3Ah	Buck-Boost disabled. Positive current limit set to 6.0A
BUCKBOOST_USR1	0x1C	98h	Recommended Buck-Boost converter configuration. Negative current limit set to 6.0A
BUCKBOOST_USR2	0x1D	5Fh	Recommended Buck-Boost converter configuration.
BUCKBOOST_USR3	0x1E	30h	Recommended Buck-Boost converter configuration.
BUCKBOOST_USR4	0x1F	F0h	Recommended Buck-Boost converter configuration.
HEADROOM_CTRL0	0x27h	10h	Recommended Buck-Boost converter control configuration.
HEADROOM_CTRL1	0x28h	17h	Recommended Buck-Boost converter control configuration.
TEMPSENS_CTRL0	0x29h	FFh	Recommended temperature sensor configuration.
DRV_CTRL	0x2Bh	C0h	Recommended Buck-Boost driver configuration
BUCKBOOST_STRT	0x2Ch	14h	Recommended Buck-Boost start-up configuration
BUCKBOOST_SPUP	0x2Dh	65h	Recommended Buck-Boost speed-up configuration

In LCOS applications the DMD supply may be used to generate 5V or some other voltage. In this case see [Section 3.5.1](#) for the configuration of registers 06h, 09h and 2Eh.

After the basic configuration is complete the Buck-Boost supply and DMD supply may be enabled.

Table 3-2. Second Step Basic Register Configuration (all other registers may be left unchanged)

Name	Address	Recommended Setting	Description
DMD_RISE	0x0B	25h	Enable DMD Supply
BUCKBOOST_USR0	0x1B	3Bh	Enable Buck-Boost Supply
FAIL_CTRL	0x21	88h	Clear alarm status

3.2 LED Drivers

The current is provided to the RGB LED through three 1.2 A high accuracy 10-bit common anode drivers controlled by pin.SEL0 and pin.SEL1 according to the following table:

Table 3-3. RGB LED Current Settings

[SEL1,SEL0]	Status
[1,1]	Blue ON
[1,0]	Green ON
[0,1]	Red ON
[0,0]	OFF

The channel associated with each color can be controlled by register **INPUT_CONT**[5:0]. If any of **INPUT_CONT** pairs of bit [1:0], [3:2] or [5:4] is 11b there is no decoding of the input signal and pin *SEL0*, *SEL1* and *PWM* control respectively channel *IOUT0*, *IOUT1* and *IOUT2*. In this mode of operation the PWM function is disabled. Please note that the PWM engine can also be shut down to save power by setting **INPUT_CONT**[7]=1b.

The current is controlled by programming registers **IOUTx.bit**[9:0]. Each current step corresponds to 1.17 mA.

It is possible to store preferred value of current into the M09000 in case a particular part is mated with an optical engine. The default value of the bits setting the output current (register 0x13h through 0x16h) can be programmed in the internal OTP memory so the white balance point of an engine mated with the M09000 can be stores into the device. Please refer to the paragraph regarding the OTP memory in Section 3.12 for details on THE programming procedure.

The M09000 features a PWM to current amplitude modulation converter. The current at the output can scale proportionally to the duty cycle of the signal applied to pin.PWM. For example, if the duty cycle at the PWM input is 25% the current at the output will be reduced to 25% of the value programmed in the M09000.

The change in the amplitude of the output current as a response to a change in duty cycle of the PWM input is not instantaneous; the current during the subsequent sub-frame will be adjusted provided that the change in PWM duty cycles happens 2 clock cycles plus 40 μ s before the change of sub-frame (toggling on pin.SEL0/pin.SEL1). This is defined as the time-out period.

The resolution of the PWM function is 8-bits: the M09000 is capable of resolving variations of 1/255 in the duty cycle of the PWM signal of frequency in the range of 5 kHz to 20 kHz. If PWM input is low continuously the output current will be forced to 1/255 of the full scale value.

To optimize power dissipation the headroom of each driver can be programmed using bits **HEADROOM_x**. To achieve the specified accuracy the drivers require 10 mV of headroom for each 100 mA of current delivered to the LED down to a minimum of 50 mV. This corresponds to a driver impedance of 100 m Ω .

For example, if the maximum current required in the system is 700 mA the headroom that must be programmed is 70 mV (0110 binary code). If the maximum current required in the system is 350 mA the headroom that can be programmed is 40 mV (0011 binary code) but to achieve the specified accuracy 50 mV (0011 binary code) should be used.

Because of the driver architecture, the current overshoot in the M09000 is maintained well below 10%.

The driver will issue an alarm at the pin.FAIL in case of open or shorted LED and in case the LED cathode is shorted to ground.

3.3 Buck-boost Converter

The M09000 buck-boost converter controls the common anode voltage of the LED sub-assembly to guarantee optimal system efficiency.

The M09000 automatically adjusts the anode voltage of the LED to guarantee enough headroom for the LED and the driver to operate.

The typical current turn-on, limited by the DC-DC converter slewing is 30 μ s with a transition of the LED anode voltage from 2.5 V to 3.5 V. This is very well representative of a red to green LED transition which is usually the slowest transition since the voltage difference between red and green LED is the highest.

The buck-boost converter is capable of delivering 1.2 A with a minimum battery voltage of 3.15 V (1 A at 2.7 V). The maximum buck-boost output voltage is 4.6 V.

The M09000 has a programmable undervoltage lockout at register **ALARM_CTRL0**.bit[7:6] and overvoltage protection.

Moreover, a programmable current limiter (both positive and negative) allows the user to select the most appropriate inductor characteristic for the specific application by trading off inductor area with series resistance.

The current limiters can be programmed through register **BUCKBOOST_USR0**.bit[5:1] and register **BUCKBOOST_USR1**.bit[4:0].

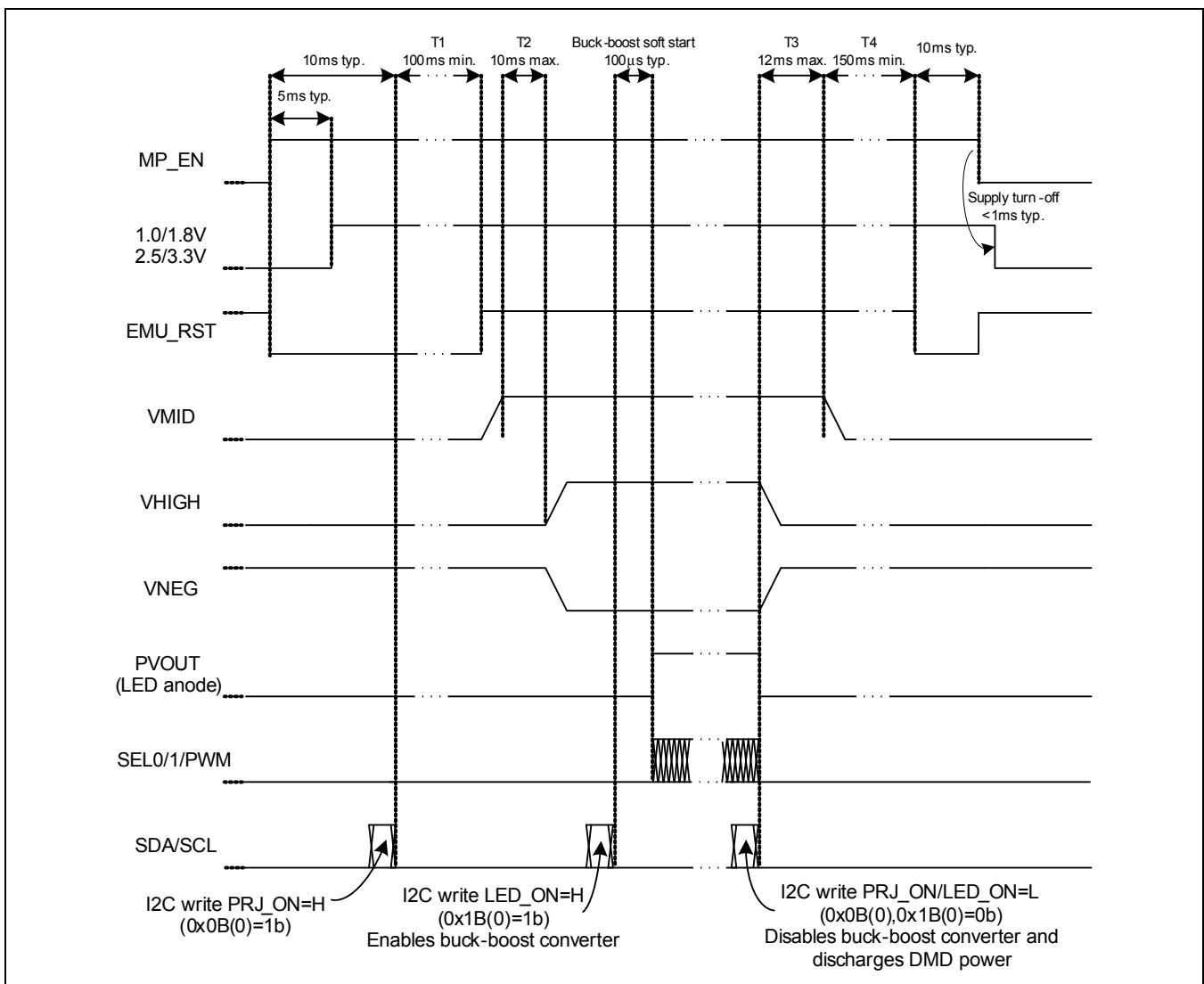
3.4 PMIC Functions

The M09000 generates all the necessary supplies from a single battery.

The power management portion includes DMD power generators, two buck converters which can generate 1.8 V and 1.0/1.1/1.2/1.8 V (programmable through BUCKV10_USR2[1:0]) and 2 LDO generators delivering 2.5 V and 3.3 V.

The following timing diagram details the power up sequence:

Figure 3-1. Power Up Sequence



It should be noticed that pin.MP_EN is capable of accepting 3.3 V as well as 1.8 V level signals provided that the battery voltage (PVDD2) is between 2.7 V and 5.25V.

The battery voltage is supplied to the power management blocks as illustrated in the block diagram on the front page of this document: PVDD1 power supplies current to the 2-buck converter and the DMD supplies generator while PVDD2 supplies the 2 LDO regulators. This allows for better noise isolation between the different supplies when appropriate decoupling is provided (1 μ F+10nF) for each one of them and a star connection to the battery is used from a board layout perspective.

LED_ON command enables the buck-boost converter. The SEL0/1 pins are locked out (i.e. will not be able to turn on the driver) unless LED_ON command is issued. The SEL0/1 pins will be able to control the drivers after the buck-boost soft-start: typically 100 μ s.

3.5 DMD Supply

The M09000 generates the high voltage DLP supplies according to the timing diagram in the previous paragraph and to the following table.

Table 3-4. DMD Supply Voltages

Supply Name	Voltage	Maximum Current Load
VHIGH	16 V+/-2%	4 mA
VMID	8.5 V+/-2%	4 mA
VNEG	-10+/-2%	4 mA

As illustrated in the block diagram, the M09000 requires only one external inductor and 2 Schottky diodes. Standard decoupling practices should be used at the input.

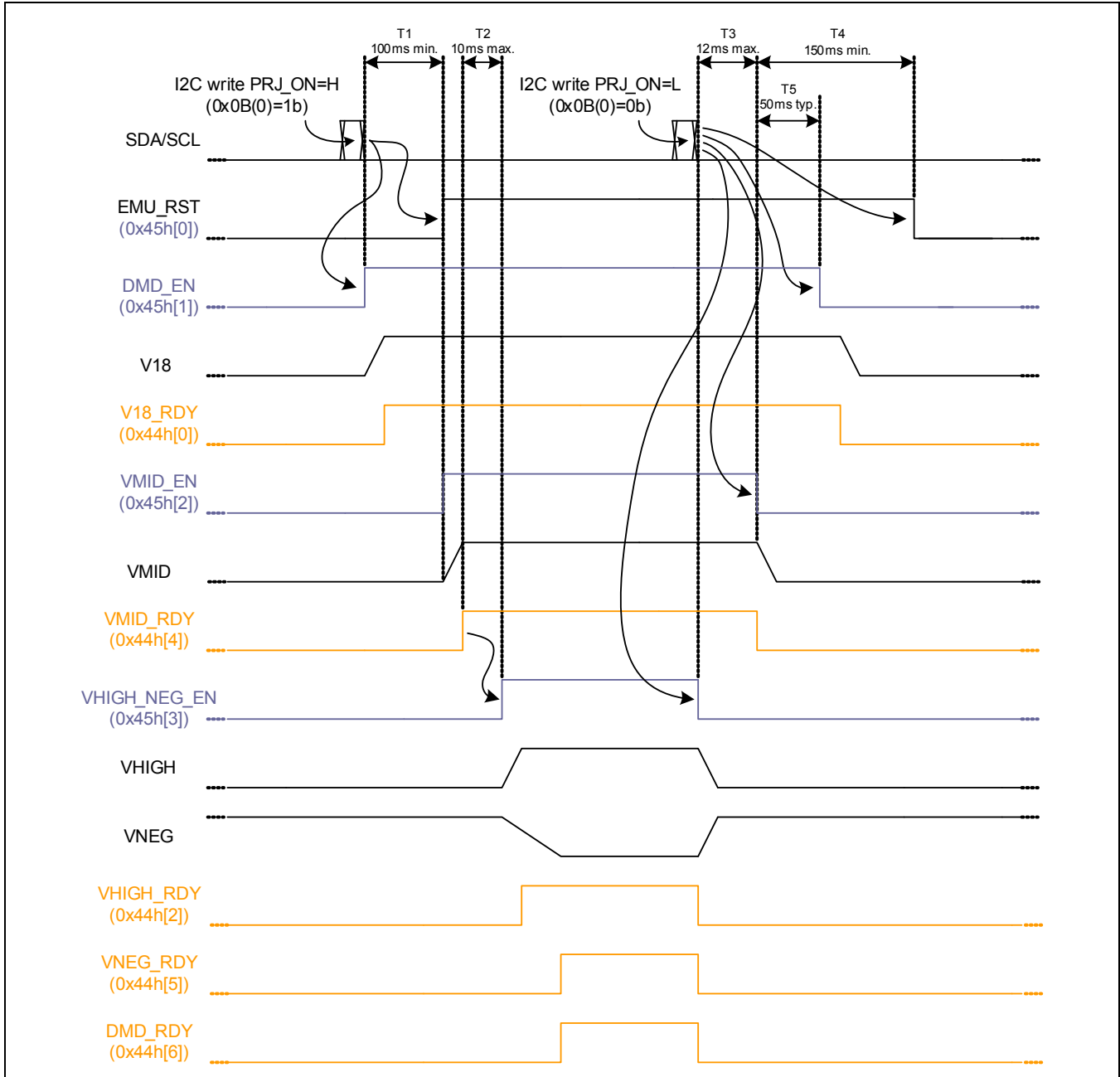
To ensure small ripple at the VHIGH, VMID and VNEG, a 2.2 μ F output capacitor is suggested for each one of them.

The digital engine is in charge of the timing of the enabling of the various DMD generators for the V18, VHIGH, VMID and VNEG as illustrated in [Figure 3-2](#). The black signals are pins, the purple signals are outputs to the digital block, while the orange signals are input to the digital block.

The timing delay of the various signals are illustrated in [Figure 3-2](#).

Since the VMID voltage must be enabled when the VHIGH is present, VHIGH_EN should be gated by VMID_RDY in such a way that if the VMID voltage drops (and VMID_RDY goes low) the VHIGH_EN also goes low.

Figure 3-2. Digital Engine Timing Diagram

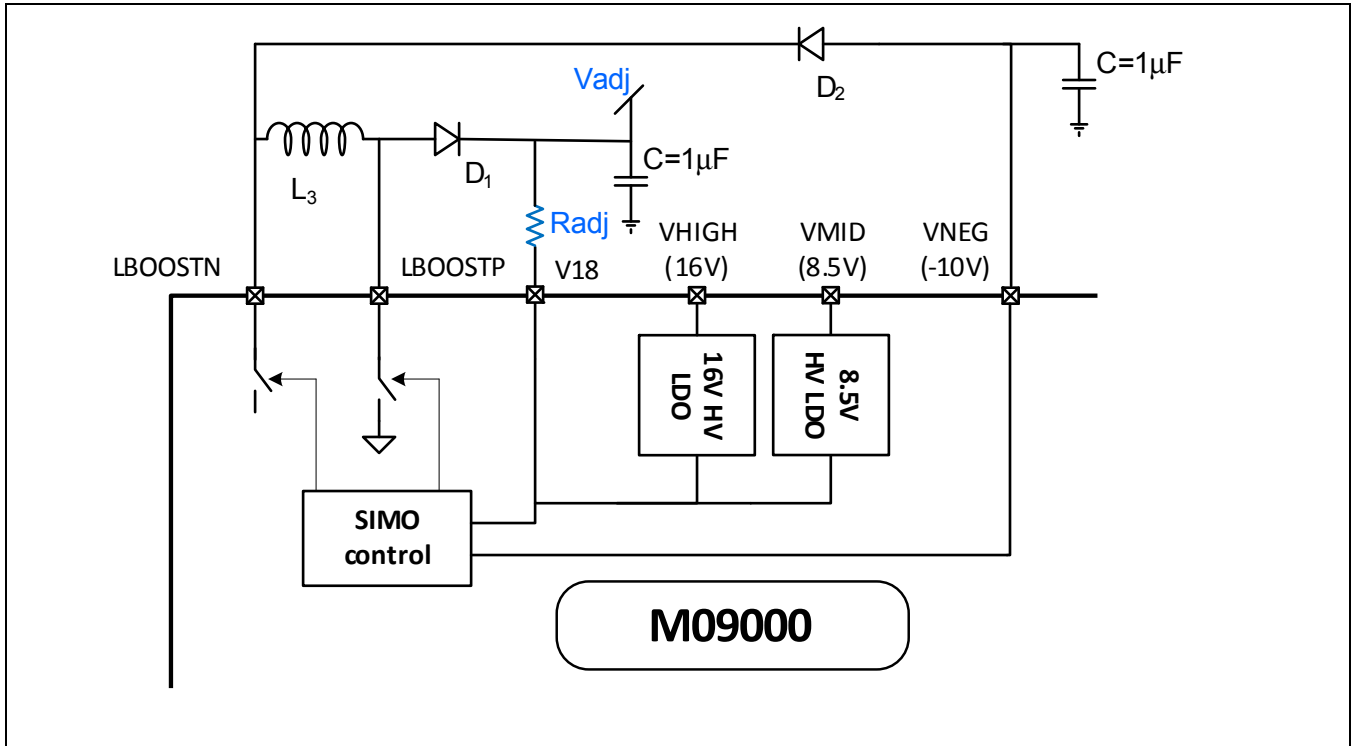


3.5.1 LCOS Applications - Other Uses for the DMD Supply

The boost converter of the DMD generator can be used to generate a 5 V supply or other voltage by setting 06h[7]=1b. In this case, all the other DMD voltage generators (VNEG, and the 2 LDO generating VMID and VHIGH) should be shut off setting 2Eh[2:0]=111b in order to save power. There will be an approximate 20% part to part

variation in the output voltage using this method. An adjustment resistor should be added as shown in [Figure 3-3](#).

Figure 3-3. Creating an Adjustable Output Voltage with the Boost Converter



Alternatively an accurate 5 V can be generated by the VMID LDO selecting 09h[3]=1b. In this configuration the VHIGH and VNEG generator should be disabled with registers 2Eh[2]=1b and 2Eh[0]=1b. This configuration will be inefficient since the 5 V at VMID will be derived from an LDO supplied by the boosted voltage of 18 V.

3.6 Low Dropout Regulators

The M09000 features 2 low dropout regulators. These provide accurate voltage by regulating the battery voltage down to the desired level.

The 2.5 V regulator will work as a regulator for battery voltages > 3.15 V.

3.7 Buck Regulators

Two high efficiency step-down DC-DC converters are also available. These provide accurate voltage by regulating the battery voltage down to the desired level.

Output voltage ripple is maintained within 2% of output voltage and typical turn-on time (soft start) of 5 msec.

3.8 Monitor ADC

The M09000 features a 10-bit 4 ksps monitor ADC which is interleaved between the internal temperature sensor, the battery input relative to the buck-boost converter (pin.PVDDD) and the buck-boost converter output (pin.PVOUT).

For each of the sub-frames (as defined by the status of SEL0 or SEL1, or SEL0, SEL1 and PWM, in case any of INPUT_CONT pairs of bit [1:0], [3:2] or [5:4] is 11b) the ADC first converts the internal temperature sensor input (junction temperature of M09000) then pin.PVDDD and finally pin.PVOUT and stores these values in the corresponding registers at address 0x49h through 0x52h. The start conversion strobe is a change in the status of the input pins (SEL0/1, PWM) and pin.PVOUT is converted last to allow time for it to settle. Since the slewing of the DC-DC converter for a red to green translation is typically < 40 μ s and the conversion rate of the ADC is 4 ksps, the conversion of the PVOUT will start only 500 μ s after the sub-frame starts guaranteeing that the PVOUT voltage is in fact settled.

The PVDDD and PVOUT voltage data is stored in a separate register for each subframe (REG/GREEN/BLUE_VLED/VBAT[9:0]), while the temperature information is stored in (TEMP[9:0]).

Since the conversion rate is 4 ksps the user should wait at least 750 μ s after the subframe change before reading back the digitized values for that subframe; alternatively the microcontroller can monitor the status bits to determine if the conversion is completed.

The ADC can be setup in such a way that it continuously cycles between the three signals to be converted regardless of the input pin (register.ADC_CONT.bit[1]=1). In that case the PVDDD and PVOUT conversion are always stored in the registers corresponding to the red subframe.

The voltage accuracy of the ADC for the PVDDD and PVOUT is determined by the slope error (+/-5%) since the offset error (+/-8 mV) will be insignificant for the voltages measured (>2 V). It should be noticed that the M09000 will measure internal PVDDD and PVOUT voltages: these may be up to 100 mV different (lower in the case of PVDDD, higher in the case of PVOUT) than the external ones due to the IR drops on the pins and bondwires of the M09000 itself.

Absolute accuracy of the temperature sensor is ± 8 °C after calibration at room temperature.

The ambient temperature of the system can be calculated from the part junction temperature, the part power dissipation and the package thermal resistance (θ_{JA}). This is highly dependent on the system characteristics. For example, area and material of the board, number of routing versus ground layers, presence of heat sinks and other mechanical factors, but a typical value for the M09000 is around 39 °C/W.

3.9 FAIL Pin

The FAIL is an active low open collector pin which will issue an alarm when abnormal operating conditions are detected. The pin can function as a status pin or in interrupt mode. In status mode pin.FAIL will go low for the duration of the internal alarm time which can be very short, while in interrupt mode the pin will generate a pulse of programmable length. The mode and pulse duration can be set through register.FAIL_CTRL.bit[3:0].

In interrupt mode the pin will return high after the programmed duration even if the alarm is still present. In interrupt mode pin.FAIL will toggle every time the status of one of the alarm pins changes. The mode and pulse duration can be set through register.FAIL_CTRL.bit[3:0].

The external microcontroller can read back the content of registers 0x70h and 0x71h (ALARM0 and ALARM1) to understand the cause of the alarm once pin.FAIL has triggered. The bits corresponding to the alarm in registers 0x70h and 0x71h remain high once an alarm is captured until the user clears the alarm registers via register.FAIL_CONT.bit[7].

Any alarm bit can be masked by setting the corresponding bit in registers register.ALARM0_MASK.bit[7:0] and register.ALARM1_MASK.bit[7:0].

The following abnormal situation can be detected by the M09000 and signaled through pin.FAIL and register.ALARM0/register.ALARM1.

1. Any of the on board regulators not ready (register.ALARM0.bit[3:0]): the regulator is enabled but its output voltage is lower than 90% of its programmed value. This generally is associated with a shorted output condition. All of the on-board regulators are monitored:
 - 2.5 V and 3.3 V LDOs
 - 1.8 V and 1.0 V Buck converters
2. DMD supplies not ready register.ALARM0.bit[4]. At the enable of the LEDs (LED_ON=H), if the PRJ_ON=H, the M09000 will monitor the status of the DMD supplies (V18, VHIGH, VMID, VNEG). If any of the supply voltages is lower than 90% of the final value, an alarm will be issued.
3. Buck-boost current limit (register.ALARM0.bits[6:5]): These alarms signal a current limit situation in the buck-boost converter.
4. Overtemperature (register.ALARM0.bit[7]): this alarm signals when the junction temperature of the part is 109 °C.
5. Undervoltage at any of following battery inputs (register.ALARM1.bit[0]):
 - PVDD1
 - PVDD2
 - PVDDD
 - PVDDM

Undervoltage alarm is generated when the input battery voltage is below a certain threshold. Programmed in register.ALARM_CTRL0.bit[7:6]. If the battery voltage goes below 2.55 V the part will automatically reset.
6. Undervoltage at pin.PVOUT (register.ALARM1.bit[1]): since over-current condition may also happen in situations other than the output voltage shorted to ground (for example current limiter set lower to prevent saturation in the external inductor during transients) a separate undervoltage alarm is provided (register.ALARM1.bit[0]). Please note that this alarm may also indicate a shorted LED. The threshold for this alarm is set at 1.5 V
7. Overvoltage at pin.PVOUT (register.ALARM1.bit[4]): the M09000 monitors the output voltage in real-time and issues an alarm if the output voltage exceeds 5.2 V.
8. LED alarm for 3 conditions:
 - LED shorted: as previously described this is detected by the pin.PVOUT undervoltage alarm.
 - LED open or LED cathode shorted to ground (register.ALARM1.bit[7:5]): this is detected when, while the driver is ON, the voltage on the driver falls below 30 mV. The threshold can be programmed with

register.**ALARM_CTRL0**.bit[1:0]. With this circuitry the user can identify which LED is creating the issue by reading register.**ALARM1**.bit[7:5]. Please note that the overvoltage alarm also may signal a LED open condition.

It should be noticed that pin.FAIL may chatter during the start-up of the buck converter (6 ms) following pin.MP_EN.

Also during thermal shutdown and undervoltage lockout pin.FAIL will be high: however, the part will signal an overtemperature and undervoltage alarm before the thresholds of the RESET state.

3.10 Overtemperature and Thermal Shutdown

The overtemperature alarm makes use of the ADC to determine if the temperature of the part is at the maximum operating limit. The threshold is set to 120 °C+/-8 °C. Please notice that the overtemperature alarm is functional only when the LED_ON=H.

A thermal shutdown block is also present. This block will force the M09000 into disable mode if the internal junction temperature reaches the thermal shutdown threshold (135 °C). This is to avoid permanent damage to the part. A hysteresis of ~30 °C allows for the part to be enabled again when the temperature drops below ~105 °C. The part registers must be re-written by the host after a thermal shutdown.

3.11 Programmable Serial Interface

The M09000 can be configured through an I²C interface (pins SDA/SCL). The maximum SCL supported is 400 kHz.

The 7-bit slave ID is 011 0110 (36h) resulting in 6Ch (for a write) and 6Dh (for a read).

4.7 kΩ pull up resistors should be used on the I²C pins.

3.12 OTP Programming

The M09000 internal OTP memory can be programmed by writing sequentially in the following registers: 0x31h, 0x32h and 0x33h the values AFh, FAh and 55h respectively. This will store in the OTP memory of the device the content of register 0x13h through 0x16h. These values are now the default values for those registers therefore when the M09000 powers up the current settings programmed will be loaded as defaults. This effectively allows to store predefined current values in the part and can be used for storing white balance control information

During programming the I²C is disabled. After finishing programming the OTP memory, user can issue a soft_reset by writing AAh to address 0x30 (or power cycle the device) to go back to the normal operating mode.

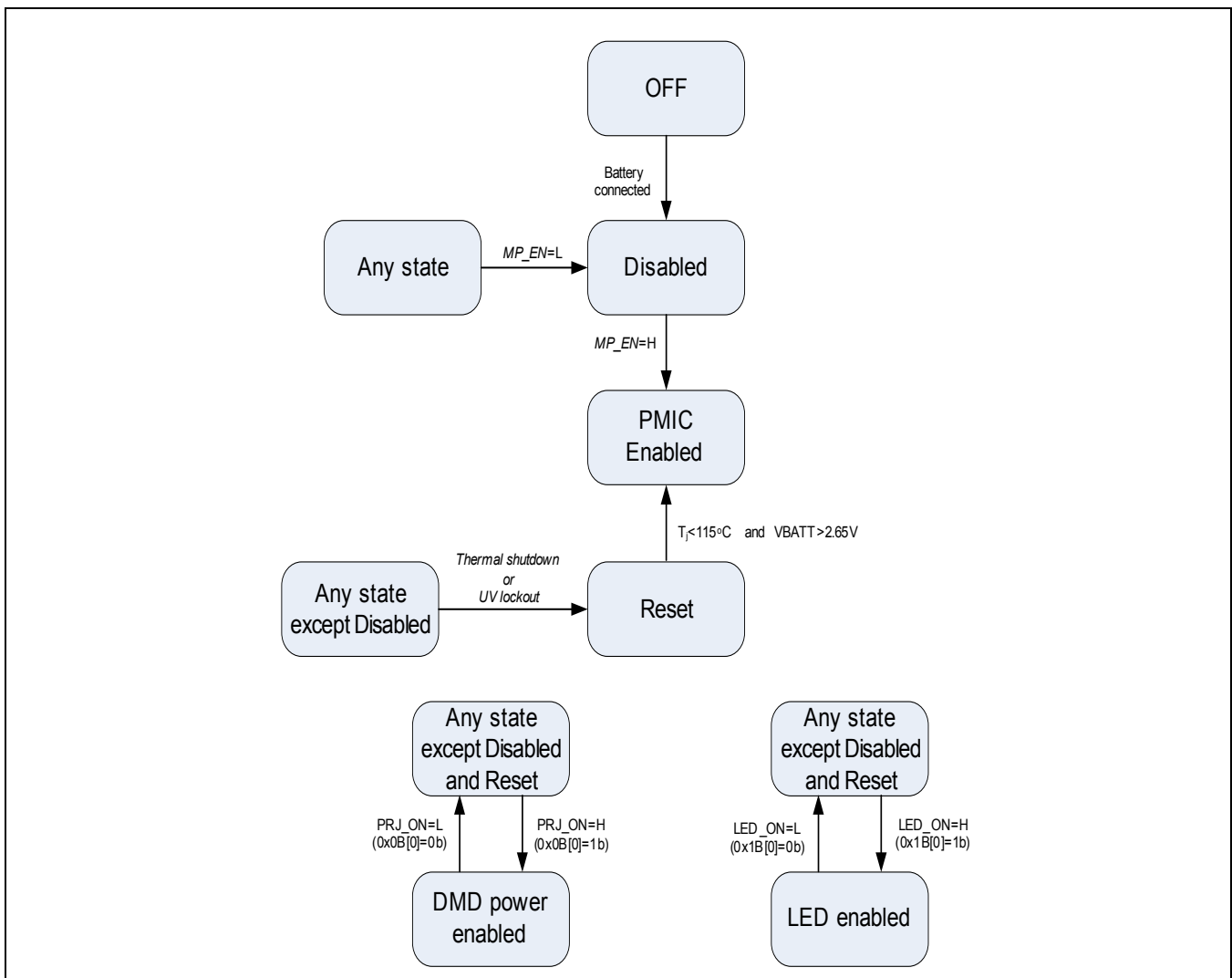
3.13 State Diagram and Description

The DMD supply and LED outputs are independent states that the user can independently enable or disable. This facilitates system testing and debug.

In a DLP system it is expected that the DMD power is functional and the proper DMD voltages are available when LED_ON=H. For this reason the part will issue an alarm if PRJ_ON=H, LED_ON=H but the outputs of the DMD are not at the proper level. As any other alarm of the M09000, this alarm can be masked.

In any of these states, if the battery voltage drops below 2.55 V or the junction temperature reaches 135 °C, the part will be reset. All registers are reset to the default state, the buck converters, LDOs, DMD power, and buck-boost converter are disabled. The part will not be in the disabled state as long as MP_EN=H because the internal voltage references, thermal shutdown and under voltage monitor are still enabled. If the supply rises above 2.65 V the part will go back to the enabled state and the registers will need to be rewritten.

Figure 3-4. State Diagram and Description



OFF

No power is connected to the part.

Disabled

Battery is connected to the part.

In case pin.MP_EN is also connected to the battery, supply ramp time must be > 500 μ s; this can be guaranteed using appropriately sized decoupling caps.

The part will return in this state in case of thermal shutdown. The part needs to be reset by lowering pin.MP_EN.

In this mode of operation the part will consume typically < 5 μ A.

RESET

The M09000 enters this mode of operation if the supply drops below 2.55 V or the junction temperature reaches 135 °C. To exit from this mode, the battery voltage needs to be above 2.65 V and the internal junction temperature must be below 102 °C.

In this mode of operation the part is in reset, the buck converters and LDOs are disabled. The only blocks enabled are the references, the overtemperature protection and the undervoltage protection. During thermal shutdown the undervoltage monitor (POR) will also be powered down.

Since the 1.8 V buck regulator generating the supply for the internal digital block is disabled, all the registers content is lost and I²C communication is not possible.

PMIC Enabled

When pin.MP_EN=H all the buck converters and the LDOs are enabled generating the required voltages.

I²C communication with the part is possible after start-up period.

All the supplies will be available within 6 ms of the MP_EN=H signal assuming 4.7 μ F capacitor is used for decoupling for each one of them. Following start-up I²C communication is possible and the external microcontroller can program the registers according to the user settings

Power dissipation in this state depends on the load on each of the generated supplies and on the battery voltage. With no load on any of the supplies, the power dissipation in this state is typically 2.5 mA.

In this state the SEL1/SEL0/PWM pins activity will be disregarded.

DMD Power Enabled

In DLP applications, 0x0B(0)=1b (PRJ_ON=H) should be set high. The digital engine waits a minimum of 100 ms before generating a EMU_RST=H signal. The V18 boost generator will be enabled to generate +18 V (V18) and the corresponding LDO generates VMID. Once VMID is ready the M09000 waits 10 msec before generating VHIGH (using the associated LDO) and VNEG.

When 0x0B(0)=0b (PRJ_ON=L) or an alarm condition is issued. VHIGH and VNEG are discharged first and within 12 msec the VMID is also discharged. The boost converter generating V18 is shut down last.

LED Enabled

When 0x1B(0)=1b (LED_ON=H), the M09000 enables the buck-boost converter. The LED common anode voltage is kept at 3.7 V. Soft start for the buck-boost is <100 μ s. The SEL1/0/PWM pins are going to be ignored until the soft start is completed.

If 0x0B(0)=1b (PRJ_ON=H) the M09000 will monitor DMD power supply (VHIGH, VMID, VNEG) and issue an alarm if any of them is not ready.

Once start-up of the buck boost is complete, the current can be delivered to the LEDs through the drivers and in turn the buck-boost converter will adjust the anode voltage to guarantee optimal driving efficiency.

When 0x1B(0)=1b (LED_ON=H) or an alarm condition is issued, the LED driver will go into a high impedance state and the buck-boost converter will be disabled forcing the 2 pins of the external inductance to ground.

3.14 Component Selection and PCB Layout

As with all switching power supply ICs, the inductors and capacitors used with the M09000 can significantly affect its performance.

When selecting inductors it should be verified that the performance will be acceptable at the expected peak currents and temperatures. The following inductors were used in the characterization of the M09000 and if alternate components are selected their characteristics should be compared with these.

Buck-Boost Converter (pins 27, 28, 29 and 30)- 1.2 μ H Vishay-Dale IHLP1212BZER1R2M11

Buck Regulators (pins 1 and 2 and pins 4 and 5) - 4.7 μ H TDK MLP2520S4R7S

DMD Supply - (pins 35 and 40) - 22 μ H Vishay-Dale IFSC1008ABER220M01

Capacitors are also important. In general, only ceramic capacitors should be used to achieve the best reliability and highest efficiency. It is particularly important that the 10 μ F capacitors on the buck circuit outputs at pins 1 and 5 be ceramic (25V rating recommended). Ceramic capacitors should be chosen with voltage ratings higher than the highest operating voltage and higher than any expected ripple voltage. Capacitors should be placed close to the M09000 or close to the load that they are decoupling and preferably they will be placed on the same side of the pcb as the M09000 or the load they are decoupling. Each capacitor should have its own vias (ground and/or power). Vias should not be shared between decoupling capacitors and other signals. As an example - do not combine ground signals from 2 different components into one via.

A snubbing network of 0.47 μ F in series with 1.5 Ω should be placed in parallel with the LED at each IOUTx pin. The inductance in series with the LED should be less than 500 nH and this should be considered if the LED will be mounted on a long flex circuit.

4.0 Control Registers Map and Descriptions

Table 4-1. Register Summary

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W		
User Configurable													
0x00	BUCKv18_USR1	RSVD		buckv18_peak		Buckv18_for- cepwm_en	buckv18_zcd			00h	R/W		
0x01	Reserved	RSVD									00h	R/W	
0x02	BUCKv10_USR1	RSVD		buckv10_peak		Buckv10_for- cepwm_en	buckv10_zcd			00h	R/W		
0x03	BUCKV10_USR2	RSVD					buckv10_outputsel		00h			R/W	
0x04	LDOv33_USR1	ldov3p3_cl_dis- able	RSVD						ldov3p3_enable	00h	R/W		
0x05	LDOv25_USR1	ldov2p5_cl_dis- able	RSVD						ldov2p5_enable	00h	R/W		
0x06	BOOST_USR1	VBOOST_SEL	RSVD		Min_Toff		Cur_Peak			00h	R/W		
0x08	LDOv16_USR1	RSVD					ldov16_cl			00h	R/W		
0x09	LDOv8_USR1	RSVD			LDO_SEL		ldov8p5_cl			00h	R/W		
0x0A	VM10_USR1	RSVD									00h	R/W	
0x0B	DMD_RISE	RSVD		T2		T1		RSVD	PRJ_ON	24h	R/W		
0x0C	DMD_FALL	RSVD		T5		T4		T3			05h	R/W	
0x0D	LED PWM_CONT	VMID_RDY_F	BUCK- BOOST_RDY_ F	RSVD			PWM_DEBUG2	PWM_DEBUG1	PWM_DEBUG0	00h	R/W		
0x0E	INPUT_CONT	DIS_PWM	POLARITY FLIP	BLUE_ASSIGN		GREEN_ASSIGN		RED_ASSIGN			24h	R/W	
0x0F	ADC_CONT	ADC test						CONVERSION timing	DISABLE	00h	R/W		
0x13	IOUTX_LSB	RSVD		IOUT2[1:0]		IOUT1[1:0]		IOUT0[1:0]			00h	R/W	
0x14	IOUT0_MSB	IOUT0[9:2]									00h	R/W	
0x15	IOUT1_MSB	IOUT1[9:2]									00h	R/W	
0x16	IOUT2_MSB	IOUT2[9:2]									00h	R/W	
0x18	OVERTEMPERATURE										E4h	R/W	
0x19	HEADROOM_0	IOUT1 HEADROOM SET				IOUT0 HEADROOM SET				00h		R/W	
0x1A	HEADROOM_1	RSVD					IOUT2 HEADROOM SET				00h		R/W
0x1B	BUCKBOOST_USR0	OV_DIS	P_ILIM_DIS	P_ILIM					LED_ON		00h	R/W	
0x1C	BUCKBOOST_USR1	INT_FBCK	UV_DIS	N_ILIM_DIS	N_ILIM					90h		R/W	

Table 4-1. Register Summary

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W		
0x1F	BUCKBOOST_USR4	MOS_POWER		RSVD							E4h	R/W	
0x20	ALARM_CTRL0	UNDERVOLTAGE ALARM		RSVD			LED ALARM TIMING	LED ALARM		C0h	R/W		
0x21	FAIL_CTRL	alarm_clear	RSVD			FAIL_PIN_MODE				08h	R/W		
0x22	RESERVED	RSVD										08h	R/W
0x23	RESERVED	RSVD										00h	R/W
0x24	DIMMER0_FORCE	FORCE DIMMER CODE IOUT0										00h	R/W
0x25	DIMMER1_FORCE	FORCE DIMMER CODE IOUT1										00h	R/W
0x26	DIMMER2_FORCE	FORCE DIMMER CODE IOUT2										00h	R/W
0x27	HEADROOM_CTRL0	HEADROOM SCALE	REGREF FILTER	REGREF RESISTANCE		DISABLE_REGREF	FLIP POLARITY	RSVD			00h	R/W	
0x28	HEADROOM_CTRL1	HEADROOM_INIT		CLK_DIV	WAIT STATES	UPDATE RATE	DECIMATION			00h	R/W		
0x29	HEADROOM_DAC_MSB	HEADROOM DAC PRELOADED VALUE										00h	R/W
0x2A	TEMP_SENS_CTRL	OVERT_EN_CLR	TEMP_SENS_EN	IPTAT_OFFSET			IPTAT_SLOPE				00h	R/W	
0x2B	DRV_CTRL	DRV_STRENGTH		BLANK_CTRL			MOS_DIS				00h	R/W	
0x2C	BUCKBOOST_STRT	FORCE_BST	FORCE_BCK	FREQ		SKIP_STARTUP	DEAD_ZONE_SIZE	RSVD			30h	R/W	
0x2D	BUCKBOOST_SPUP	DISABLE SPEED-UP	ENABLE SPEED FILTER	DIS THE OSC. SENSING	SPEED DAC						00h	R/W	
0x2E	VDMD_PDWN	RSVD					VHIGH_PD	VMID_PD	VM10_PD	00h			R/W
0x2F	OTP_SETUP	RSVD	OTP_I_READ		OTP_I_WRITE		OTP_PROG_TIME				00h	R/W	
0x30	SOFT_RESET	SOFT RESET										00h	R/W
0x31	OTP_PROG0	OTP PROGRAMMING										00h	R/W
0x32	OTP_PROG1	OTP PROGRAMMING										00h	R/W
0x33	OTP_PROG2	OTP PROGRAMMING										00h	R/W
0x3A	ALARM0_MASK	ALARM0_MASK										00h	R/W
0x3B	ALARM1_MASK	ALARM1_MASK										00h	R/W
0x3C	RESERVED	RSVD										N/A	N/A
Status / Readback													
0x40	LDO_STAT	LDOV25_RDY	RSVD	LDOV33_RDY	RSVD				LDOV33_PT	A0h	R		
0x44	BOOST_STAT	RSVD	DMD_RDY	LDOVm10_RDY	LDOV8p5_RDY	RSVD	LDOV16_RDY	RSVD	V18V_RDY	00h	R		
0x45	DMD_STAT_RB	RSVD				VHI_NEG_EN	VMID_EN	DMD_EN	EMU_RST	00h			R
0x46	BUCK_STAT	BUCKV10_RDY	BUCKV10_CL	BUCKV18_RDY	BUCKV18_CL	RSVD					00h	R	
0x48	BUCKBOOST_STAT	BOOST_ON	BUCK_ON	BUCK-BOOST_OUT_OV	BUCK-BOOST_OUT_UV	BUCK-BOOST_NEG_CL	BUCK-BOOST_POS_CL	RSVD	BUCK-BOOST_RDY	80h	R		
0x49	RED_VBAT_LSB	RED SUBFRAME BATTERY VOLTAGE (IOUT0)										00h	R
0x4A	GREEN_VBAT_LSB	GREEN SUBFRAME BATTERY VOLTAGE (IOUT1)										00h	R

Table 4-1. Register Summary

Address	Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W		
0x4B	BLUE_VBAT_LSB	BLUE SUBFRAME BATTERY VOLTAGE (IOUT2)								00h	R		
0x4C	VBAT_MSB	RSVD		BLUE SUBFRAME BATTERY VOLTAGE (IOUT2)		GREEN SUBFRAME BATTERY VOLTAGE (IOUT1)		RED SUBFRAME BATTERY VOLTAGE (IOUT0)		00h	R		
0x4D	RED_VLED_LSB	RED SUBFRAME LED ANODE VOLTAGE (IOUT0)								00h	R		
0x4E	GREEN_VLED_LSB	GREEN SUBFRAME LED ANODE VOLTAGE (IOUT1)								00h	R		
0x4F	BLUE_VLED_LSB	BLUE SUBFRAME LED ANODE VOLTAGE (IOUT2)								00h	R		
0x50	VLED_MSB	RSVD		BLUE SUBFRAME LED ANODE VOLTAGE (IOUT2)		GREEN SUBFRAME LED ANODE VOLTAGE (IOUT1)		RED SUBFRAME LED ANODE VOLTAGE (IOUT0)		00h	R		
0x51	TEMP_LSB	TEMPERATURE LSB								00h	R		
0x52	TEMP_MSB	RSVD					OVERTEMPERATURE	TEMP MSB		00h	R		
0x53	ADC_STATUS	RSVD		BLUE_SUBF_STATUS (IOUT2)		GREEN_SUBF_STATUS (IOUT1)		RED_SUBF_STATUS (IOUT0)		00h	R		
0x54	PWM_READBACK	PWM READBACK								FFh	R		
0x55	IOUT0_HDRM_DAC_READBACK	MSB READBACK OF IOUT0 HEADROOM DAC								00h	R		
0x56	IOUT1_HDRM_DAC_READBACK	MSB READBACK OF IOUT1 HEADROOM DAC								00h	R		
0x57	IOUT2_HDRM_DAC_READBACK	MSB READBACK OF IOUT2 HEADROOM DAC								00h	R		
0x60	DEVICE ID	DEVICE REVISION			DEVICE ID							2Ah	R
0x70	ALARM0	OVERTEMPERATURE	BUCK_BOOST_CL_POS	BUCK_BOOST_CL_NEG	DMD_NOT_RDY	LDOV25_NOT_RDY	LDOV33_NOT_RDY	BUCKV10_NOT_RDY	BUCKV18_NOT_RDY	xxh	R		
0x71	ALARM1	IOUT2_ALRM	IOUT1_ALRM	IOUT0_ALRM	BUCK_BOOST_OUT_OV	RSVD	RSVD	BUCK_BOOST_OUT_UV	UNDEVOLTAGE ALARM	xxh	R		
0x72	Reserved	RSVD								N/A	N/A		

4.1 User Configurable

Register Address: 0x00
 Register Name: BUCKv18_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	RW
5:4	buckv18_peak	00: 670 mA 01: 740 mA 10: 810mAV 11: 900 mA	00b	RW
3	Buckv18_forcepwm_en	1: ForcePwm mode 0: Skip mode	0b	RW
2:0	buckv18_zcd	000: 90 mA 001: 100 mA 010: 110 mA 011: 120 mA 100: 50 mA 101: 60 mA 110: 70 mA 111: 80 mA	000b	RW

Register Address: 0x01
 Register Name: BUCKv18_USR2
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	RSVD	Reserved	0000 0000b	RW

Register Address: 0x02

Register Name: BUCKv10_USR1

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	RW
5:4	buckv10_peak	00: 670 mA 01: 740 mA 10: 810mAV 11: 900 mA	00b	RW
3	Buckv10_forcepwm_en	1: ForcePwm mode 0: Skip mode	0b	RW
2:0	buckv10_zcd	000: 90 mA 001: 100 mA 010: 110 mA 011: 120 mA 100: 50 mA 101: 60 mA 110: 70 mA 111: 80 mA	000b	RW

Register Address: 0x03

Register Name: BUCKV10_USR2

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	00 0000b	RW
1:0	buckv10_outputsel	00: 1.0 V 01: 1.1 V 10: 1.2 V 11: 1.8 V	00b	RW

Register Address: 0x04

Register Name: LDOv33_USR1

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	ldov3p3_cl_disable	Disable current limit setting. 0: Enable 1: Disable	0b	RW
6:1	RSVD	Reserved	000000b	RW
0	ldov3p3_enable	Enable signal for 3.3 V LDO. 0: Enable 1: Disable	0b	RW

Register Address: 0x05
 Register Name: LDOv25_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	ldov2p5_cl_disable	Disable current limit setting. 0: Enable 1: Disable	0b	RW
6:1	RSVD	Reserved	000000b	RW
0	ldov2p5_enable	Enable signal for 2.5 V LDO. 0: Enable 1: Disable	0b	RW

Register Address: 0x06
 Register Name: BOOST_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	VBOOST_SEL	Select output voltage of boost converter. 1: 5 V 0: 18 V	0b	RW
6:5	RSVD	Reserved	00b	RW
4:3	Min_Toff	00: 1.5 μ s 01: 2.0 μ s 10: 2.5 μ s ₁₁ : 1.0 μ s	00b	RW
2:0	Cur_Peak	000: 280 mA 001: 330 mA 010: 390 mA 011: 440 mA 100: 80 mA 101: 130 mA 110: 190 mA 111: 240 mA	000b	RW

Register Address: 0x07
 Register Name: BOOST_USR2
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	RSVD	Reserved	0000 0000b	RW

Register Address: 0x08
 Register Name: LDOv16_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:3	RSVD	Reserved	0 0000b	RW
2:0	ldov16_cl	000: 10 mA 001: 20 mA 010: 30 mA 011: 40 mA 100: 50 mA 101: 60 mA 110: 70 mA 111: 80 mA	000b	RW

Register Address: 0x09
 Register Name: LDOv8_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	RW
3	LDO_SEL	Select output voltage of 8.5 V LDO 1: 5 V 0: 8.5 V	0b	RW
2:0	ldov8p5_cl	000: 10 mA 001: 20 mA 010: 30 mA 011: 40 mA 100: 50 mA 101: 60 mA 110: 70 mA 111: 80 mA	000b	RW

Register Address: 0x0A
 Register Name: VM10_USR1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	RSVD	Reserved	0000 0000b	RW

Register Address: 0x0B

Register Name: DMDTiming_rise

Default Value: 24h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	RW
5:4	T2	Defines T2 time: 00: 4 msec 01: 6 msec 10: 8 msec 11: 12 msec	10b	RW
3:2	T1	Defines T1 time: 00: 50 msec 01: 120 msec 10: 150 msec 11: 200 msec	01b	RW
1	RSVD	Reserved	0b	RW
0	PRJ_ON	Enable DMD power generators 1: Enabled 0: Disabled	0b	RW

Register Address: 0x0C

Register Name: DMDTiming_Fall

Default Value: 05h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	RW
5:4	T5	Defines T5 time: 00: 50 msec 01: 70 msec 10: 80 msec 11: 90 msec	00b	RW
3:2	T4	Defines T4 time: 00: 100 msec 01: 180 msec 10: 200 msec 11: 250 msec	01b	RW
1:0	T3	Defines T3 time: 00: 8 msec 01: 10 msec 10: 12 msec 11: 14 msec	01b	RW

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Register Address: 0x0D

Register Name: Dimming (LED_PWM_CONT)

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	VMID_RDY_F	Forces vmid_rdy signal high	0b	RW
6	BUCKBOOST_RDY_F	Forces buckboost_rdy signal high	0b	RW
5:3	RSVD	Reserved	000b	RW
2	PWM_DEBUG2	1: Revert the polarity of PWM_in at PWM module 0: Default	0b	RW
1	PWM_DEBUG1	1: Hold the previous value in illegal case. 0: Force "FF" in illegal case.	0b	RW
0	PWM_DEBUG0	1: Always counting pwm_period 0: pwm_period is counted once after pwm_ena=1	0b	RW

Register Address: 0x0E

Register Name: INPUT_CONT

Default Value: 24h

Bit(s)	Name	Description	Default	Type
7	DIS_PWM	Disable PWM function (if 0x0E[1,0] or [3,2] or [5,4] =11b PWM function is automatically disabled) 1: Disabled 0: Enabled	0b	RW
6	POLARITY_FLIP	Flips input polarity of LED_SEL0/1 and PWM	0b	RW
5:4	BLUE_ASSIGN	Defines channel on when SEL1/0 is =[1,1] (BLUE_ON) 11: No color definition (SEL0/1/PWM controls respectively IOUT0,1,2). PWM is automatically disabled 10: IOUT2 01: IOUT1 00: IOUT0	10b	RW
3:2	GREEN_ASSIGN	Defines channel on when SEL1/0 is =[1,0] (GREEN_ON) 11: No color definition (SEL0/1/PWM controls respectively IOUT0,1,2). PWM is automatically disabled 10: IOUT2 01: IOUT1 00: IOUT0	01b	RW
1:0	RED_ASSIGN	Defines channel on when SEL1/0 is =[0,1] (RED_ON) 11: No color definition (SEL0/1/PWM controls respectively IOUT0,1,2). PWM is automatically disabled 10: IOUT2 01: IOUT1 00: IOUT0	00b	RW

Register Address: 0x0F
 Register Name: ADC_CONT
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	00 0000b	RW
1	CONVERSION timing	1: Independent of LED_SEL0/1 (runs continuously) 0: Dependent on LED_SEL0/1	0b	RW
0	DISABLE	1: Disabled 0: Enabled	0b	RW

Register Address: 0x13
 Register Name: IOUX_LSB
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	RW
5:4	IOUX2[1:0]	Output current for channel IOUX2 (LSB: [1:0])	00b	RW
3:2	IOUX1[1:0]	Output current for channel IOUX1 (LSB: [1:0])	00b	RW
1:0	IOUX0[1:0]	Output current for channel IOUX0 (LSB: [1:0])	00b	RW

Register Address: 0x14
 Register Name: IOUX0_MSB
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	IOUX0[9:2]	Output current for channel IOUX0 (MSB: [9:2])	0000 0000b	RW

Register Address: 0x15
 Register Name: IOUX1_MSB
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	IOUX1[9:2]	Output current for channel IOUX1 (MSB: [9:2])	0000 0000b	RW

Register Address: 0x16
 Register Name: IOUX2_MSB
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	IOUX2[9:2]	Output current for channel IOUX2 (MSB: [9:2])	0000 0000b	RW

Register Address: 0x17

Register Name: N/A

Default Value: N/A

Bit(s)	Name	Description	Default	Type
7:0	RSVD	Reserved	N/A	N/A

Register Address: 0x18

Register Name: OVERTEMPERATURE

Default Value: EXT

Bit(s)	Name	Description	Default	Type
7:0	OVERTEMPERATURE	Overtemperature alarm threshold (Typical value = 135 °C)	1110 0100b	RW

Register Address: 0x19

Register Name: HEADROOM_0

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:4	IOUT1 HEADROOM SET	0000: 10 mV 0001: 20 mV 0010: 30 mV 0011: 40 mV 0100: 50 mV 0101: 60 mV 0110: 70 mV 0111: 80 mV 1000: 90 mV 1001: 100 mV 1010: 110 mV 1011: 120 mV 1100: 130 mV 1101: 140 mV 1110: 150 mV 1111: 160 mV	0000b	RW
3:0	IOUT0 HEADROOM SET	0000: 10 mV 0001: 20 mV 0010: 30 mV 0011: 40 mV 0100: 50 mV 0101: 60 mV 0110: 70 mV 0111: 80 mV 1000: 90 mV 1001: 100 mV 1010: 110 mV 1011: 120 mV 1100: 130 mV 1101: 140 mV 1110: 150 mV 1111: 160 mV	0000b	RW

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Register Address: 0x1A

Register Name: HEADROOM_1

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	RW
3:0	IOUT2 HEADROOM SET	0000: 10 mV 0001: 20 mV 0010: 30 mV 0011: 40 mV 0100: 50 mV 0101: 60 mV 0110: 70 mV 0111: 80 mV 1000: 90 mV 1001: 100 mV 1010: 110 mV 1011: 120 mV 1100: 130 mV 1101: 140 mV 1110: 150 mV 1111: 160 mV	0000b	RW

Register Address: 0x1B

Register Name: BUCKBOOST_USR0

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	OV_DIS	Overvoltage disable	0b	RW
6	P_ILIM_DIS	Positive current limiter disable	0b	RW
5:1	P_ILIM	Positive current limiter set from 200 mA to 6.4A (200 mA LSB)	0 0000b	RW
0	LED_ON	Enable buck boost DC-DC converter (LED_ON signal) 1: Enabled 0: Disabled (SELO/1 and PWM transitions will be disregarded)	0b	RW

Register Address: 0x1C

Register Name: BUCKBOOST_USR1

Default Value: 90h

Bit(s)	Name	Description	Default	Type
7	INT_FBCK	Internal idle feedback enable	1b	RW
6	UV_DIS	Undervoltage disable	0b	RW
5	N_ILIM_DIS	Negative current limiter disable	0b	RW
4:0	N_ILIM	Negative current limiter set from 200 mA to 6.4A (200 mA LSB)	1 0000b	RW

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Register Address: 0x1F

Register Name: BUCKBOOST_USR4

Default Value: E4h

Bit(s)	Name	Description	Default	Type
7:6	MOS_POWER	Set the size of the power mos from 00=1/4 to 11=4/4	11b	RW
5:0	RSVD	Reserved	10 0100b	RW

Register Address: 0x20

Register Name: ALARM_CTRL0

Default Value: C0h

Bit(s)	Name	Description	Default	Type
7:6	UNDERVOLTAGE ALARM	Set voltage monitor threshold for all supplies (PVDD1,2,M,D) 11: 3.15 V 10: 3.0 V 01: 2.85 V 00: 2.7 V	11b	RW
5:3	RSVD	Reserved	000b	RW
2	LED ALARM TIMING	0: 50 μ s 1: 100 μ s	0b	RW
1:0	LED ALARM	Senses LED cathode voltage when driver is on detecting LED open or cathode shorts if voltage at the driver is below the programmed threshold 00: 30 mV 01: 60 mV 10: 90 mV 11: Disable	00b	RW

Register Address: 0x21

Register Name: FAIL_CTRL

Default Value: 08h

Bit(s)	Name	Description	Default	Type
7	alarm_clear	Writing 1 to this bit clear the ALARM0/1 registers. Self clearing	0b	RW
6:4	RSVD	Reserved	000b	RW
3:0	FAIL_PIN_MODE	Controls the behavior of the FAIL pin between status mode (follows the internal alarms) and interrupt mode (the part generates a pulse of a certain width defined by the internal clock cycles) (1cycle \approx 66 ns: internal clock divided by 8) 1xxx: Status mode 0000: Interrupt mode with 1 cycle pulse width 0001: Interrupt mode with 2 cycle pulse width 0010: Interrupt mode with 4 cycle pulse width 0111: Interrupt mode with 128 cycle pulse width	1000b	RW

Register Address: 0x24

Register Name: DIMMER0_FORCE

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	FORCE DIMMER CODE IOU0	When 00h do not force dimmer: use <i>PWM</i> input to adjust current	0000 0000b	RW

Register Address: 0x25

Register Name: DIMMER1_FORCE

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	FORCE DIMMER CODE IOU1	When 00h do not force dimmer: use <i>PWM</i> input to adjust current	0000 0000b	RW

Register Address: 0x26

Register Name: DIMMER2_FORCE

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	FORCE DIMMER CODE IOU2	When 00h do not force dimmer: use <i>PWM</i> input to adjust current	0000 0000b	RW

Register Address: 0x27

Register Name: HEADROOM_CTRL0

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	HEADROOM SCALE	1: The max headroom is 320 mV 0: The max headroom is 160 mV	0b	RW
6	REGREF FILTER	Enable a 1 μ s filter on the regref comparator	0b	RW
5:4	REGREF RESISTANCE	Set the regref resistance that set the voltage: 00: 8.3k 01: 16.6k 10: 24.9k 11: 33.2k	00b	RW
3	DISABLE_REGREF		0b	RW
2	FLIP POLARITY	1: Flip the headroom comparator polarity 0: Normal polarity	0b	RW
1:0	RSVD	Reserved	00b	RW

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Register Address: 0x28

Register Name: HEADROOM_CTRL1

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	HEADROOM_INIT	Initial value of headroom calibration DAC following turn on of one channel 00: Previous value 01: Value stored in 0x29h (HEADROOM_DAC_MSB) 1x: 0	00b	RW
5	CLK_DIV	Clock divider 1: Full rate clock (12 MHz) 0: Clock divided by 8	0b	RW
4	WAIT_STATES	Wait before the digital calibration algorithm starts 1: No wait 0: ~21 μ s (256 clock cycles of the internal 12.5 MHz clock)	0b	RW
3	UPDATE_RATE	Update rate for the DAC calibration code 1: No updates (headroom control frozen) 0: 8	0b	RW
2:0	DECIMATION	Decimation factor for digital calibration: 000: 1 001: 32 010: 64 011: 128 100: 256 101: 512 110: 1024 111: 2048	000b	RW

Register Address: 0x29

Register Name: HEADROOM_DAC_MSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	HEADROOM_DAC_PRELOADED_VALUE	Initial conditions for headroom calibration DAC (8MSB of the 9 bits DAC)	0000 0000b	RW

Register Address: 0x2A

Register Name: TEMP_SENS_CTRL

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	OVERT_EN_CLR	0: Overtemperature enabled 1: Overtemperature disabled and cleared	0b	RW
6	TEMP_SENS_EN		0b	RW
5:4	IPTAT_OFFSET		00b	RW
3:0	IPTAT_SLOPE	Adjust IPTAT coefficient	0000b	RW

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Register Address: 0x2B

Register Name: DRV_CTRL

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	DRV_STRENGHT	Set the strength of the predriver from 00=1/4 to 11=4/4	00b	RW
5:4	BLANK_CTRL	Set the blanking time from shorter 00 to larger 11	00b	RW
3:0	MOS_DIS	Disable the power mos b3:D, b2:C, b1:B, b0:A	0000b	RW

Register Address: 0x2C

Register Name: BUCKBOOST_STRT

Default Value: 30h

Bit(s)	Name	Description	Default	Type
7	FORCE_BST	Force boost mode if high	0b	RW
6	FORCE_BCK	Force buck mode if high	0b	RW
5:4	FREQ	Set the operating frequency from 5 MHz (00) to 1.25 MHz (11)	11b	RW
3	SKIP_STARTUP	Skip soft start if high	0b	RW
2	DEAD_ZONE_SIZE	Set the size of the dead zone from bck to boost. 0: Smaller 1: Larger	0b	RW
1:0	RSVD	Reserved	00b	RW

Register Address: 0x2D

Register Name: BUCKBOOST_SPUP

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	DISABLE SPEED-UP	Disable the speed-up circuitry	0b	RW
6	ENABLE SPEED FILTER	Enable the filter before the speed-up circuit	0b	RW
5	DIS THE OSC. SENSING	Disable the circuit that prevent a possible oscillation	0b	RW
4:0	SPEED DAC	Set the speed-up current from 0 to 7.44 μ A (250 nA LSB)	0 0000b	RW

Register Address: 0x2E
 Register Name: VDMD_PDWN
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	RW
6:3	RSVD	Reserved	0000b	RW
2	VHIGH_PD	Forces power down of VHIGH LDO 1: Power down 0: Normal operation	0b	RW
1	VMID_PD	Forces power down of VMID LDO 1: Power down 0: Normal operation	0b	RW
0	VM10_PD	Forces power down of VM10 generator 1: Power down 0: Normal operation	0b	RW

Register Address: 0x2F
 Register Name: OTP_SETUP
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	RW
6:5	OTP_I_READ	Defines OTP reading current 00: 2.5 mA 01: 3.0 mA 10: 3.5 mA 11: 4.0 mA	00b	RW
4:3	OTP_I_WRITE	Defines OTP programming current 00: 40 mA 01: 50 mA 10: 60 mA 11: 35 mA	00b	RW
2:0	OTP_PROG_TIME	Defines OTP programming times 000: 20 μ s 001: 22 μ s 010: 25 μ s 011: 35 μ s 100: 18 μ s 101: 15 μ s 110: 10 μ s 111: 05 μ s	000b	RW

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Register Address: 0x30
 Register Name: SOFT_RESET
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	SOFT RESET	Writing AAh causes a 16 12 MHz clock cycles reset (self clearing)	0000 0000b	RW

Register Address: 0x31
 Register Name: OTP_PROG0
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	OTP PROGRAMMING	Must write AFh to this address for LED current OTP programming (all 3 registers 31/32/33h must be programmed sequentially to write OTP)	0000 0000b	W

Register Address: 0x32
 Register Name: OTP_PROG1
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	OTP PROGRAMMING	Must write FAh to this address for LED current OTP programming (all 3 registers 31/32/33h must be programmed sequentially to write OTP)	0000 0000b	W

Register Address: 0x33
 Register Name: OTP_PROG2
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	OTP PROGRAMMING	Must write 55h to this address for LED current OTP programming (all 3 registers 31/32/33h must be programmed sequentially to write OTP)	0000 0000b	W

Register Address: 0x3A
 Register Name: ALARM0_MASK
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	ALARM0_MASK	Writing 1 on any of the bits in this register will mask the corresponding alarm bit in register ALARM0 @ 0x70h	0000 0000b	RW

Register Address: 0x3B
 Register Name: ALARM1_MASK
 Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	ALARM1_MASK	Writing 1 on any of the bits in this register will mask the corresponding alarm bit in register ALARM1 @ 0x71h	0000 0000b	RW

4.2 Status / Readback

Register Address: 0x40

Register Name: LDO_STAT

Default Value: A0h

Bit(s)	Name	Description	Default	Type
7	LDOV25_RDY	LDOV25 is ready	1b	R
6	RSVD	Reserved	0b	R
5	LDOV33_RDY	LDOV33 is ready	1b	R
4:1	RSVD	Reserved	0000b	R
0	LDOV33_PT	LDOV33 is in passthrough mode	0b	R

Register Address: 0x44

Register Name: BOOST_STAT

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7	RSVD	Reserved	0b	R
6	DMD_RDY	dmd_rdy (Logic AND of bit 2, 4, 5)	0b	R
5	LDOVm10_RDY	Minus 10v is ready	0b	R
4	LDOV8p5_RDY	LDOV8p5 is ready	0b	R
3	RSVD	Reserved	0b	R
2	LDOV16_RDY	LDOV16 is ready	0b	R
1	RSVD	Reserved	0b	R
0	V18V_RDY	18 V is ready	0b	R

Register Address: 0x45

Register Name: DMD_STAT_RB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:4	RSVD	Reserved	0000b	R
3	VHI_NEG_EN	VHI_NEG_EN status	0b	R
2	VMID_EN	VMID_EN status	0b	R
1	DMD_EN	DMD_EN status	0b	R
0	EMU_RST	EMU_RST status	0b	R

Register Address: 0x48

Register Name: BUCKBOOST_STAT

Default Value: 80h

Bit(s)	Name	Description	Default	Type
7	BOOST_ON	Buck-boost converter is in boost mode	1b	R
6	BUCK_ON	Buck-boost converter is in buck mode	0b	R
5	BUCKBOOST_OUT_OV	Buck-boost converter output overvoltage	0b	R
4	BUCKBOOST_OUT_UV	Buck-boost converter output undervoltage	0b	R
3	BUCKBOOST_NEG_CL	Negative current limiter	0b	R
2	BUCKBOOST_POS_CL	Positive current limiter	0b	R
1	RSVD	Reserved	0b	R
0	BUCKBOOST_RDY	Start-up complete, buck boost ready	0b	R

Register Address: 0x49

Register Name: RED_VBAT_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	RED SUBFRAME BATTERY VOLTAGE (IOUT0)	Readback of LSB of battery monitor during red subframe	0000 0000b	R

Register Address: 0x4A

Register Name: GREEN_VBAT_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	GREEN SUBFRAME BATTERY VOLTAGE (IOUT1)	Readback of LSB of battery monitor during green subframe	0000 0000b	R

Register Address: 0x4B

Register Name: BLUE_VBAT_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	BLUE SUBFRAME BATTERY VOLTAGE (IOUT2)	Readback of LSB of battery monitor during blue subframe	0000 0000b	R

Register Address: 0x4C

Register Name: VBAT_MSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:4	BLUE SUBFRAME BATTERY VOLTAGE (IOUT2)	Readback of MSB of battery monitor during blue subframe	00b	R
3:2	GREEN SUBFRAME BATTERY VOLTAGE (IOUT1)	Readback of MSB of battery monitor during green subframe	00b	R
1:0	RED SUBFRAME BATTERY VOLTAGE (IOUT0)	Readback of MSB of battery monitor during red subframe	00b	R

Register Address: 0x4D

Register Name: RED_VLED_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	RED SUBFRAME LED ANODE VOLTAGE (IOUT0)	Readback of LSB of led anode monitor during red subframe	0000 0000b	R

Register Address: 0x4E

Register Name: GREEN_VLED_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	GREEN SUBFRAME LED ANODE VOLTAGE (IOUT1)	Readback of LSB of led anode monitor during green subframe	0000 0000b	R

Register Address: 0x4F

Register Name: BLUE_VLED_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	BLUE SUBFRAME LED ANODE VOLTAGE (IOUT2)	Readback of LSB of led anode monitor during blue subframe	0000 0000b	R

Register Address: 0x50

Register Name: VLED_MSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:4	BLUE SUBFRAME LED ANODE VOLTAGE (IOUT2)	Readback of MSB of led anode monitor during blue subframe	00b	R
3:2	GREEN SUBFRAME LED ANODE VOLTAGE (IOUT1)	Readback of MSB of led anode monitor during green subframe	00b	R
1:0	RED SUBFRAME LED ANODE VOLTAGE (IOUT0)	Readback of MSB of led anode monitor during red subframe	00b	R

Register Address: 0x51

Register Name: TEMP_LSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	TEMPERATURE LSB	Readback of LSB of junction temperature	0000 0000b	R

Register Address: 0x52

Register Name: TEMP_MSB

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:2	RSVD	Reserved	00 0000b	R
1:0	TEMP MSB	Readback of MSB of junction temperature	00b	R

Register Address: 0x53
Register Name: ADC_STATUS
Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:6	RSVD	Reserved	00b	R
5:4	BLUE_SUBF_STATUS (IOUT2)	IOUT2 (BLUE) subframe conversion status: 11: PVOOUT done (all done) 10: PVDDD done 01: Temperature done 00: Conversion not done	00b	R
3:2	GREEN_SUBF_STATUS (IOUT1)	IOUT1 (GREEN) subframe conversion status: 11: PVOOUT done (all done) 10: PVDDD done 01: Temperature done 00: Conversion not done	00b	R
1:0	RED_SUBF_STATUS (IOUT0)	IOUT0 (RED) subframe conversion status: 11: PVOOUT done (all done) 10: PVDDD done 01: Temperature done 00: Conversion not done	00b	R

Register Address: 0x54
Register Name: PWM_READBACK
Default Value: FFh

Bit(s)	Name	Description	Default	Type
7:0	PWM READBACK	Readback of PWM dimmer settings	1111 1111b	R

Register Address: 0x55
Register Name: IOUT0_HDRM_DAC_READBACK
Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	MSB READBACK OF IOUT0 HEADROOM DAC	Readback of the value of the DAC when IOUT0 is ON (8 MSB of the 9 bits DAC)	0000 0000b	R

Register Address: 0x56
Register Name: IOUT1_HDRM_DAC_READBACK
Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	MSB READBACK OF IOUT1 HEADROOM DAC	Readback of the value of the DAC when IOUT1 is ON (8 MSB of the 9 bits DAC)	0000 0000b	R

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Register Address: 0x57

Register Name: IOUT2_HDRM_DAC_READBACK

Default Value: 00h

Bit(s)	Name	Description	Default	Type
7:0	MSB READBACK OF IOUT2 HEADROOM DAC	Readback of the value of the DAC when IOUT2 is ON (8 MSB of the 9 bits DAC)	0000 0000b	R

Register Address: 0x60

Register Name: DEVICE ID

Default Value: 2A

Bit(s)	Name	Description	Default	Type
7:6	DEVICE REVISION	Device revision: 00	00	R
5:0	DEVICE ID	Device ID [101010]	101010	R

Register Address: 0x70

Register Name: ALARM0

Default Value: 12h

Bit(s)	Name	Description	Default	Type
7	OVERTEMPERATURE	Part junction temperature is above ~110 °C (±8 °C)	0b	R
6	BUCK_BOOST_CLP	Buck-boost is current limiting (positive)	0b	R
5	BUCK_BOOST_CLN	Buck-boost is current limiting (negative)	0b	R
4	DMD_NOT_RDY	DMD_EN=H & DMD_RDY=L & LED_ON=H (goes to 0 on soft reset)	1b	R
3	LDOV25_NOT_RDY	LDOV25 is not ready	0b	R
2	LDOV33_NOT_RDY	LDOV33 is not ready	0b	R
1	BUCKV10_NOT_RDY	BUCK10 is not ready (goes to 0 on soft reset)	1b	R
0	BUCKV18_NOT_RDY	BUCK18 is not ready	0b	R

Register Address: 0x71

Register Name: ALARM1

Default Value: 01h

Bit(s)	Name	Description	Default	Type
7	IOUT2_ALARM	Open/short at IOUT2 LED	0b	R
6	IOUT1_ALARM	Open/short at IOUT1 LED	0b	R
5	IOUT0_ALARM	Open/short at IOUT0 LED	0b	R
4	BUCKBOOST_OUT_OV	Buck-boost overvoltage (PVOOUT overvoltage)	0b	R
3:2	RSVD	Reserved	00b	R
1	BUCKBOOST_OUT_UV	Buck-boost undervoltage (PVOOUT overvoltage)	0b	R
0	UNDERVOLTAGE_ALARM	PVDD1/2/M/D undervoltage alarm (goes to 0 on soft reset)	1b	R

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