BM63

Bluetooth® 4.2 Stereo Audio Module

Features

- Qualified for Bluetooth v4.2 specifications
- Supports HFP 1.6, HSP 1.2, A2DP 1.3, SPP 1.2, AVRCP 1.6
- Supports Bluetooth 4.2 dual-mode (BR/EDR/BLE) specifications (FW dependent)
- Stand-alone module with on-board PCB antenna and Bluetooth stack
- Supports high resolution up to 24-bit, 96 kHz audio data format
- Supports to connect two hosts with HFP/A2DP profiles simultaneously
- Supports to connect one host with SPP/BTLE
- Transparent UART mode for seamless serial data over UART interface
- Easy to configure with Windows® GUI or directly by external MCU
- Supports firmware field upgrade
- Supports one microphone
- Castellated surface mount pads for easy and reliable host PCB mounting
- RoHS compliant
- Ideal for portable battery operated devices
- Internal battery regulator circuitry

DSP Audio Processing

- Supports 64 kbps A-Law, μ-Law PCM format/ Continuous Variable Slope Delta (CVSD) Modulation for SCO channel operation
- Supports 8/16 kHz noise suppression
- Supports 8/16 kHz echo cancellation
- Supports Modified Sub-Band Coding (MSBC) decoder for wide band speech
- Built-in High Definition Clean Audio (HCA) algorithms for both narrow band and wide band speech processing
- Packet loss concealment (PLC)
- Built-in audio effect algorithms to enhance audio streaming
- Supports Serial Copy Management System (SCMS-T) content protection

FIGURE 1: BM63 MODULE

Audio Codec

- SBC and optional AAC decoding
- 20-bit DAC with 98 dB SNR
- 16-bit ADC with 92 dB SNR
- Up to 24-bit, 96 kHz, I^2S digital audio

Peripherals

- Built-in lithium-ion and lithium-polymer battery charger (up to 350 mA)
- Integrated 1.8V and 3V configurable switching regulator and low-dropout (LDO)
- Built-in ADC for battery voltage sense
- An AUX-In port for external audio input
- Three LED drivers
- Multiple I/O pins for control and status

RF/Analog

- Frequency spectrum: 2.402 GHz to 2.480 GHz
- Receive sensitivity: -90 dBm (2 Mbps EDR)
- Class 2 output power (+2 dBm typical)

HCI Interface

- High-speed HCI-UART interface (supports up to 921,600 bps)

MAC/Baseband Processor

- Supports Bluetooth 4.2 dual-mode (FW dependent)
  - BR/EDR transport for audio, voice and SPP data exchange
  - BLE transport for proprietary transparent service and ANCS data exchange

Operating Condition

- Operating voltage: 3.2V to 4.2V
- Operating temperature: -20°C to +70°C

Compliance

- Bluetooth SIG QDID: 83345

Applications

- Soundbar and Subwoofer (FW dependent)
- Bluetooth portable speaker phone
- Multi-speaker (FW dependent)

Description

The BM63 module is a fully qualified Bluetooth v4.2 dual-mode (BDR/EDR/BLE) module for designers to add wireless audio and voice applications to their products. The BM63 module is a Bluetooth Special Interest Group (SIG) certified module that provides a complete wireless solution with a Bluetooth stack and an integrated PCB antenna in a compact surface-mount package.

The BM63 module has an integrated lithium-ion and lithium-polymer battery charger, and a digital audio interface. The module supports HSP, HFP, SPP, A2DP and AVRCP profiles, and AAC and SBC codecs.

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NOTES:

1.0 DEVICE OVERVIEW

The BM63 module is built around Microchip Technology IS2063 SoC. The IS2063 SoC integrates the Bluetooth 4.2 dual-mode radio transceiver, Power Management Unit (PMU), crystal and DSP. Users can configure the BM63 module by using the UI tool and DSP tool, a Windows-based utility.

Figure 1-1 illustrates a typical example of the BM63 module which is connected to an external MCU and a DSP/codec.

FIGURE 1-1: APPLICATION USING BM63 MODULE

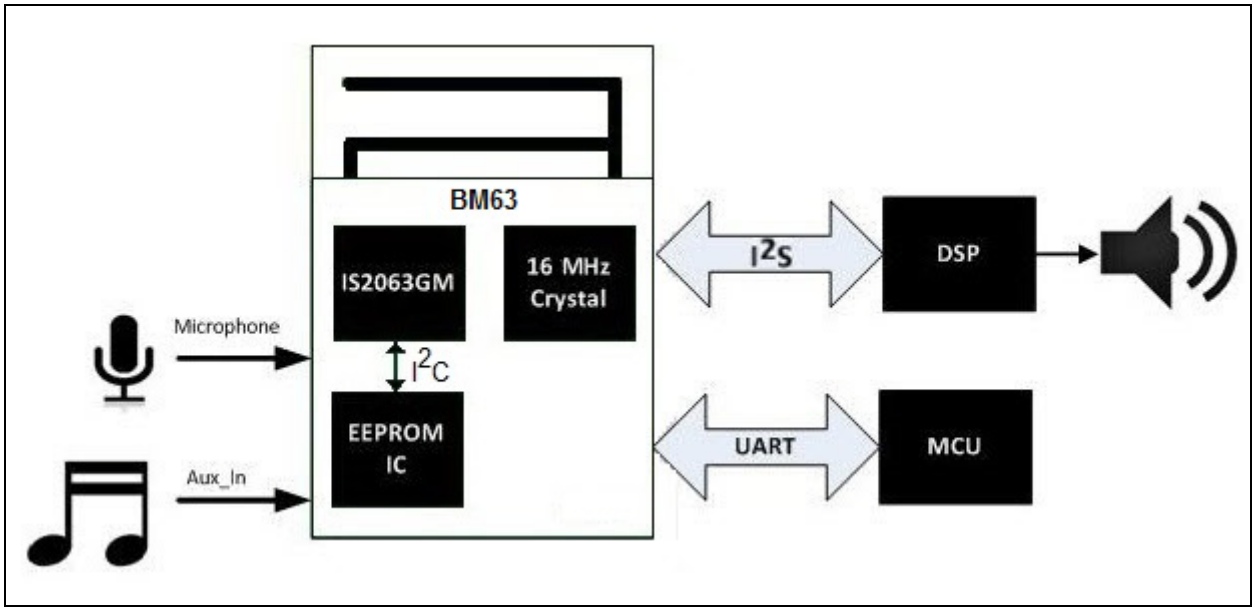


Figure 1-2 shows Soundbar and Subwoofer applications using the BM63 module.

FIGURE 1-2: SOUNDBAR AND SUBWOOFER APPLICATIONS USING BM63 MODULE

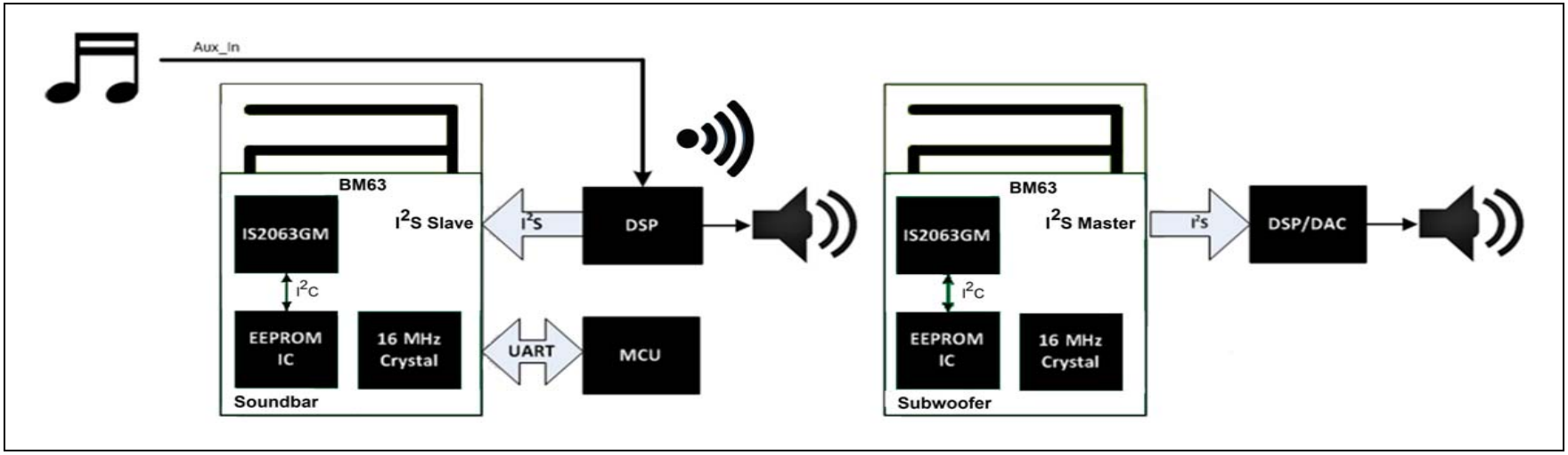


Figure 1-3 shows Soundbar and Subwoofer applications using the BM63 module and smartphone.

FIGURE 1-3: SOUNDBAR AND SUBWOOFER APPLICATIONS USING BM63 MODULE AND SMARTPHONE

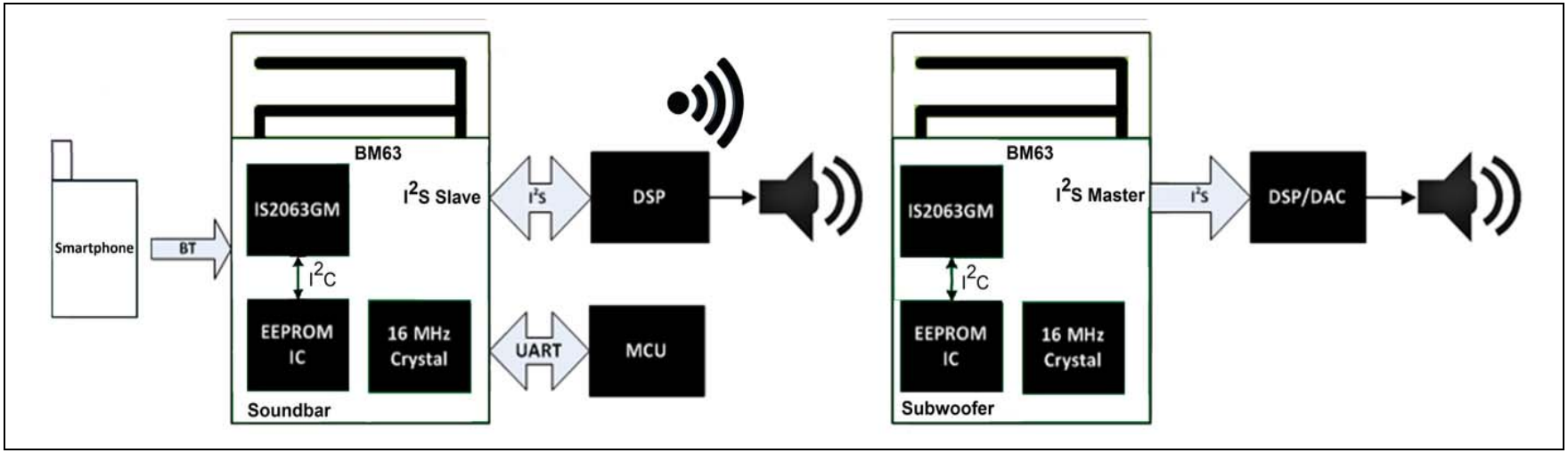


Figure 1-4 illustrates the Multi-speaker application using the BM63 module.

FIGURE 1-4: MULTI-SPEAKER APPLICATION USING BM63 MODULE

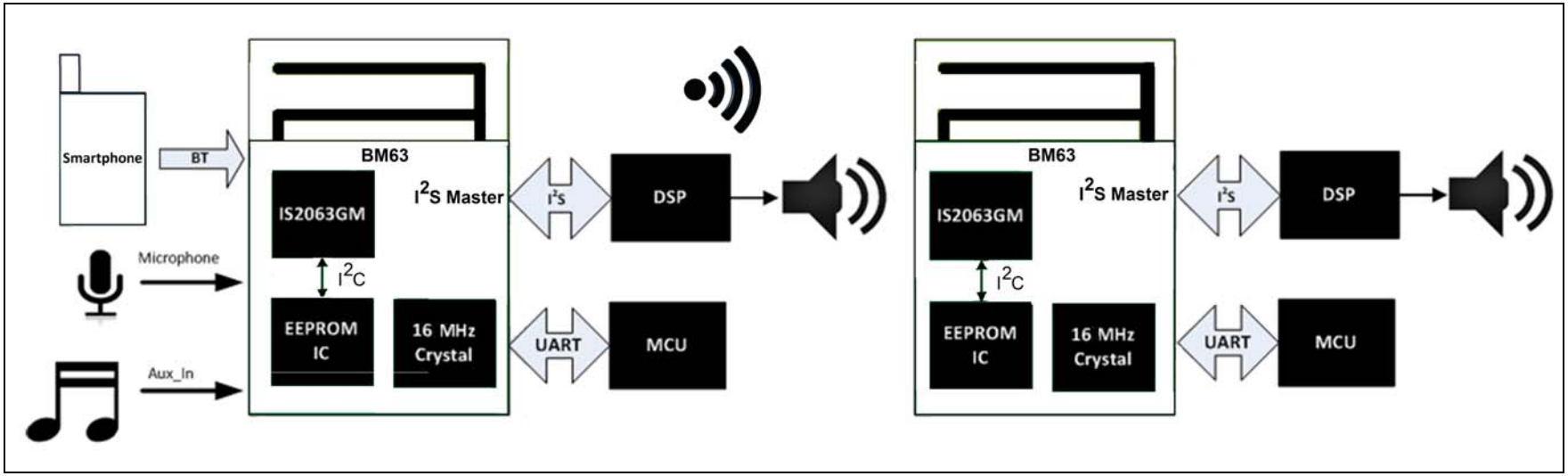


Table 1-1 provides the key features of the BM63 module.

TABLE 1-1: BM63 KEY FEATURES

Feature	BM63
Application	Multi-speaker/Soundbar/Subwoofer
Stereo/mono	Stereo
Pin count	48
Dimensions (mm^2)	15 x 32
PCB antenna	Yes
Tx power (typical)	2 dBm
Audio DAC output	2 Channel
DAC (single-ended) SNR at 2.8V (dB)	-98
DAC (capless) SNR at 2.8V (dB)	-98
ADC SNR at 2.8V (dB)	-92
I^2S digital interface	Yes
Analog AUX-In	Yes
Mono MIC	1
External audio amplifier interface	Yes
UART	Yes
LED driver	3
Internal DC-DC step-down regulator	Yes
DC 5V adapter input	Yes
Battery charger (350 mA max)	Yes
ADC for thermal charger protection	No
Undervoltage protection (UVP)	No
GPIO	15
Button support	6
NFC (triggered by external NFC)	Yes
EEPROM	Yes
Customized voice prompt	No
Multitone	Yes
DSP sound effect	Yes
BLE	Yes
Bluetooth profiles	
HFP	1.6
AVRCP	1.6
A2DP	1.3
HSP	1.2
SPP	1.2

Figure 1-5 illustrates the pin diagram of the BM63 module.

FIGURE 1-5: BM63 MODULE PIN DIAGRAM

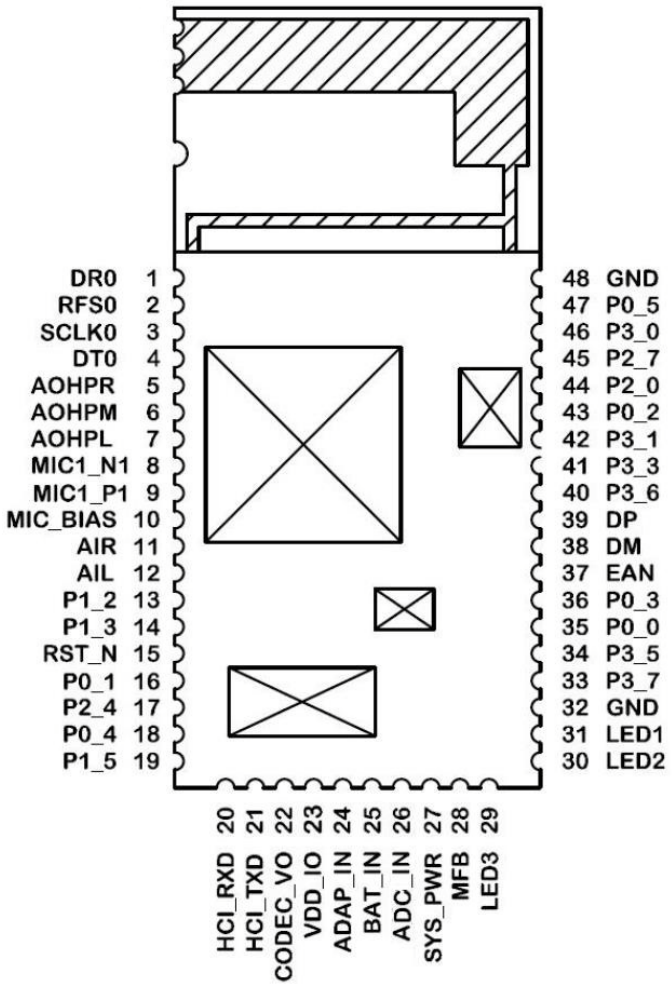


Table 1-2 provides the pin description of the module.

TABLE 1-2: BM63 PIN DESCRIPTION

Pin No	Pin Type	Name	Description
1	I	DR0	I^2S interface: digital left/right data
2	I/O	RFS0	I^2S interface: left/right clock
3	I/O	SCLK0	I^2S interface: bit clock
4	O	DT0	I^2S interface: digital left/right data
5	O	AOHPR	Headphone output, right channel
6	O	AOHPM	Headphone common mode output/sense input
7	O	AOHPL	Headphone output, left channel
8	I	MIC_N1	MIC1 mono differential analog negative input
9	I	MIC_P1	MIC1 mono differential analog positive input
10	P	MIC_BIAS	Electric microphone biasing voltage
11	I	AIR	Right-channel single-ended analog input
12	I	AIL	Left-channel single-ended analog input
13	I/O	P1_2	EEPROM clock SCL
14	I/O	P1_3	EEPROM data SDA
15	I	RST_N	System reset (active-low)
16	I/O	P0_1	Configurable control or indication pin (Internally pulled-up if configured as an input)
17	I/O	P2_4	System configuration pin along with P2_0 and EAN pins used to set the module in any one of these modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to enter the new firmware into the module), refer to Table 5-1
18	I/O	P0_4	Configurable control or indication pin (Internally pulled-up if configured as an input) • NFC detection pin, active-low • Out_Ind_1
19	I/O	P1_5	Configurable control or indication pin (Internally pulled-up if configured as an input) • NFC detection pin • Slide switch detector, active-high • Out_Ind_1 • Multi-SPK Master/Slave mode control (FW dependent)
20	I	HCI_RXD	HCI-UART data input
21	O	HCI_TXD	HCI-UART data output
22	P	CODEC_VO	Power supply/reference voltage for codec. Do not connect, for internal use only
23	P	VDD_IO	I/O positive supply. Do not connect, for internal use only
24	P	ADAP_IN	5V power adapter input

TABLE 1-2: BM63 PIN DESCRIPTION (CONTINUED)

Pin No	Pin Type	Name	Description
25	P	BAT_IN	Battery input. Voltage range: 3.2V to 4.2V. When an external power supply is connected to the ADAP_IN pin, the BAT_IN pin can be left open if battery is not connected.
26	P	ADC_IN	Analog input
27	P	SYS_PWR	System power output
28	I	MFB	Multi-function button and power-on key UART RX_IND, active-high
29	I	LED3	LED driver 3
30	I	LED2	LED driver 2
31	I	LED1	LED driver 1
32	P	GND	Ground reference
33	I/O	P3_7	Configurable control or indication pin (Internally pulled-up, if configured as an input) UART TX_IND, active-low
34	I/O	P3_5	Configurable control or indication pin (Internally pulled-down, if configured as an input)
35	I/O	P0_0	Configurable control or indication pin (Internally pulled-up if configured as an input) Slide switch detector, active-high
36	I/O	P0_3	Configurable control or indication pin (Internally pulled-up if configured as an input)
37	I	EAN	External address bus negative System configuration pin along with P2_0 and P2_4 pins used to set the module in any one of these modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to enter new firmware into the module), refer to Table 5-1
38	I/O	DM	Differential data-minus USB
39	I/O	DP	Differential data-plus USB
40	I/O	P3_6	Configurable control or indication pin (Internally pulled-up if configured as an input) Multi-SPK Master/Slave mode control (FW dependent)
41	I/O	P3_3	Configurable control or indication pin (Internally pulled-up if configured as an input) FWD key, active-low
42	I/O	P3_1	Configurable control or indication pin (Internally pulled-up if configured as an input) REV key, active-low
43	I/O	P0_2	Configurable control or indication pin (Internally pulled-up if configured as an input) Play/Pause key (default)
44	I/O	P2_0	System configuration pin along with P2_4 and EAN pins used to set the module in one of these modes: • Application mode (for normal operation) • Test mode (to change EEPROM values) • Write Flash mode (to enter the new firmware into the module), refer to Table 5-1 • Pulse/PWM signal output

TABLE 1-2: BM63 PIN DESCRIPTION (CONTINUED)

Pin No	Pin Type	Name	Description
45	I/O	P2_7	Configurable control or indication pin (Internally pulled-up if configured as an input) Volume-up key (default), active-low
46	I/O	P3_0	Configurable control or indication pin (Internally pulled-up if configured as an input) AUX-In detector, active-low
47	I/O	P0_5	Configurable control or indication pin (Internally pulled-up if configured as an input) Volume-down key (default), active-low
48	P	GND	Ground reference

Legend: I= Input pin O= Output pin I/O= Input/Output pin P= Power pin

Note: All I/O pins can be configured using the UI tool.

2.0 AUDIO

The input and output audios have different stages and each stage can be programmed to vary the characteristics of the gain response. For microphones, both single-ended inputs and differential inputs are supported. To maintain a high-quality signal, a stable bias voltage source to the condenser microphone's FET is provided. The DC blocking capacitors can be used at positive and negative sides of the input. Internally, this analog signal is converted to 16-bit, 8/16 kHz linear PCM data.

2.1 Digital Signal Processor

Digital Signal Processor (DSP) is used to perform speech and audio processing. The advanced speech features, such as acoustic echo cancellation and noise reduction are in-built. To reduce nonlinear distortion and help echo cancellation, an outgoing signal level to the speaker is monitored and adjusted to avoid saturation of speaker output or microphone input. Adaptive filtering is also applied to track the echo path impulse in response to provide echo free and full-duplex user experience. The embedded noise reduction algorithm helps to extract clean speech signals from a noisy input captured by the microphones, and improves mutual understanding in communication.

Advanced audio features, such as multi-band dynamic range control, parametric multi-band equalizer, audio widening and virtual bass are in-built. The audio effect algorithms improve the user's audio listening experience in terms of better quality after audio signal processing.

Figure 2-1 and Figure 2-2 illustrate the processing flow of speaker-phone applications for speech and audio signal processing.

FIGURE 2-1: SPEECH SIGNAL PROCESSING

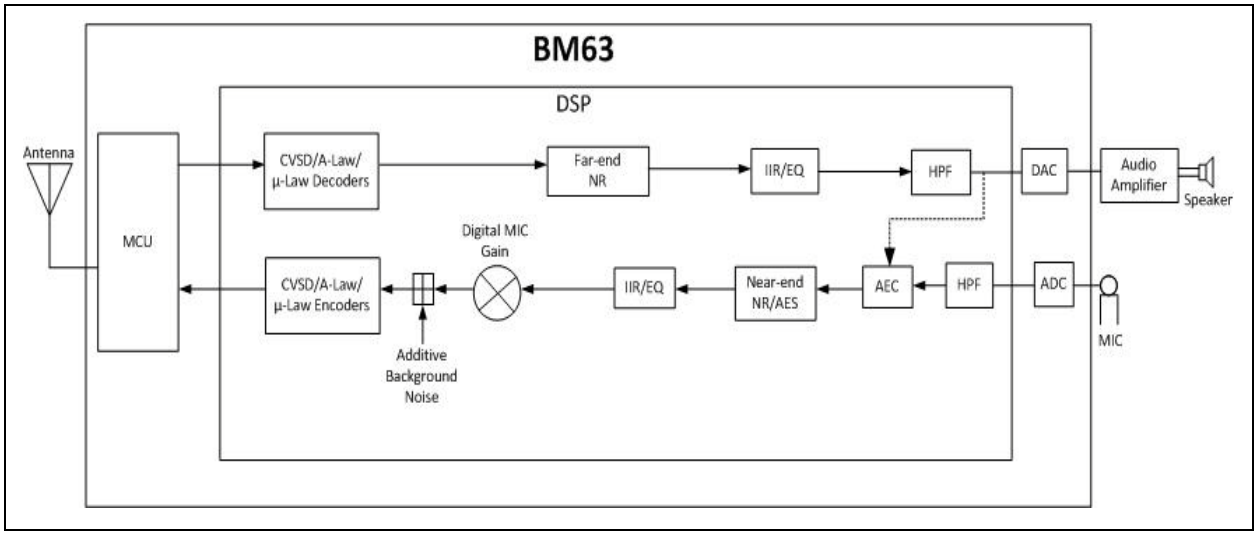
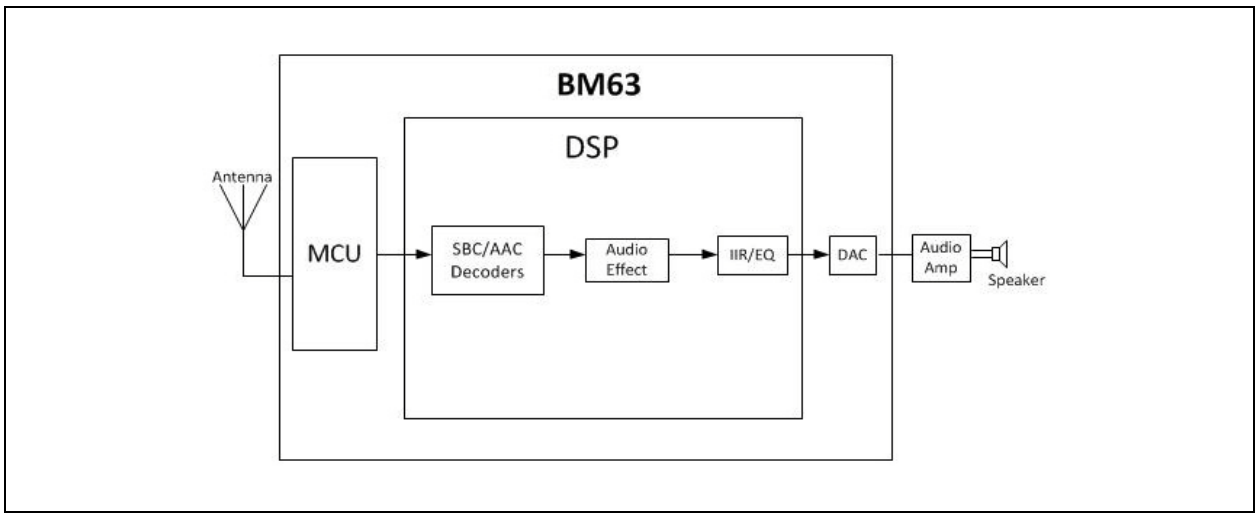


FIGURE 2-2: AUDIO SIGNAL PROCESSING



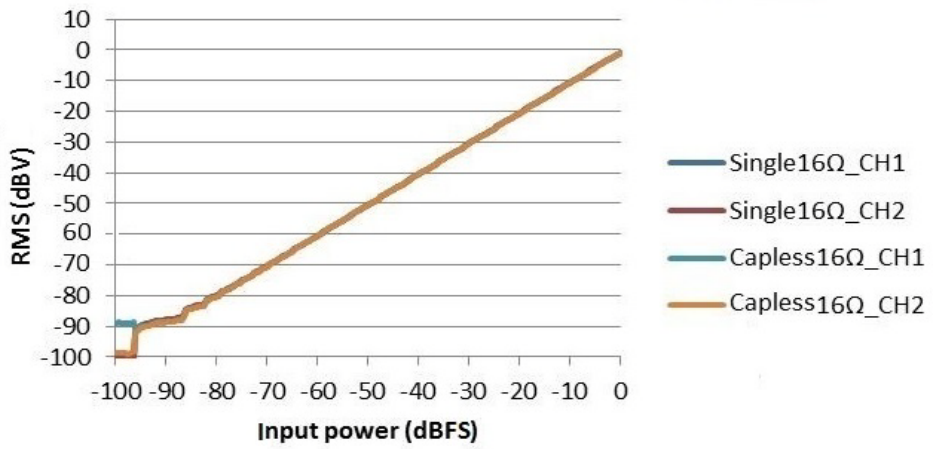
Users can configure DSP parameters using the DSP tool. For additional information, refer to the "*IS206X DSP Application Note*".

Note:	The DSP tool and "*IS206X DSP Application Note*" document, are available for download from the Microchip web site at: www.microchip.com/BM63.

2.2 Codec

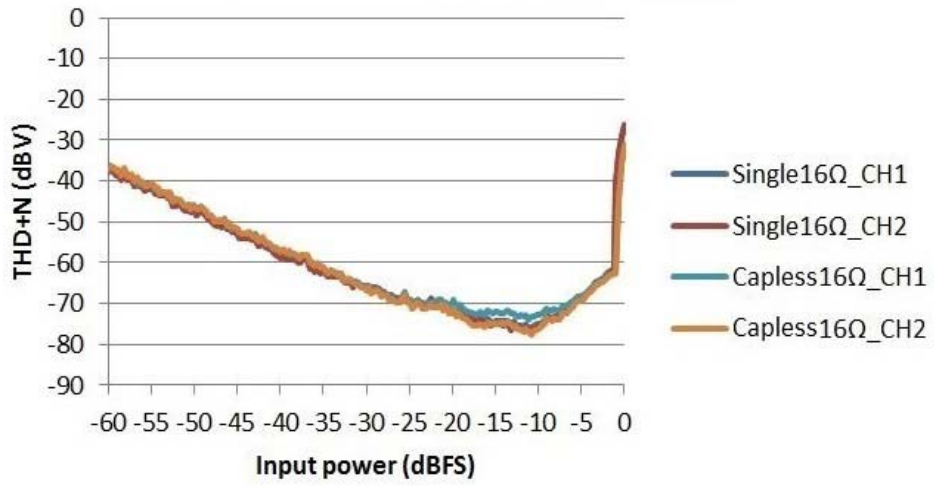
The built-in codec has a high signal-to-noise ratio (SNR) and it consist of an ADC, a DAC and an additional analog circuitry. Figure 2-3 through Figure 2-6 illustrate the dynamic range and frequency response of the codec.

FIGURE 2-3: CODEC DAC DYNAMIC RANGE



Note: The data corresponds to the 16 ohm load with 2.8V operating voltage at 25°C room temperature.

FIGURE 2-4: CODEC DAC THD+N VERSUS INPUT POWER



Note: The data corresponds to the 16 ohm load with 2.8V operating voltage at 25°C room temperature.

FIGURE 2-5: CODEC DAC FREQUENCY RESPONSE (CAPLESS MODE)

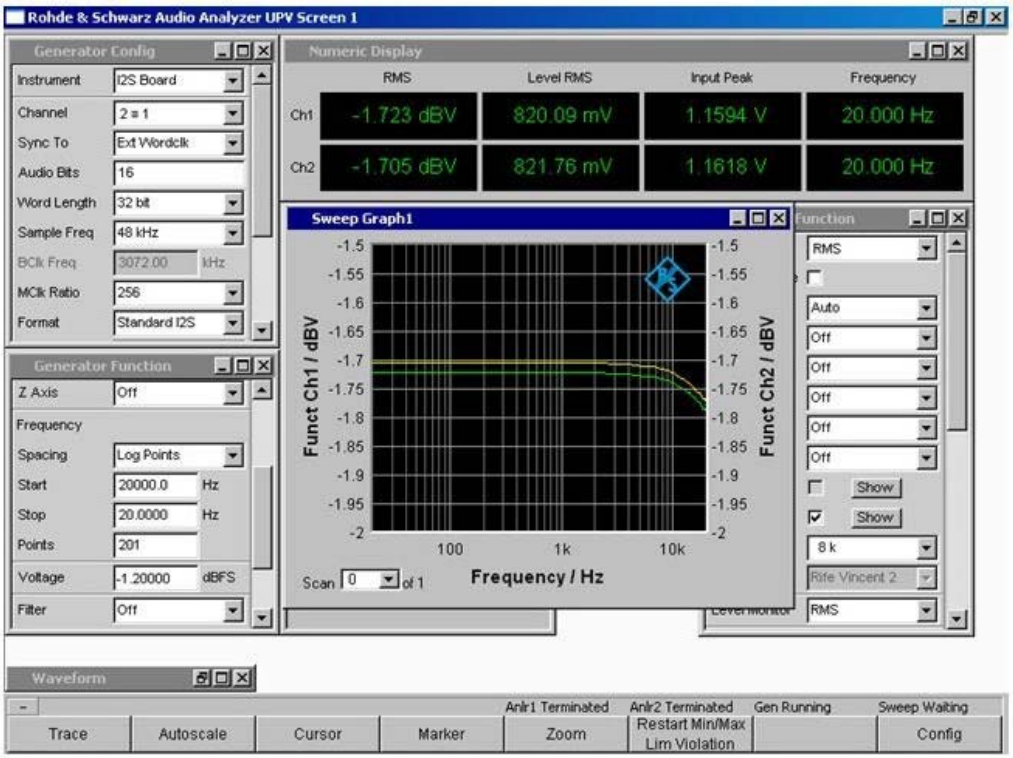
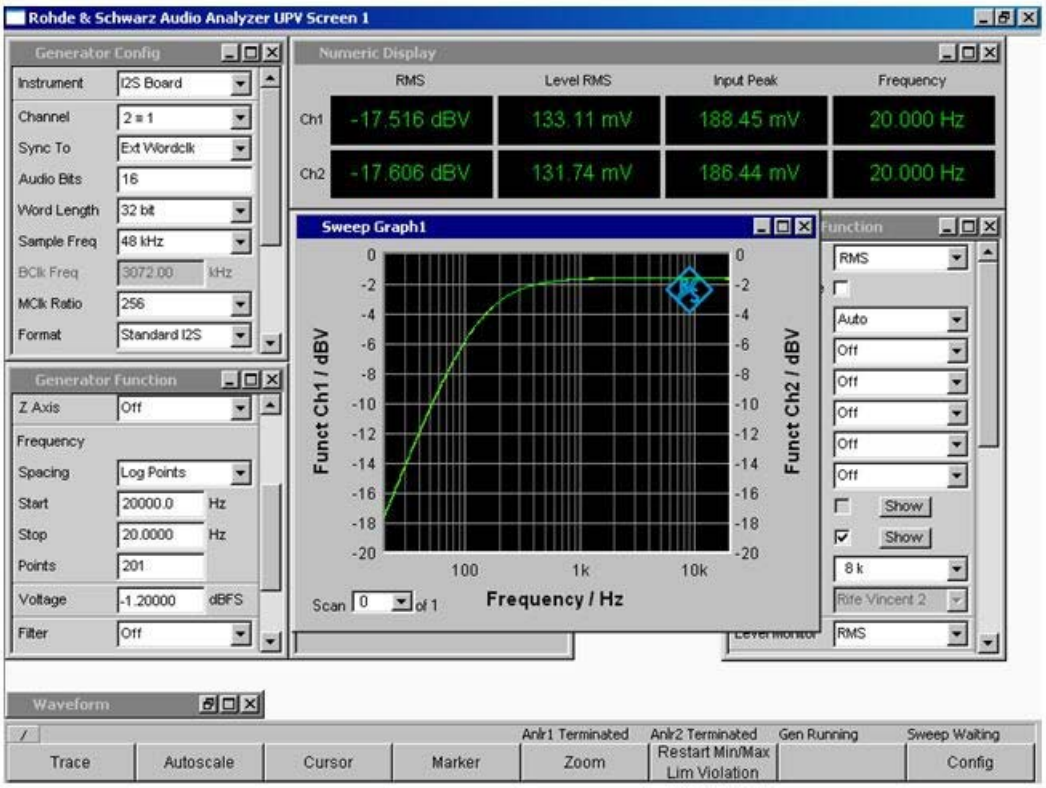


FIGURE 2-6: CODEC DAC FREQUENCY RESPONSE (SINGLE-ENDED MODE)



Note: The DAC frequency response corresponds to Single-ended mode with a 47 µF DC block

2.3 Auxiliary Port

The BM63 module supports analog (line-in) signals from the external audio source. The analog (line-in) signal can be processed by the DSP to generate different sound effects (multi-band, dynamic range compression and audio widening), which can be set by using the DSP tool.

2.4 Analog Speaker Output

The BM63 module supports the following analog speaker output modes:

- Capless mode – Recommended for headphone applications in which capless output connection helps to save the BOM cost by avoiding a large DC blocking capacitor. Figure 2-7 illustrates the capless mode.
- Single-ended mode – Used for driving an external audio amplifier where a DC blocking capacitor is required. Figure 2-8 illustrates the single-ended mode.

FIGURE 2-7: CAPLESS MODE

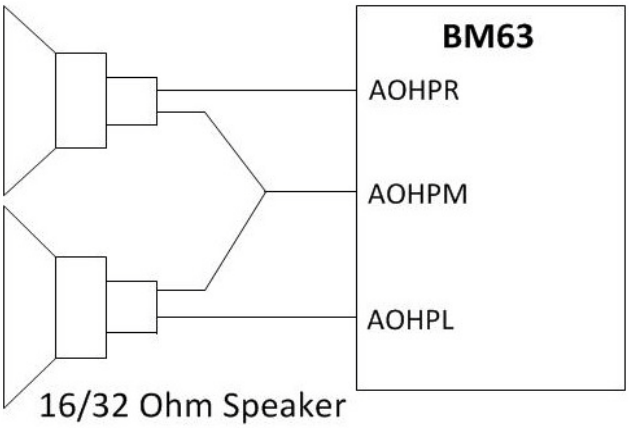
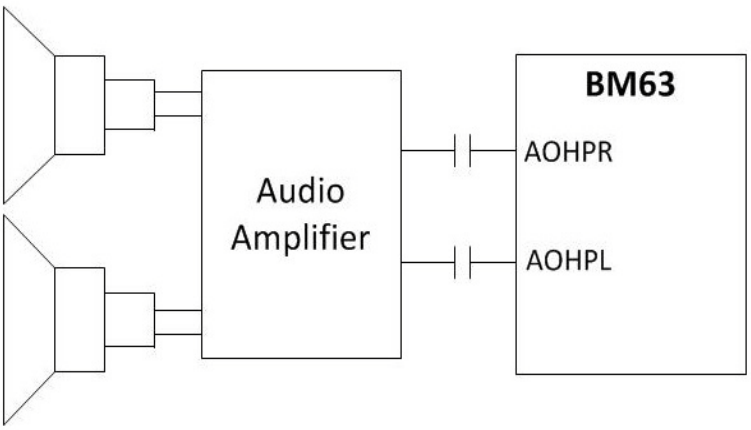


FIGURE 2-8: SINGLE-ENDED MODE



3.0 TRANSCEIVER

The BM63 module is designed and optimized for Bluetooth 2.4 GHz system. It contains a complete radio frequency transmitter/receiver section. An internal synthesizer generates a stable clock for synchronizing with another device.

3.1 Transmitter

The internal power amplifier (PA) has a maximum output power of +4 dBm. This is applied for class 2 or class 3 radios without an external RF PA.

The transmitter performs IQ conversion to minimize the frequency drift.

3.2 Receiver

The low-noise amplifier (LNA) operates with TR-combined mode for single port application. It can save a pin on package without having an external Tx/Rx switch.

The ADC can sample the input analog signal and convert it into a digital signal for demodulator analysis. A channel filter has been integrated into receiver channel before the ADC, which is used to reduce the external component count and increase the anti-interference capability.

The image rejection filter is used to reject the image frequency for low-IF architecture. This filter for low-IF architecture is intended to reduce external Band Pass Filter (BPF) component for super heterodyne architecture.

The Received Signal Strength Indicator (RSSI) signal feedback to the processor is used to control the RF output power to make a good trade-off for effective distance and current consumption.

3.3 Synthesizer

Synthesizer generates a clock for radio transceiver operation. There is a VCO inside, with a tunable internal LC tank that can reduce variation for components. A crystal oscillator with internal digital trimming circuit provides a stable clock for synthesizer.

3.4 Modem

For Bluetooth 1.2 specification and below, 1 Mbps was the standard data rate based on Gaussian Frequency Shift Keying (GFSK) modulation scheme. This basic rate modem meets Basic Data Rate (BDR) requirements of Bluetooth 2.0 with Enhanced Data Rate (EDR) specification.

For Bluetooth 2.0 and above specifications, EDR has been introduced to provide data rates of 3/2/1 Mbps. For baseband, both BDR and EDR utilize the same 1 MHz symbol rate and 1.6 kHz slot rate. For BDR, symbol 1 represents 1-bit. However, each symbol in the payload part of EDR packets represents 2 or 3 bits. This is achieved by using two different modulations, π/4 DQPSK and 8 DPSK.

3.5 Adaptive Frequency Hopping (AFH)

The BM63 module has AFH function to avoid RF interference. It has an algorithm to check the nearby interference and to choose clear channel for transceiver Bluetooth signal.

NOTES:

4.0 POWER MANAGEMENT UNIT

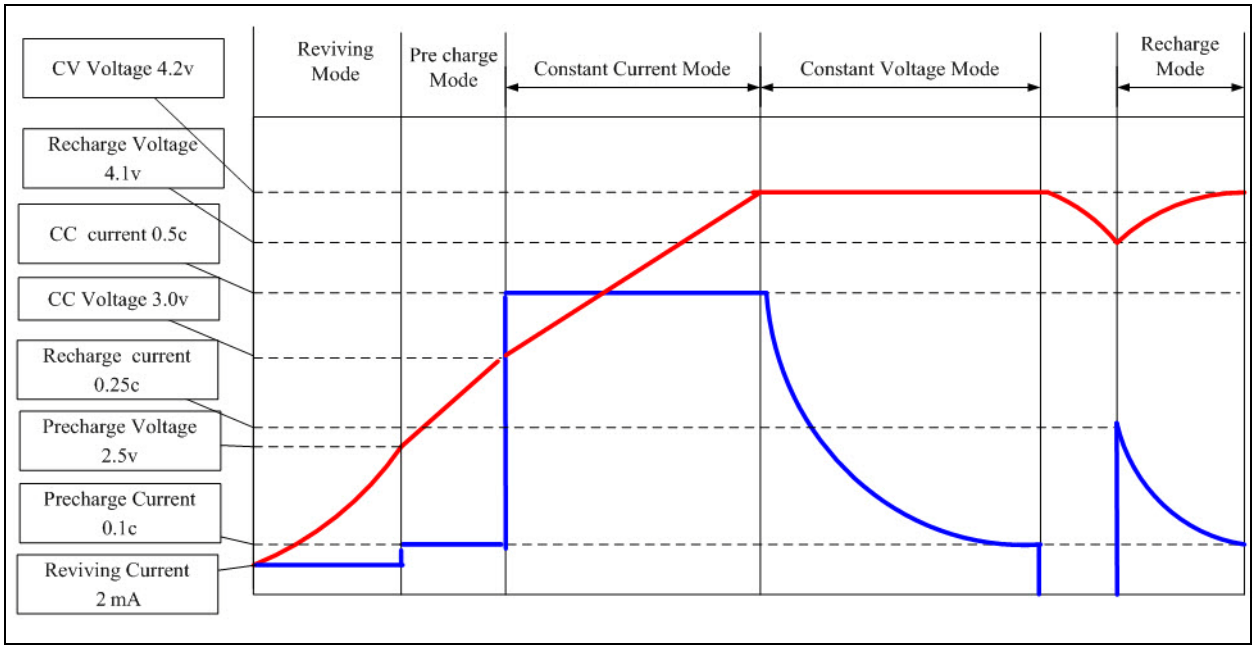
The on-chip Power Management Unit (PMU) has two main features: lithium-ion and lithium-polymer battery charger, and voltage regulation. A power switch is used to switch over the power source between the battery and adapter. Also, the PMU provides current to drive three LEDs.

4.1 Charging a Battery

The BM63 module has a built-in battery charger which is optimized for lithium-ion and lithium-polymer batteries.The charger includes a current sensor for charging control, user programmable current regulation and high-accuracy voltage regulation.

The charging current parameters are configured by the UI tool. Reviving, pre-charging, constant current and constant voltage modes and re-charging functions are included. The maximum charging current is 350 mA. Figure 4-1 illustrates the charging curve of a battery.

FIGURE 4-1: CHARGING CURVE



4.2 Voltage Monitoring

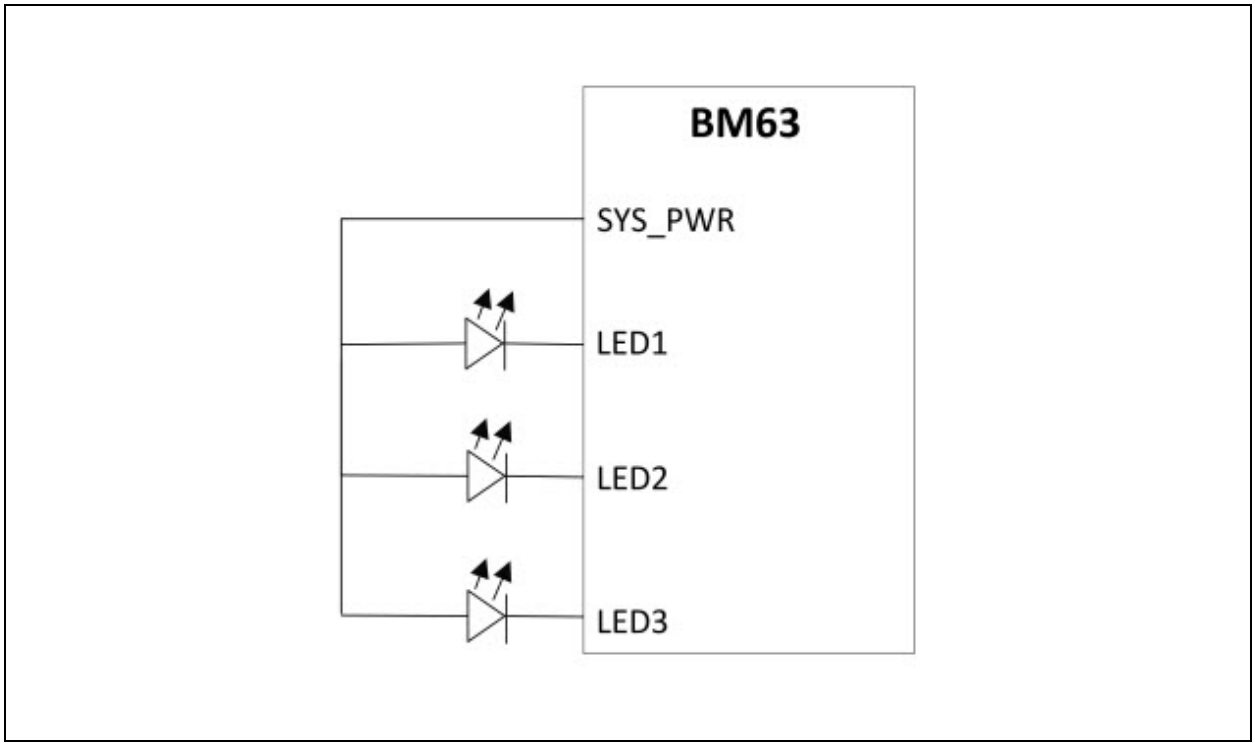
A 10-bit successive approximation register ADC (SAR ADC) provides a dedicated channel for battery voltage level detection. The warning level can be programmed by using the UI tool. The ADC provides a granular resolution to enable the external MCU to take control over the charging process.

4.3 LED Driver

Three dedicated LED drivers control the LEDs. They provide enough sink current (16 step control and 0.35 mA for each step), thus LEDs can be connected directly with the BM63 module.

The LED settings can be configured using the UI tool. Figure 4-2 illustrates the LED drivers in the BM63 module.

FIGURE 4-2: LED DRIVER



4.4 Under Voltage Protection

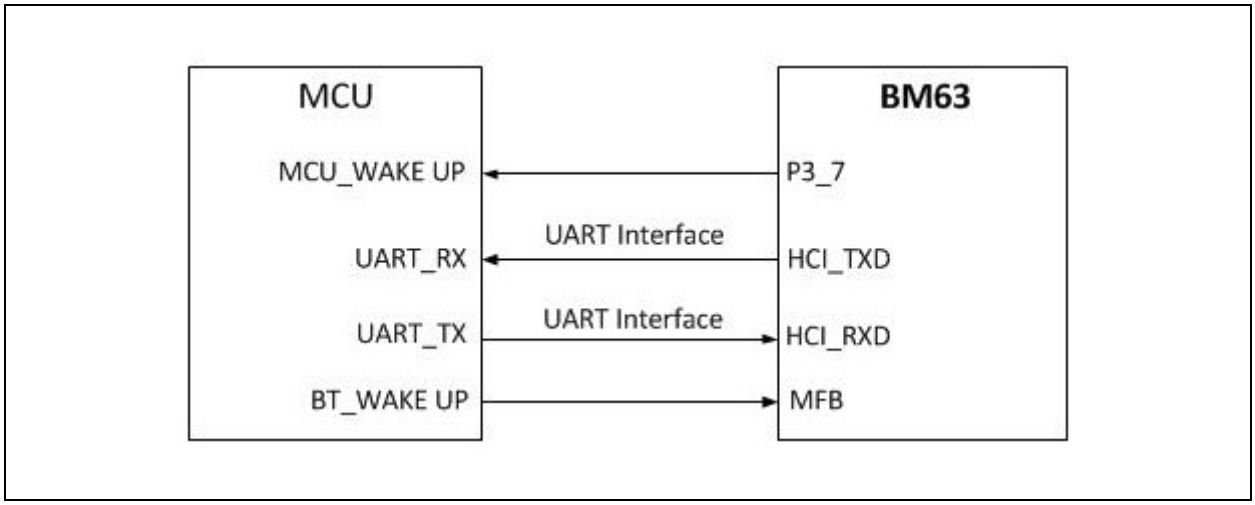
When the voltage of the SYS_PWR pin drops below the voltage level of 2.9V, the system will shutdown automatically.

5.0 APPLICATION INFORMATION

5.1 Host MCU Interface

The BM63 module supports UART commands. The UART commands enable an external MCU to control the BM63 module. Figure 5-1 illustrates the UART interface between the BM63 module and an external MCU.

FIGURE 5-1: HOST MCU INTERFACE OVER UART



The MCU can control the BM63 module over the UART interface and wake-up the module using the MFB pin, the P3_7 pin can be used for this function.

Refer to the *"UART_CommandSet"* document for a list of functions the BM63 module supports and how to use the UI tool to configure the UART and UART Command Set tool.

Note:	The UART Command set Tool (SPKCommandSetTool v160.xx) and *"UART_CommandSet"* document are available for download from the Microchip web site at: www.microchip.com/BM63

Figure 5-2 through Figure 5-6 illustrate the timing sequences of various UART control signals.

FIGURE 5-2: POWER ON/OFF SEQUENCE

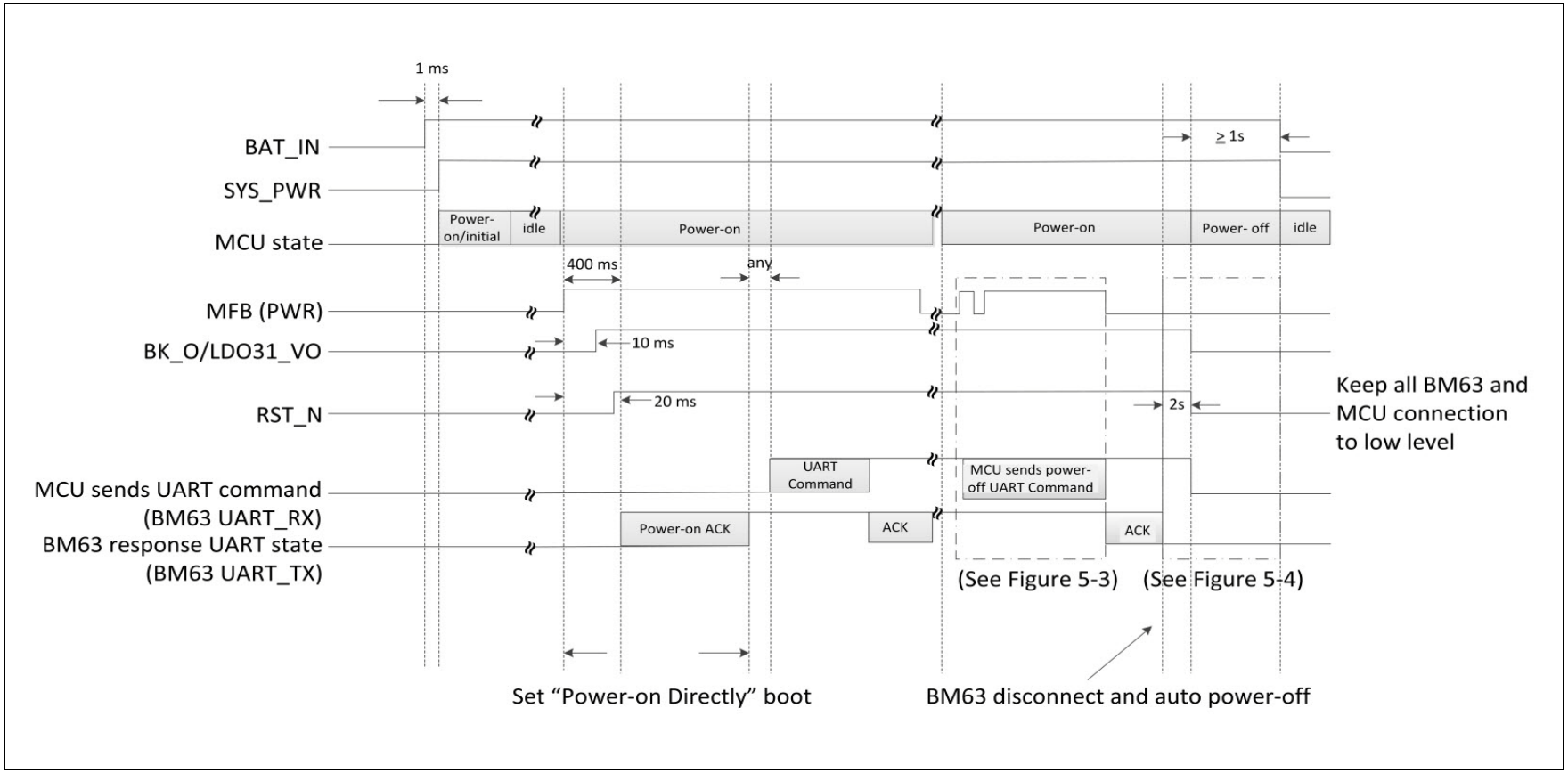


FIGURE 5-3: RX TIMING SEQUENCE (POWER-ON STATE)

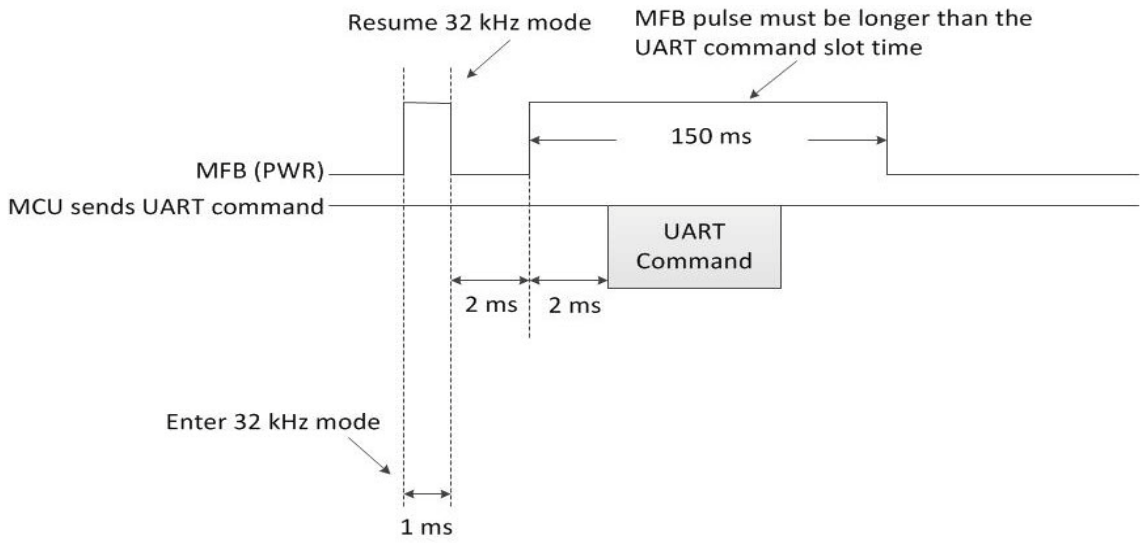
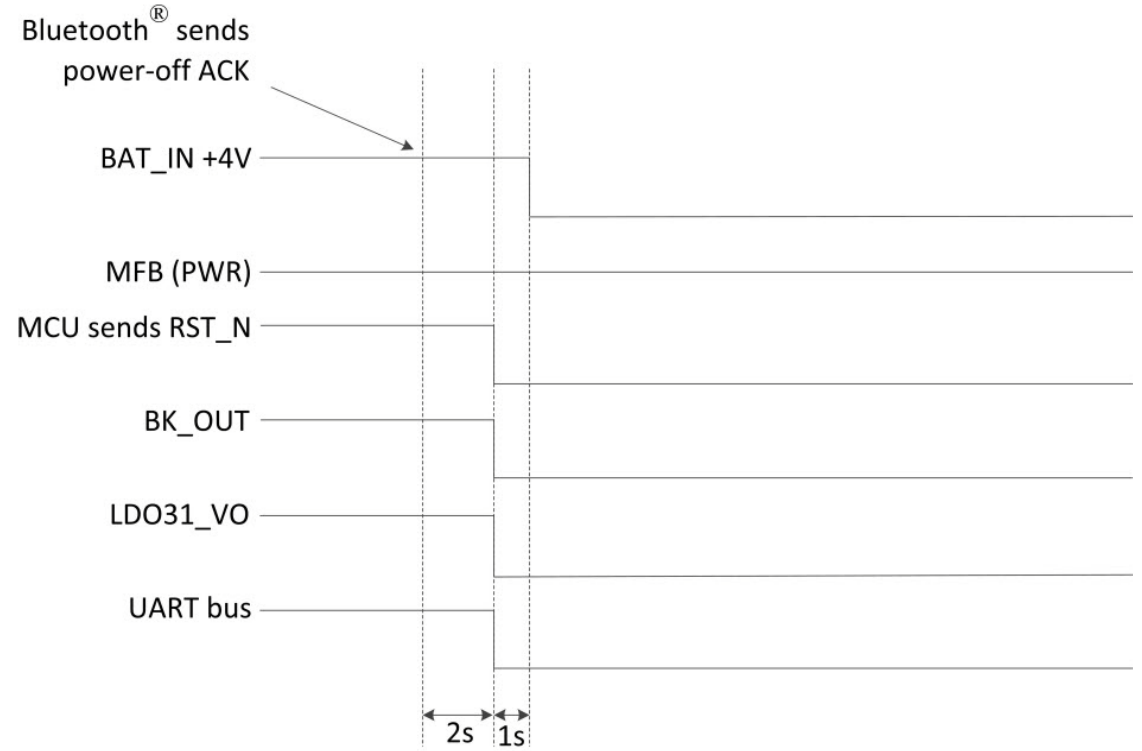


FIGURE 5-4: TIMING SEQUENCE (POWER-OFF STATE)



Note 1: EEPROM clock = 100 kHz.

2: For byte write: 0.01 ms x 32 clock x 2 = 640 µs.

3: It is recommended to have a ramp-down time more than 640 µs during the power-off sequence to ensure safe operation of the device.

FIGURE 5-5: TIMING SEQUENCE OF POWER-ON (NACK)

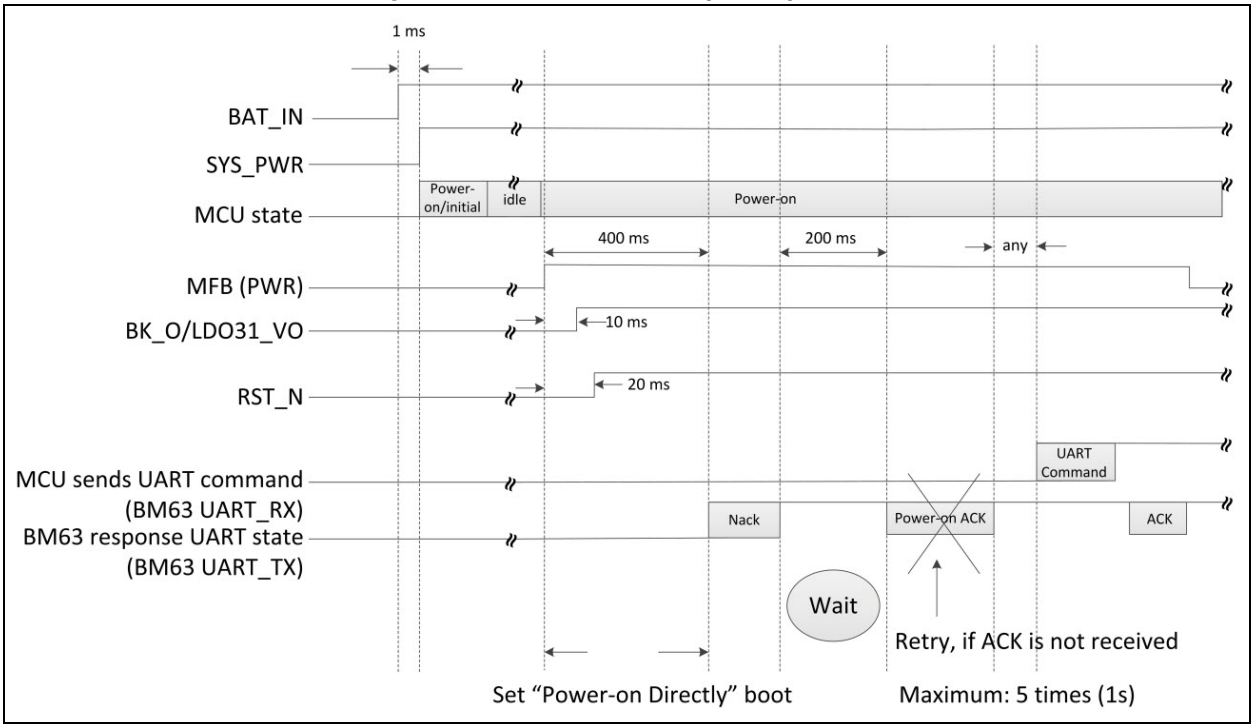
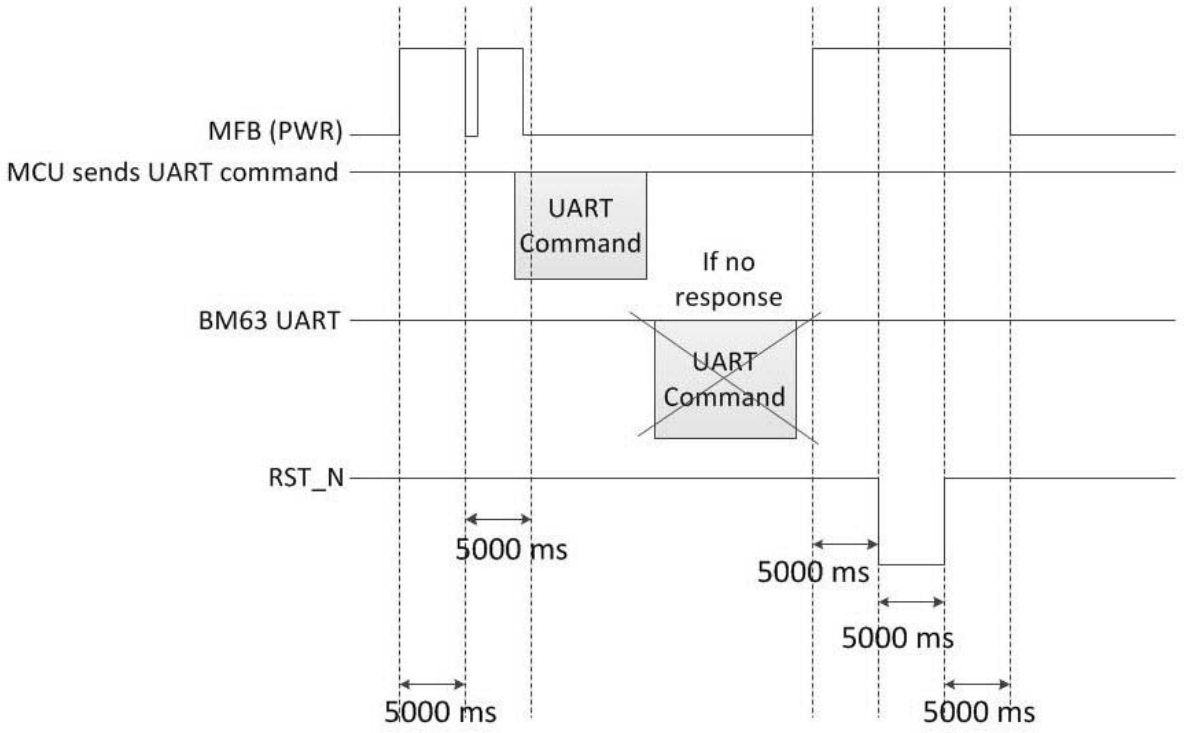


FIGURE 5-6: RESET TIMING SEQUENCE IN NO RESPONSE FROM MODULE TO HOST MCU



Note: When the host MCU sends a UART command and the BM63 module does not respond, the MCU resends the UART command. If the module does not respond within 5 secs, the MCU will force the system to Reset.

5.2 I²S Mode Application

The BM63 module provides an I²S digital audio output interface to connect with the external codec or DSP. It provides 8, 16, 44.1, 48, 88.2 and 96 kHz sampling rates for 16-bit and 24-bit data formats. The I²S setting can be configured by using the UI and DSP tools.

Note:	The UI and DSP tools are available for download from the Microchip web site at: www.microchip.com/BM63.

Figure 5-7 and Figure 5-8 illustrate the I²S signal connection between the BM63 module and an external DSP. Use the DSP tool to configure the BM63 module as a master/slave.

For additional information on timing specifications, refer to **8.1 "Timing specifications"**.

FIGURE 5-7: BM63 MODULE IN I²S MASTER MODE

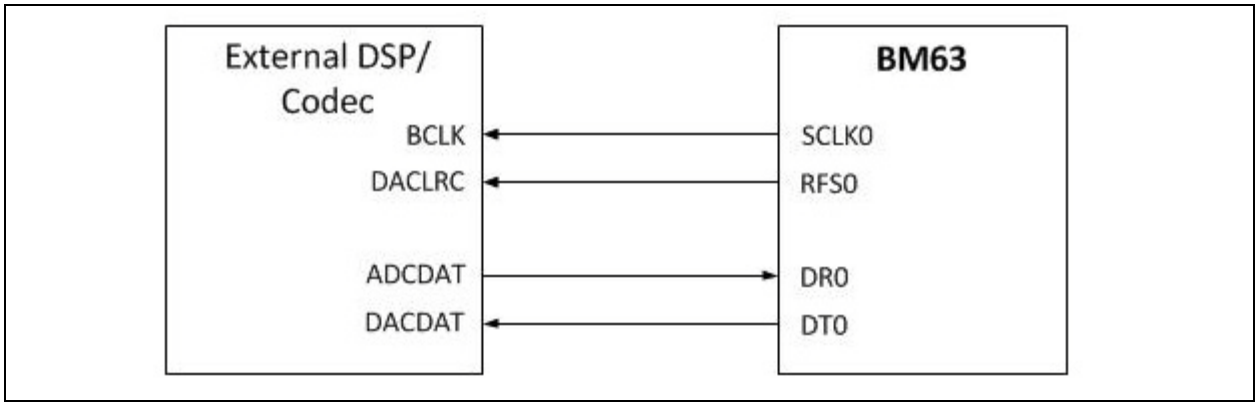
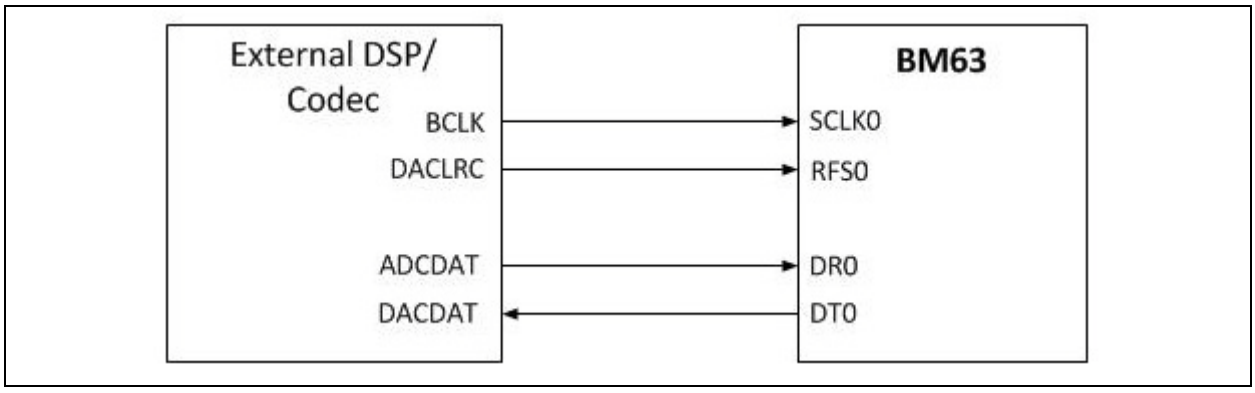


FIGURE 5-8: BM63 MODULE IN I²S SLAVE MODE



5.3 Reset

The BM63 module provides a watchdog timer (WDT) to reset the chip. It has an integrated Power-on Reset (POR) circuit that resets all circuits to a known Power-on state. This action can be driven by an external reset signal which is used to control the device externally by forcing it into a POR state. The RST_N signal input is active-low and no connection is required in most of the applications.

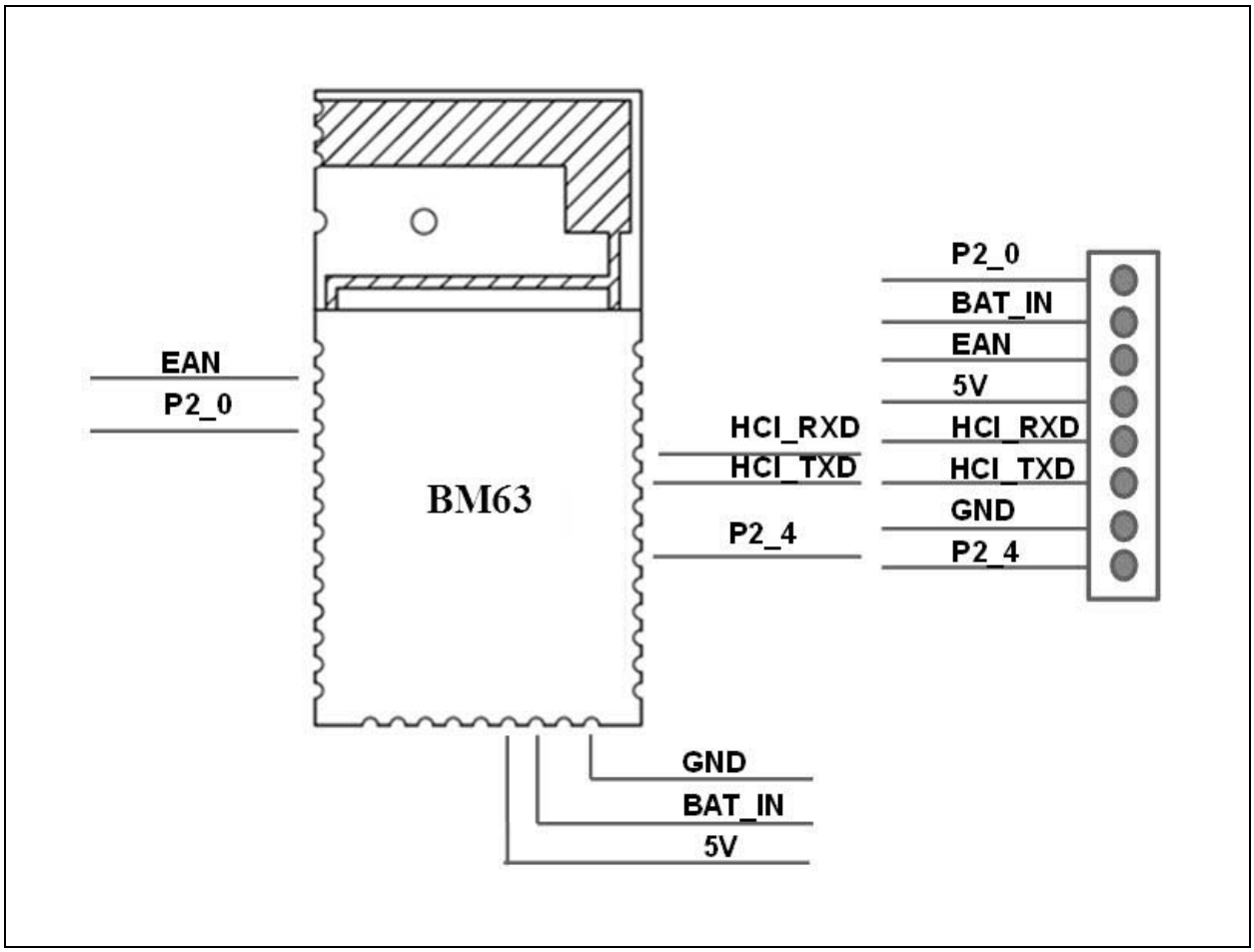
5.4 External Configuration and Programming

The BM63 module can be configured by using an external configuration tool (EEPROM tool) and firmware is programmed by using a programming tool (Flash tool).

Note:	The EEPROM and Flash tools are available for download from the Microchip web site at: www.microchip.com/BM63.

Figure 5-9 illustrates the configuration and firmware programming interface on the BM63 module. It is recommended to include a header pin on the main PCB for development.

FIGURE 5-9: EXTERNAL PROGRAMMING HEADER CONNECTIONS



Configuration and firmware programming modes are entered according to the system configuration I/O pins. Table 5-1 provides the system configuration settings. The P2_0, P2_4 and EAN pins have internal pull up.

TABLE 5-1: SYSTEM CONFIGURATION SETTINGS

P2_0	P2_4	EAN	Operating Mode
High	High	Low (Flash), High (ROM)	APP mode (Normal operation)
Low	High	Low (Flash), High (ROM)	Test mode (Write EEPROM)
Low	Low	High	Write Flash

5.5 Reference Circuit

Figure 5-10 through Figure 5-13 illustrate the BM63 module reference circuit for a stereo headset application.

FIGURE 5-10: BM63 REFERENCE CIRCUIT FOR STEREO HEADSET

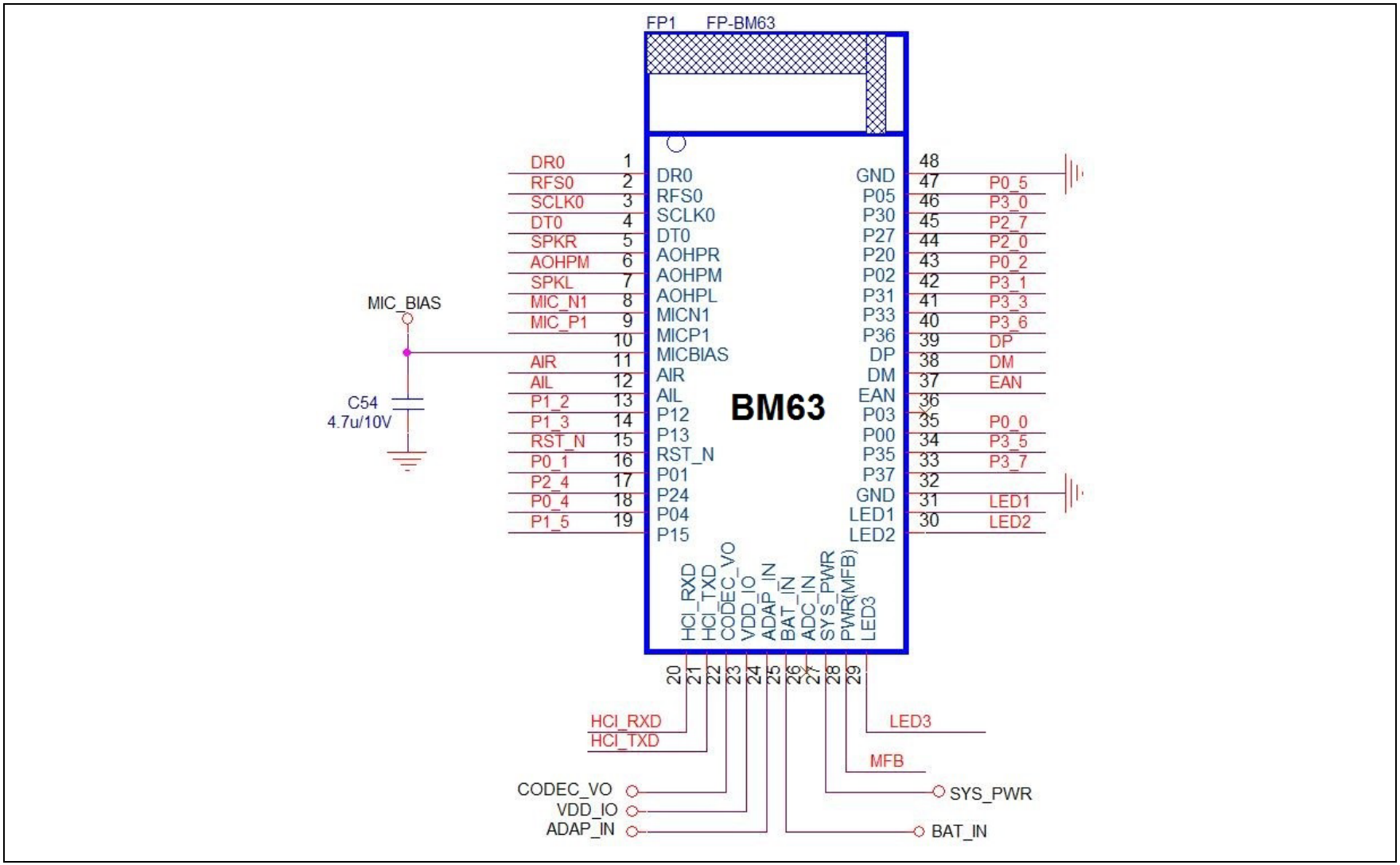
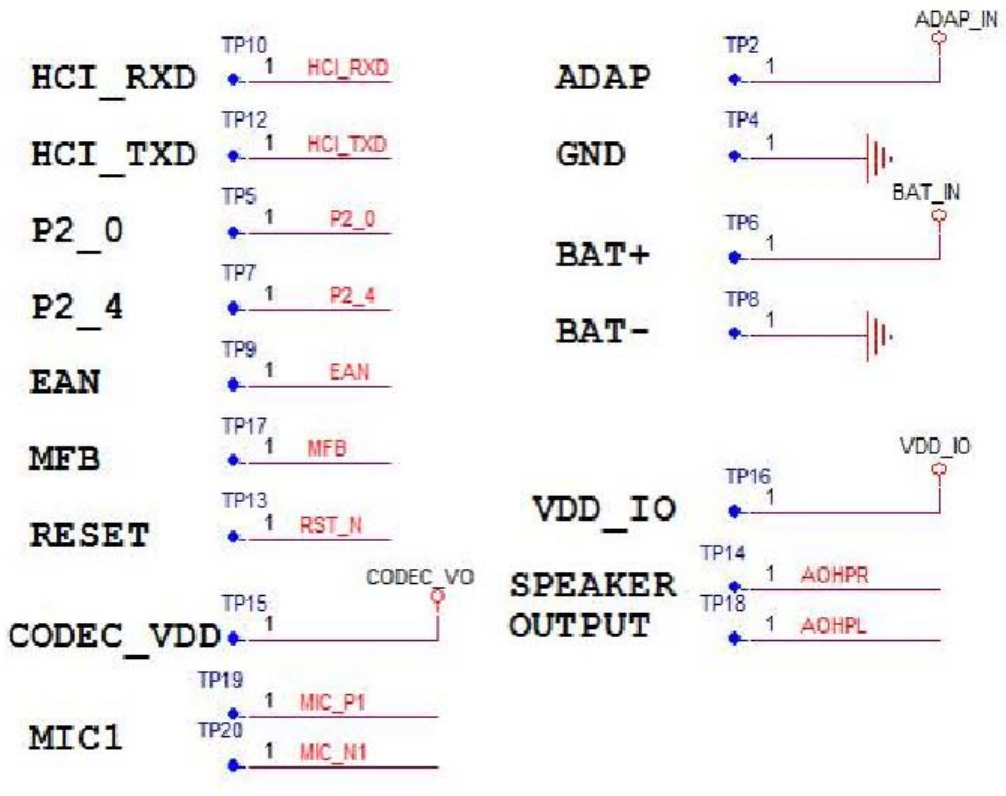


FIGURE 5-11: BM63 REFERENCE CIRCUIT FOR STEREO HEADSET



GPIO Description

MFB	UART_RX_IND; MFB
P0_2	PLAY/PAUSE
P2_7	VOL+
P0_5	VOL-
P3_1	REV
P3_3	FWD
P0_0	SLDIE SWITCH
P0_4	AMP_EN/NFC
P3_0	AUX IN Detection
P3_7	UART_TX_IND
P1_5	AMP_EN/SLIDE_SWITCH
	Multi-SPK Master/Slave mode control
P3_6	Multi-SPK Master/Slave mode control
P2_0	System Configuration
EAN	System Configuration

FIGURE 5-12: BM63 REFERENCE CIRCUIT FOR STEREO HEADSET

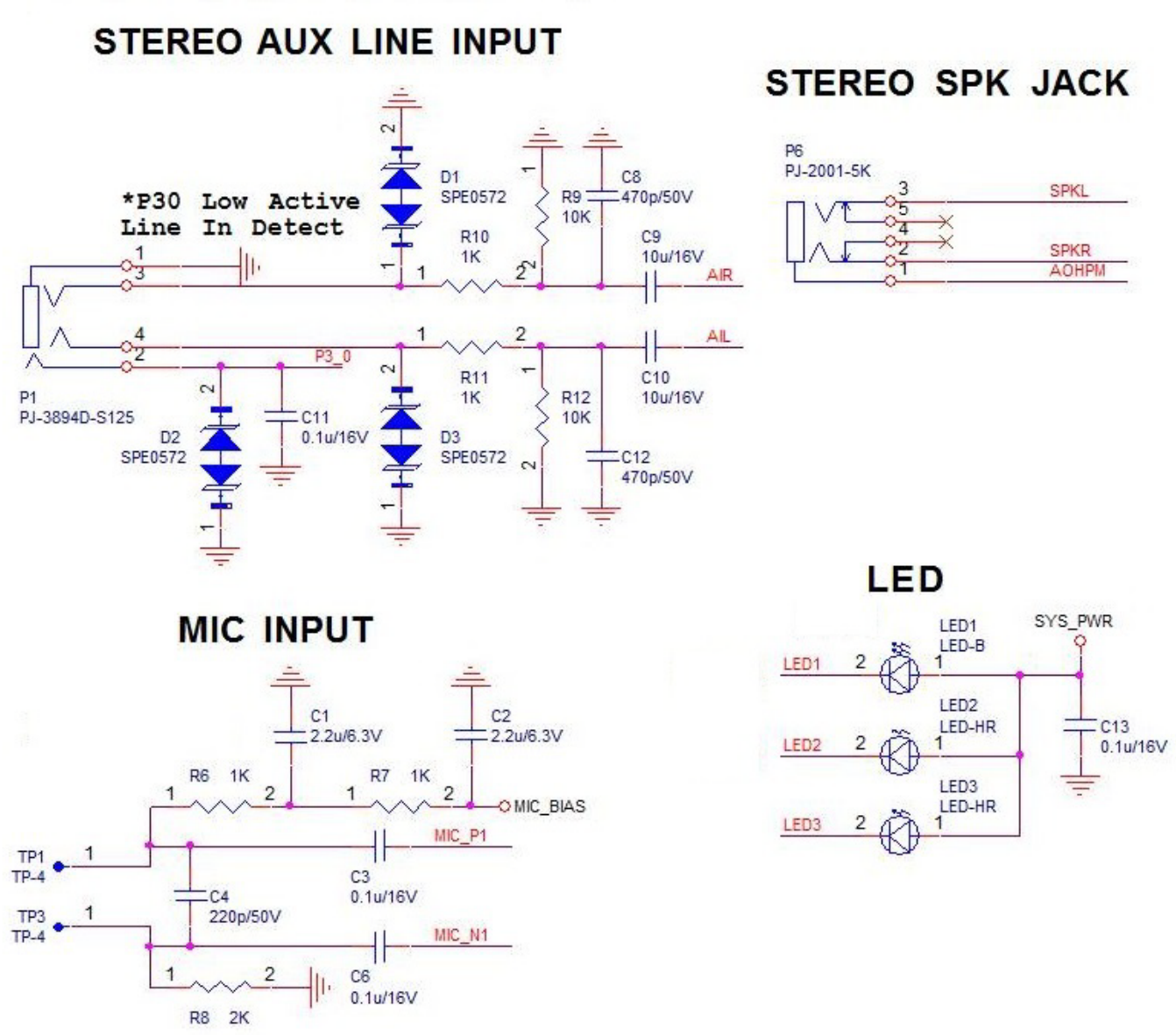


FIGURE 5-13: BM63 REFERENCE CIRCUIT FOR STEREO HEADSET

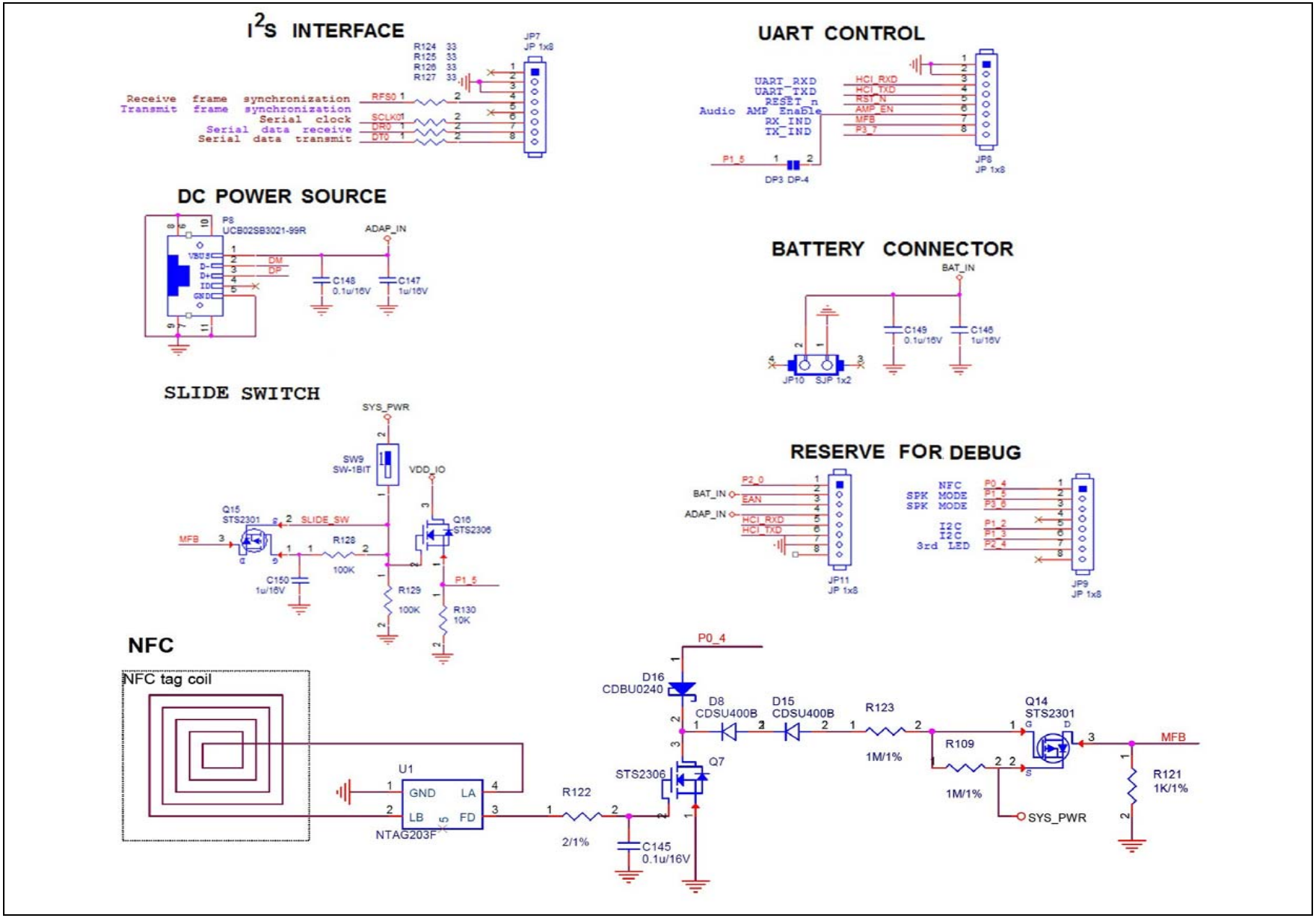
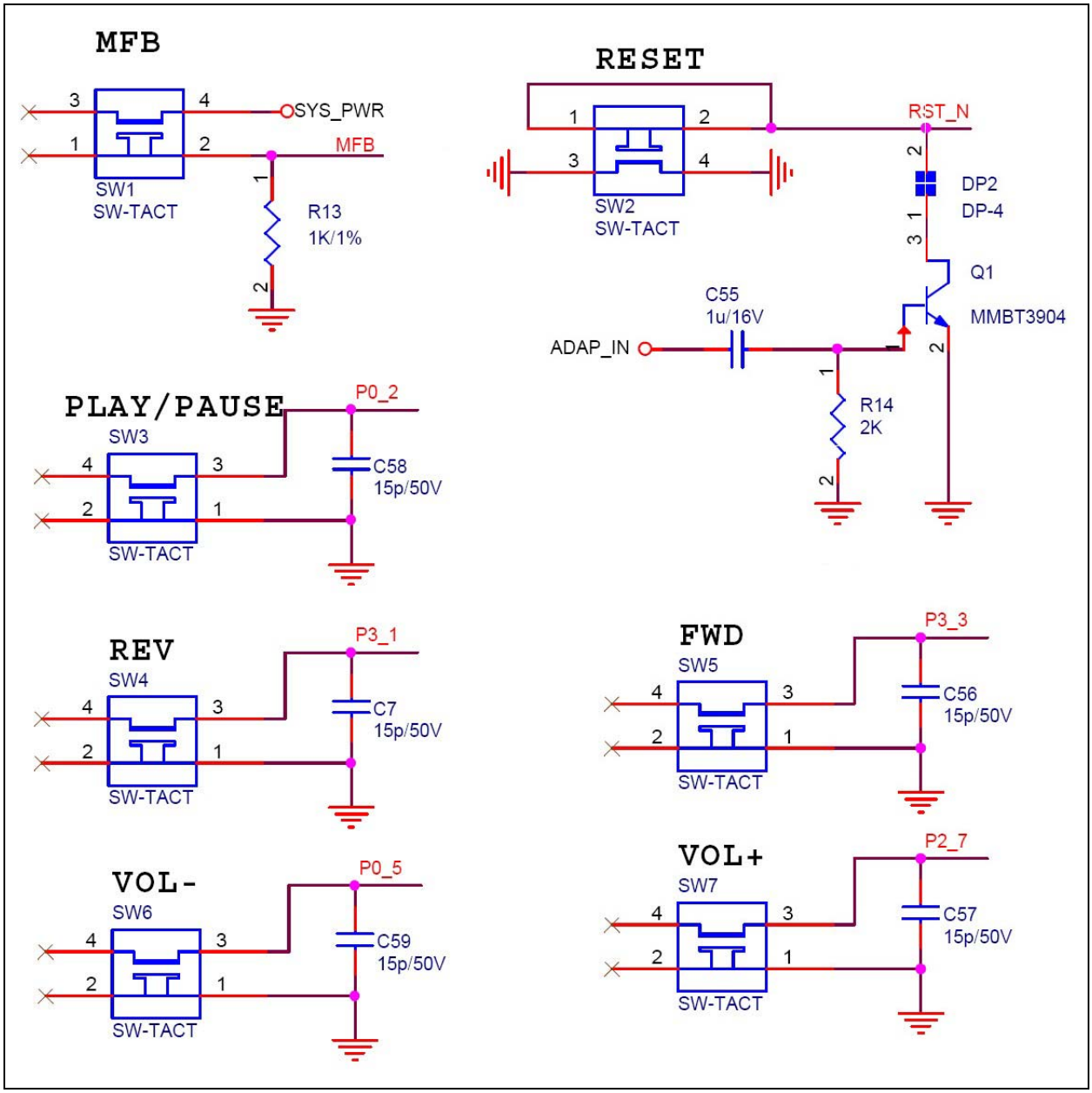


FIGURE 5-14: BM63 REFERENCE CIRCUIT FOR STEREO HEADSET



NOTES:

6.0 PRINTED ANTENNA INFORMATION

6.1 Antenna Radiation Pattern

The BM63 module is integrated with one PCB printed antenna, see Figure 6-1.

FIGURE 6-1: RECOMMENDED KEEP OUT AREA FOR PCB ANTENNA

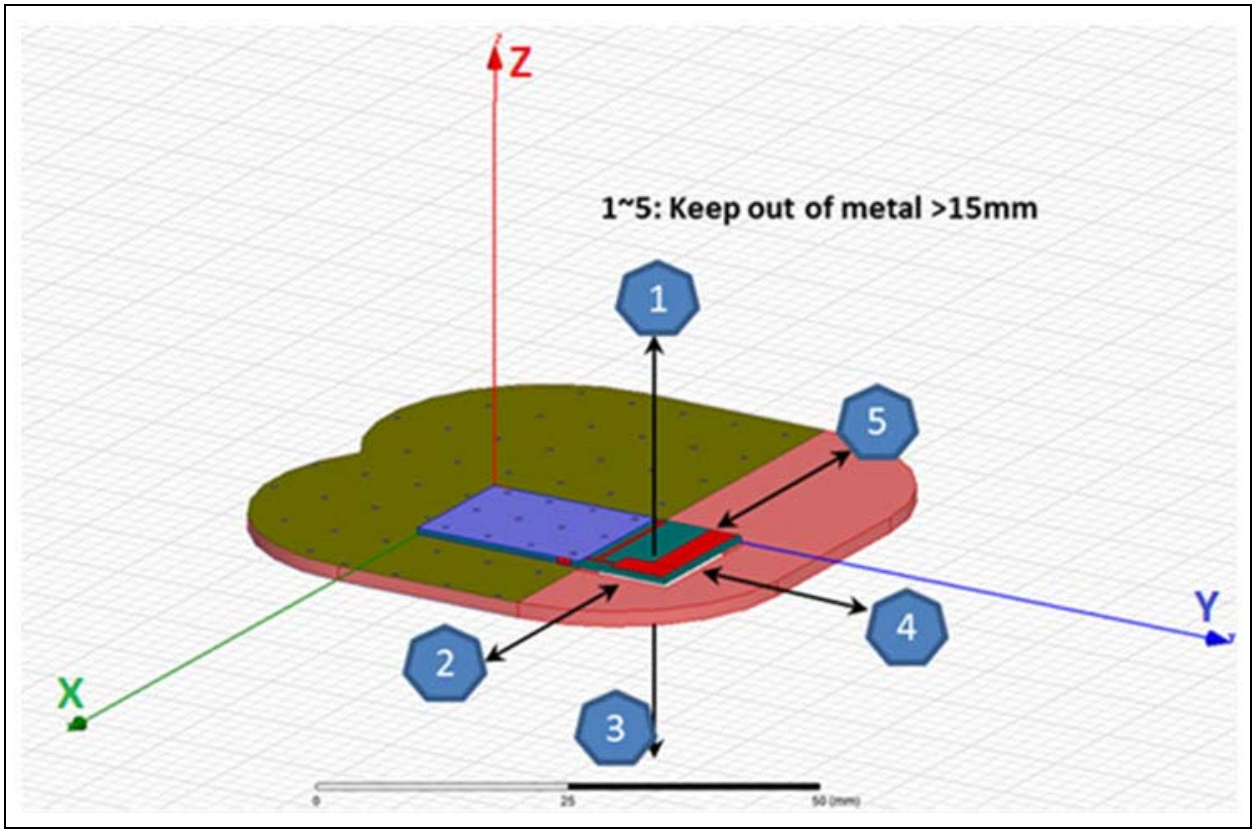


Figure 6-2 illustrates the 3D radiation pattern of the PCB printed antenna at 2441 MHz.

FIGURE 6-2: PCB ANTENNA RADIATION PATTERN

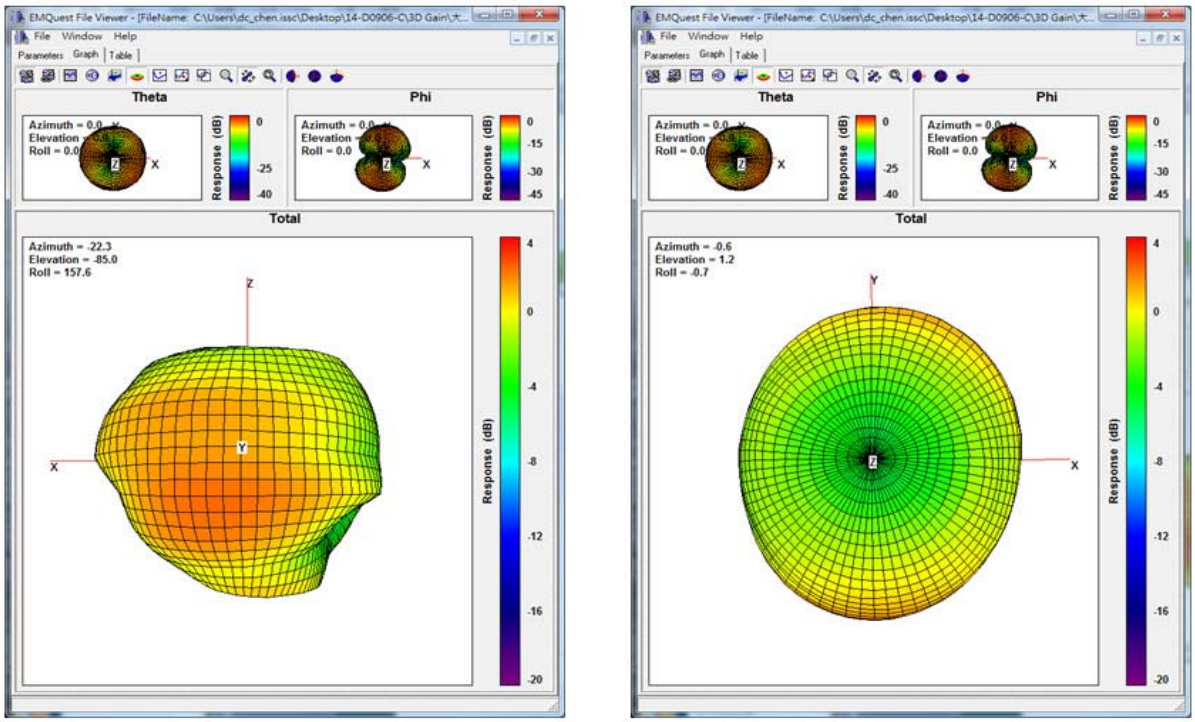


TABLE 6-1: PCB ANTENNA CHARACTERISTICS

Parameter	Values
Frequency	2400 MHz ~ 2480 MHz
Peak Gain	1.927 dBi
Efficiency	73.41%

6.2 Module Placement Guidelines

For Bluetooth-enabled products, the antenna placement affects the overall performance of the system. The antenna requires free space to radiate RF signals and it should not be surrounded by the ground plane. Microchip recommends that the areas underneath the antenna on the host PCB must not contain copper on the top, inner, or bottom layers, as illustrated in Figure 6-1.

A low-impedance ground plane will ensure the best radio performance (best range, lowest noise). The ground plane can be extended beyond the minimum recommendation as required for the main PCB EMC noise reduction. For the best range performance, keep all external metal at least 15 mm away from the on-board PCB trace antenna. Figure 6-3 and Figure 6-4 illustrate the good and poor placement of the BM63 module on a host board with GND plane.

FIGURE 6-3: BM63 PLACEMENT GUIDELINES

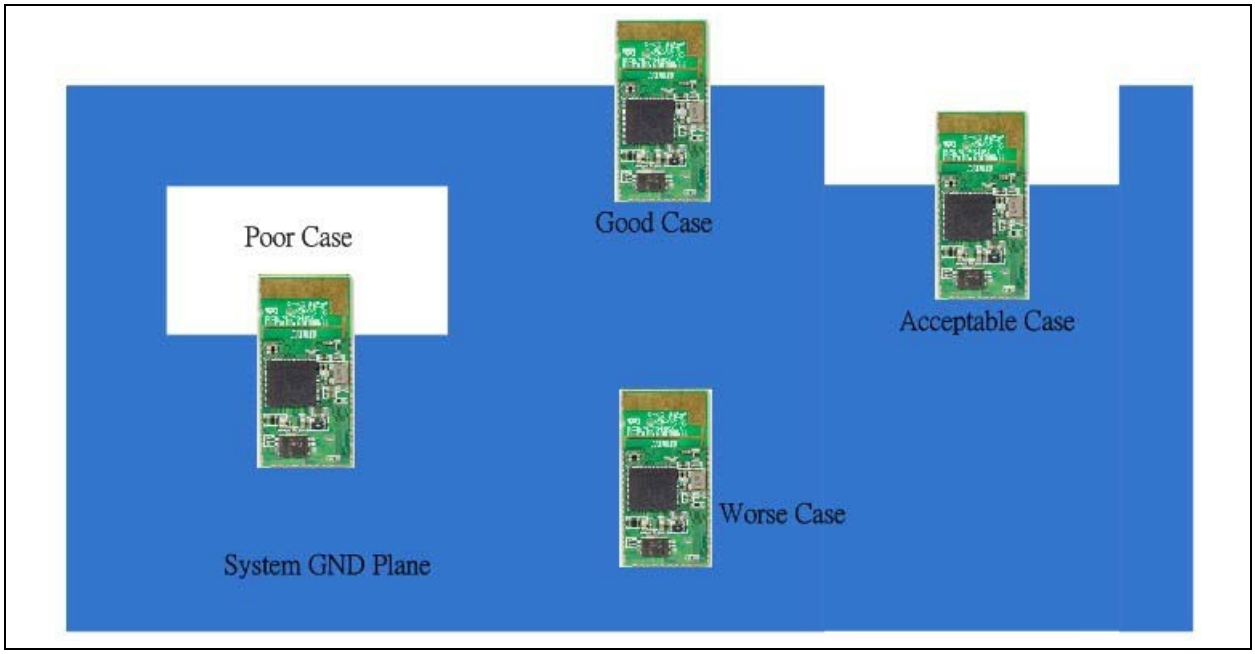
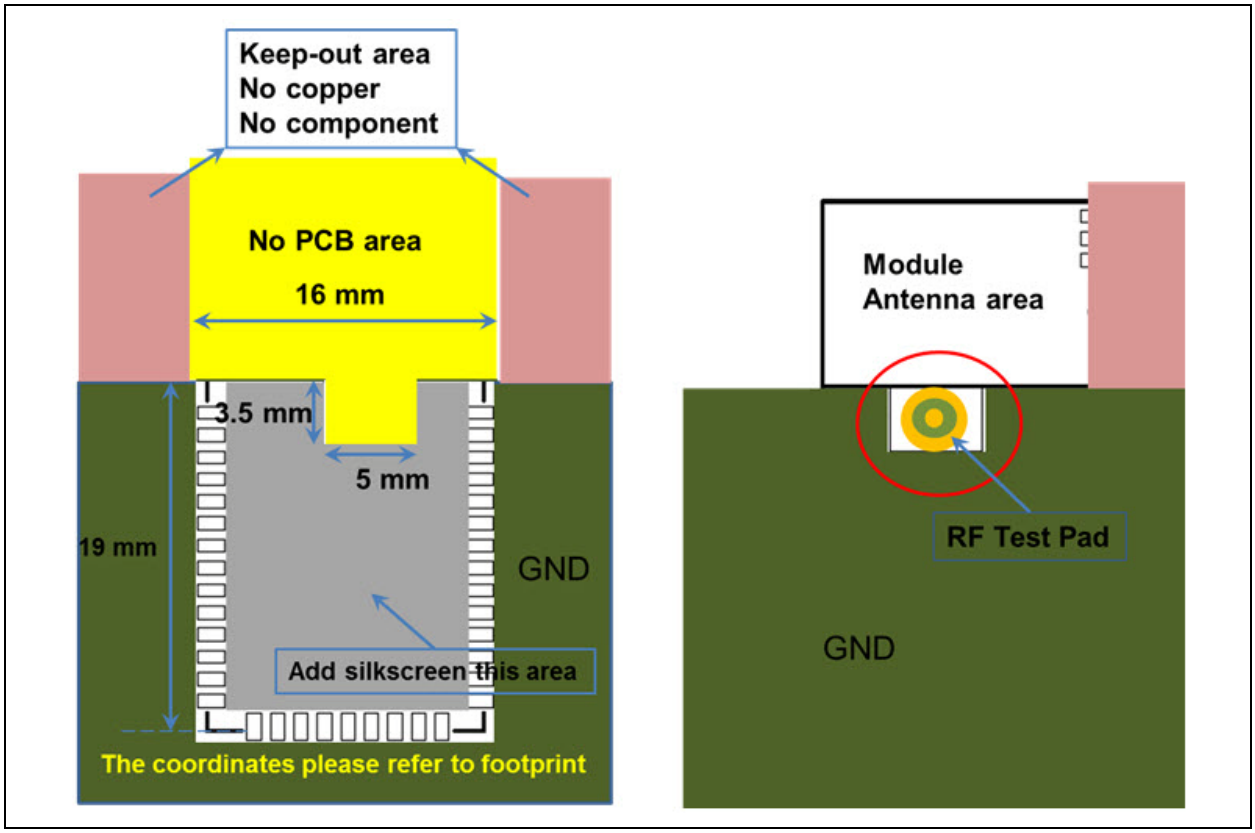


FIGURE 6-4: GND PLANE ON MAIN APPLICATION BOARD

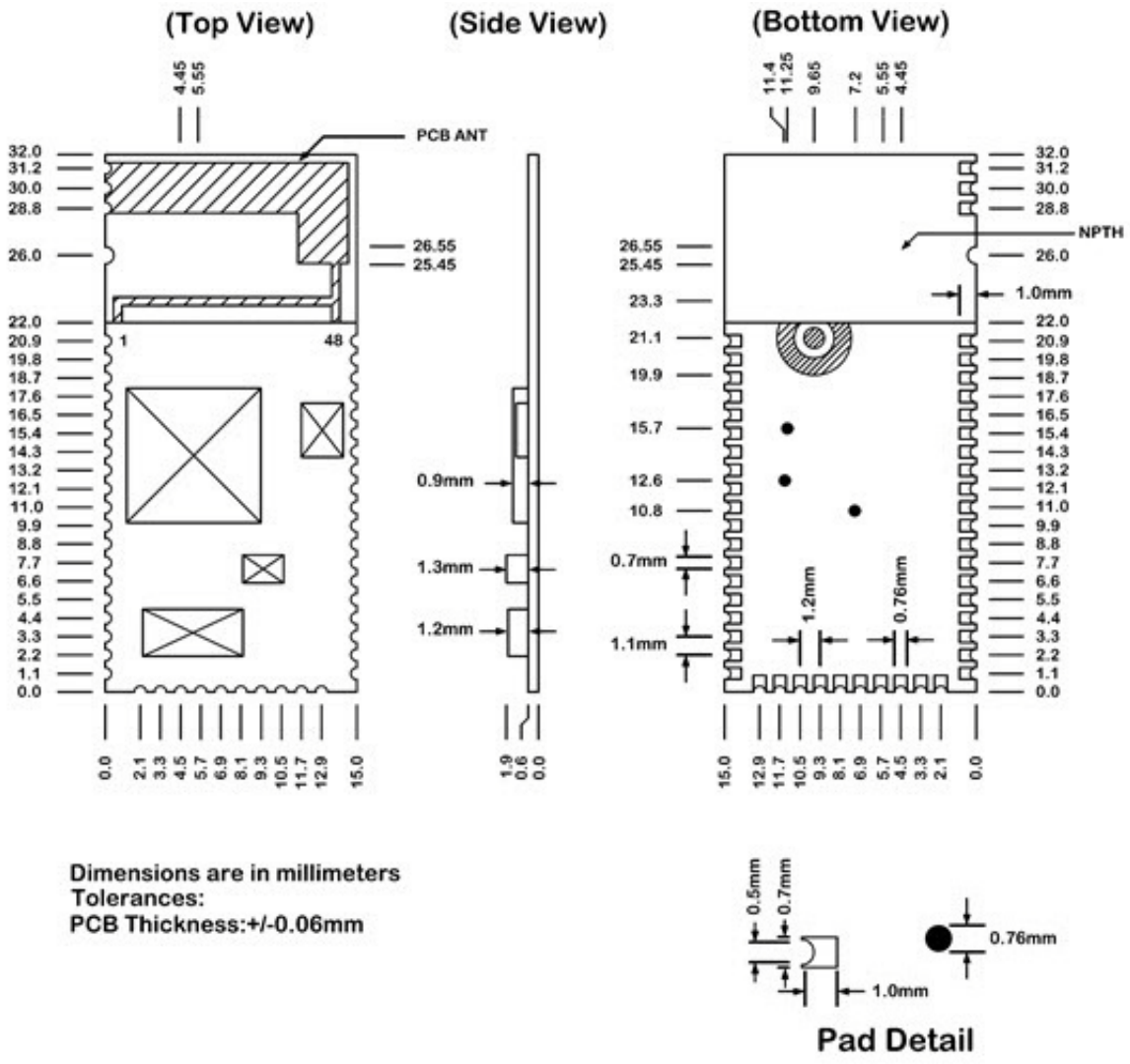


NOTES:

7.0 PHYSICAL DIMENSIONS

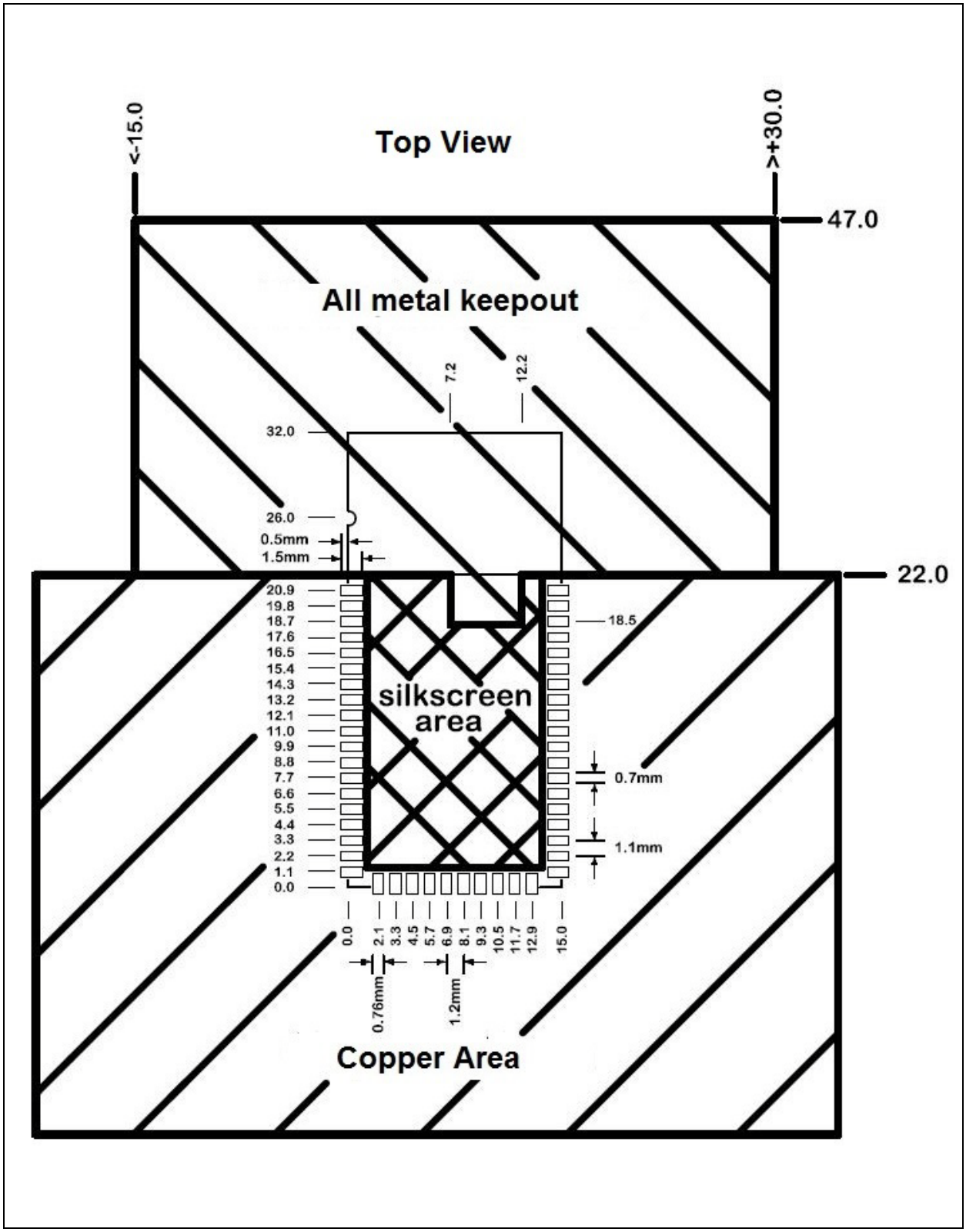
Figure 7-1 illustrates the PCB dimension of the BM63 module and Figure 7-2 illustrates the PCB footprint of the BM63 module.

FIGURE 7-1: BM63 PCB DIMENSION



Note: PCB Dimensions: X: 15.0 mm, Y: 32.0 mm, tolerances: 0.25 mm

FIGURE 7-2: RECOMMENDED BM63 PCB FOOTPRINT



8.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the BM63 module electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the BM63 module are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions, above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings

Ambient temperature under bias.....-20°C to +70°C
Storage temperature .....-40°C to +125°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +3.6V
Maximum output current sink by any I/O pin.....12 mA
Maximum output current sourced by any I/O pin.....12 mA

Note: Stresses listed under **"Absolute Maximum Ratings"** may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions and those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 8-1: RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min.	Typical	Max.	Unit
BAT_IN	Input voltage for battery	3.2	3.8	4.2	V
ADAP_IN	Input voltage for adapter	4.5	5	5.5	V
$T_{OPERATION}$	Operation temperature	-20	+25	+70	ºC

TABLE 8-2: I/O AND RESET LEVEL

Parameter	Min.	Typical	Max.	Unit
I/O Supply Voltage (VDD_IO)	3.0	3.3	3.6	V
I/O Voltage Levels				
VIL input logic levels low	0	–	0.8	V
VIH input logic levels high	2.0	–	3.6	V
VOL output logic levels low	–	–	0.4	V
VOH output logic levels high	2.4	–	–	V
RST_N				
Threshold voltage	–	0.8	–	V

Note: These parameters are characterized but not tested in manufacturing.

TABLE 8-3: BATTERY CHARGER(1,3)

Parameter		Min.	Typical	Max.	Unit
ADAP_IN Input Voltage		4.5	5.0	5.5	V
Supply current to charger only		–	3	4.5	mA
Maximum Battery Fast Charge Current	Headroom > 0.7V (ADAP_IN = 5V)	–	350	–	mA
	Headroom = 0.3V~0.7V (ADAP_IN = 4.5V)	–	175(2)	–	mA
Trickle Charge Voltage Threshold		–	3	–	V
Battery Charge Termination Current, (% of Fast Charge Current)		–	10	–	%

Note 1: Headroom = $V_{ADAP\_IN} - V_{BAT}$

2: When $V_{ADAP\_IN} - V_{BAT} > 2V$, the maximum fast charge current is 175 mA for thermal protection.

3: These parameters are characterized but not tested in manufacturing.

TABLE 8-4: LED DRIVER(1,2)

Parameter	Min.	Typical	Max.	Unit
Open-drain Voltage	–	–	3.6	V
Programmable Current Range	0	–	5.25	mA
Intensity Control	–	16	–	step
Current Step	–	0.35	–	mA
Power Down Open-drain Current	–	–	1	µA
Shutdown Current	–	–	1	µA

Note 1: Test condition: BK_O = 1.8V with temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-5: AUDIO CODEC ANALOG TO DIGITAL CONVERTER(2)

T = 25 ^{o}C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz				
Parameter (Condition)	**Min.**	**Typical**	**Max.**	**Unit**
Resolution	–	–	16	Bit
Output Sample Rate	8	–	48	kHz
Signal to Noise Ratio **(Note 1)** (SNR at MIC or Line-in mode)	–	92	–	dB
Digital Gain	-54	–	4.85	dB
Digital Gain Resolution	–	2~6	–	dB
MIC Boost Gain	–	20	–	dB
Analog Gain	–	-	60	dB
Analog Gain Resolution	–	2.0	–	dB
Input full-scale at maximum gain (differential)	–	4	–	mV/rms
Input full-scale at minimum gain (differential)	–	800	–	mV/rms
3 dB bandwidth	–	20	–	kHz
Microphone mode (input impedance)	–	24	–	kOhm
THD+N (microphone input) at 30 mV/rms input	–	0.02	–	%

Note 1: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 1%, 150 mV_{pp} input.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-6: AUDIO CODEC DIGITAL TO ANALOG CONVERTER(4)

T = 25 °C, VDD = 2.8V, 1 kHz sine wave input, Bandwidth = 20 Hz~20 kHz					
Parameter (Condition)		**Min.**	**Typical**	**Max.**	**Unit**
Over-sampling rate		–	128	–	f_s
Resolution		16	–	20	Bit
Output Sample Rate		8	–	48	kHz
Signal to Noise Ratio **(Note 1)** (SNR at capless mode) for 48 kHz		–	98	–	dB
Signal to Noise Ratio **(Note 1)** (SNR at single-ended mode) for 48 kHz		–	98	–	dB
Digital Gain		-54	–	4.85	dB
Digital Gain Resolution		–	2~6	–	dB
Analog Gain		-28	–	3	dB
Analog Gain Resolution		–	1	–	dB
Output Voltage Full-scale Swing (AVDD = 2.8V)		495	742.5	–	mV/rms
Maximum Output Power (16 Ohm load)		–	34.5	–	mW
Maximum Output Power (32 Ohm load)		–	17.2	–	mW
Allowed Load	Resistive	–	16	O.C.	Ohm
	Capacitive	–	–	500	pF
THD+N (16 Ohm load) **(Note 2)**		–	0.05	–	%
Signal to Noise Ratio (SNR at 16 Ohm load) **(Note 3)**		–	98	–	dB

Note 1: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 0.01%, 0dBFS signal, Load = 100 kOhm

2: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, -1dBFS signal, Load =16 Ohm

3: f_{in} = 1 kHz, B/W = 20~20 kHz, A-weighted, THD+N < 0.05%, 0dBFS signal, Load = 16 Ohm

4: These parameters are characterized but not tested in manufacturing.

TABLE 8-7: TRANSMITTER SECTION FOR BDR AND EDR(1,2,3)

Parameter	**Min.**	**Typical**	**Max.**	**Bluetooth specification**	**Unit**
Maximum RF transmit power	–	2	–	-6 to 4	dBm
EDR/BDR Relative transmit power	-4	-1.8	1	-4 to 1	dB

Note 1: The RF Tx power is modulation value.

2: The RF Transmit power is calibrated during the production using the MP tool and MT8852 Bluetooth Test equipment.

3: Test condition: VCC_RF = 1.28V, temperature +25 ºC.

TABLE 8-8: RECEIVER SECTION FOR BDR AND EDR(1,2)

	Modulation	Min.	Typical	Max.	Bluetooth specification	Unit
Sensitivity at 0.1% BER	GFSK	–	-89	–	≤-70	dBm
Sensitivity at 0.01% BER	π/4 DQPSK	–	-90	–	≤-70	dBm
	8 DPSK	–	-83	–	≤-70	dBm

Note 1: Test condition: VCC_RF = 1.28V with temperature +25 ºC.

2: These parameters are characterized but not tested in manufacturing.

TABLE 8-9: SYSTEM CURRENT CONSUMPTION OF BM63(2,3)

System Status	Typical(1)	Max.	Unit
System-off mode	–	10	μA
Stop advertising (Samsung S5 (SM-G900I)/Android™ 4.4.2)			
Stand-by mode	0.57	–	mA
Link mode	0.5	–	mA
ESCO link	15.1	–	mA
A2DP link	14.3	–	mA
Stop advertising (iPhone® 6/iOS 8.4)			
Stand-by mode	0.6	–	mA
Link mode	0.6	–	mA
SCO link	15.3	–	mA
A2DP link	15.4	–	mA

Note 1: The measurement data corresponds to Firmware v1.0.

2: Mode definition:
Stand-by mode: Power-on without Bluetooth link
Link mode: With Bluetooth link in Low-Power mode.

3: The current consumption values are measured with the BM63 EVB as a test platform, with BAT_IN = 3.8V. The distance between the smartphone and BM63 EVB is 30 cm, and the speaker is without loading.

8.1 Timing specifications

Figure 8-1 and Figure 8-2 illustrate the timing diagram of the BM63 module in I^2S and PCM modes.

FIGURE 8-1: TIMING DIAGRAM FOR I^2S MODES (MASTER/SLAVE)

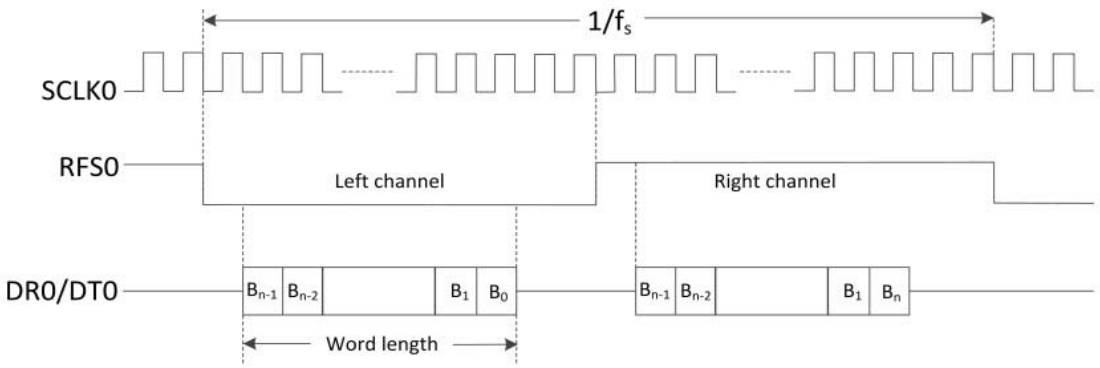
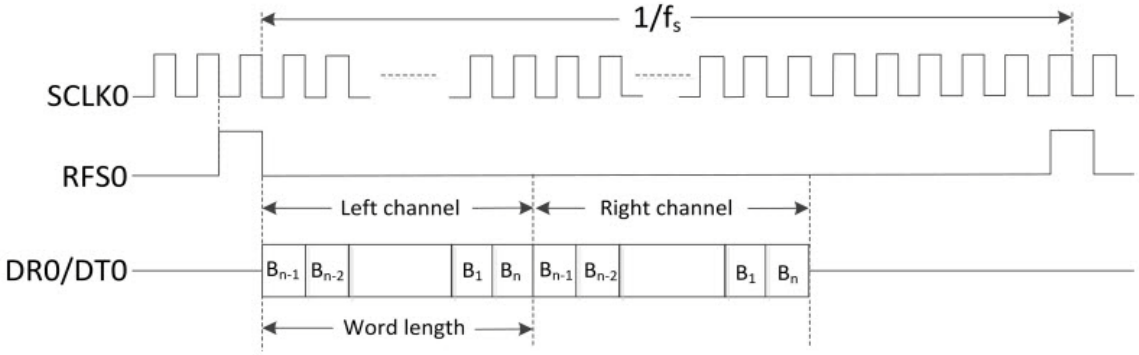


FIGURE 8-2: TIMING DIAGRAM FOR PCM MODES (MASTER/SLAVE)



Note 1: f_S: 8,16, 32, 44.1, 48, 88.2 and 96 kHz.

2: SCLK0: $64*f_S/256*f_S$.

3: Word length: 16-bit and 24-bit.

Figure 8-3 illustrates the timing diagram of the audio interface and Table 8-10 provides the timing specifications.

FIGURE 8-3: AUDIO INTERFACE TIMING DIAGRAM

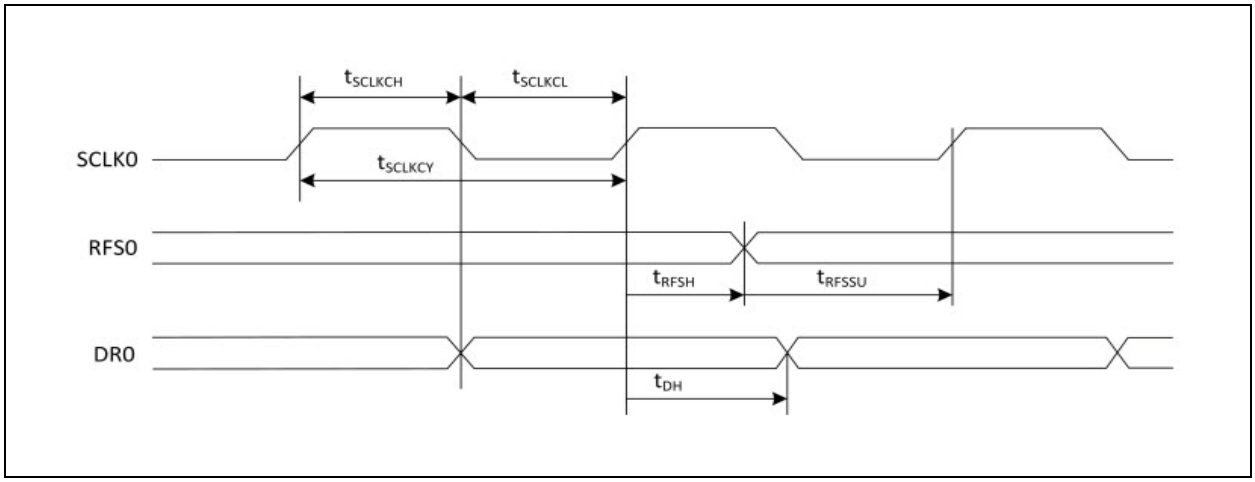


TABLE 8-10: AUDIO INTERFACE TIMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK0 duty ratio	d_{SCLK}	–	50	–	%
SCLK0 cycle time	t_{SCLKCY}	50	–	–	ns
SCLK0 pulse width high	t_{SCLKCH}	20	–	–	ns
SCLK0 pulse width low	t_{SCLKCL}	20	–	–	ns
RFS0 set-up time to SCLK0 rising edge	t_{RFSSU}	10	–	–	ns
RFS0 hold time from SCLK0 rising edge	t_{RFSH}	10	–	–	ns
DR0 hold time from SCLK0 rising edge	t_{DH}	10	–	–	ns

Note: Test Conditions: Slave mode, f_s = 48 kHz, 24-bit data and SCLK0 period = 256 f_s.

NOTES:

9.0 SOLDERING RECOMMENDATIONS

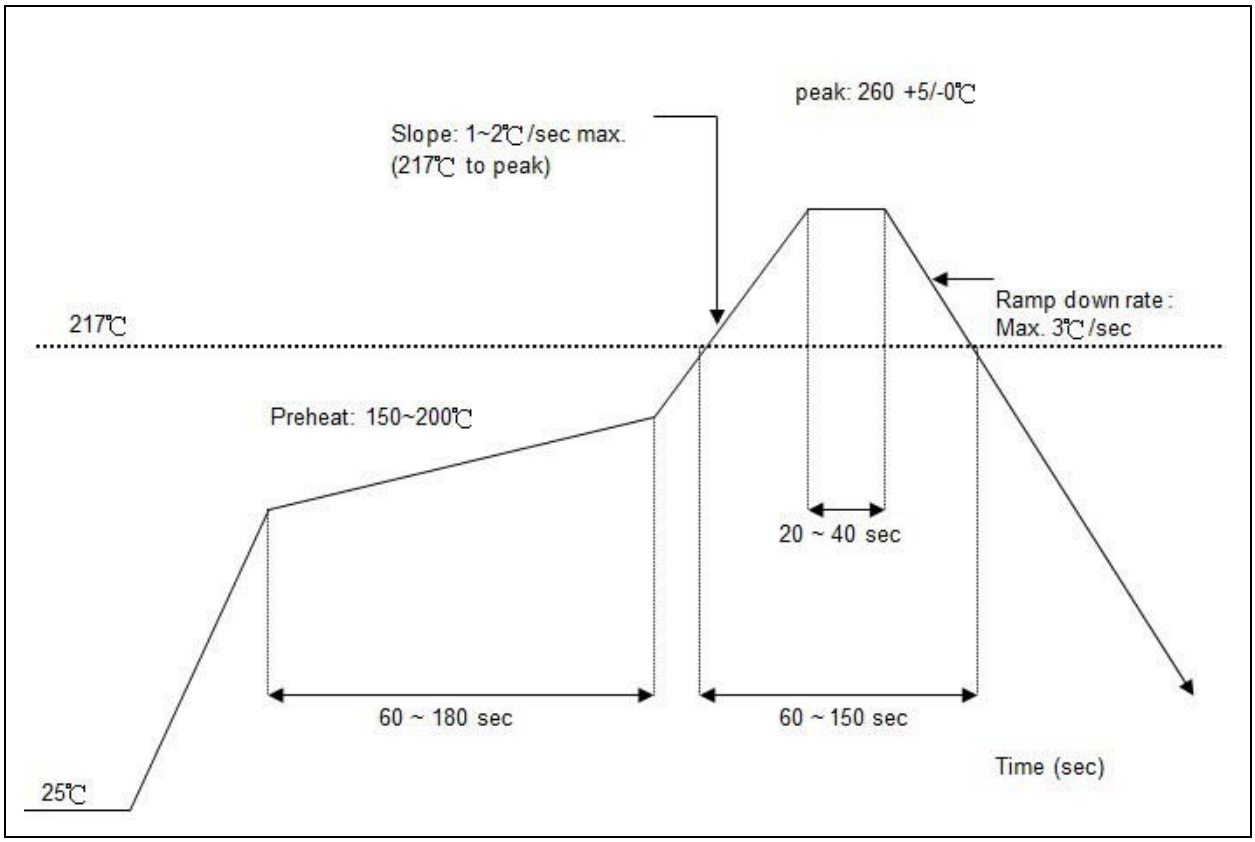
The BM63 module is assembled using a standard lead-free reflow profile, IPC/JEDEC J-STD-020. The BM63 module can be soldered to the main PCB using a standard leaded and lead-free solder reflow profiles.

To avoid any damage to the module, follow these recommendations:

- Refer to the *"AN233 Solder Reflow Recommendation"* (DS00233) document for the soldering reflow recommendations
- The peak temperature should not exceed (T_P) of +250 ºC
- Refer to the "Solder Paste" data sheet for specific reflow profile recommendations
- Use no-clean flux solder paste
- Do not wash the module as moisture can be trapped under the shield
- Use only one flow. If the PCB requires multiple flows, apply the module on the final flow.

Figure 9-1 illustrates the reflow profile of the BM63 module.

FIGURE 9-1: REFLOW PROFILE



NOTES:

10.0 ORDERING INFORMATION

Table 10-1 provides the ordering information of the BM63 module.

TABLE 10-1: ORDERING INFORMATION

Module	Microchip IC	Description	Part No
BM63	IS2063GM	Bluetooth 4.2 Stereo Audio with BLE, I^2S, Flash, Class 2, no shield, built-in antenna	BM63SPKA1MC2

Note: The BM63 module can be purchased through a Microchip representative. Go to Microchip website www.microchip.com/ for the current pricing and a list of distributors for the product.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (June 2016)

This is the initial released version of this document.

NOTES:

THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user's guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://microchip.com/support

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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ISBN: 978-1-5224-0705-8

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