

**KS8721BL / KS8721CL / KS8001L  
Design Guide for Interchangeability**

## Introduction

This application note highlights the differences between the KS8721BL, KS8721CL and the KS8001L single-port 10BASE-T/100BASE-TX/100BASE-FX PHYs. It serves also as an aid to transition those designs using either the KS8721BL or KS8721CL to a new design using the KS8001L. Descriptions of pin and register differences between the three devices are provided. Pin tables show the hardware migration from an existing KS8721BL or KS8721CL design to a new KS8001L design.

The KS8721BL is Micrel's fourth generation of Fast Ethernet single-port PHY. The KS8721CL is derived directly from the KS8721BL and changes the LED output pins to support separate LINK and ACTIVITY LEDs. The KS8001L is Micrel's fifth generation of Fast Ethernet single-port PHY and adds advanced features such as LinkMD cable diagnostics, reduced pin count serial interfaces to MAC/switch and programmable LED modes. The KS8001L is not drop-in compatible with the KS8721BL/KS8721CL. Contact your local Micrel FAE for details.

## MII / RMII / SMII Pins

The MII and RMII pin outs are the same for all three devices. SMII is supported only by the KS8001L. Table 1 below shows how the additional SMII mode select, data and control pins are mapped to some of the MII and RMII pins. Refer to the respective datasheets for more information.

**Table 1: SMII Pin Mapping to MII/RMII Pins**

KS8721BL / KS8721CL		KS8001L		
Pin No.	Signal	Pin No.	Signal	Pin Description
6	RXD0 / RXD[0]	6	RXD0 / RXD[0] / RX	<b>MII Mode:</b> Receive Data Output[0] / <b>RMII Mode:</b> Receive Data Output[0] / <b>SMII Mode:</b> Receive Data and Control
10	RXC	10	RXC /  SMII_SELECT	<b>MII Mode:</b> Receive Clock Output <b>Operating at:</b> 25 MHz = 100 Mbps 2.5 MHz = 10 Mbps <b>SMII Mode:</b> Select pin. An external pull-up on this pin enables SMII mode during reset
15	TXC / REFCLK	15	TXC / REFCLK / CLOCK	<b>MII Mode:</b> Transmit Clock Output / <b>RMII Mode:</b> 50 MHz Reference Clock Input / <b>SMII Mode:</b> 125 MHz Synchronization Clock Input
17	TXD0 / TXD[0]	17	TXD0 / TXD[0] / TX	<b>MII Mode:</b> Transmit Data Input[0] / <b>RMII Mode:</b> Transmit Data Input[0] / <b>SMII Mode:</b> Transmit Data and Control
18	TXD1 / TXD[1]	18	TXD1 / TXD[1] / SYNC	<b>MII Mode:</b> Transmit Data Input[1] / <b>RMII Mode:</b> Transmit Data Input[1] / <b>SMII Mode:</b> SYNC



## LED Output Pins

The KS8001L features software programmable LED outputs, enabling flexible link status reporting. LED mode 0 (default) of the KS8001L corresponds to the LED behavior on the KS8721BL. LED mode 1 of the KS8001L splits LINK and ACTIVITY into separate pins (26 and 29), corresponding to the LED behavior on the KS8721CL. Table 2 below lists the LED pin definitions for the KS8721BL, KS8721CL and KS8001L.

**Table 2: LED Pin Definitions**

Pin No.	Signal	KS8721BL	KS8721CL	KS8001L																																																												
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## Power and Ground

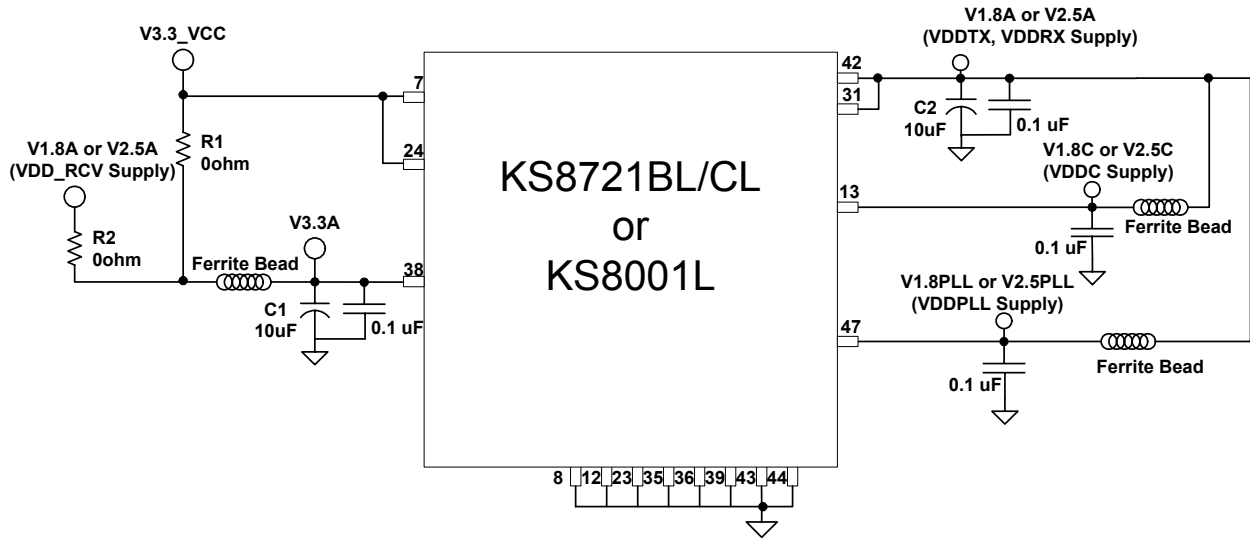
The KS8721BL, KS8721CL and KS8001L require only a single 3.3V supply. The device's internal regulator circuit produces the necessary core voltages. Core voltage levels are 2.5V and 1.8V for KS8721BL/KS8721CL and KS8001L, respectively. The difference in supply voltage to VDDRCV (pin 38) between the KS8721BL/KS8721CL and KS8001L prevent drop-in replacement with the KS8001L in an existing KS8721BL/KS8721CL design. However, with the resistor options to select the supply source for VDDRCV, as shown in Figure 1 on the following page, all three devices can be layout on a single PCB design. Table 3 below lists the power and ground pins for the KS8721BL/KS8721CL and KS8001L.

**Table 3: Pin Definition for Power & Ground**

Pin No.	KS8721BL / KS8721CL	Pin No.	KS8001L
7, 24	V3.3_VCC	7, 24	V3.3_VCC
		38	V3.3A
31, 38, 42	V2.5A	31	V1.8A
13	V2.5C	13	V1.8C
47	V2.5PLL	47	V1.8PLL
8, 12, 23, 35, 36, 39, 43, 44	Ground	8, 12, 23, 35, 36, 39, 44	Ground
		42, 43	NC*

\* Pins 42 and 43 can be safely connected to power (2.5V) and ground, respectively. In the KS8001L, these pins are not bonded to the die, and reserved for future use.

Figure 1: Single PCB Layout for KS8721BL/KS8721CL and KS8001L

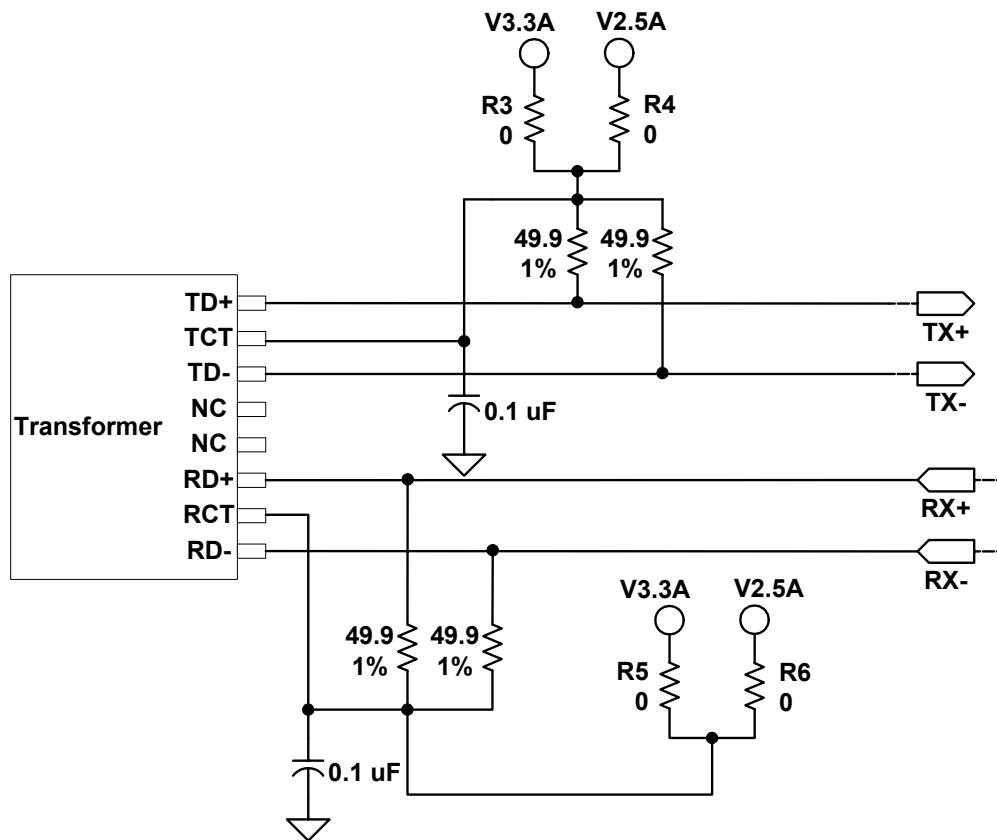


Device Type	Install	Do Not Install	Change
KS8721BL / KS8721CL	R2	R1	-
KS8001L	R1	R2, C2	C1 to 1uF

## Transformer Center-Tap Pins and Differential Pair Terminations

The KS8721BL/KS8721CL and KS8001L require the transformer center-tap pins and the transmit/receive differential pair terminations to be pulled up to the transceiver supply level. The difference in transceiver supply level between the KS8721BL/KS8721CL and KS8001L requires resistor options to select the appropriate supply for the pull-ups if a single PCB layout design is used to support all three devices. Figure 2 on the following page shows the resistor options to select between V2.5A and V3.3A for the pull-ups for the KS8721BL/KS8721CL and KS8001L, respectively.

Figure 2: Single PCB Layout for Transformer Center-Tap Pins & Differential Pair Terminations



Device Type	Install	Do Not Install
KS8721BL / KS8721CL	R4, R6	R3, R5
KS8001L	R3, R5	R4, R6

## Register Map

The KS8001L register set is a superset of the KS8721BL/KS8721CL register set with new registers added in unused portions of the KS8721BL/KS8721CL register map. The additional registers are used to support new features, such as LinkMD cable diagnostics and programmable LED modes. Also, the PHY model and revision numbers have been updated in PHY register 03h. Querying register 03h allows software to determine which one of the three PHY devices is installed. Refer to KS8721BL, KS8721CL and KS8001L datasheets for additional information. The KS8001L's additional registers are listed in Table 4 below.



Table 4: KS8001L Register Additions

Register 1dh – LinkMD Control/Status Register				
Address	Name	Description	Mode	Default
1d.15	Cable diagnostic test enable	0 = it indicates the cable diagnostic test is completed and the status information is valid for read. 1 = the cable diagnostic test is activated. This bit is self-cleared.	RW SC	0
1d.14:13	Cable diagnostic test result	[00] = normal condition [01] = open condition has been detected in cable [10] = short condition has been detected in cable [11] = cable diagnostic test is failed	RO	0
1d.12:9	Reserved			
1d.8:0	Cable fault counter	Distance to fault, approximately 0.75m*cabfaultcnt value	RO	0
Register 1eh – PHY Control				
Address	Name	Description	Mode	Default
1e:15:14	LED mode	[00] = LED3 <- collision LED2 <- full duplex LED1 <- speed LED0 <- link/activity  [01] = LED3 <- activity LED2 <- full duplex/collision LED1 <- speed LED0 <- link  [10] = LED3 <- activity LED2 <- full duplex LED1 <- 100Mbps link LED0 <- 10Mbps link  [11] = reserved	RW	0
1e.13	Polarity	0 = Polarity is not reversed 1 = Polarity is reversed	RO	
1e.12	Far end fault detect	0 = Far end fault detected 1 = Far end fault not detected	RO	
1e.11	MDIX/MDI state	0 = MDIX 1 = MDI	RO	
1e:10:8	Reserved			
1e:7	Remote loopback	0: normal mode 1: remote (analog) loop back is enable	RW	0
1e:6:0	Reserved			



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