



# High Performance Resonant Mode Controller

## TC33067

### ABSOLUTE MAXIMUM RATINGS\*

Power Supply Voltage .....  $V_{CC} = 20V$   
 Drive Output Current, Source or Sink (Note 1):  
     Continuous .....  $I_O = 0.3A$   
     Pulsed (0.5 $\mu$ sec, 25% Duty Cycle) ..... 1.5A  
 Error Amplifier, Fault, One-Shot, Oscillator and  
 Soft-Start Inputs .....  $V_{IN} = -1.0$  to  $+6.0V$   
 UVLO Adjust Input .....  $V_{IN}(UVLO) = -1.0$  to  $V_{CC}V$   
 Power Dissipation and Thermal Characteristics  
 16-Pin SOIC (W) Package:  
      $T_A = 25^\circ C$  .....  $P_D = 862mW$   
     Thermal Resistance, Junction-to-Air ....  $R_{\theta JA} = 145^\circ C/W$

16-Pin PDIP (N) Package:  
      $T_A = 25^\circ C$  .....  $P_D = 1.25W$   
     Thermal Resistance, Junction-to-Air .....  $R_{\theta JA} = 100^\circ C/W$   
 Operating Junction Temperature .....  $T_J = +150^\circ C$   
 Operating Ambient Temperature ( $T_A$  °C) .....  $-40$  to  $+85^\circ C$   
 Storage Temperature .....  $T_{STG} = -55$  to  $+150^\circ C$

\*This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.

**ELECTRICAL CHARACTERISTICS:** ( $V_{CC} = 12V$  [Note 2],  $R_{OSC} = 18.2k$ ,  $R_{VFO} = 2940$ ,  $C_{OSC} = 300pF$ ,  $R_T = 2370k$ ,  $C_T = 300pF$ ,  $C_L = 1.0nF$ . For typical values  $T_A = 25^\circ C$ , for min/max values  $T_A$  is the operating ambient temperature range that applies [Note 3], unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{REF}$	Reference Output Voltage	$I_O = 0mA$ , $T_J = 25^\circ C$	5.0	5.1	5.2	V
Reg <sub>LINE</sub>	Line Regulation	$V_{CC} = 10$ to $8V$	—	1.0	20	mV
Reg <sub>LOAD</sub>	Load Regulation	$I_O = 0mA$ to $10mA$	—	1.0	20	mV
$V_{REF}$	Total Output Variation Over Line, Load, and Temperature		4.9	—	5.3	V
$I_O$	Output Short Circuit Current		25	100	190	mA
$V_{TH}$	Reference Undervoltage Lockout Threshold		3.8	4.3	4.8	V
<b>Error Amplifier</b>						
$V_{IO}$	Input Offset Voltage	$V_{CM} = 1.5V$	—	1.0	10	mV
$I_{IB}$	Input Bias Current	$V_{CM} = 1.5V$	—	0.2	1.0	$\mu A$
$I_{IO}$	Input Offset Current	$V_{CM} = 1.5V$	—	0	0.5	$\mu A$
$A_{VOL}$	Open Loop Voltage Gain	$V_{CM} = 1.5V$ , $V_O = 2.0V$	70	100	—	dB
GBW	Gain Bandwidth Product	$f = 100kHz$	3.0	5.0	—	MHz
CMR	Input Common Mode Rejection Ratio	$V_{CM} = 1.5$ to $5.0V$	70	95	—	dB
PSR	Power Supply Rejection Ratio	$V_{CC} = 10$ to $18V$ , $f = 120Hz$	80	100	—	dB
	Output Voltage Swing					V
$V_{OH}$		High State	2.8	3.2	—	
$V_{OL}$		Low State	—	0.6	0.8	

- NOTES:**
1. Maximum package power dissipation limits must be observed.
  2. Adjust  $V_{CC}$  above the Startup threshold before setting to 12V.
  3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 $T_{LOW} = -40^\circ C$ ,  $T_{HIGH} = +85^\circ C$

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Oscillator</b>						
$f_{OSC(Low)}$	Frequency (Error Amp Output Low)		500	525	540	kHz
	$T_A = 25^\circ\text{C}$					
	Total Variation	$V_{CC} = 10\text{ to }18\text{ V}$ , $T_A = T_{LOW}\text{ to }T_{HIGH}$	490	—	550	
$f_{OSC(HIGH)}$	Frequency (Error Amp Output High)		1900	2050	2150	kHz
	$T_A = 25^\circ\text{C}$					
	Total Variation	$V_{CC} = 10\text{ to }18\text{ V}$ , $T_A = T_{LOW}\text{ to }T_{HIGH}$	1850	—	2200	
$V_{IN}$	Oscillator Control Input Voltage, Pin 3 @ $25^\circ\text{C}$		—	2.5	—	V
<b>One Shot</b>						
$t_{BLANK}$	Drive Output Off-Time		235	250	270	nsec
	$T_A = 25^\circ\text{C}$					
	Total Variation	$V_{CC} = 10\text{ to }18\text{ V}$ , $T_A = T_{LOW}\text{ to }T_{HIGH}$	225	—	280	
<b>Drive Outputs</b>						
$V_{OL}$	Output Voltage		—	0.8	1.2	V
	Low State ( $I_{Sink} = 20\text{ mA}$ )					
		( $I_{Sink} = 20\text{ mA}$ )	—	1.5	2.0	
$V_{OH}$	High State ( $I_{Source} = 20\text{ mA}$ )		9.5	10.3	—	
	High State ( $I_{Source} = 200\text{ mA}$ )		9.0	9.7	—	
$V_{OL(UVLO)}$	Output Voltage with UVLO Activated ( $V_{CC} = 6.0\text{ V}$ , $I_{Sink} = 1.0\text{ mA}$ )		—	0.8	1.2	V
$t_r$	Output Voltage Rise Time	$C_L = 1.0\text{ nF}$	—	20	50	nsec
$t_f$	Output Voltage Fall Time	$C_L = 1.0\text{ nF}$	—	15	50	nsec
<b>Fault Comparator</b>						
$V_{TH}$	Input Threshold		0.93	1.0	1.07	V
$I_{IB}$	Input Bias Current	V Pin 10 = 0V	—	-2.0	-10	$\mu\text{A}$
$t_{PLH(IN/OUT)}$	Propagation Delay to Drive Outputs (10mV Overdrive)		—	60	100	nsec
<b>Soft-Start</b>						
$I_{CHG}$	Capacitor Charge Current	(V Pin 11 = 2.5 V)	4.5	9.0	14	$\mu\text{A}$
$I_{DISCHG}$	Capacitor Discharge Current	(V Pin 11 = 2.5 V)	3.0	8.0	—	mA
<b>Undervoltage Lockout</b>						
$V_{TH(UVLO)}$	Startup Threshold, $V_{CC}$ Increasing		14.8	16	17.2	V
	Enable/UVLO Adjust Pin Open		8.0	9.0	10	
	Enable/UVLO Adjust Pin Connected to $V_{CC}$					
$V_{CC(MIN)}$	Minimum Operating Voltage After Turn-On		8.0	9.0	10	V
	Enable/UVLO Adjust Pin Open		7.6	8.6	9.6	
	Enable/UVLO Adjust Pin Connected to $V_{CC}$					
$V_{TH(Enable)}$	Enable/UVLO Adjust Shutdown Threshold Voltage		6.0	7.0	—	V
$I_{IN(Enable)}$	Enable/UVLO Adjust Input Current (Pin 9 = 0V)		—	-0.2	-1.0	mA
<b>TOTAL DEVICE</b>						
$I_{CC}$	Power Supply Current (Enable/UVLO Adjust Pin Open)		—	0.5	0.8	mA
	Startup ( $V_{CC} = 13.5\text{ V}$ )	—		27	35	
	Operating ( $f_{OSC} = 500\text{ kHz}$ ) (Note 2)					

- NOTES:**
- Maximum package power dissipation limits must be observed.
  - Adjust  $V_{CC}$  above the Startup threshold before setting to 12V.
  - Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.  
 $T_{LOW} = -40^\circ\text{C}$ ,  $T_{HIGH} = +85^\circ\text{C}$

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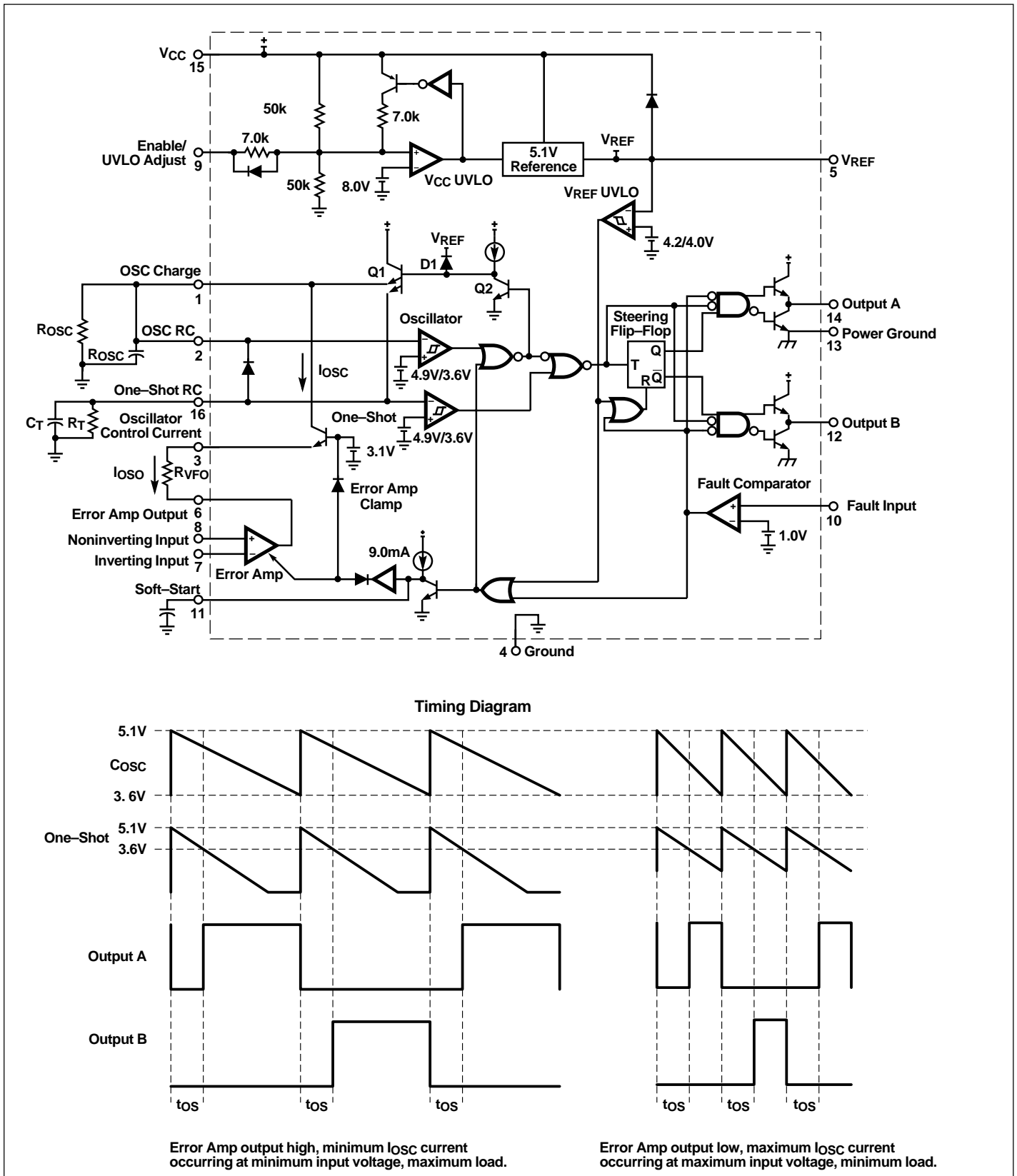


Figure 1. Representative Block Diagram

### INTRODUCTION

As power supply designers have strived to increase power conversion efficiency and reduce passive component size, high frequency resonant mode power converters have emerged as attractive alternatives to conventional pulse-width modulated control. When compared to pulse-width modulated converters, resonant mode control offers several benefits including lower switching losses, higher efficiency, lower EMI emission, and smaller size. A new integrated circuit has been developed to support this trend in power supply design. The TC33067 Resonant Mode Controller is a high performance bipolar IC dedicated to variable frequency power control at frequencies exceeding 1.0 MHz. This integrated circuit provides the features and performance specifically for zero voltage switching resonant mode power supply applications.

The primary purpose of the control chip is to provide a fixed off-time to the gates of external power MOSFETs at a repetition rate regulated by a feedback control loop. Additional features of the IC ensure that system startup and fault conditions are administered in a safe, controlled manner.

A simplified block diagram of the IC is shown on the front page, which identifies the main functional blocks and the block-to-block interconnects. Figure 1 is a detailed functional diagram which accurately represents the internal circuitry. The various functions can be divided into two sections. The first section includes the primary control path which produces precise output pulses at the desired frequency. Included in this section are a variable frequency Oscillator, a One-Shot, a pulse Steering Flip-Flop, a pair of power MOSFET Drivers, and a wide bandwidth Error Amplifier. The second section provides several peripheral support functions including a voltage reference, undervoltage lock-out, Soft-Start circuit, and a fault detector.

### Primary Control Path

The output pulse width and repetition rate are regulated through the interaction of the variable frequency Oscillator, One-Shot timer and Error Amplifier. The Oscillator triggers the One-Shot which generates a pulse that is alternately steered to a pair of totem pole output drivers by a toggle Flip-Flop. The Error Amplifier monitors the output of the regulator and modulates the frequency of the Oscillator. High speed Schottky logic is used throughout the primary control channel to minimize delays and enhance high frequency characteristics.

### Oscillator

The characteristics of the variable frequency Oscillator are crucial for precise controller performance at high operating frequencies. In addition to triggering the One-Shot

timer and initiating the output deadtime, the oscillator also determines the initial voltage for the one-shot capacitor. The Oscillator is designed to operate at frequencies exceeding 1.0MHz. The Error Amplifier can control the oscillator frequency over a 1000:1 frequency range, and both the minimum and maximum frequencies are easily and accurately programmed by the proper selection of external components.

The functional diagram of the Oscillator and One-Shot timer is shown in Figure 2. The oscillator capacitor ( $C_{OSC}$ ) is initially charged by transistor Q1. When  $C_{OSC}$  exceeds the 4.9V upper threshold of the oscillator comparator, the base of Q1 is pulled low allowing  $C_{OSC}$  to discharge through the external resistor, ( $R_{OSC}$ ), and the oscillator control current, ( $I_{OSC}$ ). When the voltage on  $C_{OSC}$  falls below the comparator's 3.6V lower threshold, Q1 turns on and again charges  $C_{OSC}$ .

$C_{OSC}$  charges from 3.6V to 5.1V in less than 50nsec. The high slew rate of  $C_{OSC}$  and the propagation delay of the comparator make it difficult to control the peak voltage. This accuracy issue is overcome by clamping the base of Q1 through a diode to a voltage reference. The peak voltage of the oscillator waveform is thereby precisely set at 5.1V.

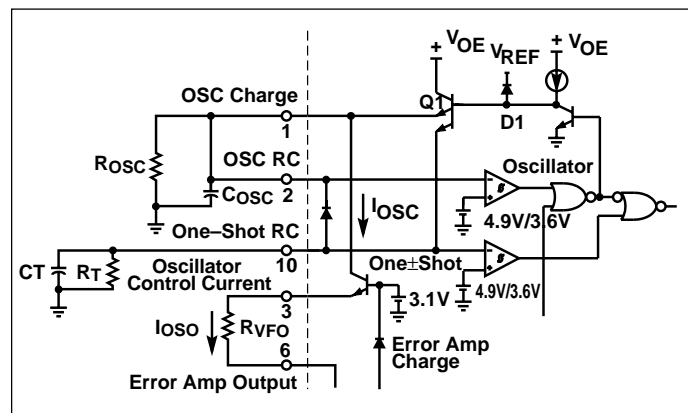


Figure 2. Oscillator and One-Shot Timer

The frequency of the Oscillator is modulated by varying the current flowing out of the Oscillator Control Current ( $I_{OSC}$ ) pin. The  $I_{OSC}$  pin is the output of a voltage regulator. The input of the voltage regulator is tied to the variable frequency oscillator. The discharge current of the Oscillator increases by increasing the current out of the  $I_{OSC}$  pin. Resistor  $R_{VFO}$  is used in conjunction with the Error Amp output to change the  $I_{OSC}$  current. Maximum frequency occurs when the Error Amplifier output is at its low state with a saturation voltage of 0.1V at 1.0mA.

The minimum oscillator frequency will result when the  $I_{OSC}$  current is zero, and  $C_{OSC}$  is discharged through the external resistor ( $R_{OSC}$ ). This occurs when the Error Amplifier output is at its high state of 2.5V. The minimum and maximum oscillator frequencies are programmed by the

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proper selection of resistor  $R_{OSC}$  and  $R_{VFO}$ . The minimum frequency is programmed by  $R_{OSC}$  using Equation 1:

$$R_{OSC} = \frac{\frac{1}{f(\min)} - t_{PD}}{C_{OSC} \ell_n \left( \frac{5.1}{3.6} \right)} = \frac{t(\max) - 70\text{nsec}}{0.348 C_{OSC}}$$

Equation 1.

where  $t_{PD}$  is the internal propagation delay.

The maximum oscillator frequency is set by the current through resistor  $R_{VFO}$ . The current required to discharge  $C_{OSC}$  at the maximum oscillator frequency can be calculated by Equation 2:

$$I_{(\max)} C_{OSC} \frac{5.1 - 3.6}{1} = 1.5 \text{ OSCf}(\max)$$

Equation 2.

The discharge current through  $R_{OSC}$  must also be known and can be calculated by Equation 3:

$$\begin{aligned} I_{R_{OSC}} &= \frac{5.1 - 3.6}{R_{OSC}} e^{\left( -\frac{1}{f(\min) R_{OSC} C_{OSC}} \right)} \\ &= \frac{1.5}{R_{OSC}} e^{\left( -\frac{1}{f(\min) R_{OSC} C_{OSC}} \right)} \end{aligned}$$

Equation 3.

Resistor  $R_{VFO}$  can now be calculated by Equation 4:

$$R_{VFO} = \frac{2.5 - V_{EAsat}}{I_{(\max)} - I_{R_{OSC}}}$$

Equation 4.

## One-Shot Timer

The One-Shot is designed to disable both outputs simultaneously providing a deadtime before either output is enabled. The One-Shot capacitor ( $C_T$ ) is charged concurrently with the oscillator capacitor by transistor Q1, as shown in Figure 2. The one-shot period begins when the oscillator comparator turns off Q1, allowing  $C_T$  to discharge.

The period ends when resistor  $R_T$  discharges  $C_T$  to the threshold of the One-Shot comparator. The lower threshold of the One-Shot is 3.6 V. By choosing  $C_T$ ,  $R_T$  can be solved by Equation 5:

$$R_T = \frac{t_{OS}}{C_T \ell_n \left( \frac{5.1}{3.6} \right)} = \frac{t_{OS}}{0.348 C_T}$$

Equation 5.

Errors in the threshold voltage and propagation delay through the output drivers will affect the One-Shot period. To guarantee accuracy, the output pulse of the control chip is trimmed to within 5% of 250nsec with nominal values of  $R_T$  and  $C_T$ .

The outputs of the Oscillator and One-Shot comparators are OR'd together to produce the pulse  $t_{OS}$ , which drives the Flip-Flop and output drivers. The output pulse ( $t_{OS}$ ) is initiated by the Oscillator and terminated by the One-Shot comparator. With zero-voltage resonant mode converters, the oscillator discharge time should never be set less than the one-shot period.

## Error Amplifier

A fully accessible high performance Error Amplifier is provided for feedback control of the power supply system.

The Error Amplifier is internally compensated and features dc open loop gain greater than 70dB, input offset voltage of less than 10 mV and a guaranteed minimum gain-bandwidth product of 2.5 MHz. The input common mode range extends from 1.5V to 5.1V, which includes the reference voltage.

When the Error Amplifier output is coupled to the  $I_{OSC}$  pin by  $R_{VFO}$ , as illustrated in Figure 3, it provides the Oscillator Control Current,  $I_{OSC}$ . The output swing of the Error Amplifier is restricted by a clamp circuit to improve its transient recovery time.

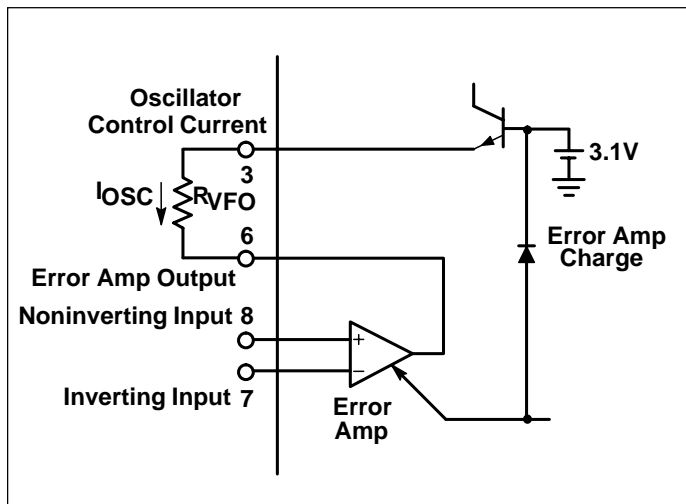


Figure 3. Error Amplifier and Clamp

### Output Section

The pulse ( $t_{OS}$ ), generated by the Oscillator and One-Shot timer is gated to dual totem-pole output drives by the Steering Flip-Flop shown in Figure 4. Positive transitions of  $t_{OS}$  toggle the Flip-Flop, which causes the pulses to alternate between Output A and Output B. The flip-flop is reset by the undervoltage lockout circuit during startup to guarantee that the first pulse appears at Output A.

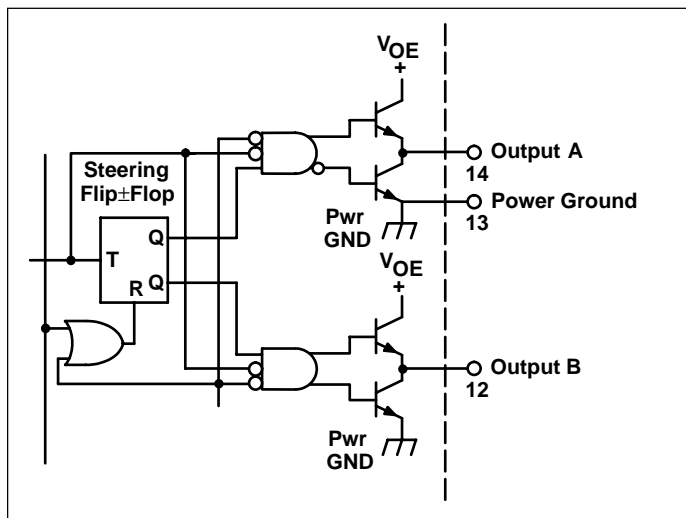


Figure 4. Steering Flip-Flop and Output Drivers

The totem-pole output drivers are ideally suited for driving power MOSFETs and are capable of sourcing and sinking 1.5A. Rise and fall times are typically 20nsec when driving a 1.0nF load. High source/sink capability in a totem-pole driver normally increases the risk of high cross conduction current during output transitions. The TC33067 utilizes a unique design that virtually eliminates cross conduction,

thus controlling the chip power dissipation at high frequencies. A separate power ground pin is provided to isolate the sensitive analog circuitry from large transient currents.

### PERIPHERAL SUPPORT FUNCTIONS

The TC33067 Resonant Controller provides a number of support and protection functions including a precision voltage reference, undervoltage lockout comparators, soft-start circuitry, and a fault detector. These peripheral circuits ensure that the power supply can be turned on and off in a controlled manner and that the system will be quickly disabled when a fault condition occurs.

### Undervoltage Lockout and Voltage Reference

Separate undervoltage lockout comparators sense the input  $V_{CC}$  voltage and the regulated reference voltage as illustrated in Figure 5. When  $V_{CC}$  increases to the upper threshold voltage, the  $V_{CC}$  UVLO comparator enables the Reference Regulator. After the  $V_{REF}$  output of the Reference Regulator rises to 4.2V, the  $V_{REF}$  UVLO comparator switches the UVLO signal to a logic zero state enabling the primary control path. Reducing  $V_{CC}$  to the lower threshold voltage causes the  $V_{CC}$  UVLO comparator to disable the Reference Regulator. The  $V_{REF}$  UVLO comparator then switches the UVLO output to a logic one state disabling the controller.

The Enable/UVLO Adjust pin allows the power supply designer to select the  $V_{CC}$  UVLO threshold voltages. When this pin is open, the comparator switches the controller on at 16V and off at 9.0V. If this pin is connected to the  $V_{CC}$  terminal, the upper and lower thresholds are reduced to 9.0V and 8.6V, respectively. Forcing the Enable/UVLO adjust pin low will pull the  $V_{CC}$  UVLO comparator input low (through an internal diode) turning off the controller.

The Reference Regulator provides a precise 5.1V reference to internal circuitry and can deliver up to 10mA to external loads. The reference is trimmed to better than 2% initial accuracy and includes active short circuit protection.

### Fault Detector

The high speed Fault Comparator illustrated in Figure 6 can protect a power supply from destruction under fault conditions. The Fault Input pin connects to the input of the Fault Comparator. The Fault Comparator output connects to the output drivers. This direct path reduces the propagation delay from the Fault Input to the A and B outputs to typically 70nsec. The Fault Comparator output is also OR'd with the UVLO output from the  $V_{REF}$  UVLO comparator to produce the logic output labeled "UVLO+Fault". This signal disables the Oscillator and One-Shot by forcing both the  $C_{OSC}$  and  $C_T$  capacitors to be continually charged.

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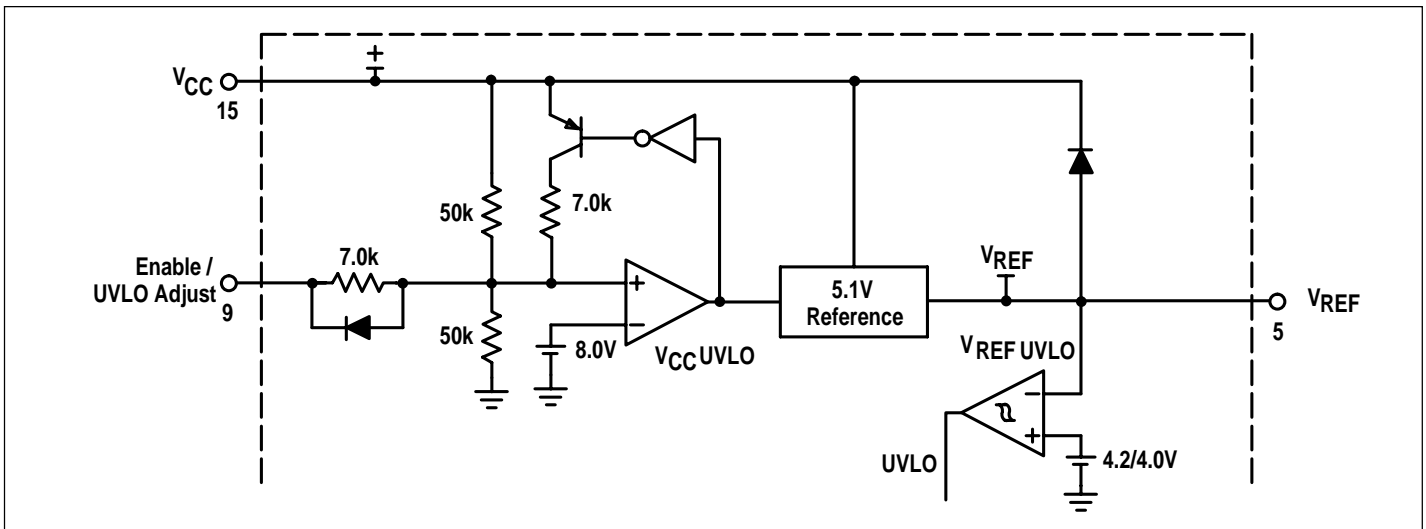


Figure 5. Undervoltage Lockout and Reference

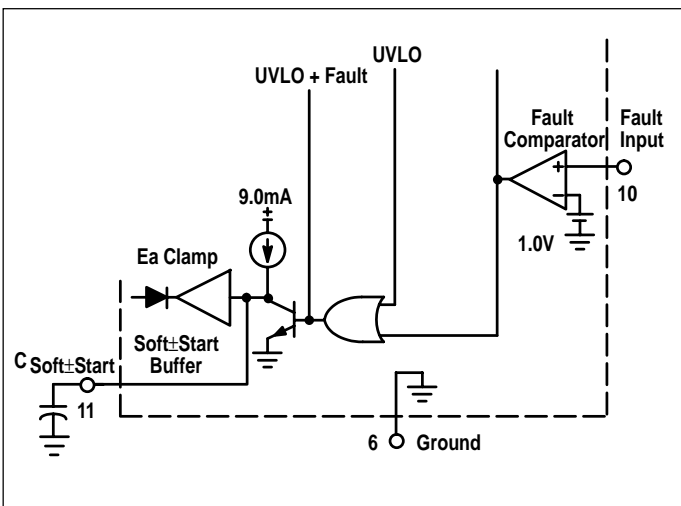


Figure 6. Fault Detector and Soft-Start

### Soft-Start Circuit

The Soft-Start circuit shown in Figure 6 forces the variable frequency Oscillator to start at the maximum frequency and ramp downward until regulated by the feedback control loop. The external capacitor at the  $C_{Soft-Start}$  terminal is initially discharged by the UVLO+Fault signal. The low voltage on the capacitor passes through the Soft-Start Buffer to hold the Error Amplifier output low. After UVLO+Fault switches to a logic zero, the soft-start capacitor is charged by a 9.0 $\mu$ A current source. The buffer allows the Error Amplifier output to follow the soft-start capacitor until it is regulated by the Error Amplifier inputs. The soft-start function is generally applicable to controllers operating below resonance and can be disabled by simply opening the  $C_{Soft-Start}$  terminal.

The TC33067 is specifically designed for zero voltage switching (ZVS) quasi-resonant converter (QRC) applications. The IC is optimized for double-ended push-pull or bridge type converters operating in continuous conduction mode. Operation of this type of ZVS with resonant properties is similar to standard push-pull or bridge circuits in that the energy is transferred during the transistor on-time. The difference is that a series resonant tank is usually introduced to shape the voltage across the power transistor prior to turn-on. The resonant tank in this topology is not used to deliver energy to the output as is the case with zero current switch topologies. When the power transistor is enabled the voltage across it should already be zero, yielding minimal switching loss. Figure 7 shows a timing diagram for a half-bridge ZVS QRC. An application circuit is shown in Figure 8. The circuit built is a DC-to-DC half-bridge converter delivering 75W to the output from a 48V source.

When building a zero voltage switch (ZVS) circuit, the objective is to waveshape the power transistor's voltage waveform so that the voltage across the transistor is zero when the device is turned on. The purpose of the control IC is to allow a resonant tank to waveshape the voltage across the power transistor while still maintaining regulation. This is accomplished by maintaining a fixed deadtime and by varying the frequency; thus the effective duty cycle is changed.

Primary side resonance can be used with ZVS circuits. In the application circuit, the elements that make the resonant tank are the primary leakage inductance of the transformer ( $L_L$ ) and the average output capacitance ( $C_{OSS}$ ) of a power MOSFET ( $C_R$ ). The desired resonant frequency for the application circuit is calculated by Equation 6:



$$f_r = \frac{1}{2 \pi \sqrt{L_L 2C_R}}$$

In the application circuit, the operating voltage is low and the value of  $C_{OSS}$  versus Drain Voltage is known. Because the  $C_{OSS}$  of a MOSFET changes with drain voltage, the value of the  $C_R$  is approximated as the average  $C_{OSS}$  of the MOSFET. For the application circuit the average  $C_{OSS}$  can be calculated by Equation 7.

$$C_R = \sqrt{2} \times C_{OSS} \text{ measured at } \frac{1}{2} V_{IN}$$

The MOSFET chosen fixes  $C_R$  and that  $L_L$  is adjusted to achieve the desired resonant frequency.

However, the desired resonant frequency is less critical than the leakage inductance. Figure 7 shows the primary current ramping toward its peak value during the resonant transition. During this time, there is circulating current flowing through the secondary inductance, which effectively makes the primary inductance appear shorted. Therefore, the current through the primary will ramp to its peak value at a rate controlled by the leakage inductance and the applied voltage. Energy is not transferred to the secondary during this stage, because the primary current has not overcome the circulating current in the secondary. The larger the leakage inductance, the longer it takes for the primary current to slew. The practical effect of this is to lower the duty cycle, thus reducing the operating range.

The maximum duty cycle is controlled by the leakage inductance, not by the TC33067. The One-Shot in the TC33067 only assures that the power switch is turned on under a zero voltage condition. Adjust the one-shot period so that the output switch is activated while the primary current is slewing but before the current changes polarity. The resonant stage should then be designed to be as long as the time for the primary current to go to zero amps.

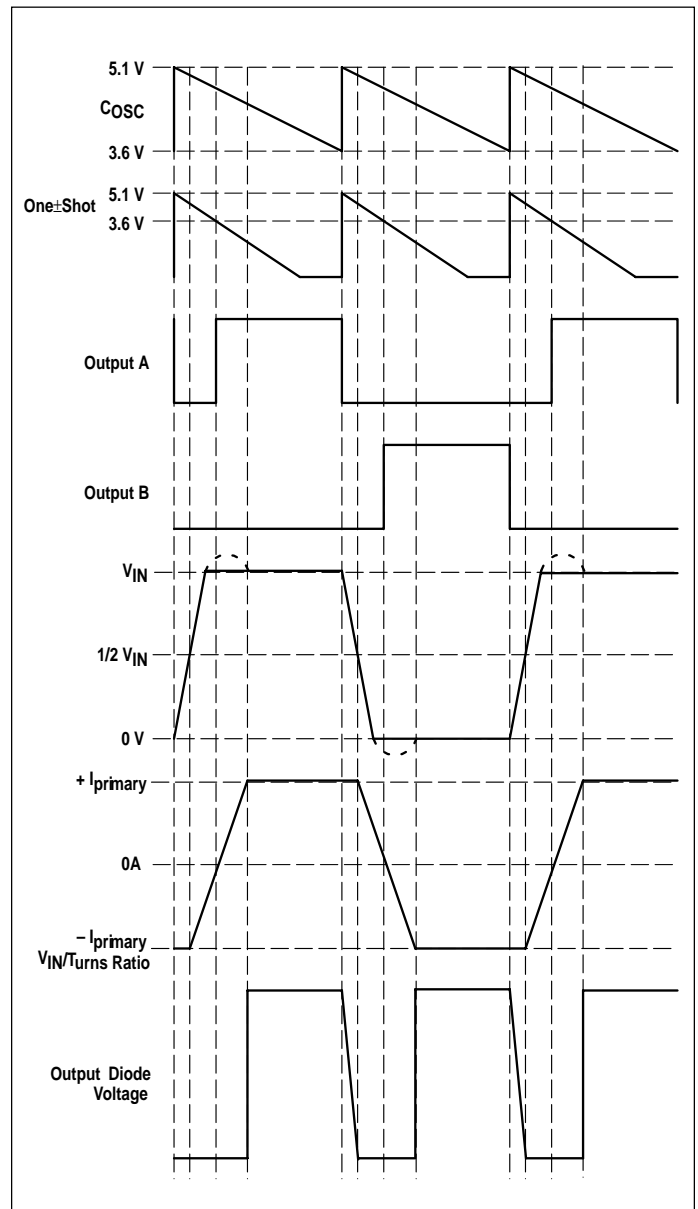


Figure 7. Fault Detector and Soft-Start

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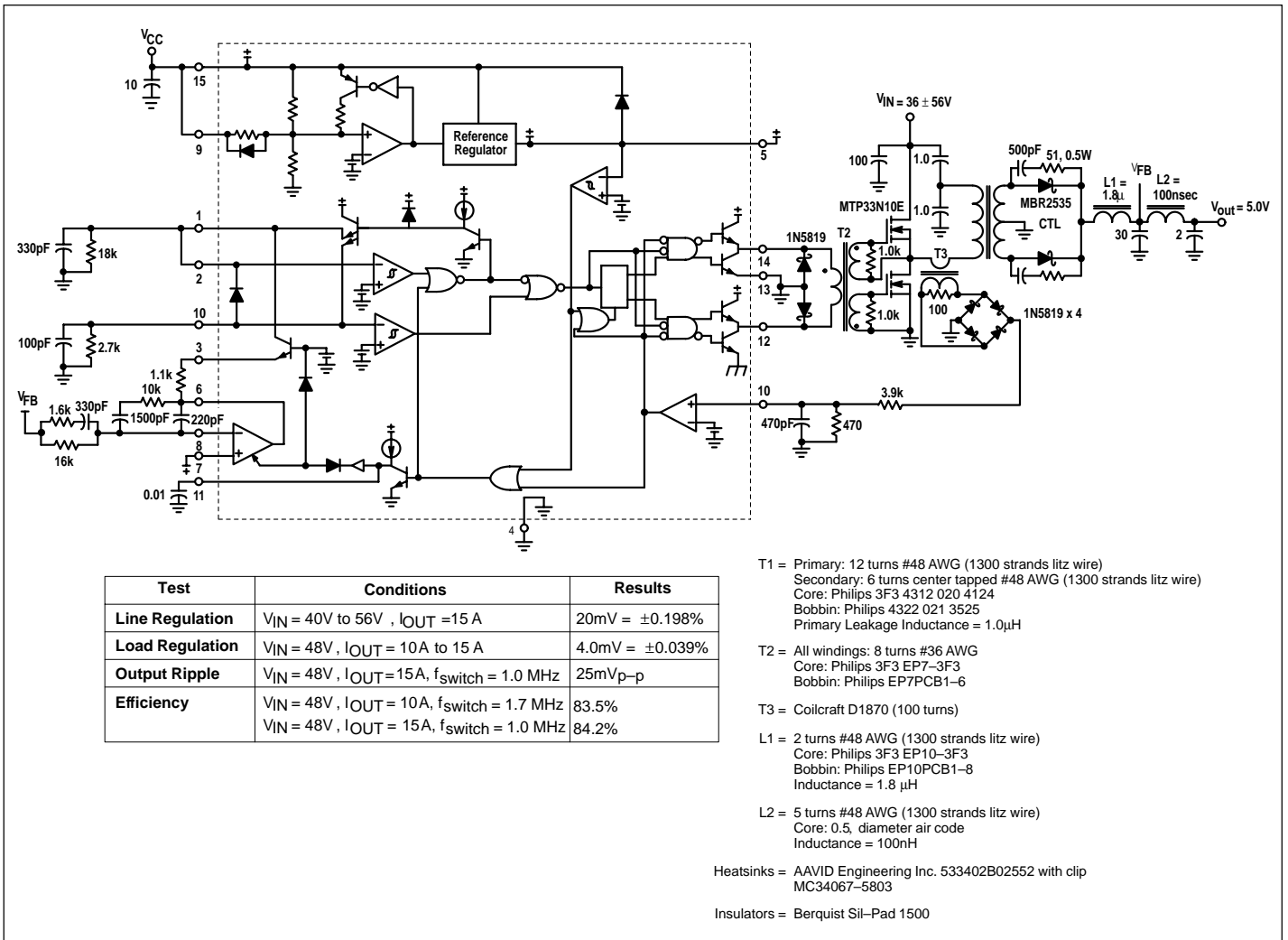
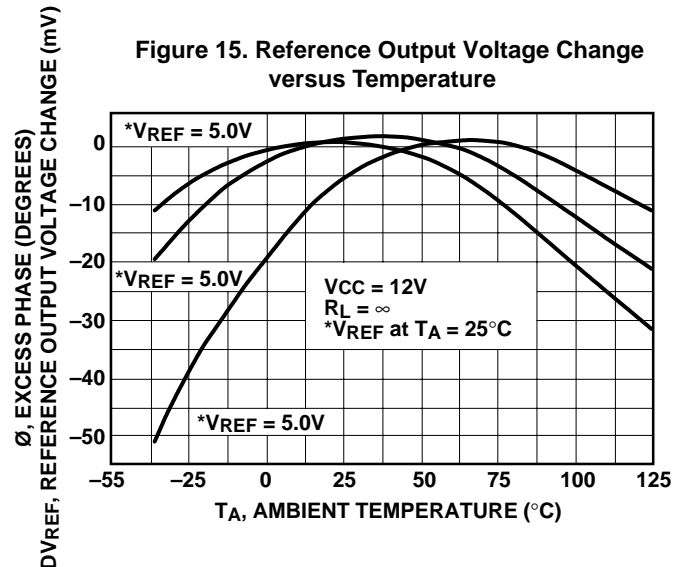
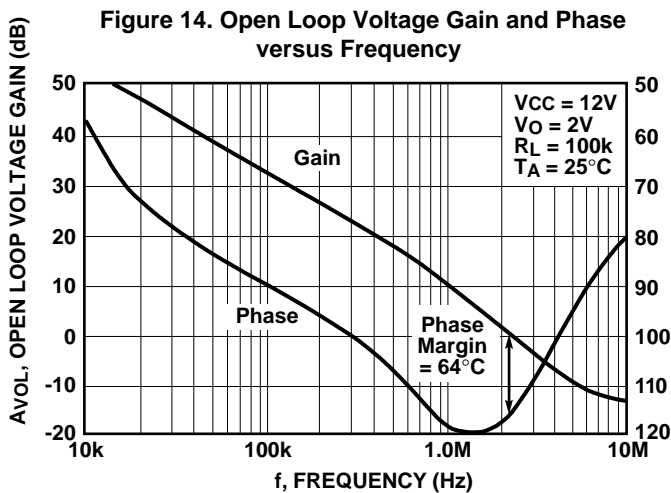
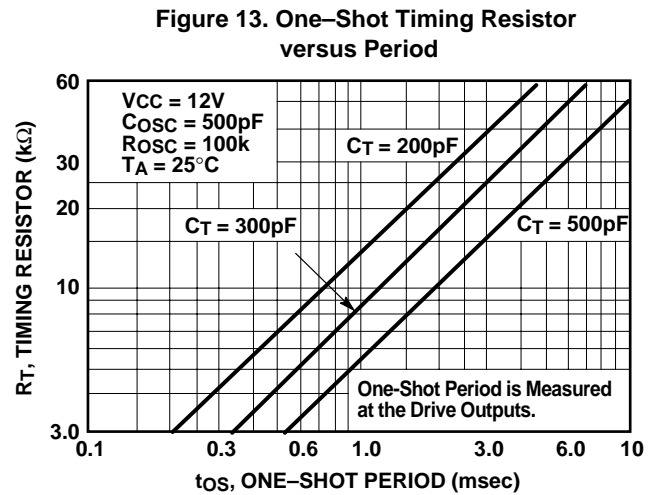
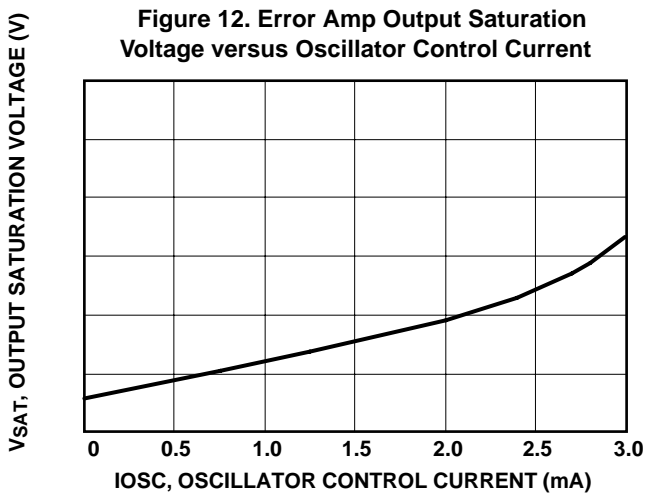
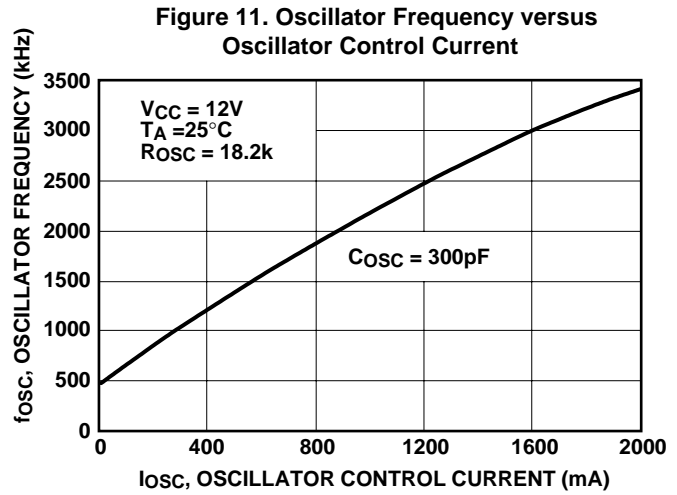
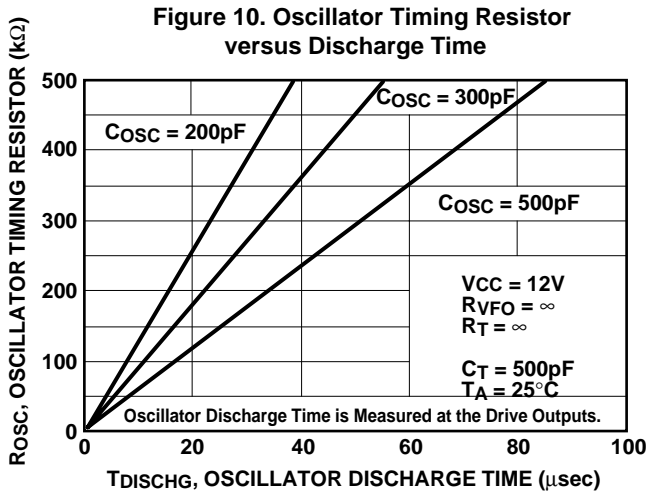


Figure 8. Application Circuit



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## TYPICAL CHARACTERISTICS



### TYPICAL CHARACTERISTICS

Figure 16. Reference Voltage Change versus Source Current

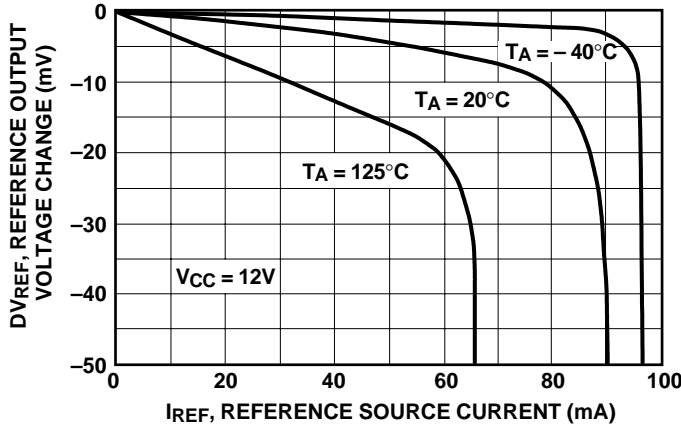


Figure 17. Drive Output Saturation Voltage versus Load Current

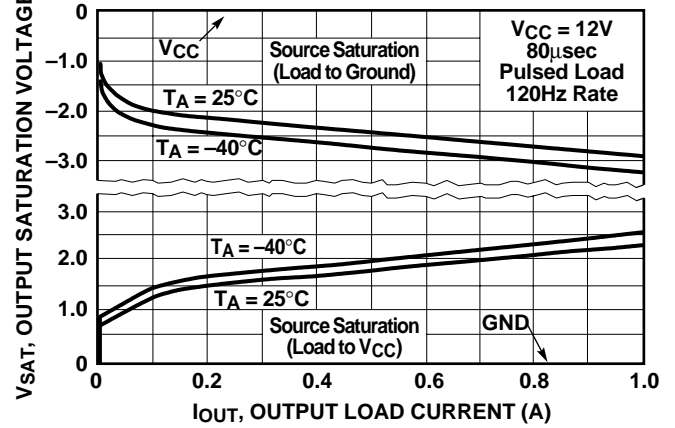


Figure 18. Drive Output Waveform

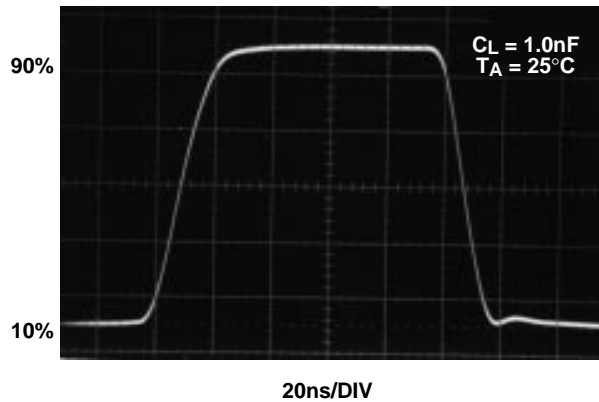


Figure 19. Soft-Start Saturation Voltage versus Capacitor Discharge Current

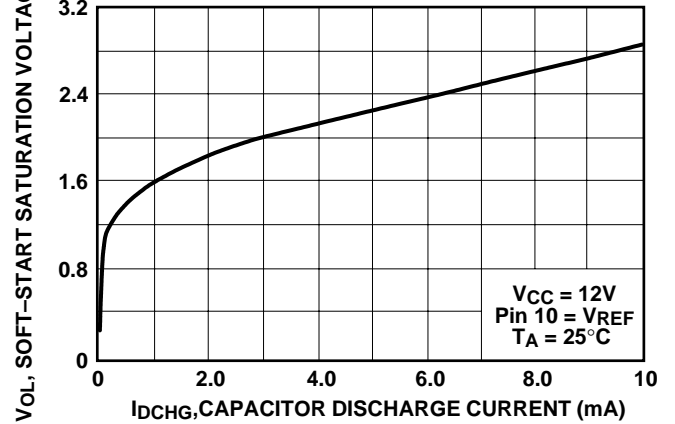


Figure 20. Operating Frequency versus Supply Current

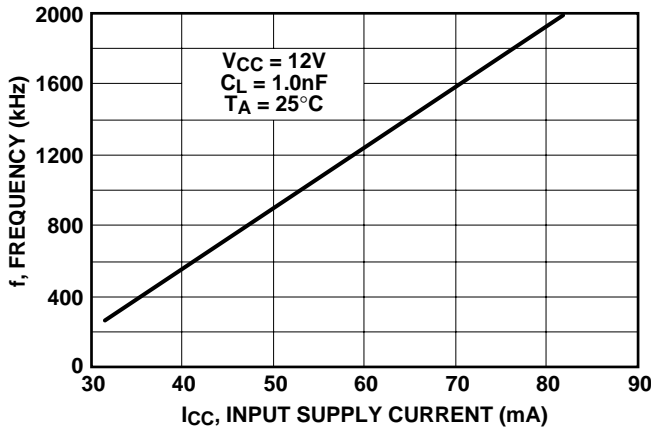
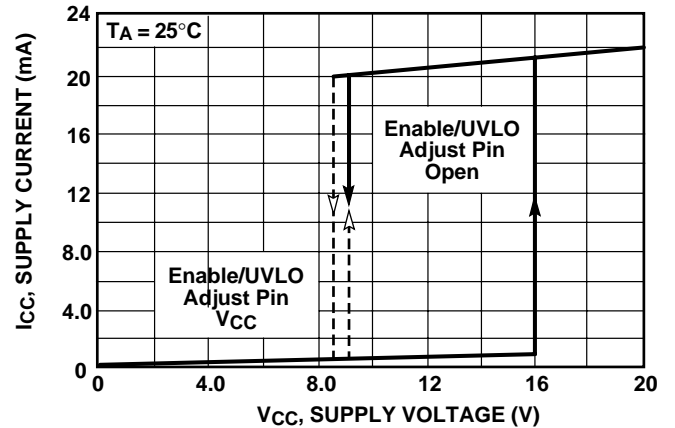


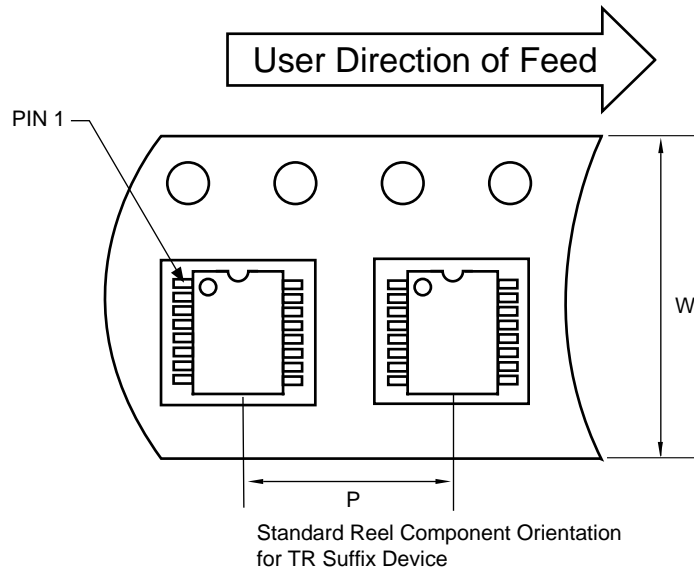
Figure 21. Supply Current versus Supply Voltage



## TC33067

### TAPE AND REEL SPECIFICATIONS

#### Component Taping Orientation for 16-Pin SOIC (Wide) Devices



#### Carrier Tape, Reel Size, and Number of Components Per Reel

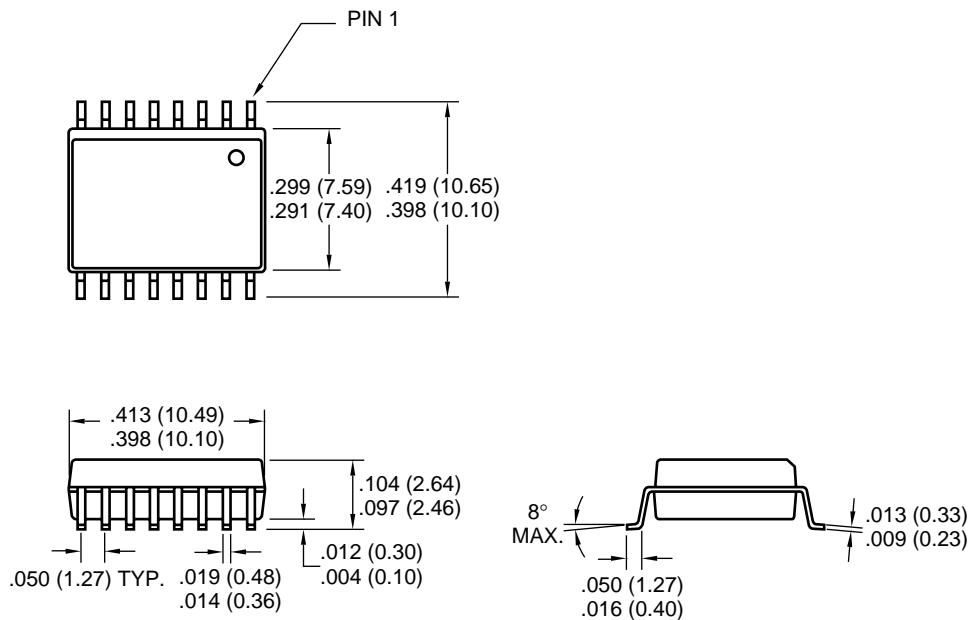
Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (W)	16 mm	12 mm	1000	13 in

# High Performance Resonant Mode Controller

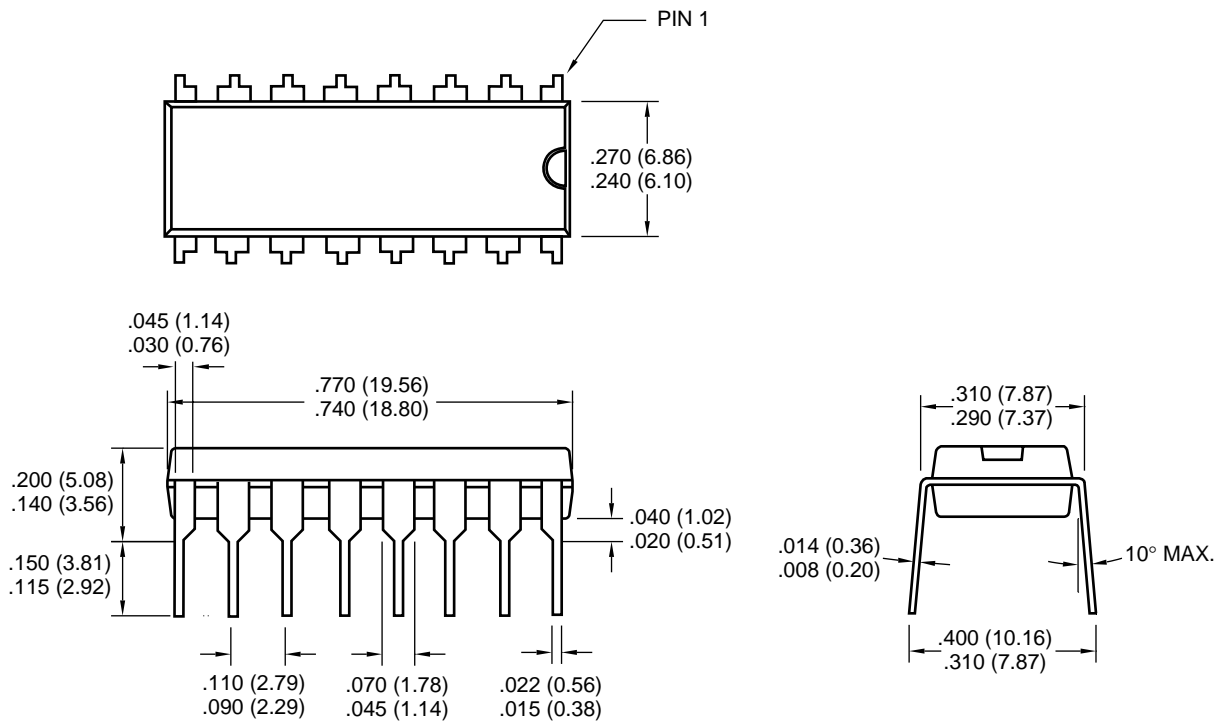
TC33067

## PACKAGE DIMENSIONS

### 16-Pin SOIC (Wide)



### 16-Pin PDIP (Narrow)



Dimensions: inches (mm)

**TC33067**

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