TelCom Semiconductor, Inc.

TC33166

Power Switching Regulator

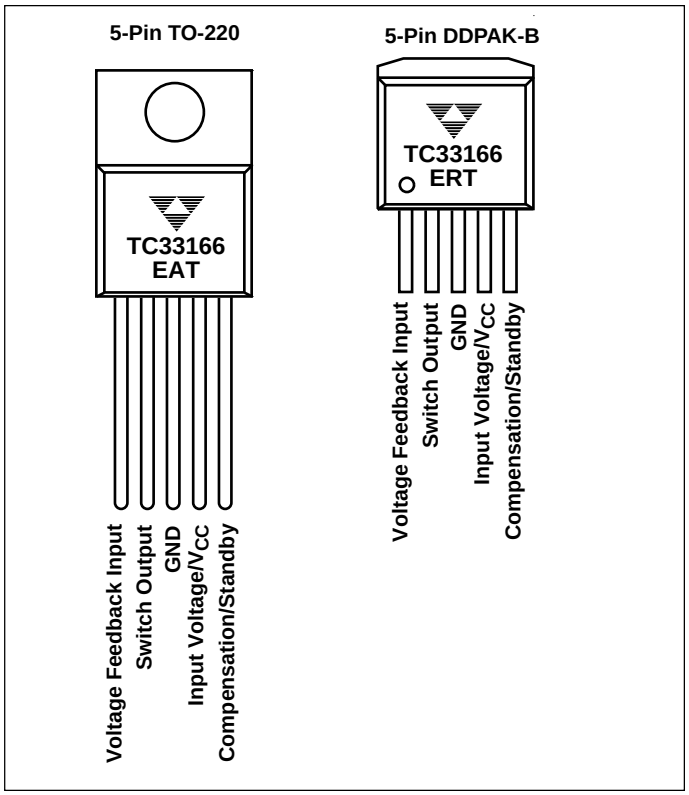
FEATURES

- **Output Switch Current in Excess of 3.0A**
- **Fixed Frequency Oscillator (72kHz) with On-Chip Timing**
- **Provides 5.05V Output without External Resistor Divider**
- **Precision 2% Reference**
- **0% to 95% Output Duty Cycle**
- **Cycle-by-Cycle Current Limiting**
- **Undervoltage Lockout with Hysteresis**
- **Internal Thermal Shutdown**
- **Operation from 7.5V to 40V**
- **Standby Mode Reduces Power Supply Current to 36μA**
- **Available in a Surface Mount 5-Pin DDPAK and 5-Pin TO-220 Packages**

APPLICATIONS

- **Automotive**
- **Computing**
- **Industrial Controllers**
- **Consumer Electronics**

PIN CONFIGURATIONS



GENERAL DESCRIPTION

The TC33166 is a high performance fixed frequency power switching regulator that contains the primary functions required for DC-to-DC converters. This device was specifically designed to be incorporated in step-down and voltage-inverting configurations with a minimum number of external components and can also be used cost effectively in step-up applications.

This device consists of an internal temperature compensated reference, fixed frequency oscillator with on-chip timing components, latching pulse width modulator for single pulse metering, high gain error amplifier, and a high current output switch.

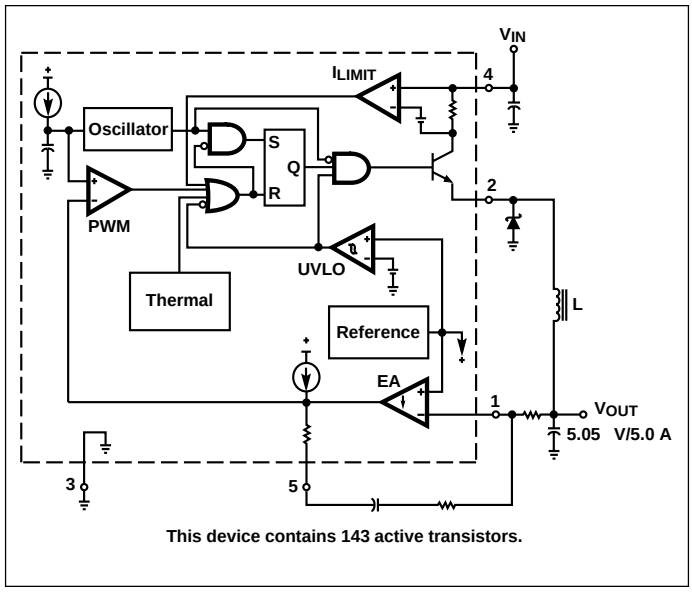
Protective features consist of cycle-by-cycle current limiting, undervoltage lockout, and thermal shutdown. Also included is a low power standby mode that reduces power supply current to 36μA.

ORDERING INFORMATION

Part Number	Package	Temperature Range
TC33166ERT	5-Pin DDPAK-B	–40 to + 85°C
TC33166EAT	5-Pin TO-220	–40 to + 85°C

SIMPLIFIED BLOCK DIAGRAM

(Step Down Application)



TC33166

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage ..... V_{CC} = 40V
Switch Output Voltage..... $V_{OUT\ (SWITCH)}$ = –1.5 to +V_{IN}
Voltage Feedback and
Compensation Input ..... $V_{FB,}V_{COMP}$ = –1.0 to + 7.0V
Power Dissipation
5-Pin TO-220 (T_A = +25°C) ..... Internally Limited
Thermal Resistance (Junction to Ambient) ..... θ_{JA} = 65°C/W
Thermal Resistance(Junction to Case) ..... θ_{JC} = 5.0°C/W
5-Pin DDPAK-B (T_A = +25°C) ..... Internally Limited
Thermal Resistance (Junction to Ambient) ... θ_{JA} = 70°C/W
Thermal Resistance(Junction to Case) .. θ_{JC} = 5.0°C/W
Operating Junction Temperature ..... T_J +150°C
Operating Ambient Temperature Range (Note 3) ..... –40 to +85°C
Storage Temperature Range ..... T_{STG} = –65 to +150°C

*This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operation section of the specifications is not implied. Exposure to absolute maximum ratings conditions for extended periods of time may affect device reliability.

ELECTRICAL CHARACTERISTICS: V_{CC} = 12V, for typical values T_A = +25°C, for min/max T_A is the operating ambient temperature range that applies [Note 2, 3], unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Oscillator						
f_{OSC}	Frequency (V_{CC} 7.5V to 40V),	T_A = +25°C	65	72	79	kHz
		$T_A = T_{LOW}$ to T_{HIGH}	62	—	81	
Error Amplifier						
$V_{FB(TH)}$	Voltage Feedback Input Threshold	T_A = +25°C	4.95	5.05	5.15	V
		$T_A = T_{LOW}$ to T_{HIGH}	4.85	—	5.20	
R_{egline}	Line Regulation	V_{CC} = 7.5V to 40V, T_A = +25°C	—	0.03	0.078	%V
I_{IB}	Input Bias Current	$V_{FB} = V_{FB(TH)}$ + 0.15V	—	0.15	1.0	µA
PSSR	Power Supply Rejection Ratio	V_{CC} = 10V to 20V, f = 120Hz	60	80	—	dB
V_{OH}	Output Voltage Swing	High State (I_{SOURCE} = 75µA, V_{FB} = 4.5V	4.2	4.9	—	V
V_{OL}		Low State I_{SINK} = 0.4mA, V_{FB} = 5.5V	—	1.6	1.9	
PWM Comparator						
$DC_{(MAX)}$	Duty Cycle	Maximum (V_{FB} = 0V)	92	95	100	%
$DC_{(MIN)}$		Minimum (V_{COMP} = 1.9V)	0	0	0	
Switch Output						
V_{SAT}	Output Voltage Source Saturation	V_{CC} = 7.5V, I_{SOURCE} = 3.0A	—	V_{CC} –1.5	V_{CC} –1.8	V
$I_{SW(OFF)}$	Off–State Leakage	V_{CC} = 40V, Pin 2 = GND	—	0	100	µA
Ipk_{SWITCH}	Current Limit Threshold		3.3	4.3	6.0	A
	Switching Times (V_{CC} = 40 V, I_{PK} = 3.0A,					nsec
t_r	L = 375µH, T_A = +25°C)	Output Voltage Rise Time	—	100	200	
t_r		Output Voltage Fall Time	—	50	100	
Undervoltage Lockout						
$V_{TH(UVLO)}$	Startup Threshold	V_{CC} Increasing, T_A = +25°C	5.5	5.9	6.3	V
$V_{H(UVLO)}$	Hysteresis	V_{CC} Decreasing, T_A = +25°C	0.6	0.9	1.2	V
Total Device						
I_{CC}	Power Supply Current (T_A = +25°C)					
		Standby (V_{CC} = 12V, V_{COMP} < 0.15V)	—	36	100	µA
		Operating (V_{CC} = 40V, Pin 1 = GND for maximum duty cycle)	—	31	55	mA

NOTES: 1. Maximum package power dissipation limits must be observed to prevent thermal shutdown activation.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
3. T_{LOW} = –40°C, T_{HIGH} = + 85°C

INTRODUCTION

The TC33166 is a monolithic power switching regulator that is optimized for DC-to-DC converter applications. This device operates as a fixed frequency, voltage mode regulator containing all the active functions required to directly implement step–down and voltage–inverting converters with a minimum number of external components. It can also be used cost effectively in step–up converter applications. Potential markets include automotive, computer, industrial, and cost sensitive consumer products. A description of each section of the device is given below with the representative block diagram shown in Figure 1.

Oscillator

The oscillator frequency is internally programmed to 72 kHz by capacitor C_T and a trimmed current source. The charge to discharge ratio is controlled to yield a 95% maximum duty cycle at the Switch Output. During the discharge of C_T, the oscillator generates an internal blanking pulse that holds the inverting input of the AND gate high, disabling the output switch transistor. The nominal oscillator peak and valley thresholds are 4.1V and 2.3V respectively.

Pulse Width Modulator

The Pulse Width Modulator consists of a comparator with the oscillator ramp voltage applied to the noninverting input, while the error amplifier output is applied into the inverting input. Output switch conduction is initiated when C_T is discharged to the oscillator valley voltage. As C_T charges to a voltage that exceeds the error amplifier output, the latch resets, terminating output transistor conduction for the duration of the oscillator ramp-up period. This PWM/ Latch combination prevents multiple output pulses during a given oscillator clock cycle. Figures 2 and 22 illustrate the switch output duty cycle versus the compensation voltage.

Current Sense

The TC33166 utilizes cycle-by-cycle current limiting as a means of protecting the output switch transistor from overstress. Each on-cycle is treated as a separate situation. Current limiting is implemented by monitoring the output switch transistor current buildup during conduction, and upon sensing an overcurrent condition, immediately turning off the switch for the duration of the oscillator ramp-up period.

The collector current is converted to a voltage by an internal trimmed resistor and compared against a reference by the Current Sense comparator. When the current limit threshold is reached, the comparator resets the PWM latch.

The current limit threshold is typically set at 4.3A. Figure 25 illustrates switch output current limit threshold versus temperature.

Error Amplifier and Reference

A high gain Error Amplifier is provided with access to the inverting input and output. This amplifier features a typical DC voltage gain of 80dB, and a unity gain bandwidth of 600kHz with 70 degrees of phase margin (Figure 19). The noninverting input is biased to the internal 5.05V reference, and is not pinned out. The reference has an accuracy of $\pm$ 2.0% at room temperature. To provide 5.0V at the load, the reference is programmed 50mV above 5.0V to compensate for a 1.0% voltage drop in the cable and connector from the converter output. If the converter design requires an output voltage greater than 5.05V, resistor R_1 must be added to form a divider network at the feedback input as shown in Figures 1 and 6. The equation for determining the output voltage with the divider network is:

$$V_{OUT} = 5.05 \left(\frac{R_2}{R_1}\right) + 1$$

External loop compensation is required for converter stability. A simple low–pass filter is formed by connecting a resistor (R_2) from the regulated output to the inverting input, and a series resistor–capacitor (R_F , C_F) between Pins 1 and 5. The compensation network component values shown in each of the applications circuits were selected to provide stability over the tested operating conditions. The step-down converter (Figure 6) is the easiest to compensate for stability. The step-up (Figure 8) and voltage–-inverting (Figure 10) configurations operate as continuous conduction flyback converters, and are more difficult to compensate. The simplest way to optimize the compensation network is to observe the response of the output voltage to a step load change, while adjusting R_F and C_F for critical damping. The final circuit should be verified for stability under four boundary conditions. These conditions are minimum and maximum input voltages, with minimum and maximum loads.

By clamping the voltage on the error amplifier output (Pin 5) to less than 150mV, the internal circuitry will be placed into a low power standby mode, reducing the power supply current to 36µA with a 12V supply voltage. Figure 26 illustrates the standby supply current versus supply voltage.

The Error Amplifier output has a 100µA current sourcepull-up that can be used to implement soft-start. Figure 5 shows the current source charging capacitor C_{SS} through a series diode. The diode disconnects C_{SS} from the feedback loop when the 1.0M resistor charges it above the operating range of Pin 5.

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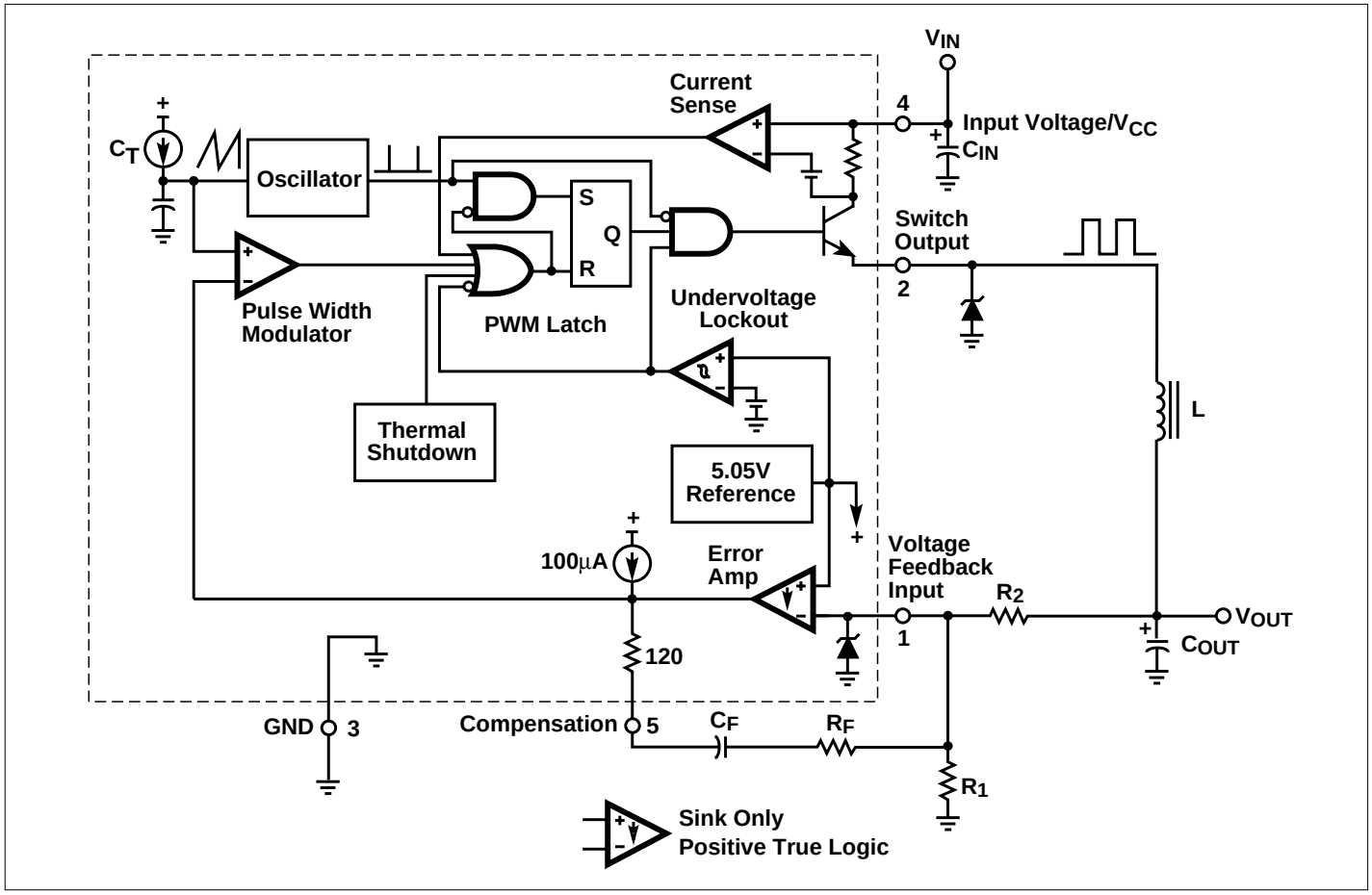

Figure 1. Representative Block Diagram

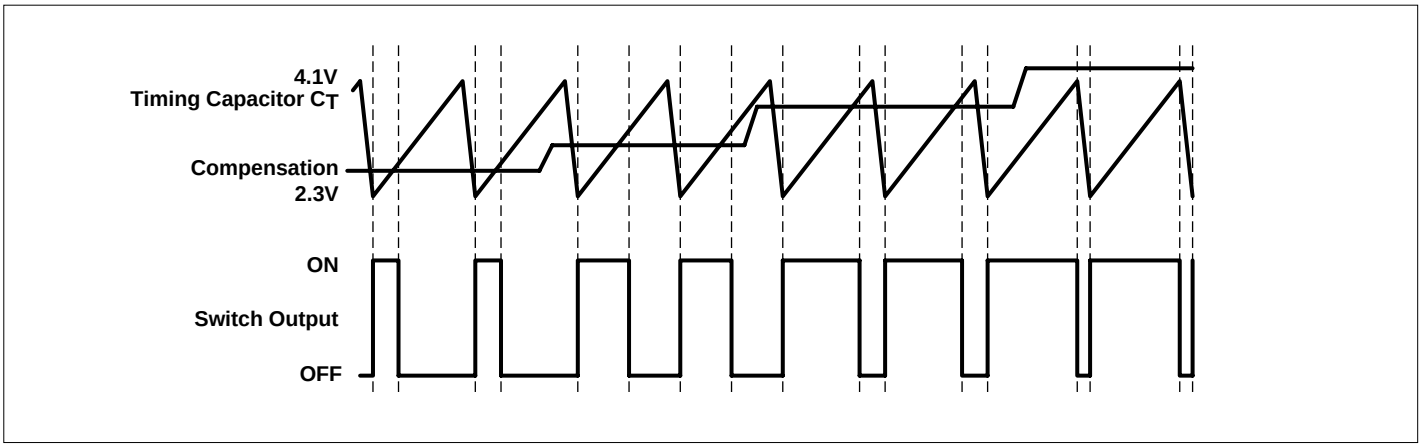

Figure 2. Timing Diagram

Switch Output

The output transistor is designed to switch a maximum of 40V, with a minimum peak collector current of 3.3 A. When configured for step-down or voltage-inverting applications, as in Figures 6 and 10, the inductor will forward bias the output rectifier when the switch turns off. Rectifiers with a high forward voltage drop or long turn-on delay time should not be used. If the emitter is allowed to go sufficiently negative, collector current will flow, causing additional device heating and reduced conversion efficiency. Figure 24 shows that by clamping the emitter to 0.5 V, the collector current will be in the range of 100µA over temperature. A 1N5825 or equivalent Schottky barrier rectifier is recommended to fulfill these requirements.

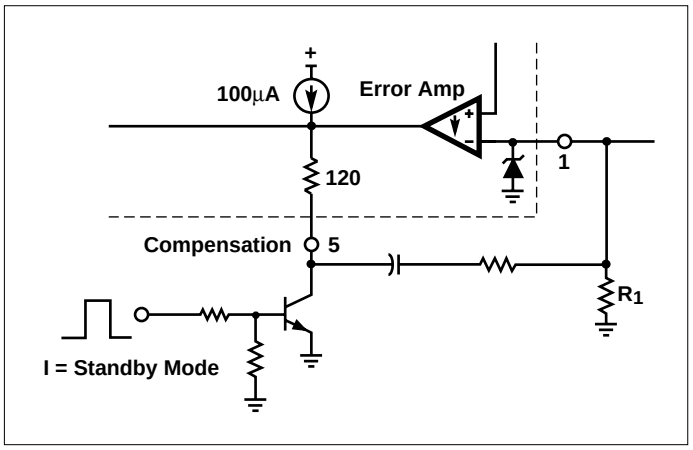

Figure 3. Low Power Standby Circuit

Undervoltage Lockout

An Undervoltage Lockout comparator has been incorporated to guarantee that the integrated circuit is fully functional before the output stage is enabled. The internal reference voltage is monitored by the comparator which enables the output stage when V_{CC} exceeds 5.9V. To prevent erratic output switching as the threshold is crossed, 0.9V of hysteresis is provided.

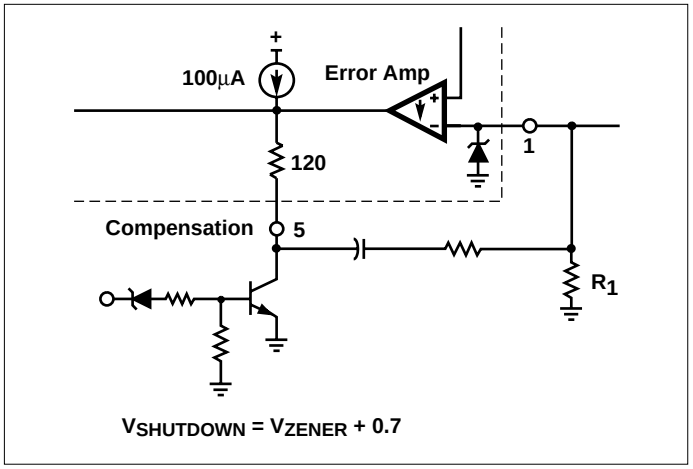

Figure 4. Over Voltage Shutdown Circuit

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 170°C the latch is forced into a 'reset' state, disabling the output switch. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.** The TC33166 is contained in a 5-Pin TO–220 type package. The tab of the package is common with the center pins (Pin 3) and is normally connected to ground.

DESIGN CONSIDERATIONS

Do not attempt to construct a converter on wire–wrap or plug–in prototype boards. Special care should be taken to separate ground paths from signal currents and ground paths from load currents. All high current loops should be kept as short as possible using heavy copper runs to minimize ringing and radiated EMI. For best operation, a tight component layout is recommended. Capacitors C_{IN} , C_{OUT}, and all feedback components should be placed as close to the IC as physically possible. It is also imperative that the Schottky diode connected to the Switch Output be located as close to the IC as possible.

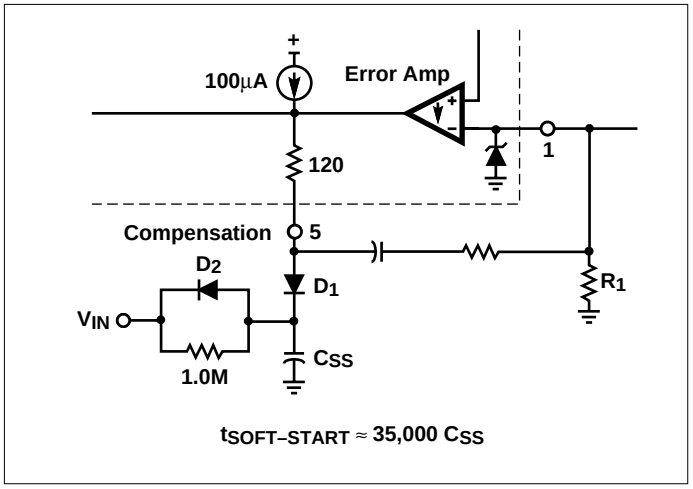

Figure 5. Soft-Start Circuit

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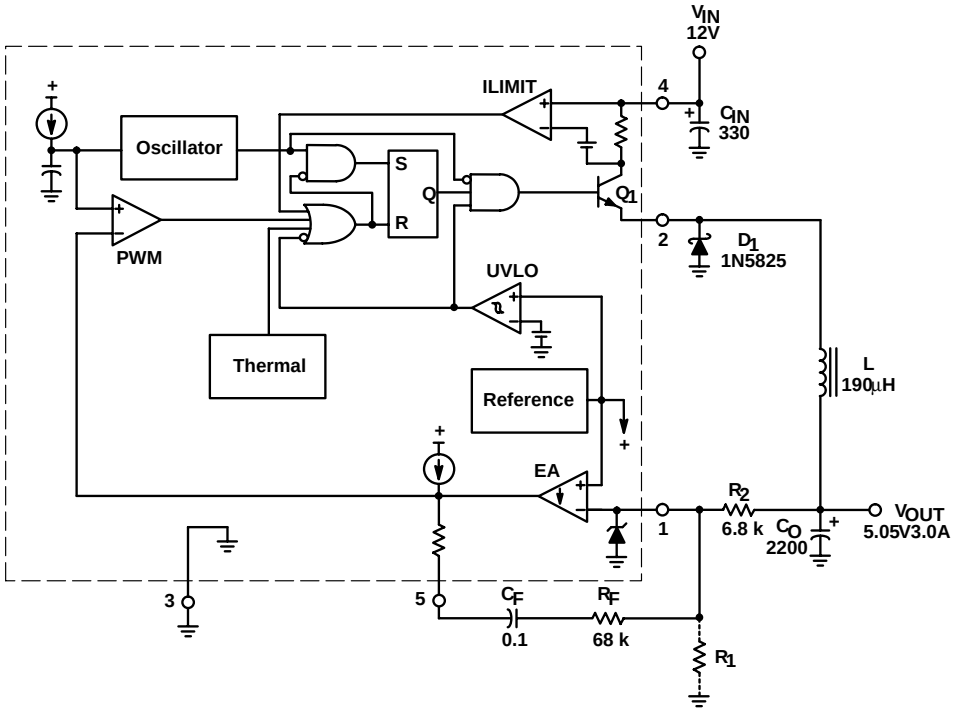


Test	Conditions	Results
Line Regulation	V_{IN} = 8.0V to 36V, I_{OUT} = 3.0A	5.0mV = ±0.05%
Load Regulation	V_{IN} = 12V, I_{OUT} = 0.25A to 3.0A	2.0mV = ±0.02%
Output Ripple	V_{IN} = 12V, I_{OUT} = 3.0A	10mVpp
Short Circuit Current	V_{IN} = 12V, R_L = 0.1Ω	4.3A
Efficiency	V_{IN} = 12V, I_{OUT} = 3.0A	82.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns if #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

The Step–Down Converter application is shown in Figure above. The output switch transistor Q1 interrupts the input voltage, generating squarewave at the LC_O filter input. The filter averages the squarewaves, producing a DC output voltage that can be set to any level between V_{IN} and V_{REF} by controlling the percent conduction time of Q1 to that of the total oscillator cycle time. If the converter design requires an output voltage greater than 5.05V, resistor R_1 must be added to form a divider network at the feedback input.

Figure 6. Step-Down Converter

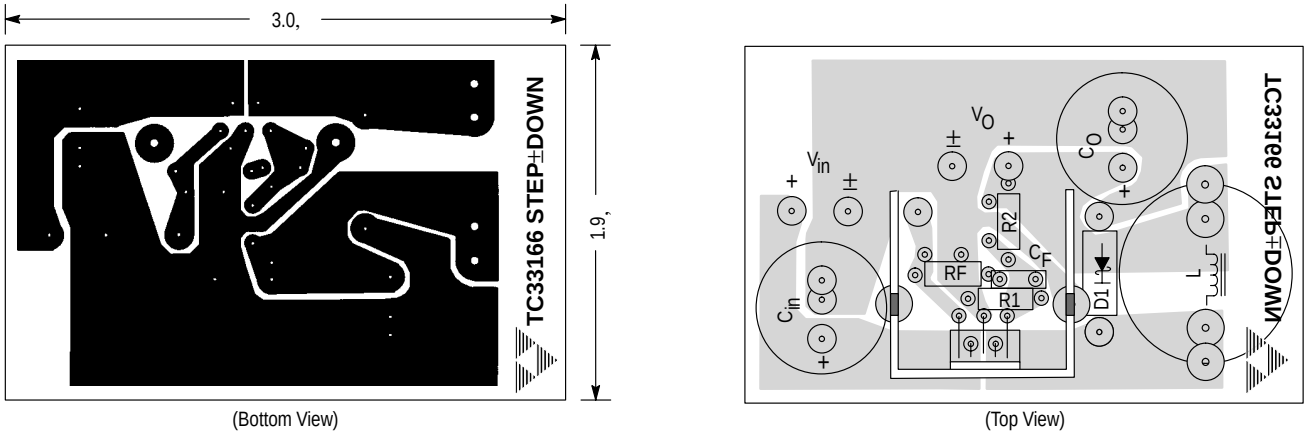
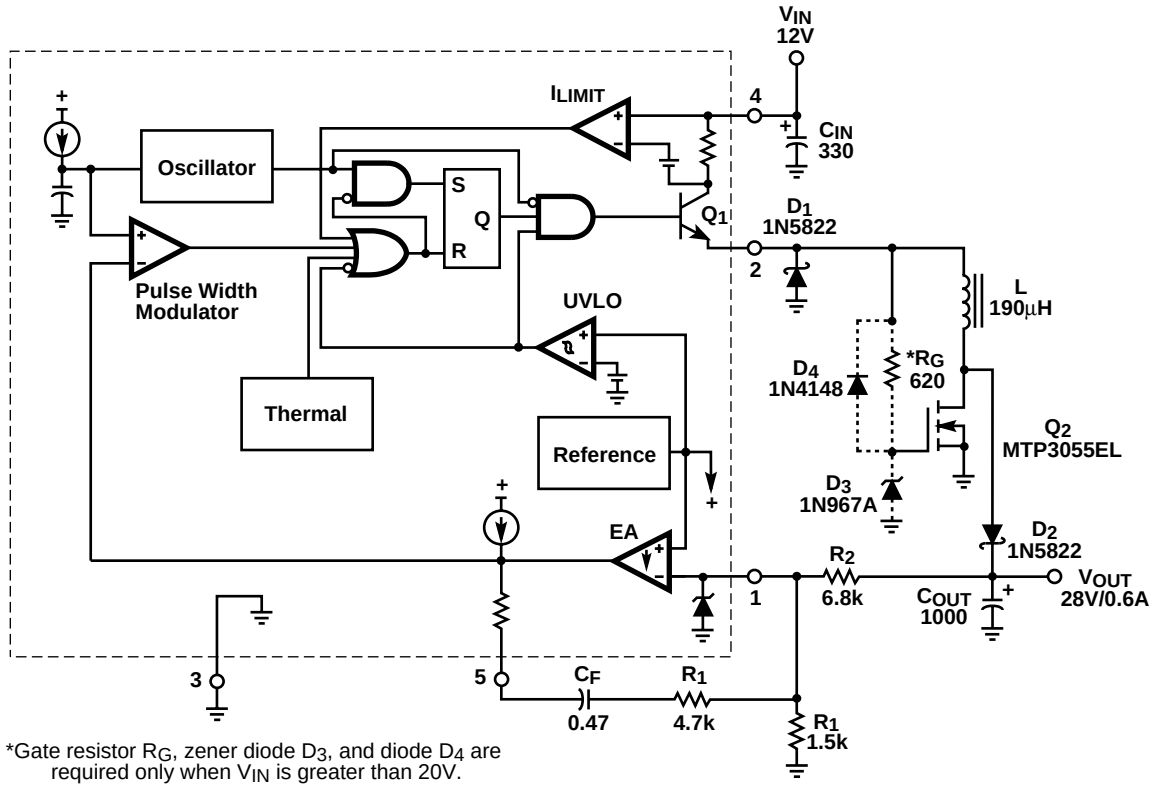


Figure 7. Step-Down Converter Printed Circuit Board and Component Layout



*Gate resistor R_G, zener diode D_3, and diode D_4 are required only when V_{IN} is greater than 20V.

Test	Conditions	Results
Line Regulation	V_{IN} = 8.0V to 24V, I_{OUT} = 0.6A	23mV = ±0.41%
Load Regulation	V_{IN} = 12V, I_{OUT} = 0.1A to 0.6A	3.0mV = ±0.005%
Output Ripple	V_{IN} = 12V, I_{OUT} = 0.6A	100mVpp
Short Circuit Current	V_{IN} = 12V, R_L = 0.1Ω	4.0A
Efficiency	V_{IN} = 12V, I_{OUT} = 0.6A	82.8%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns if #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc.
TC34166: 5903B, or 5930B
MTP3055EL: 5925B

Figure above shows that the TC33166 can be configured as a step–up/down converter with the addition of an external power MOSFET. Energy is stored in the inductor during the ON time of transistors Q1 and Q2 . During the OFF time, the energy is transferred, with respect to ground, to the output filter capacitor and load. This circuit configuration has two significant advantages over the basic step–up converter circuit. The first advantage is that output short -circuit protection is provided by the TC33166, since Q1 is directly in series with V_{IN} and the load. Second, the output voltage can be programmed to be less than V_{IN} . Notice that during the OFF time, the inductor forward biases diodes D_1 and D_2 , transferring its energy with respect to ground rather than with respect to V_{IN} . When operating with V_{IN} greater than 20V, a gate protection network is required for the MOSFET. The network consists of components R_G , D_3, and D_4 .

Figure 8. Step-Up / Down Converter

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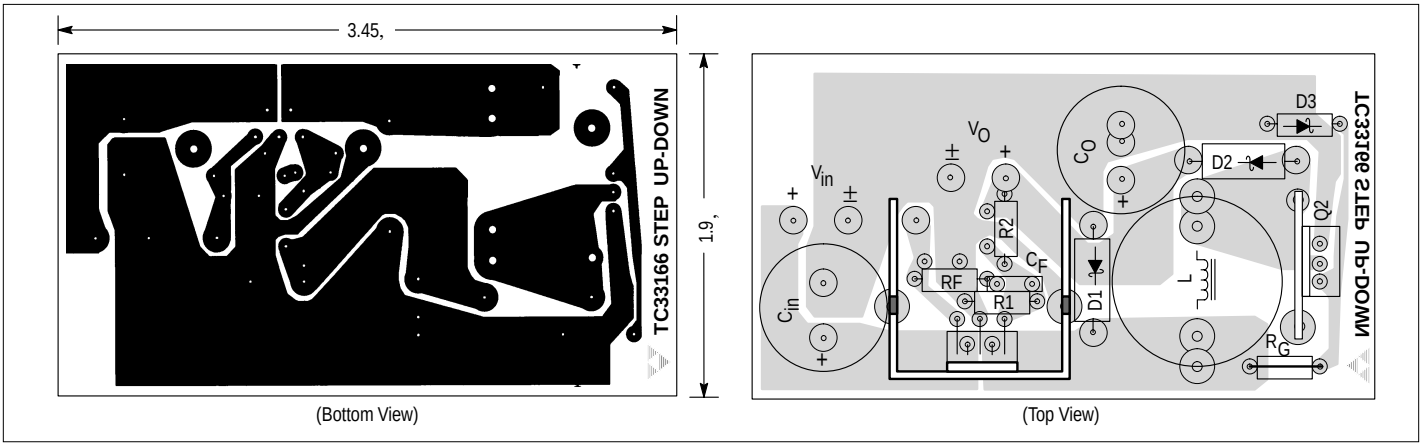
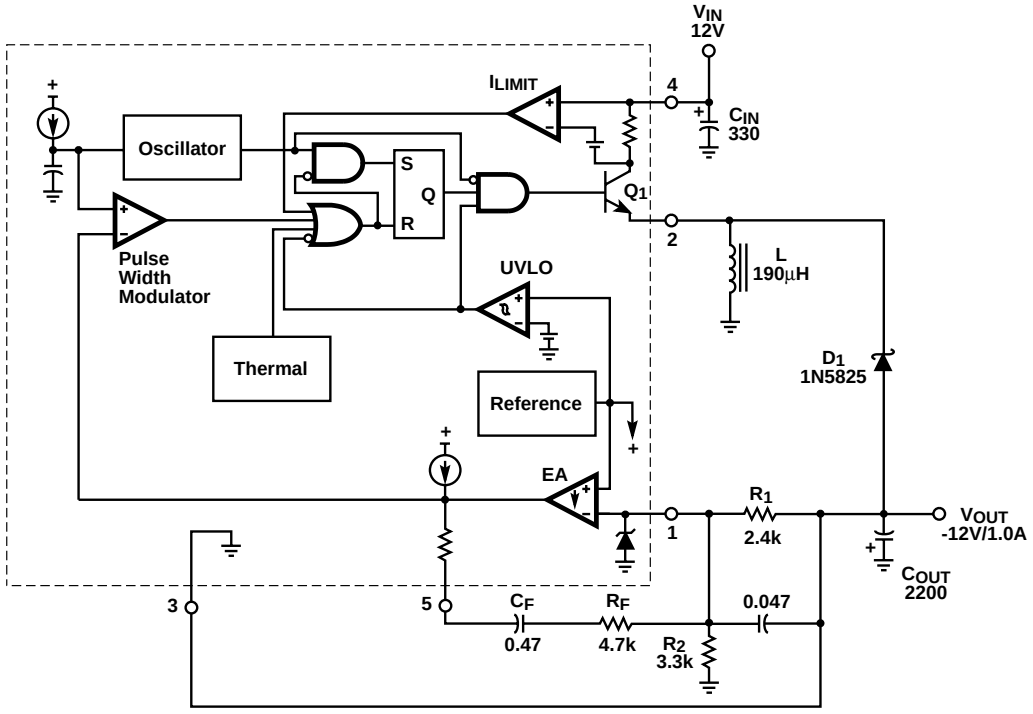


Figure 9. Step-Up/Down Converter Printed Circuit Board and Component Layout



Test	Conditions	Results
Line Regulation	V_{IN} = 8V to 24V, I_{OUT} = 1.0A	1.5mV = ±0.01%
Load Regulation	V_{IN} = 12V, I_{OUT} = 0.1A to 1.0A	4.0mV = ±0.017%
Output Ripple	V_{IN} = 12V, I_{OUT} = 1.7A	80mVpp
Short Circuit Current	V_{IN} = 12V, R_L = 0.1Ω	3.74A
Efficiency	V_{IN} = 12V, I_{OUT} = 1.0A	81.2%

L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns if #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Two potential problems arise when designing the standard voltage–inverting converter with the TC33166. First, the Switch Output emitter is limited to –1.5V with respect to the ground pin and second, the Error Amplifier's noninverting input is internally committed to the reference and is not pinned out. Both of these problems are resolved by connecting the IC ground pin to the converter's negative output as shown in Figure 10. This keeps the emitter of Q1 positive with respect to the ground pin and has the effect of reversing the Error Amplifier inputs. Note that the voltage drop across R_1 is equal to 5.05V when the output is in regulation.

Figure 10. Voltage Inverting Converter

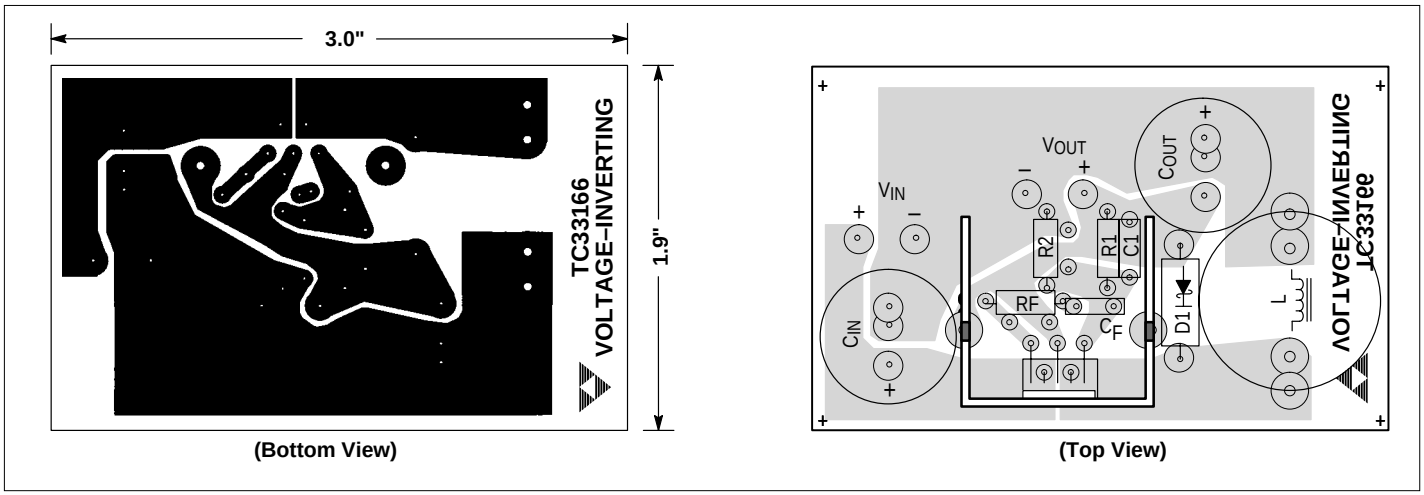


Figure 11. Voltage-Inverting Converter Printed Circuit Board and Component Layout

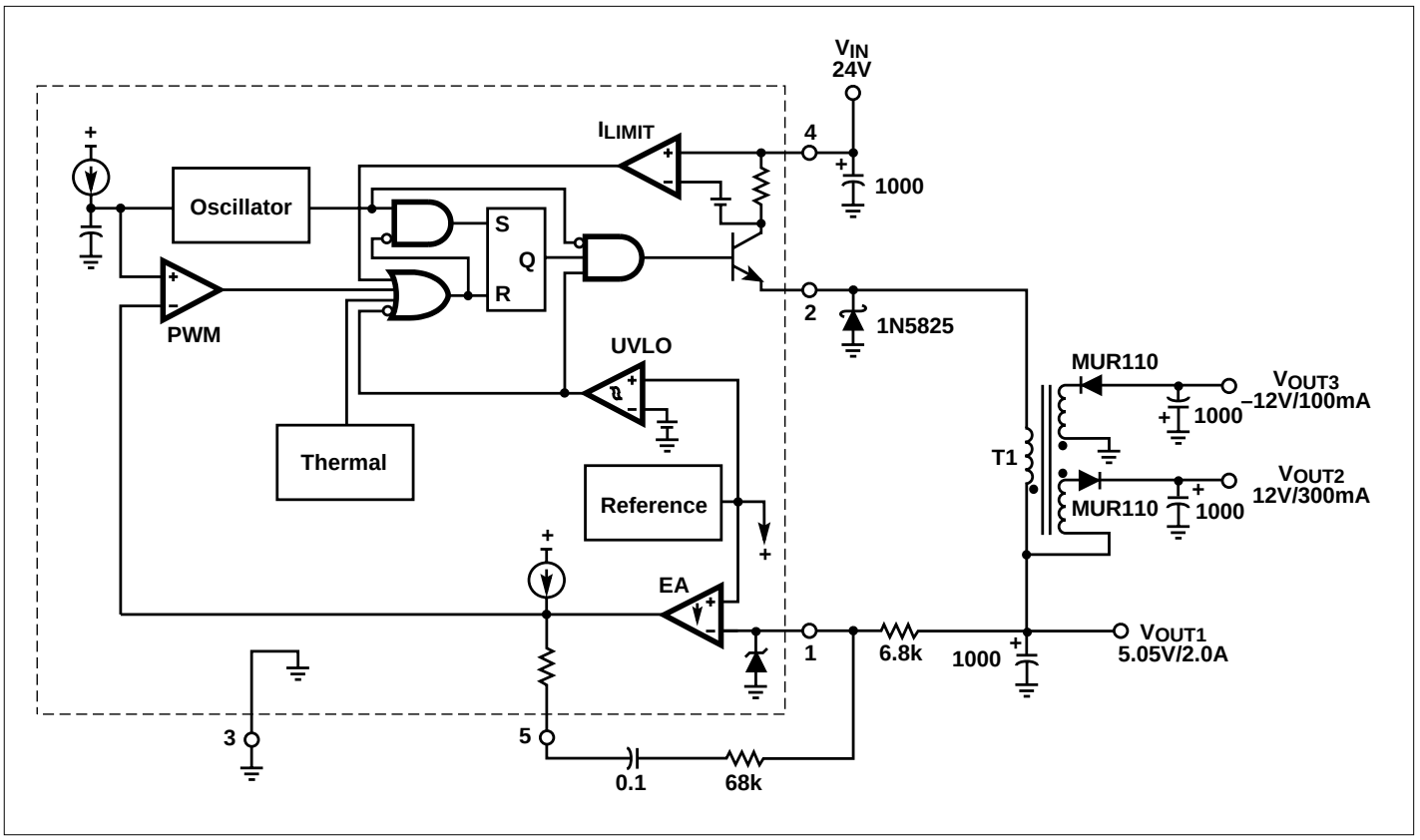


Figure 12. Triple Output Converter

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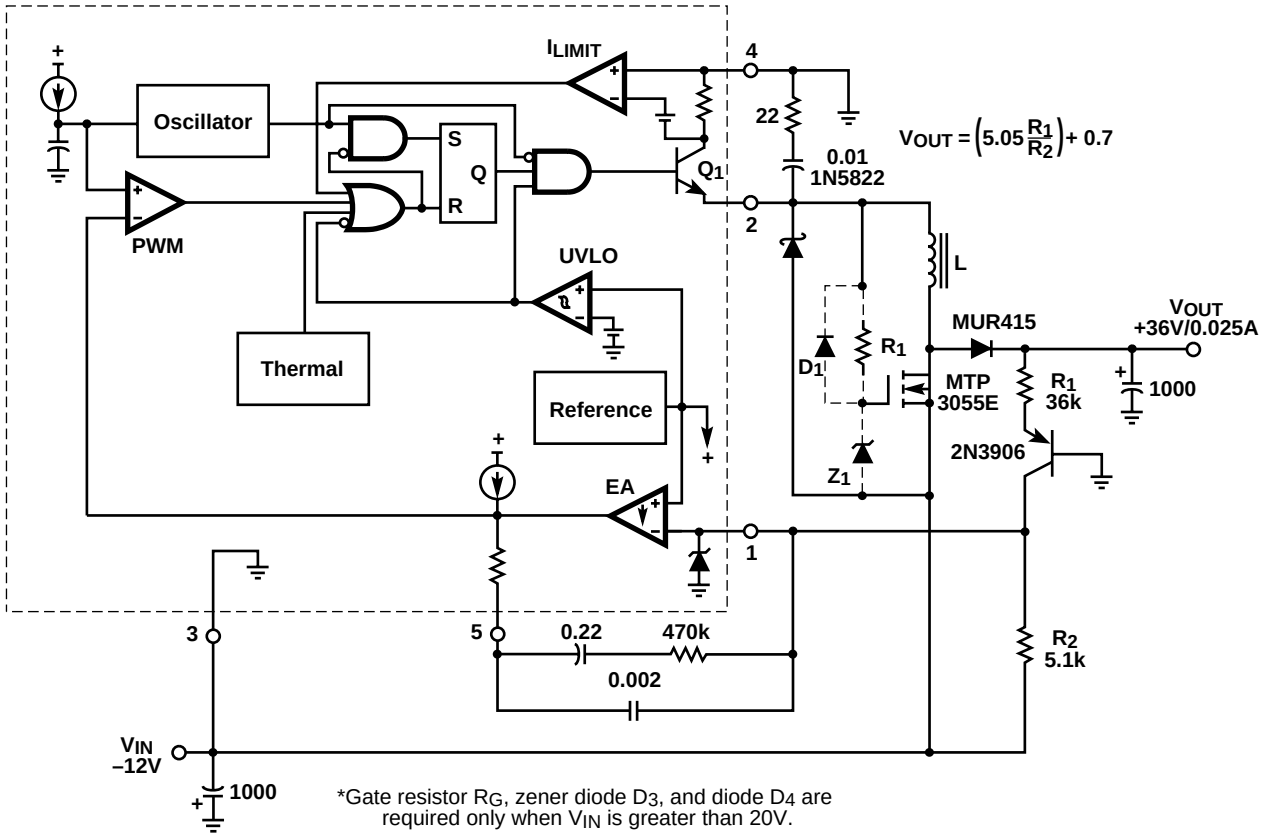
Tests		Conditions	Results
Line Regulation	5.0V	V_{IN} = 15V to 30V, I_{OUT1} = 2.0A, I_{OUT2} = 300mA, I_{OUT3} = 100mA	4.0mV = ± 0.04%
	12V		450mV = ±1.9%
	–12V		350mV = ±1.5%
Load Regulation	5.0V	V_{IN} = 24V, I_{OUT1} = 500mA to 2.0A, I_{OUT2} = 300mA, I_{OUT3} = 100mA	2.0mV = ± 0.02%
	12V	V_{IN} = 24V, I_{OUT1} = 2.0A, I_{OUT2} = 100mA to 250mA, I_{OUT3} = 200mA	420mV = ±1.7%
	–12V	V_{IN} = 24V, I_{OUT1} = 2.0A, I_{OUT2} = 300mA, I_{OUT3} = 30mA to 100mA	310mV = ±1.3%
Output Ripple	5.0V	V_{IN} = 24V, I_{OUT1} = 2.0A, I_{OUT2} = 300mA, I_{OUT3} = 100mA	50mV_{PP}
	12V		25mV_{PP}
	–12V		10mV_{PP}
Short Circuit Current	5.0V	V_{IN} = 24V, R_L = 0.1Ω	4.3A
	12V		1.83A
	–12V		1.47A
Efficiency	TOTAL	V_{IN} = 24V, I_{OUT1} = 2.0A, I_{OUT2} = 300mA, I_{OUT3} = 100mA	83.3%

T1 = Primary: Coilcraft M1496-A or General Magnetics Technology GMT–0223, 42 turns of #16 AWG on Magnetics Inc. 58350-A2 core.
Secondary: V_{OUT2} — 65 turns of #26 AWG
— 96 turns of #28 AWG
Heatsink = AAVID Engineering Inc. 5903B, or 5930B.

Multiple auxiliary outputs can easily be derived by winding secondaries on the main output inductor to form a transformer. The secondaries must be connected so that the energy is delivered to the auxiliary outputs when the Switch Output turns off. During the OFF time, the voltage across the primary winding is regulated by the feedback loop, yielding a constant Volts/Turn ratio. The number of turns for any given secondary voltage can be calculated by the following equation:

$$\#\,TURNS_{(SEC)} = \frac{V_{OUT(SEC)} + V_{F(SEC)}}{\left(\frac{V_{OUT(PRI)} + V_{F(PRI)}}{\#TURNS_{(PRI)}}\right)}$$

Note that the 12 V winding is stacked on top of the 5.0V output. This reduces the number of secondary turns and improves lead regulation. For best auxiliary regulation, the auxiliary outputs should be less than 33% of the total output power.
L = Coilcraft M1496–A or General Magnetics Technology GMT–0223, 42 turns if #16 AWG on Magnetics Inc. 58350–A2 core. Heatsink = AAVID Engineering Inc. 5903B, or 5930B.



Test	Conditions	Results
Line Regulation	V_{IN} = –10V to – 20V, I_{OUT} = 0.25A	250mV = ± 0.35%
Load Regulation	V_{IN} = –12V, I_{OUT} = 0.025A to 0.25A	790mV = ±1.19%
Output Ripple	V_{IN} = –12V, I_{OUT} = 0.25A	80mV_{PP}
Efficiency	V_{IN} = –12V, I_{OUT} = 0.25A	79.2%

L = Coilcraft M1496–A or ELMACO CHK1050, 42 turns of #16 AWG on Magnetics Inc. 58350–A2 core.
Heatsink = AAVID Engineering Inc. 5903B or 5930B

Figure 13. Negative Input/Positive Output Regulator

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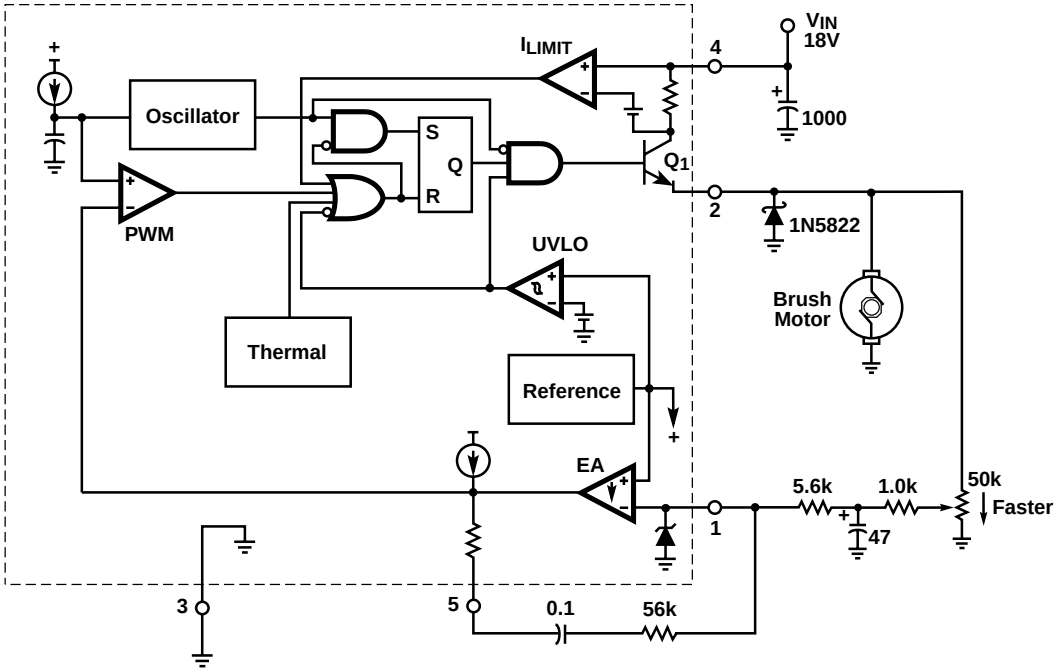
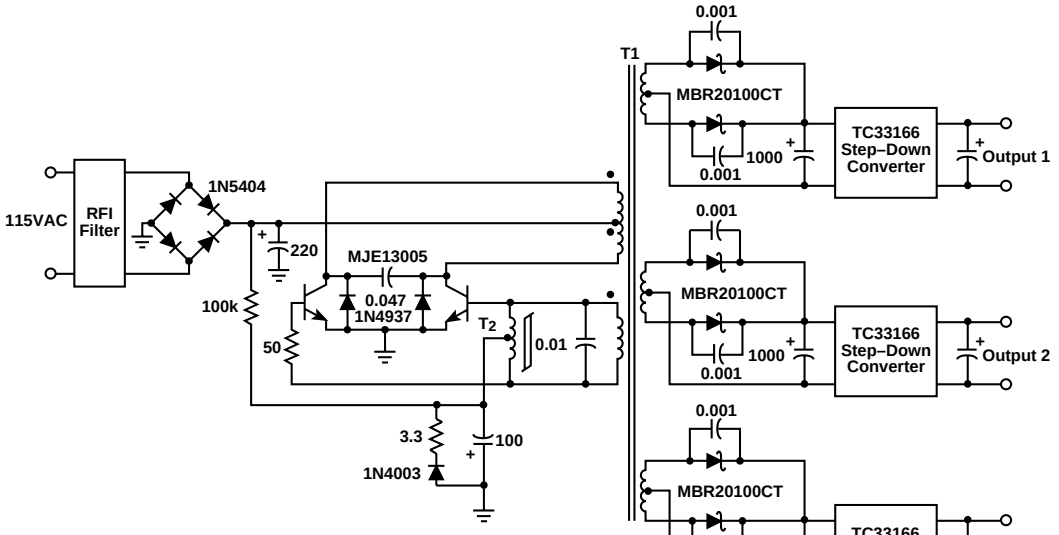


Test	Conditions	Results
Low Speed Line Regulation	V_{IN} = 12V to 24V	1760 RPM ±1%
High Speed Line Regulation	V_{IN} = 12V to 24V	3260 RPM ±6%

Figure 14. Variable Motor Speed Control with EMF Feedback Sensing



T_1 = Core and Bobbin — Coilcraft PT3595
Primary — 104 turns #26 AWG
Base Drive — 3 turns #26 AWG
Secondaries — 16 turns #16 AWG
Total Gap — 0.002"

T_2 = Core — TDK T6 x 1.5 x 3 H5C2
14 turns center tapped #30 AWG
Heatsink = AAVID Engineering Inc.
TC34166 and MJE13005 — 5903B
MBR20100CT — 5925B

The TC33166 can be used cost effectively in off—line applications even though it is limited to a maximum input voltage of 40V. Figure 15 shows a simple and efficient method for converting the AC line voltage down to 24V. This preconverter has a total power rating of 125W with a conversion efficiency of 90%. Transformer T_1 provides output isolation from the AC line and isolation between each of the secondaries. The circuit self—oscillates at 50kHz and is controlled by the saturation characteristics of T_2. Multiple TC33166 post regulators can be used to provide accurate independently regulated outputs for a distributed power system.

Figure 15. Off-Line Preconverter

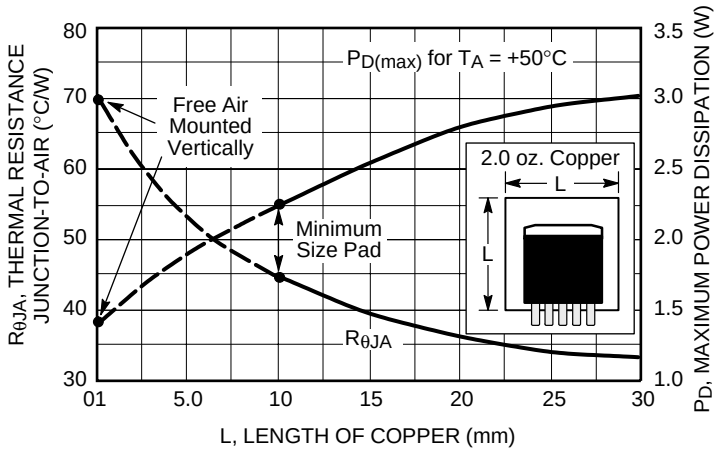


Figure 16. DDPAK Thermal Resistance and Maximum Power Dissipation vs. P.C.B. Copper Length

Design Equation Table

Calculation	Step-Down	Step-Up/Down	Voltage-Inverting
$\frac{t_{ON}}{t_{OFF}}$ (Notes 1, 2)	$\frac{V_{OUT} - V_F}{V_{IN} - V_{SAT} - V_{OUT}}$	$\frac{V_{OUT} - V_{F1} + V_{F2}}{V_{IN} - V_{SATQ1} - V_{SATQ2}}$	$\frac{\lvert V_{OUT}\rvert + V_F}{V_{IN} - V_{SAT}}$
t_{ON}	$\frac{\frac{t_{ON}}{t_{OFF}}}{f_{OSC}\left(\frac{t_{ON}}{t_{OFF}}+1\right)}$	$\frac{\frac{t_{ON}}{t_{OFF}}}{f_{OSC}\left(\frac{t_{ON}}{t_{OFF}}+1\right)}$	$\frac{\frac{t_{ON}}{t_{OFF}}}{f_{OSC}\left(\frac{t_{ON}}{t_{OFF}}+1\right)}$
Duty Cycle (Note 3)	$t_{ON}\ f_{OSC}$	$t_{ON}\ f_{OSC}$	$t_{ON}\ f_{OSC}$
I_{Lavg}	I_{OUT}	$I_{OUT}\left(\frac{t_{ON}}{t_{OFF}}+1\right)$	$I_{OUT}\left(\frac{t_{ON}}{t_{OFF}}+1\right)$
$I_{pk(SWITCH)}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$	$I_{L\ avg} + \frac{\Delta I_L}{2}$
L	$\left(\frac{V_{IN} - V_{SAT} - V_{OUT}}{\Delta I_L}\right) t_{ON}$	$\left(\frac{V_{IN} - V_{SATQ1} - V_{SATQ2}}{\Delta I_L}\right) t_{ON}$	$\left(\frac{V_{IN} - V_{SAT}}{\Delta I_L}\right) t_{ON}$
$V_{RIPPLE(pp)}$	$\Delta I_L \sqrt{\left(\frac{1}{8 f_{osc} C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{ON}}{t_{OFF}}+1\right) \sqrt{\left(\frac{1}{f_{osc} C_O}\right)^2 + (ESR)^2}$	$\left(\frac{t_{ON}}{t_{OFF}}+1\right) \sqrt{\left(\frac{1}{f_{osc} C_O}\right)^2 + (ESR)^2}$
V_{OUT}	$V_{REF}\left(\frac{R_2}{R_1}+1\right)$	$V_{REF}\left(\frac{R_2}{R_1}+1\right)$	$V_{REF}\left(\frac{R_2}{R_1}+1\right)$

NOTES: 1. V_{SAT} – Switch Output source saturation voltage, refer to Figure 23

2. V_F – Output rectifier forward voltage drop. Typical value for 1N5822 Schottky barrier rectifier is 0.5V.

3. Duty cycle is calculated at the minimum operating input voltage and must not exceed the guaranteed minimum DC (max) specification of 0.92.

The following converter characteristics must be chosen:

V_{OUT} – Desired output voltage.

I_{OUT} – Desired output current.

ΔI_L – Desired peak–to–peak inductor ripple current. For maximum output current especially when the duty cycle is greater than 0.5, it is suggested that ΔI_L be chosen minimum current limit threshold of 3.3A. If the design goal is to use a minimum inductance value, let $\Delta I_L = 2\ (I_L avg)$. This will proportionally reduce the converter's output current capability.

VRIPPLE(pp) – Desired peak-to-peak output ripple voltage. For best performance, the ripple voltage should be kept to less than 2% of V_{OUT}. Capacitor C_O should be a low equivalent series resistance (ESR) electrolytic designed for switching regulator applications.

TC33166

TYPICAL CHARACTERISTICS

Figure 17. Voltage Feedback Input Threshold versus Temperature

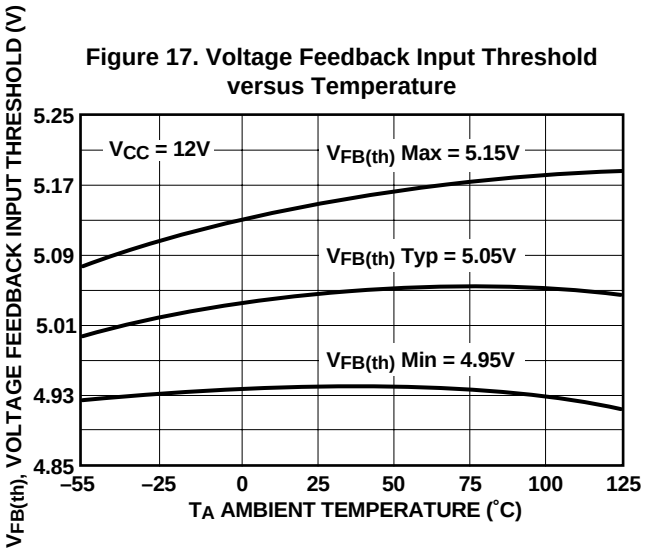


Figure 18. Voltage Feedback Input Bias Current versus Temperature

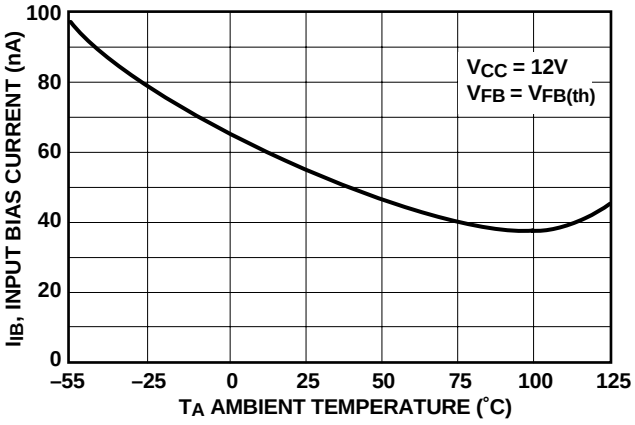


Figure 19. Error Amp Open Loop Gain and Phase versus Frequency

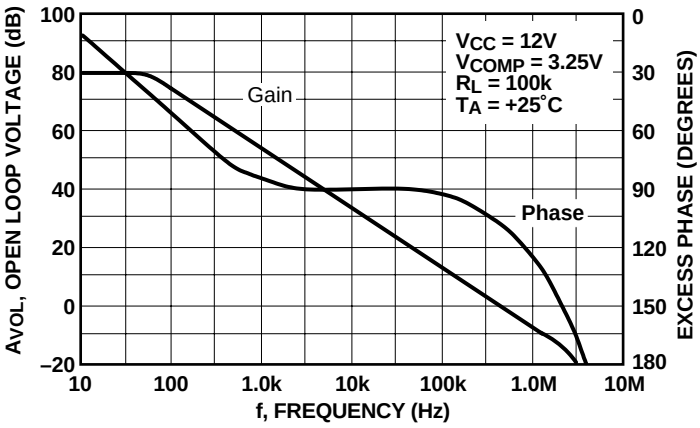


Figure 20. Error Amp Output Saturation versus Sink Current

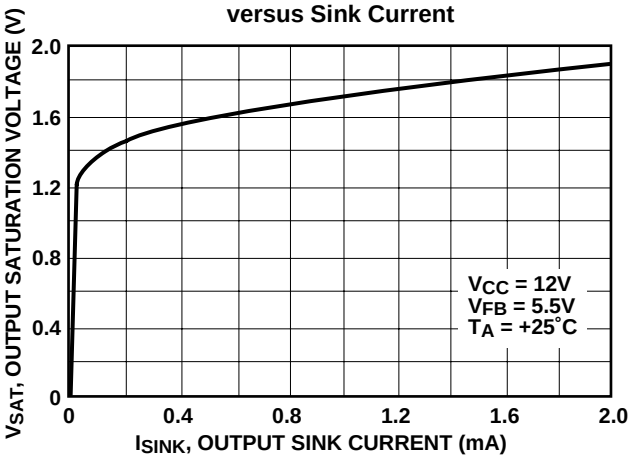


Figure 21. Oscillator Frequency Change versus Temperature

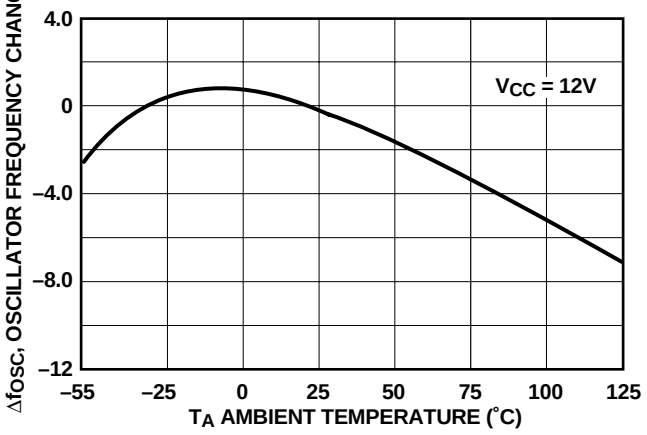
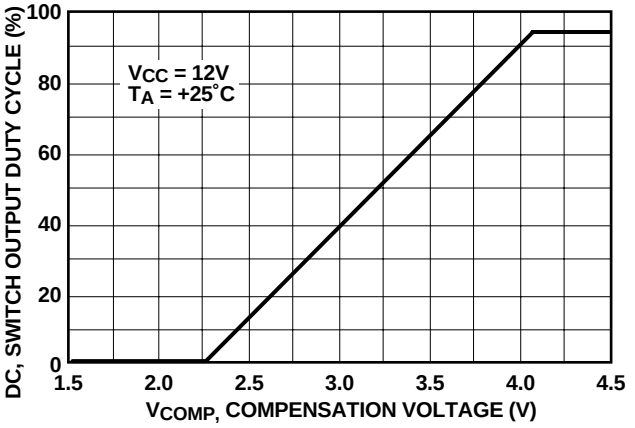


Figure 22. Switch Output Duty Cycle versus Compensation Voltage



TYPICAL CHARACTERISTICS

Figure 23. Switch Output Source Saturation versus Source Current

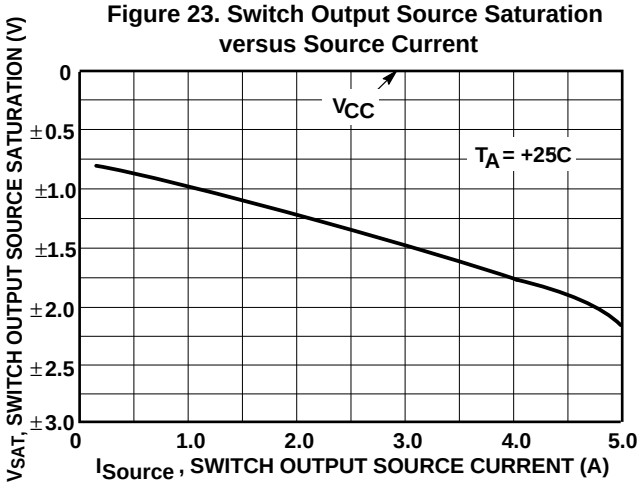


Figure 24. Negative Switch Output Voltage versus Temperature

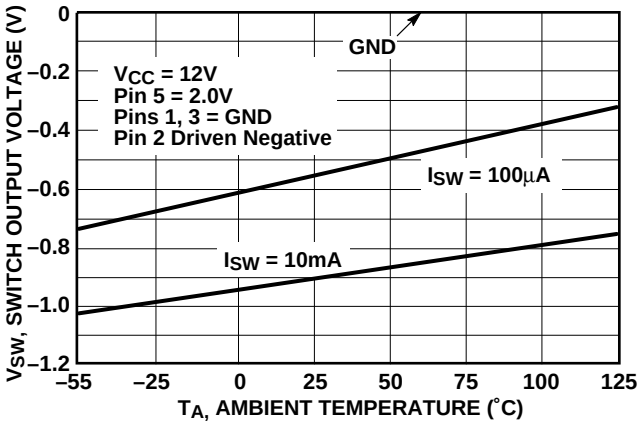


Figure 25. Switch Output Current Limit Threshold versus Temperature

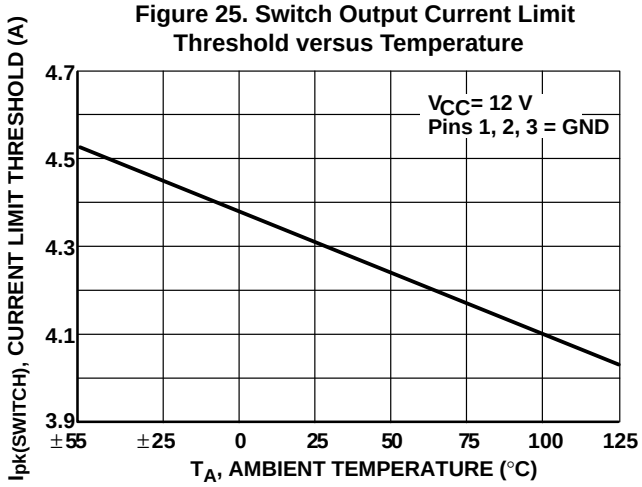


Figure 26. Standby Supply Current versus Supply Voltage

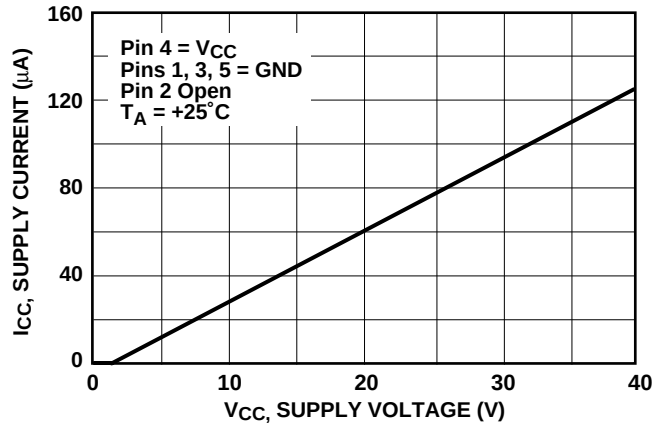


Figure 27. Undervoltage Lockout Threshold versus Temperature

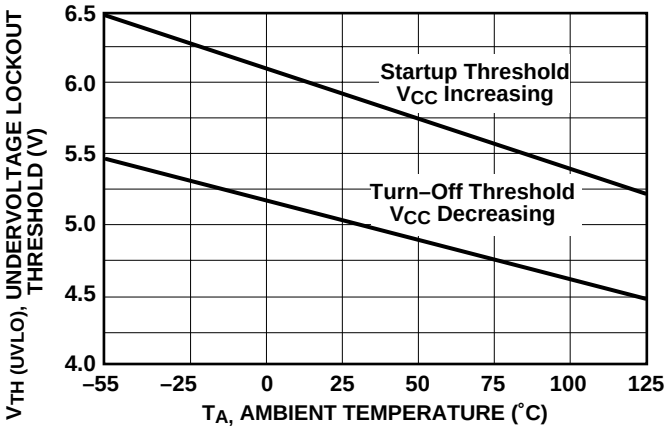
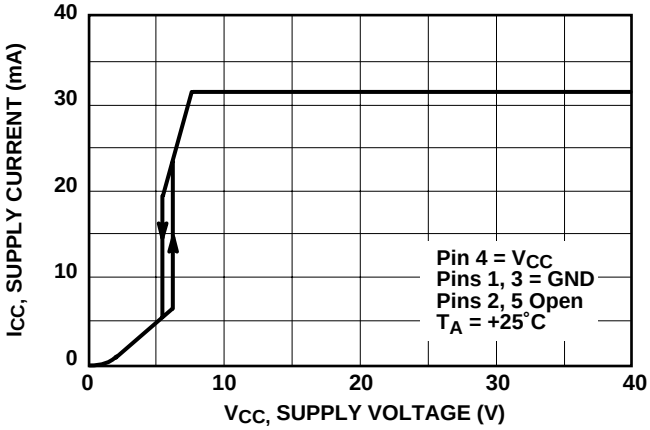


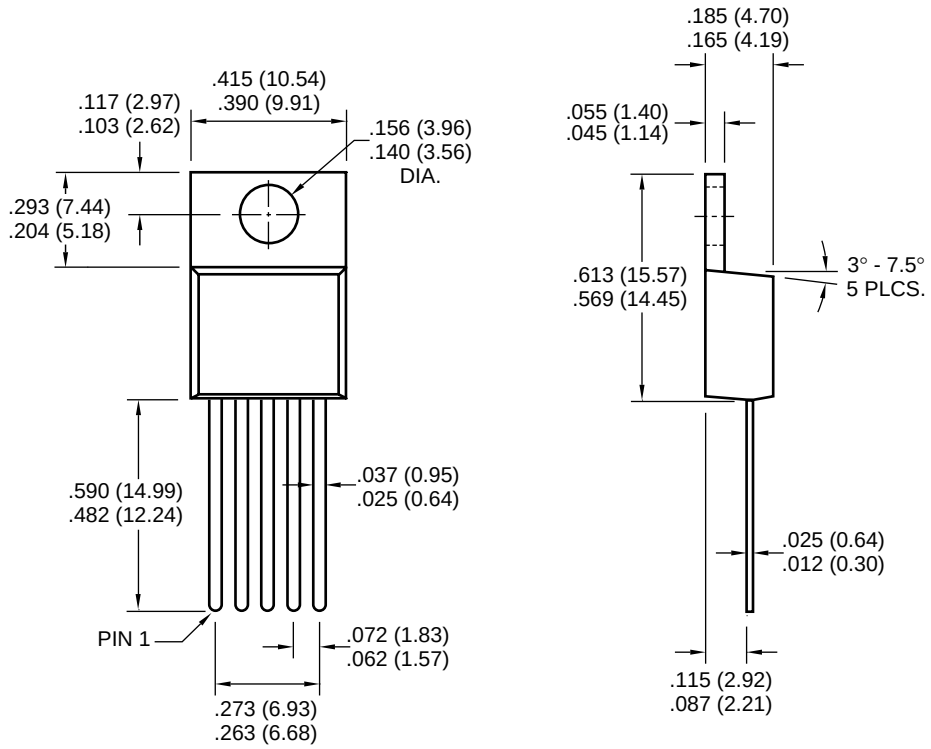
Figure 28. Operating Supply Current versus Supply Voltage



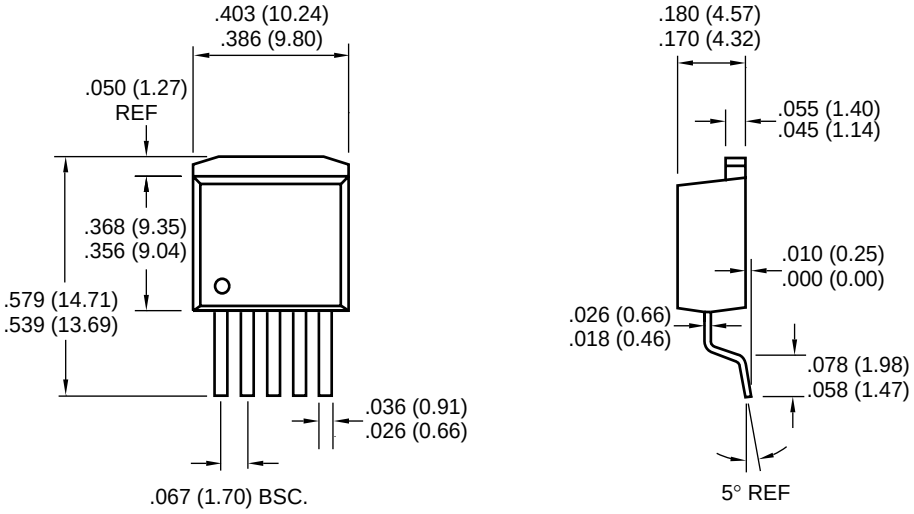
TC33166

PACKAGE DIMENSIONS

5-Pin TO-220



5-Pin DDPAK-B



Dimensions: inches (mm)

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