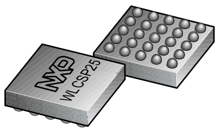


IP4855CX25

SD 3.0-compliant memory card integrated dual voltage level translator with EMI filter and ESD protection

Rev. 4 — 2 June 2014 Preliminary data sheet

1. General description

The device is an SD 3.0-compliant 6-bit bidirectional dual voltage level translator. It is designed to interface between a memory card operating at 1.8 V or 2.9 V signal levels and a host with a fixed nominal supply voltage of 1.2 V to 3.3 V. The device supports SD 3.0 SDR50, DDR50, SDR25, SDR12 and SD 2.0 high-speed (50 MHz) and default-speed (25 MHz) modes. The device has an integrated voltage selectable low dropout regulator to supply the card-side I/Os, built-in EMI filters and robust ESD protections (IEC 61000-4-2, level 4).

2. Features and benefits

- Supports up to 100 MHz clock rate
- Feedback channel for clock synchronization
- SD 3.0 specification-compliant voltage translation to support SDR50, DDR50, SDR25, SDR12, high-speed and default-speed modes
- 50 mA low dropout voltage regulator to supply the card-side I/Os
- Low power consumption by push-pull output stage with break-before-make architecture
- Integrated pull-up and pull-down resistors: no external resistors required
- Integrated EMI filters suppress higher harmonics of digital I/Os
- Integrated 8 kV ESD protection according to IEC 61000-4-2, level 4 on card side
- Level shifting buffers keep ESD stress away from the host (zero-clamping concept)
- 25-ball WLCSP; pitch 0.4 mm

3. Applications

- Smartphones
- Mobile handsets
- Digital cameras
- Tablet PCs
- Laptop computers
- SD, MMC or microSD card readers

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4855CX25	WLCSP25	wafer level chip-size package; 25 bumps (5 × 5)[1]	-
IP4855CX25/C	WLCSP25	wafer level chip-size package with back side coating; 25 bumps (5 × 5)[2]	-

[1] Typical size: 2.05 mm × 2.05 mm × 0.47 mm.

[2] Typical size: 2.05 mm × 2.05 mm × 0.51 mm.

5. Block diagram

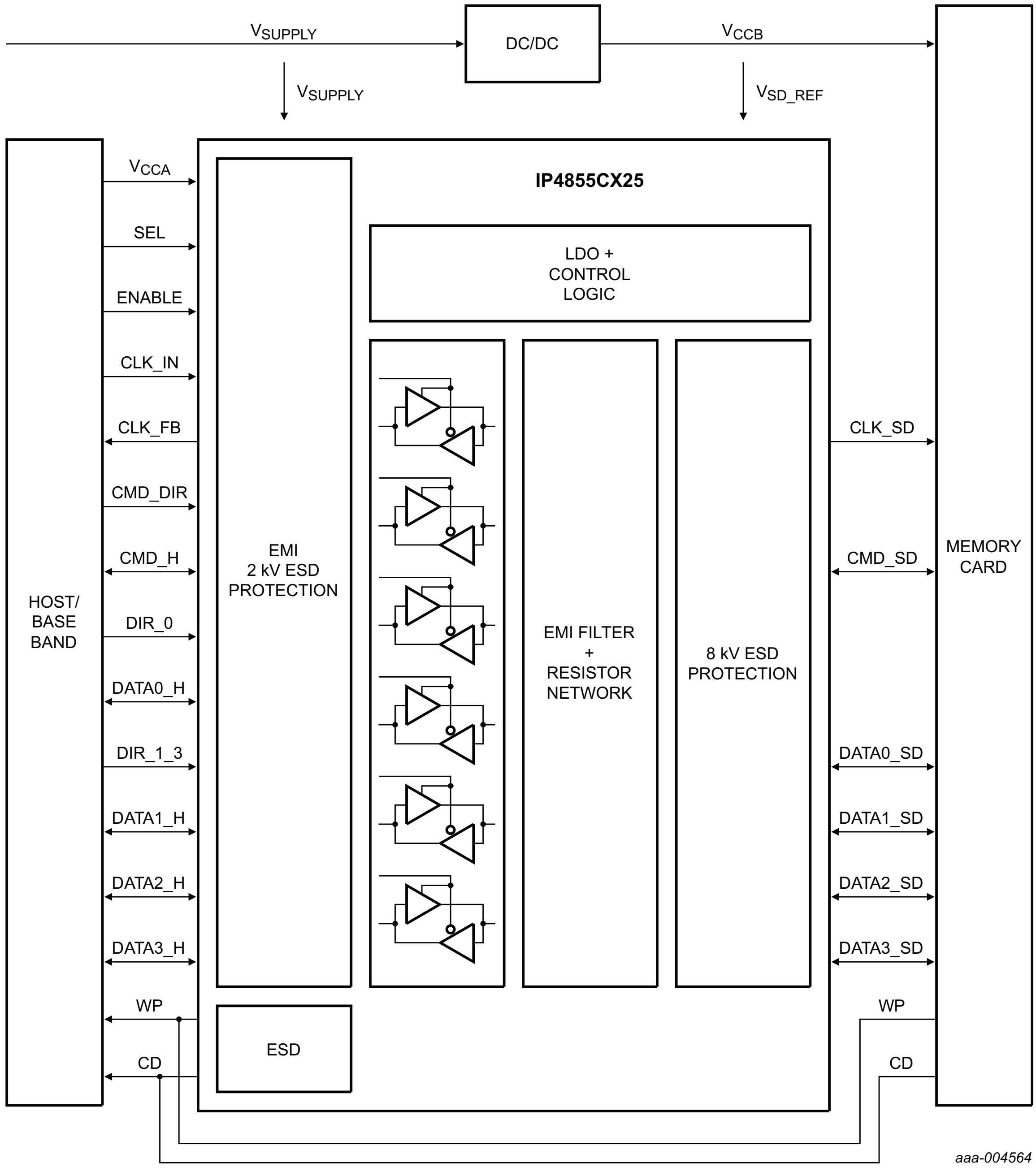


Fig 1. Block diagram

6. Functional diagram

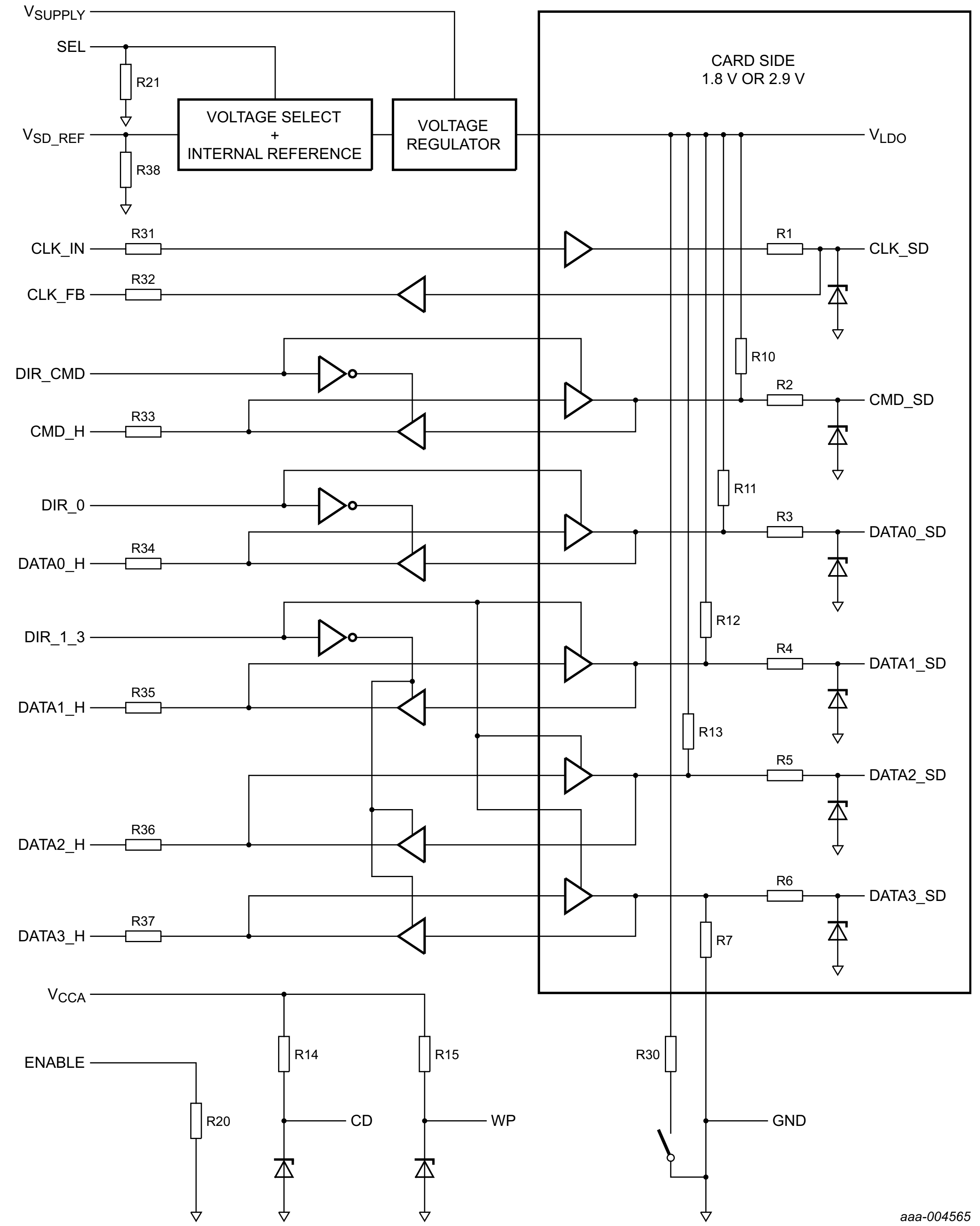


Fig 2. Functional diagram

7. Pinning information

7.1 Pinning

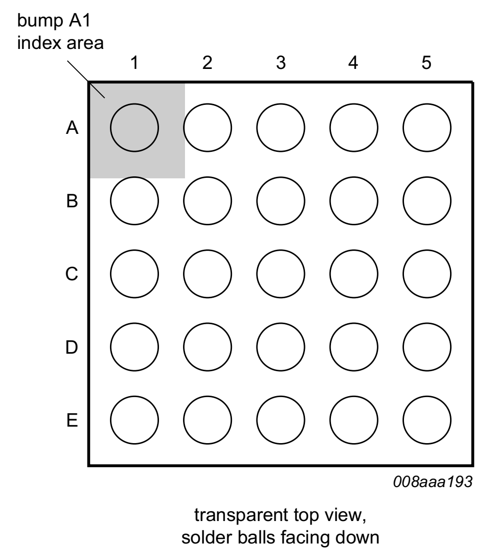


Fig 3. Pin configuration WLCSP25

Table 2. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
A1	DATA2_H	A2	DIR_CMD	A3	DIR_0	A4	V_{SUPPLY}	A5	DATA2_SD
B1	DATA3_H	B2	SEL	B3	V_{CCA}	B4	V_{LDO}	B5	DATA3_SD
C1	CLK_IN	C2	ENABLE	C3	GND	C4	V_{SD_REF}	C5	CLK_SD
D1	DATA0_H	D2	CMD_H	D3	CD	D4	CMD_SD	D5	DATA0_SD
E1	DATA1_H	E2	CLK_FB	E3	DIR_1_3	E4	WP	E5	DATA1_SD

7.2 Pin description

Table 3. Pin description

Symbol[1]	Pin	Type[2]	Description
DATA2_H	A1	I/O	data 2 input or output on host side
DIR_CMD	A2	I	direction control input for command
DIR_0	A3	I	direction control input for data 0
V_{SUPPLY}	A4	S	supply voltage (from battery or regulator)
DATA2_SD	A5	I/O	data 2 input or output on memory card side
DATA3_H	B1	I/O	data 3 input or output on host side
SEL	B2	I	card side I/O voltage level select
V_{CCA}	B3	S	supply voltage from host side
V_{LDO}	B4	O	internal supply decoupling; to be connected to C_{ext} (Figure 6)
DATA3_SD	B5	I/O	data 3 input or output on memory card side

Table 3. Pin description *...continued*

Symbol[1]	Pin	Type[2]	Description
CLK_IN	C1	I	clock signal input on host side
ENABLE	C2	I	device enable input
GND	C3	S	supply ground
V_{SD_REF}	C4	I	reference voltage for the internal voltage regulator
CLK_SD	C5	O	clock signal output on memory card side
DATA0_H	D1	I/O	data 0 input or output on host side
CMD_H	D2	I/O	command input or output on host side
CD	D3	O	card detect switch biasing output
CMD_SD	D4	I/O	command input or output on memory card side
DATA0_SD	D5	I/O	data 0 input or output on memory card side
DATA1_H	E1	I/O	data 1 input or output on host side
CLK_FB	E2	O	clock feedback output on host side
DIR_1_3	E3	I	direction control input for data 1, data 2, data 3
WP	E4	O	write protect switch biasing output
DATA1_SD	E5	I/O	data 1 input or output on memory card side

[1] The pin names relate particularly to SD memory cards, but also apply to microSD and MMC memory cards.

[2] I = input, O = output, I/O = input and output, S = power supply.

8. Functional description

8.1 Level translator

The bidirectional level translator shifts the data between the I/O supply levels of the host and the memory card. Dedicated direction control signals determine if a command and data signals are transferred from the memory card to the host (card read mode) or from the host to the memory card (card write mode). The voltage translator has to support several clock and data transfer rates at the signaling levels specified in the SD 3.0 standard specification.

Table 4. Supported modes

Bus speed mode	Signal level (V)	Clock rate (MHz)	Data rate (MB/s)
Default-speed	3.3	25	12.5
High-speed	3.3	50	25
SDR12	1.8	25	12.5
SDR25	1.8	50	25
SDR50	1.8	100	50
DDR50	1.8	50	50

8.2 Enable and direction control

The pin ENABLE enables/disables the internal Low DropOut (LDO) regulator and is used to put the host-side and card-side I/O drivers into high-ohmic (3-state) mode.

Table 5. I/O function control signal truth table

Control		Host side		Memory card side	
Pin	**Level[1]**	**Pin**	**Function**	**Pin**	**Function**
Pin ENABLE = HIGH and $V_{CCA} \geq 1.62$ V					
DIR_CMD	H	CMD_H	input	CMD_SD	output
	L	CMD_H	output	CMD_SD	input
DIR_0	H	DATA0_H	input	DATA0_SD	output
	L	DATA0_H	output	DATA0_SD	input
DIR_1_3	H	DATA1_H DATA2_H DATA3_H	input	DATA1_SD DATA2_SD DATA3_SD	output
	L	DATA1_H DATA2_H DATA3_H	output	DATA1_SD DATA2_SD DATA3_SD	input
-	-	CLK_IN	input	CLK_SD	output
-	-	CLK_FB	output	-	-
Pin ENABLE = LOW or $V_{CCA} \leq 0.8$ V					
DIR_CMD	X	CMD_H	high-ohmic	CMD_SD	high-ohmic
DIR_0	X	DATA0_H	high-ohmic	DATA0_SD	high-ohmic
DIR_1_3	X	DATA1_H DATA2_H DATA3_H	high-ohmic	DATA1_SD DATA2_SD DATA3_SD	high-ohmic
-	-	CLK_IN	input	CLK_SD	high-ohmic
-	-	CLK_IN	high-ohmic	-	-

[1] H = HIGH; L = LOW; X = don't care.

8.3 Integrated voltage regulator

The low dropout voltage regulator delivers supply voltage for the voltage translators and the card-side input/output stages. It has to support 1.8 V and 3 V signaling modes as stipulated in the SD 3.0 specification. The switching time between the two output voltage modes is compliant with SD 3.0 specification. Depending on the signaling level at pin SEL, the regulator delivers 1.8 V (SEL = HIGH) or 2.9 V (SEL = LOW, $V_{SD\_REF} < 1$ V). For card supply voltage, see Section 8.4.

Table 6. SD card side voltage level control signal truth table

Input		Output		
SEL[1]	**V_{SD_REF}[1]**	**V_{LDO}**	**Pin[2]**	**Function**
H	X	1.8 V	DATA0_SD to DATA3_SD, CLK_SD	low supply voltage level (1.8 V typical)
L	< 1 V	2.9 V	DATA0_SD to DATA3_SD, CLK_SD	high supply voltage level (2.9 V typical)
	> 1.5 V	V_{SD_REF}	DATA0_SD to DATA3_SD, CLK_SD	supply voltage level based on V_{SD_REF}

[1] H = HIGH; L = LOW; X = don't care.

[2] Host-side pins are not influenced by SEL.

An external capacitor is needed between the regulator output pin V_{LDO} and ground for proper operation of the integrated voltage regulator. See Table 8 for recommended capacitance and equivalent series resistance. To place the capacitor close to the V_{LDO} pin and maintain short connections to both, to the V_{LDO} and to the ground, is recommended.

8.4 Memory card voltage tracking (reference select)

The device can track the memory card supply via pin V_{SD_REF}. This allows achieving optimum interoperability by perfectly matching input/output levels between voltage translator and memory card in the 3 V signaling mode. Therefore, the voltage regulator aims to follow the reference voltage provided at input V_{SD_REF} directly. If tracking of the memory card supply is not desired, connect pin V_{SD_REF} to ground so the voltage regulator refers to an integrated voltage reference. For 1.8 V (SEL = HIGH) signaling, the voltage regulator is referred to the internal reference which is independent of the voltage at V_{SD_REF}.

8.5 Feedback clock channel

The clock is transmitted from the host to the memory card side. The voltage translator and the Printed-Circuit Board (PCB) tracks introduce some amount of delay. It reduces timing margin for data read back from memory card, especially at higher data rates. Therefore, a feedback path is provided to compensate the delay. The reasoning behind this approach is the fact that the clock is always delivered by the host, while the data in the timing critical read mode comes from the card.

8.6 EMI filter

All input/output driver stages are equipped with EMI filters to reduce interferences towards sensitive mobile communication.

8.7 ESD protection

The device has robust ESD protections on all memory card pins as well as on the V_{SD_REF} and V_{SUPPLY} pins. The architecture prevents any stress for the host: the voltage translator discharges any stress to supply ground.

Pins Write Protect (WP) and Card Detection (CD) might be pulled down by the memory card which has to be detected by the host. Both signals must be HIGH if no card is inserted. Therefore the pins are equipped with International Electrotechnical Commission (IEC) system-level ESD protections and pull-up resistors connected to the host supply V_{CCA}.

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	4 ms transient			
		on pin V_{SUPPLY}	−0.5	+6.0	V
		on pin V_{CCA}	−0.5	+4.6	V
V_I	input voltage	4 ms transient at I/O pins	−0.5	+4.6	V
P_{tot}	total power dissipation	T_{amb} = −40 °C to +85 °C	-	1000	mW
T_{stg}	storage temperature		−55	+150	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4, all memory card-side pins, V_{SUPPLY}, V_{SD_REF}, WP and CD to ground [1]			
		contact discharge	−8	+8	kV
		air discharge	−15	+15	kV
		Human Body Model (HBM) JEDEC JESD22-A114F; all pins	−2000	+2000	V
		Machine Model (MM) JEDEC JESD22-A115; all pins	−200	+200	V
$I_{lu(IO)}$	input/output latch-up current	JESD78B: −0.5 × V_{CC} < V_I < 1.5 × V_{CC}; T_j < 125 °C	−100	+100	mA

[1] All system level tests are performed with the application-specific capacitors connected to the supply pins V_{SUPPLY}, V_{LDO} and V_{CCA}.

10. Recommended operating conditions

Table 8. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	on pin V_{SUPPLY} [1]	2.5	-	5.5	V
		on pin V_{CCA}	1.1	-	3.6	V
V_I	input voltage	host side [2]	−0.3	-	V_{CCA} + 0.3	V
		memory card side	−0.3	-	$V_{O(reg)}$ + 0.3	V
C_{ext}	external capacitance	recommended capacitor at pin V_{LDO}	-	1.0	-	μF
ESR	equivalent series resistance	at pin V_{LDO}	0	-	50	mΩ
C_{ext}	external capacitance	recommended capacitor at pin V_{SUPPLY}	-	0.1	-	μF
		recommended capacitor at pin V_{CCA}	-	0.1	-	μF

[1] By minimum value the device is still fully functional, but the voltage on pin V_{LDO} might drop below the recommended memory card supply voltage.

[2] The voltage must not exceed 3.6 V.

Table 9. Integrated resistors

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{pd}	pull-down resistance	R7	272	470	668	kΩ
		R30	70	100	130	Ω
		R20; R21; R38	200	350	500	kΩ
R_{pu}	pull-up resistance	R10	10.5	15	19.5	kΩ
		R11 to R13	49	70	91	kΩ
		R14 and R15	70	100	130	kΩ
R_s	series resistance	card side; R1 to R6 [1]	32	40	48	Ω
		host side; R31 to R37 [1]	26	33	40	Ω

[1] Guaranteed by design and characterization.

11. Static characteristics

Table 10. Static characteristics

At recommended operating conditions; T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 1 μF at pin V_{LDO}; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Supply voltage regulator for card-side I/O pin: V_{LDO}						
$V_{O(reg)}$	regulator output voltage	SEL = LOW; V_{SD_REF} < 1 V; $V_{SUPPLY} \geq$ 2.9 V	2.7	2.9	3.3	V
		SEL = LOW; V_{SD_REF} > 1.5 V; $V_{SUPPLY} \geq V_{SD\_REF}$	V_{SD_REF} − 0.15	V_{SD_REF}	V_{SD_REF} + 0.15	V
		SEL = HIGH; $V_{SUPPLY} \geq$ 2.5 V	1.7	1.85	2.0	V
$V_{do(reg)}$	regulator dropout voltage	SEL = LOW; $V_{SUPPLY} \leq$ 2.9 V; I_O = 50 mA	-	-	150	mV
$I_{O(reg)}$	regulator output current		-	-	50	mA
Host-side input signals: CMD_H, DATA0_H to DATA3_H and CLK_IN						
V_{IH}	HIGH-level input voltage		0.625 × V_{CCA}	-	V_{CCA} + 0.3	V
V_{IL}	LOW-level input voltage		−0.3	-	0.35 × V_{CCA}	V
I_{LI}	input leakage current	V_{CCA} = 1.8 V; ENABLE = LOW [2]	-	-	1.0	nA
Host-side control signals						
SEL, ENABLE, DIR_0, DIR_1_3 and DIR_CMD						
V_{IH}	HIGH-level input voltage		0.625 × V_{CCA}	-	V_{CCA} + 0.30	V
V_{IL}	LOW-level input voltage		−0.3	-	0.35 × V_{CCA}	V
V_{SD_REF}						
V_{IH}	HIGH-level input voltage		1.50	-	3.63	V
V_{IL}	LOW-level input voltage		−0.3	-	+1.0	V

Table 10. Static characteristics *…continued*

At recommended operating conditions; T_{amb} = –40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); C_{ext} = 1 μF at pin V_{LDO}; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
Host-side output signals: CLK_FB, CMD_H and DATA0_H to DATA3_H						
V_{OH}	HIGH-level output voltage	I_O = 2 mA; V_I = V_{IH} (card side)	0.85 × V_{CCA}		-	V
V_{OL}	LOW-level output voltage	I_O = –2 mA; V_I = V_{IL} (card side)	-	-	0.125 × V_{CCA}	V
Card-side input signals: CMD_SD and DATA0_SD to DATA3_SD						
V_{IH}	HIGH-level input voltage	SEL = LOW (2.9 V interface)	0.625 × $V_{O(reg)}$	-	$V_{O(reg)}$ + 0.3	V
		SEL = HIGH (1.8 V interface)	0.625 × $V_{O(reg)}$	-	$V_{O(reg)}$ + 0.3	V
V_{IL}	LOW-level input voltage	SEL = LOW (2.9 V interface)	–0.3	-	0.35 × $V_{O(reg)}$	V
		SEL = HIGH (1.8 V interface)	–0.3	-	0.35 × $V_{O(reg)}$	V
Card-side output signal						
CMD_SD, DATA0_SD to DATA3_SD and CLK_SD						
V_{OH}	HIGH-level output voltage	I_O = 4 mA; V_I = V_{IH} (host side); SEL = LOW (2.9 V interface)	0.85 × $V_{O(reg)}$	-	$V_{O(reg)}$ + 0.3	V
		I_O = 2 mA; V_I = V_{IH} (host side); SEL = HIGH (1.8 V interface)	0.85 × $V_{O(reg)}$	-	2.0	V
V_{OL}	LOW-level output voltage	I_O = –4 mA; V_I = V_{IL} (host side); SEL = LOW (2.9 V interface)	–0.3	-	0.125 × $V_{O(reg)}$	V
		I_O = –2 mA; V_I = V_{IL} (host side); SEL = HIGH (1.8 V interface)	–0.3	-	0.125 × $V_{O(reg)}$	V
Bus signal equivalent capacitance						
C_{ch}	channel capacitance	V_I = 0 V; f_i = 1 MHz; V_{SUPPLY} = 3.5 V; V_{CCA} = 1.8 V [3]				
		host side	-	3.5	5.0	pF
		card side	-	5.0	10.0	pF
Current consumption						
$I_{CC(stat)}$	static supply current	ENABLE = HIGH (active mode); all inputs = HIGH; DIR = LOW				
		SEL = LOW (2.9 V interface)	-	-	100	μA
		SEL = HIGH (1.8 V interface)	-	-	100	μA
$I_{CC(stb)}$	standby supply current	ENABLE = LOW (inactive mode)	-	-	1	μA

[1] Typical values are measured at T_{amb} = 25 °C.

[2] Guaranteed by design and characterization.

[3] EMI filter line capacitance per data channel from I/O driver to pin; C_{ch} is guaranteed by design.

12. Dynamic characteristics

12.1 Voltage regulator

Table 11. Voltage regulator
T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage regulator output pin: V_{LDO}						
$t_{startup(reg)}$	regulator start-up time	V_{CCA} = 1.8 V; V_{SUPPLY} = 3.5 V; C_{ext} = 1 μF; see Figure 5	-	-	100	μs
$t_{f(o)}$	output fall time	$V_{O(reg)}$ = 2.9 V to 1.8 V; SEL = LOW to HIGH; see Figure 4	-	-	1	ms
$t_{r(o)}$	output rise time	$V_{O(reg)}$ = 1.8 V to 2.9 V; SEL = HIGH to LOW; see Figure 4	-	-	100	μs

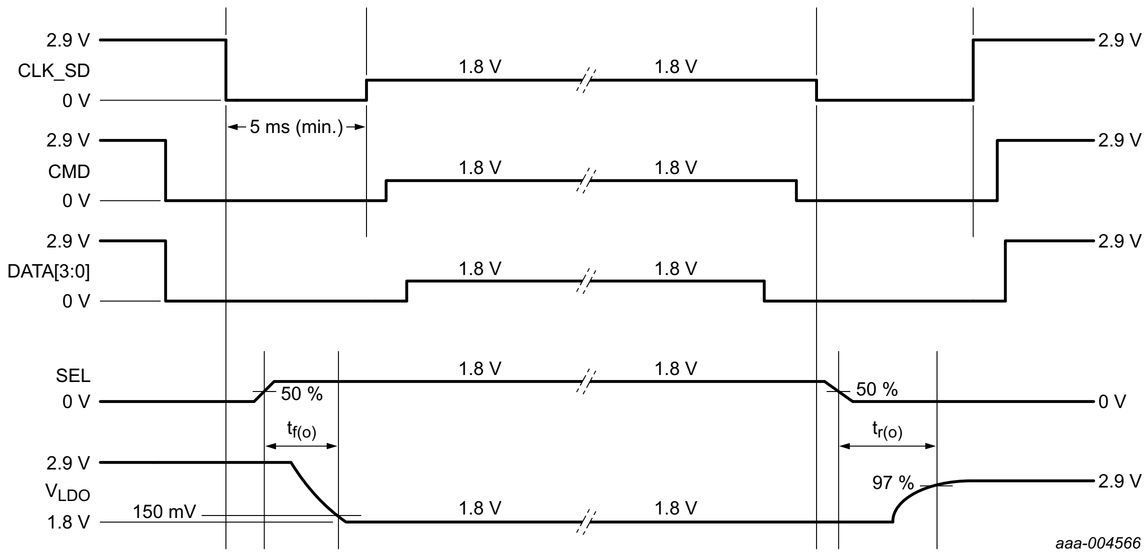
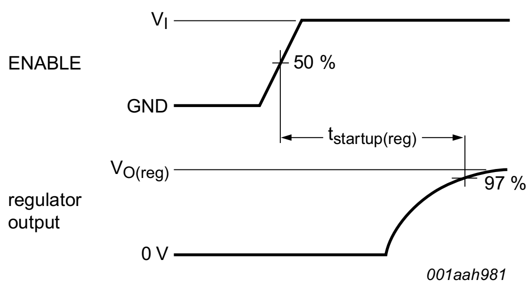


Fig 4. Regulator mode change timing



Measuring points: ENABLE signal at 0.5 V_{CCA} and regulator output signal at 0.97 $V_{O(reg)}$.

Fig 5. Regulator start-up time

12.2 ESD characteristic of pin write protect and card detect

Table 12. ESD characteristic of write protect and card detect

At recommended operating conditions; T_{amb} = 25 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ESD protection pins: WP and CD							
V_{BR}	breakdown voltage	TLP; I = 1 mA		-	8	-	V
r_{dyn}	dynamic resistance	positive transient	[1]	-	0.5	-	Ω
		negative transient	[1]	-	0.5	-	Ω

[1] TLP according to ANSI-ESD STM5.5.1/IEC 62615 Z_o = 50 Ω; pulse width = 100 ns; rise time = 200 ps; averaging window = 50 ns to 80 ns.

13. Application information

The IP4855CX25 is optimized to connect SD 3.0 and SD 2.0 compatible memory cards to 1.8 V base band/host interfaces. While the internal I/O interface towards the memory card is supplied by the IP4855CX25 integrated voltage regulator, any connected memory card has to be supplied from an external source. Using for example DDR50 or SDR50 modes requires a power supply with up to 400 mA DC current capabilities.

Place IP4855CX25 as close as possible to the card holder to minimize the influence of trace length on the timing values. The trace length between IP4855CX25 and the card has a much bigger influence on the timing than the identical length between the host interface and the IP4855CX25.

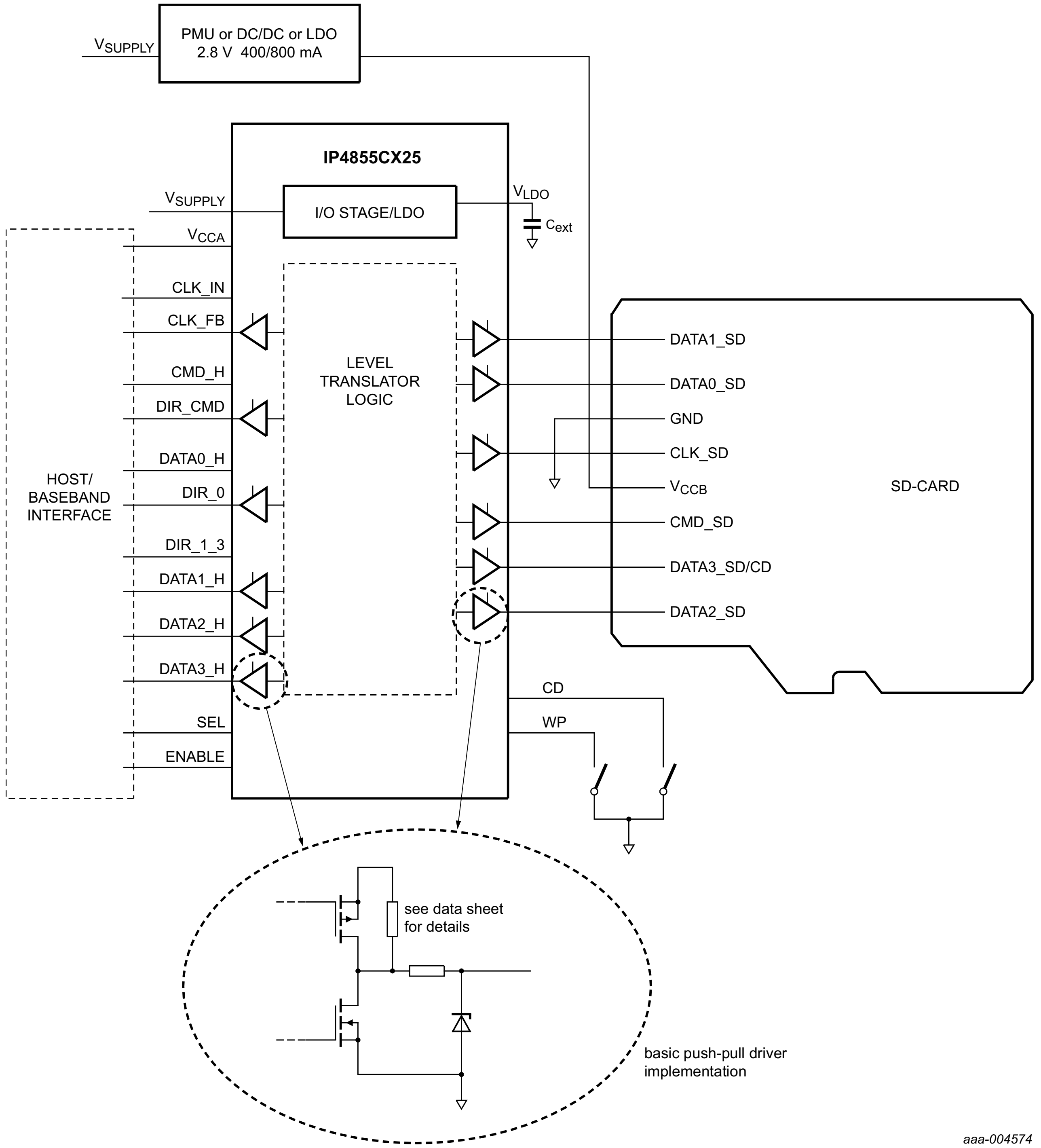
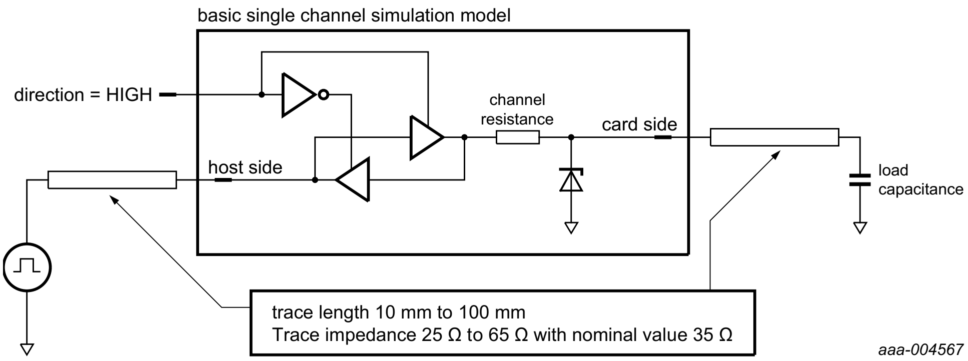


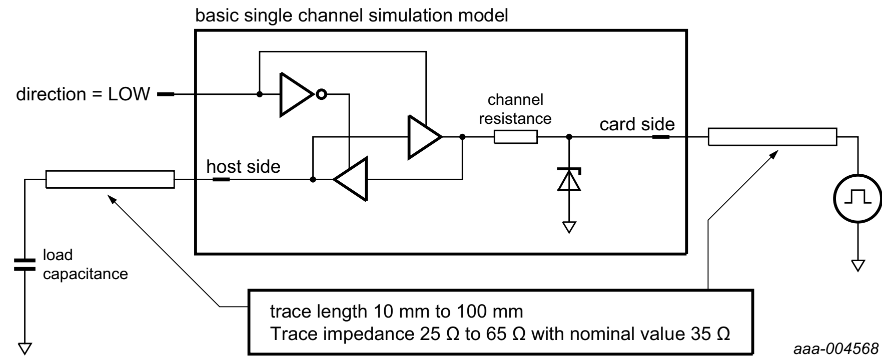
Fig 6. IP4855CX25 application diagram and output driver structure

One main task of the level translator is to shift the signal within the SD 3.0 specification. Therefore, the following simulation results show the low impact of the device. Use the clock feedback channel for a compensation of delay introduced by PCB traces and IP4855CX25.

13.1 Simulation setup for transition time, propagation delay and setup/hold times



a. Host-side to card-side simulation setup



b. Card-side to host-side simulation setup

Fig 7. Timing simulation setup

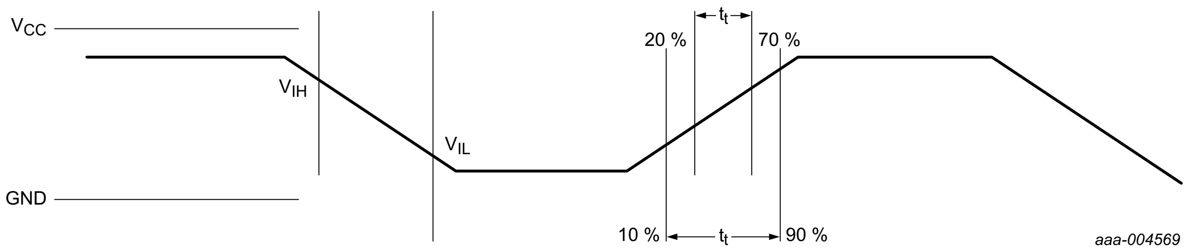


Fig 8. Output rise and fall times

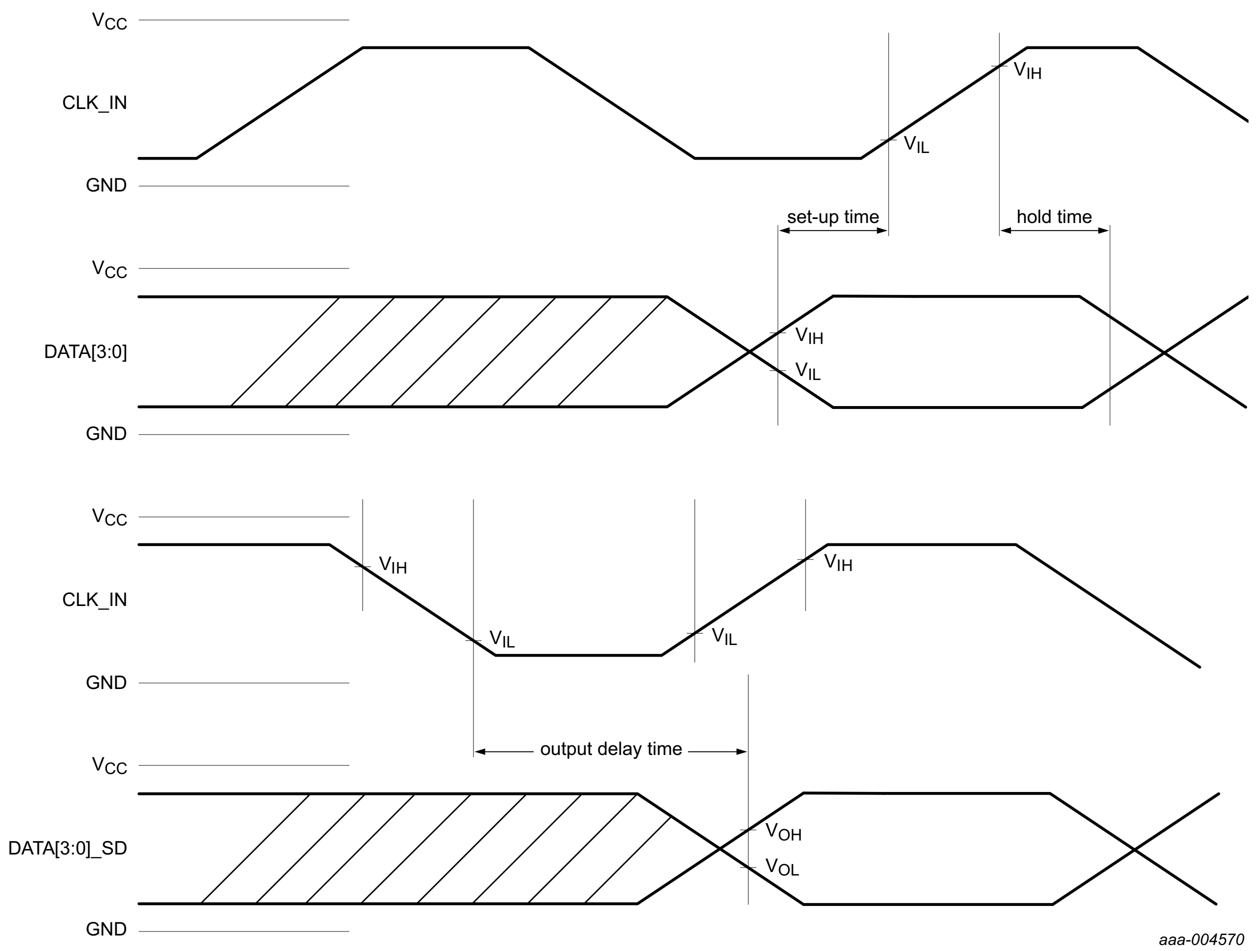


Fig 9. Setup, hold and output delay timing

13.2 Interface voltage timing data

Table 13. Output rise and fall times card side

V_{SUPPLY} = 4 V; track impedance 35 Ω; track length (to and from IP4855CX25) 15 mm; R_{source} = 50 Ω; see Figure 7 for setup circuit and Figure 8 for timing diagram; V_{CCA} = 1.8 V; transition time is the same as output rise time and output fall time; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Memory card-side output pins: CLK_SD, CMD_SD and DATA0_SD to DATA3_SD; 2.9 V mode (SEL = LOW)						
Reference points at 20 % and 70 %						
t_t	transition time	C_L = 10 pF				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 2.9 V	0.8	1.1	1.3	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 3.6 V	0.8	1.0	1.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 2.7 V	0.8	1.1	1.3	ns
		C_L = 20 pF [1]				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 2.9 V	1.4	1.6	1.9	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 3.6 V	1.3	1.6	1.8	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 2.7 V	1.4	1.6	1.9	ns
Reference points at 10 % and 90 % [2]						
t_t	transition time	C_L = 10 pF				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 2.9 V	1.9	2.1	2.4	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 3.6 V	1.9	2.0	2.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 2.7 V	2.0	2.2	2.4	ns
		C_L = 20 pF [1]				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 2.9 V	2.9	3.1	3.4	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 3.6 V	2.9	3.0	3.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 2.7 V	2.9	3.2	3.5	ns
Memory card-side output pins: CLK_SD, CMD_SD and DATA0_SD to DATA3_SD; 1.8 V mode (SEL = HIGH)						
Reference points at 20 % and 70 %						
t_t	transition time	C_L = 10 pF				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 1.8 V	0.8	1.1	1.3	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 1.95 V	0.8	1.0	1.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 1.7 V	0.8	1.1	1.3	ns
		C_L = 20 pF [1]				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 1.8 V	1.4	1.6	1.9	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 1.95 V	1.3	1.6	1.8	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 1.7 V	1.4	1.6	1.9	ns
Reference points at 10 % and 90 % [2]						
t_t	transition time	C_L = 10 pF				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 1.8 V	1.9	2.1	2.4	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 1.95 V	1.9	2.0	2.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 1.7 V	2.0	2.2	2.4	ns

Table 13. Output rise and fall times card side *...continued*

V_{SUPPLY} = 4 V; track impedance 35 Ω; track length (to and from IP4855CX25) 15 mm; R_{source} = 50 Ω; see Figure 7 for setup circuit and Figure 8 for timing diagram; V_{CCA} = 1.8 V; transition time is the same as output rise time and output fall time; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_t	transition time	C_L = 20 pF [1]				
		nominal case; T_{amb} = +25 °C; V_{LDO} = 1.8 V	2.9	3.1	3.4	ns
		best case; T_{amb} = −40 °C; V_{LDO} = 1.95 V	2.9	3.0	3.2	ns
		worst case; T_{amb} = +85 °C; V_{LDO} = 1.7 V	2.9	3.2	3.5	ns

[1] A capacitive load of C_L = 20 pF is out of the range of allowed SD card interface parasitic capacitance.

[2] Reference points 90 % and 10 % are not required according to the SD 3.0 specification.

Table 14. Output rise and fall times host side

V_{SUPPLY} = 4.0 V; SEL = LOW; $V_{O(reg)}$ = 2.9 V; track impedance 35 Ω; track length (to and from IP4855CX25) 15 mm; R_{source} = 50 Ω; see Figure 7 for setup circuit and Figure 8 timing diagram; transition time is the same as output rise time and output fall time; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Host-side output pins: CLK_FB, CMD_H and DATA0_H to DATA3_H (3.3 V host)						
Reference points at 20 % and 70 %						
t_t	transition time	C_L = 5 pF				
		nominal case; T_{amb} = +25 °C; V_{CCA} = 3.3 V	0.5	0.6	0.7	ns
		best case; T_{amb} = −40 °C; V_{CCA} = 3.6 V	0.5	0.6	0.7	ns
		worst case; T_{amb} = +85 °C; V_{CCA} = 2.7 V	0.5	0.6	0.7	ns
Reference points at 10 % and 90 %[1]						
t_t	transition time	C_L = 5 pF				
		nominal case; T_{amb} = +25 °C; V_{CCA} = 3.3 V	1.0	1.3	1.5	ns
		best case; T_{amb} = −40 °C; V_{CCA} = 3.6 V	1.0	1.2	1.4	ns
		worst case; T_{amb} = +85 °C; V_{CCA} = 2.7 V	1.3	1.4	1.6	ns
Host-side output pins: CLK_FB, CMD_H and DATA0_H to DATA3_H (1.8 V host)						
Reference points at 20 % and 70 %						
t_t	transition time	C_L = 5 pF				
		nominal case; T_{amb} = +25 °C; V_{CCA} = 1.8 V	0.5	0.6	0.7	ns
		best case; T_{amb} = −40 °C; V_{CCA} = 1.9 V	0.5	0.6	0.7	ns
		worst case; T_{amb} = +85 °C; V_{CCA} = 1.62 V	0.5	0.6	0.7	ns
Reference points at 10 % and 90 %[1]						
t_t	transition time	C_L = 5 pF				
		nominal case; T_{amb} = +25 °C; V_{CCA} = 1.8 V	1.0	1.3	1.5	ns
		best case; T_{amb} = −40 °C; V_{CCA} = 1.9 V	1.0	1.2	1.4	ns
		worst case; T_{amb} = +85 °C; V_{CCA} = 1.62 V	1.3	1.4	1.6	ns

[1] Reference points 90 % and 10 % are not required according to the SD 3.0 specification.

13.3 DDR50 mode timing details

The Default-Speed (DS) and High-Speed (HS) modes use 3.3 V signaling and offer a maximum of 25 MB/s. Besides these modes, IP4855CX25 also supports the SDR12, SDR25 and DDR50 modes using 1.8 V signaling and up to 50 MB/s.

Especially the DDR50 mode introduces a basic change in the timing behavior of the SD card interface. The SDR12 and SDR50 modes are similar to the DS and HS modes.

Any delay on all relevant signal lines (as shown in the timing diagram in Figure 10) is uncritical for SD card write operations as long as the skew between the different signals is small enough.

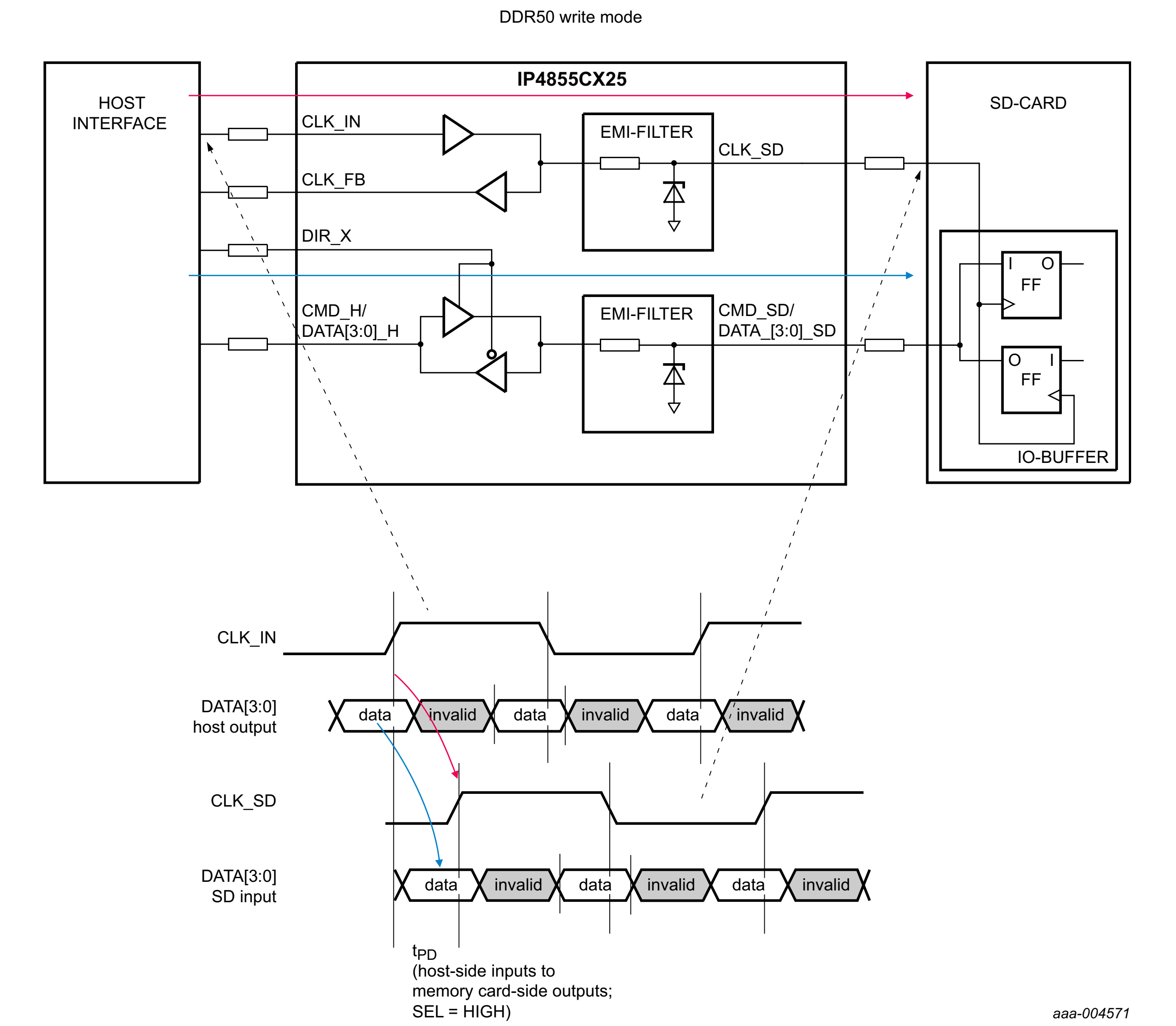


Fig 10. DDR50 write timing diagram

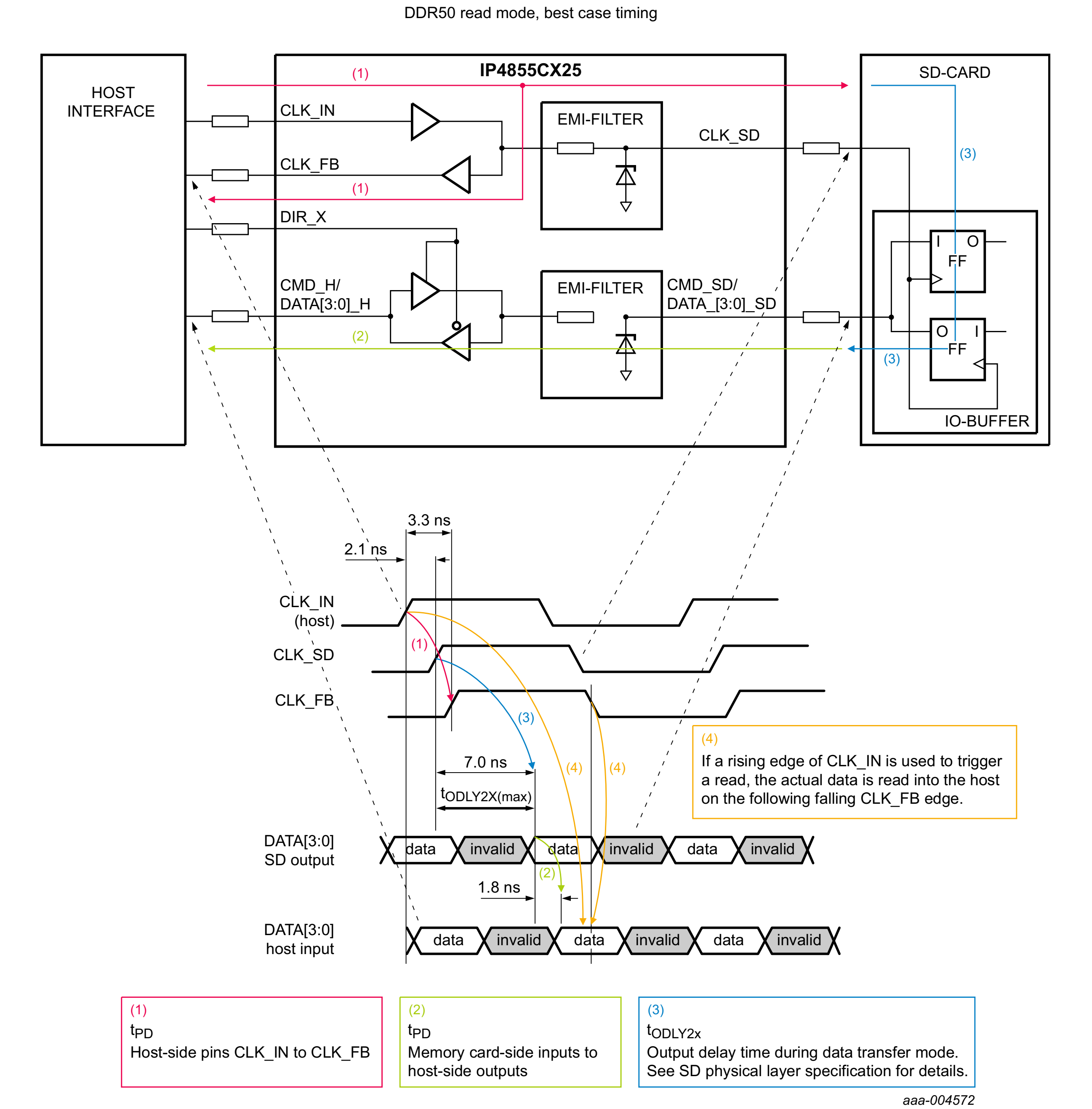
In contrast to the write cycle, the read cycle is more complex to analyze and depends on the IP4855CX25 delay, the maximum delay added by the PCB and the additional setup time of the SD card.

Table 15. DDR50 read mode: parameters for best case and worst case timings

Parameter	Best case timing (Figure 11)	Worst case timing (Figure 12)
PCB output impedance Z_o	65 Ω	25 Ω
Symmetrical trace length	15 mm per side	100 mm per side
t_{PD}	minimum	maximum
Driver model	fast	slow

The same mechanism is triggered on each falling clock edge too, as the DDR50 mode uses both edges of the clock signal for data transfer.

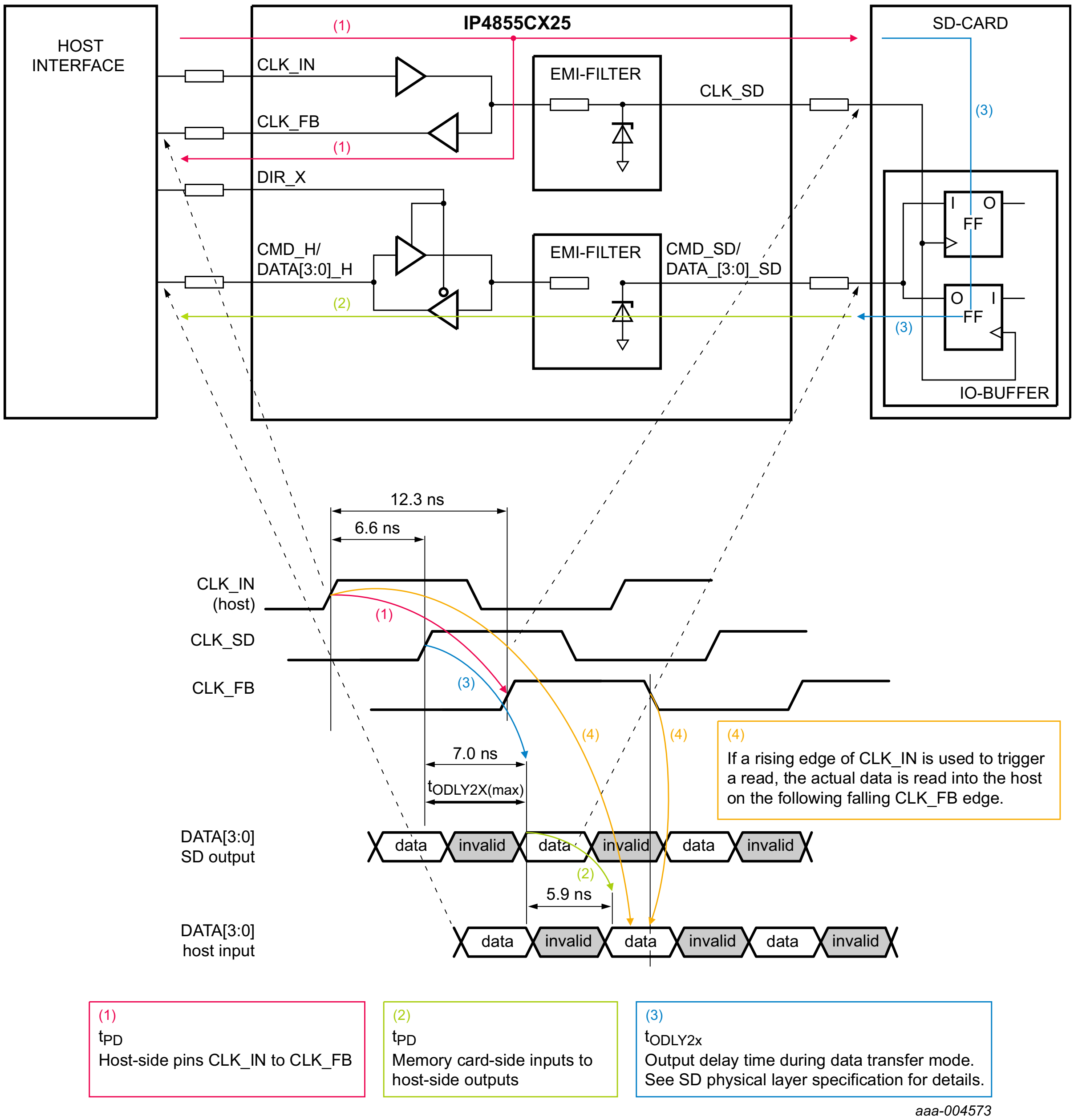
According to the SD 3.01 physical layer specification, the maximum delay between CLK_IN (CLK_SD signal) at the SD card and data out from the SD card (DATA[3:0]_SD out) is 7.0 ns. This value is specified for a load of $C_L \leq 25$ pF.



PCB Z_0 = 65 Ω, trace length = 15 mm, t_{PD} = minimum, fast driver model

Fig 11. Detailed description of a DDR50 read cycle, best case timing

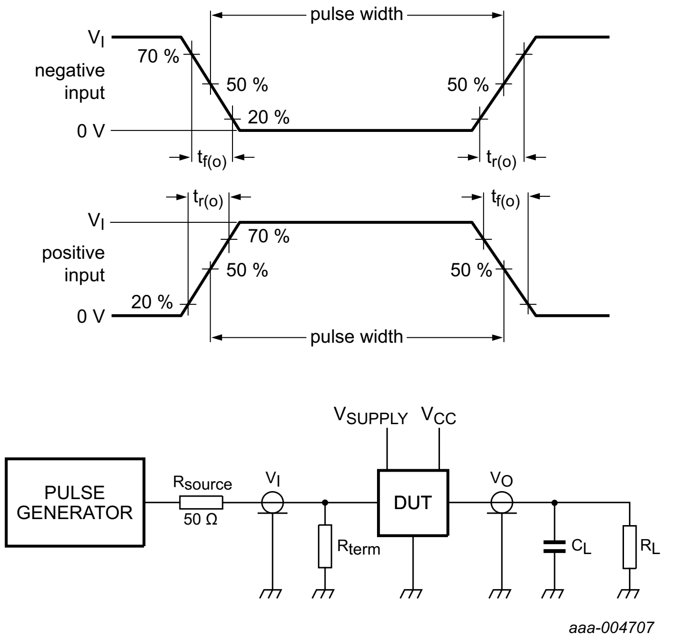
DDR50 read mode, worst case timing



PCB Z_0 = 25 Ω, trace length = 100 mm, t_{PD} = maximum, slow driver model

Fig 12. Detailed description of a DDR50 read cycle, worst case timing

14. Test information



Definitions test circuit:

R_{source} = source resistance of pulse generator.

R_{term} = termination resistance should be equal to output impedance Z_o of pulse generator.

C_L = load capacitance including jig and probe capacitance.

R_L = load resistance.

Fig 13. Load circuitry for measuring switching time

15. Package outline

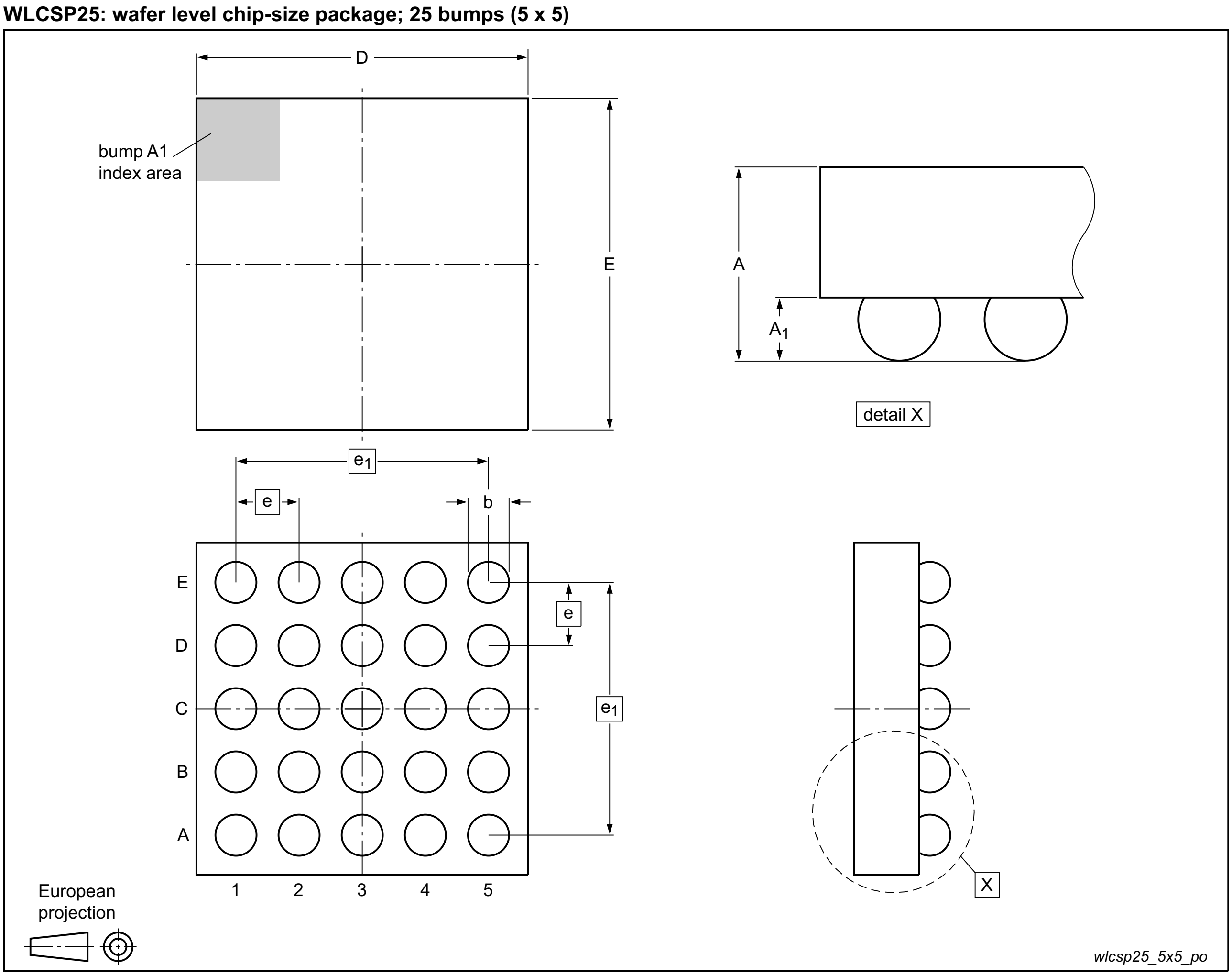


Fig 14. Package outline IP4855CX25 (WLCSP25)

Table 16. Dimensions for Figure 14

Symbol	Min	Typ	Max	Unit
A	0.44	0.47	0.50	mm
A_1	0.18	0.20	0.22	mm
b	0.23	0.25	0.27	mm
D	2.01	2.05	2.09	mm
E	2.01	2.05	2.09	mm
e	-	0.4	-	mm
e_1	-	1.6	-	mm

WLCSP25: wafer level chip-size package with back side coating; 25 bumps (5 x 5)

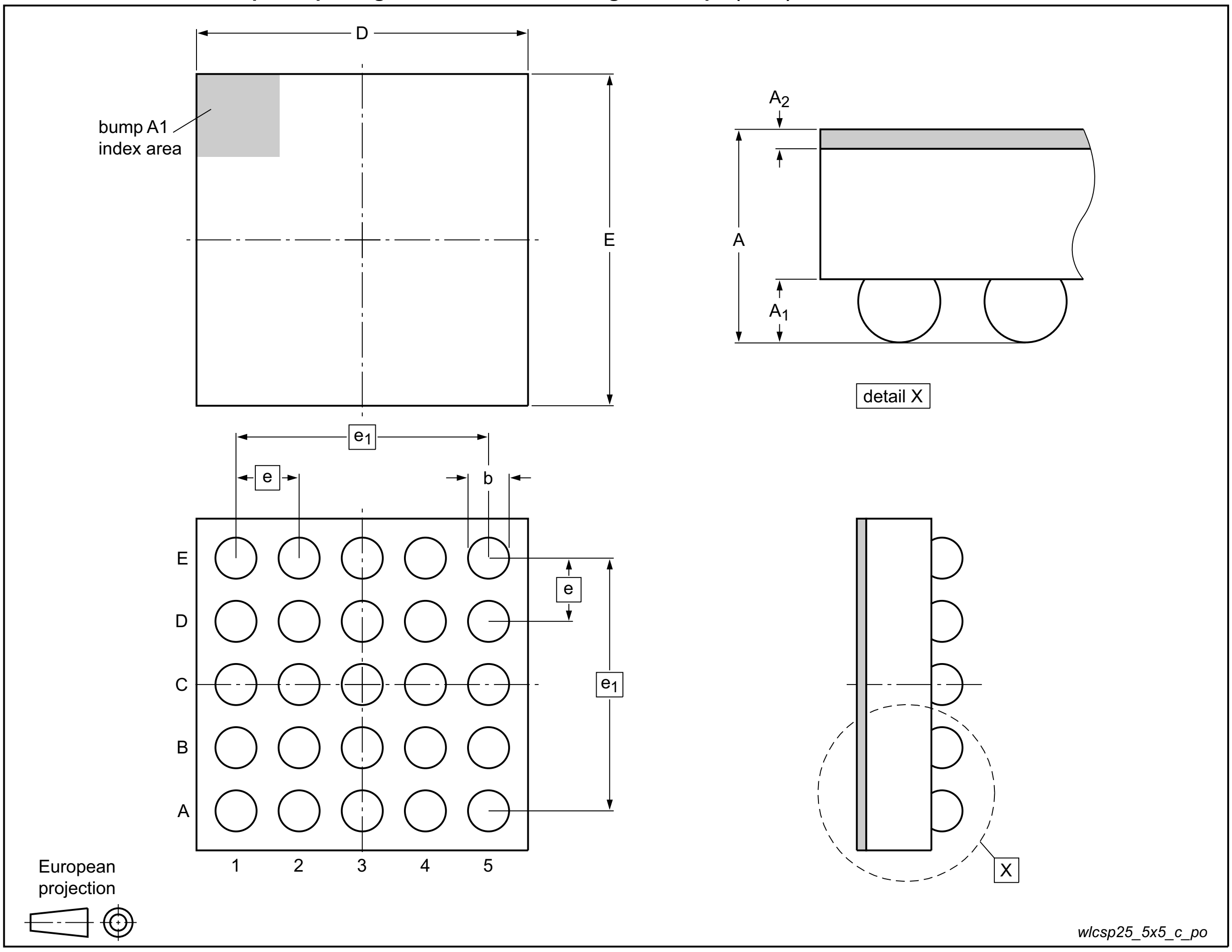


Fig 15. Package outline IP4855CX25/C (WLCSP25 with back side coating)

Table 17. Dimensions for Figure 15

Symbol	Min	Typ	Max	Unit
A	0.47	0.51	0.55	mm
A_1	0.18	0.20	0.22	mm
A_2	0.03	0.04	0.05	mm
b	0.23	0.25	0.27	mm
D	2.01	2.05	2.09	mm
E	2.01	2.05	2.09	mm
e	-	0.4	-	mm
e_1	-	1.6	-	mm

16. Design and assembly recommendations

16.1 PCB design guidelines

For optimum performance, use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 18 for the recommended PCB design parameters.

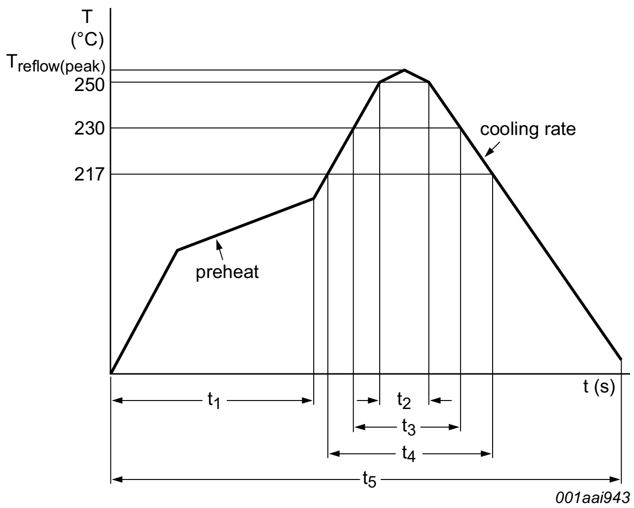
Table 18. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	250 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	325 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi or OSP
PCB material	FR4

16.2 PCB assembly guidelines for Pb-free soldering

Table 19. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	290 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder to flux ratio	50 : 50
Solder reflow profile	see Figure 16



The device can withstand at least three reflows with this profile.

Fig 16. Pb-free solder reflow profile

Table 20. Reflow soldering process characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		preheat	2.5	-	4.0	°C/s

17. Abbreviations

Table 21. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
MMC	MultiMedia Card
NSMD	Non-Solder Mask PCB Design
OSP	Organic Solderability Preservation
PCB	Printed-Circuit Board
RoHS	Restriction of Hazardous Substances
SD	Secure Digital
WLCSP	Wafer-Level Chip-Scale Package

18. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4855CX25 v.4	20140602	Preliminary data sheet	-	IP4855CX25 v.3
Modifications:	• Table 9: pull-down resistance R7 changed; revised conditions			
IP4855CX25 v.3	20140513	Preliminary data sheet	-	IP4855CX25 v.2
IP4855CX25 v.2	20130524	Product data sheet	-	IP4855CX25 v.1
IP4855CX25 v.1	20120913	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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