ES_LPC11E1x

Errata sheet LPC11E1x

Rev. 2 — 1 February 2013 **Errata sheet**

Document information

Info	Content
Keywords	LPC11E11FHN33, LPC11E12FBD48, LPC11E13FBD48, LPC11E14FHN33, LPC11E14FBD48, LPC11E14FBD64, LPC11E1x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
2	20130201	• Added I2C.1.
1.1	20121130	• Added Note.2.
1	20120119	• Initial version.

Contact information

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1. Product identification

The LPC11E1x devices typically have the following top-side marking:

LPC11E1x

/xxx

xxxxxxx

xxYYWWxR[x]

The last letter in the last line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC11E1x:

Table 1. Device revision table

Revision identifier (R)	Revision description
'B'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

2. Errata overview

Table 2. Errata summary table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	A/D Global Data register should not be used with burst mode or hardware triggering.	'B'	Section 3.1
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'B'	Section 3.2

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'B'	Section 5.1
Note.2	For LPC11E14/401 devices with date codes 1238 and before, the 2 kB SRAM located at address 0x20000000-0x20000800 is not available.	'B'	Section 5.2

3. Functional problems detail

3.1 ADC.1: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC11E1x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.2 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I2C bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I2C bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the VDD level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the VDD supply ramps up.

5.2 Note.2

For LPC11E14/401 devices with date codes 1238 and before, the 2 kB SRAM located at address 0x20000000-0x20000800 is not available.

The 2 kB SRAM (0x20000000-0x20000800) is available for LPC11E14/401 devices with date codes 1239 and later.

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