ES_LPC176x

Errata sheet LPC1769/68/67/66/65/64/63

Rev. 10.3 — 2 June 2016 **Errata sheet**

Document information

Info	Content
Keywords	LPC1769FBD100; LPC1768FBD100; LPC1768FET100; LPC1768UK; LPC1767FBD100; LPC1766FBD100; LPC1765FBD100; LPC1765FET100; LPC1764FBD100; LPC1763FBD100, LPC176x errata
Abstract	This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document. Each deviation is assigned a number and its history is tracked in a table.

Revision history

Rev	Date	Description
10.3	20160602	• Added ADC.3. • Removed Rev ‘B’.
10.2	20150219	• Added Ibat.1
10.1	20140401	• Added LPC1768UK.
10	20130917	• Added Rev ‘B’. • Added I2C.1.
9.2	20120503	• Added Note.2.
9.1	20120117	• Added ADC.2, GPIO.1 and GPIO.2.
9	20110601	• Added USB.1.
8	20110322	• Combined LPC1769/68/67/66/65/64/63 errata into one document. • Added errata Note.1.
7	20110208	• Added Rev. A.
6	20110113	• Added ADC.1 and PWM.1.
5	20100719	• Added $V_{DD(REG)(3V3)}$.1.
4	20100701	• Added RTC.1.
3	20100604	• Removed Ethernet.1; LPC1765 does not have Ethernet feature.
2	20100316	• The format of this errata sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Added I2S.1 and Ethernet.1
1	20091014	• Added MCPWM.1

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1. Product identification

The LPC176x devices typically have the following top-side marking:

LPC176xxxx

xxxxxxx

xxYYWWR[x]

The last/second to last letter in the third line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC176x:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘-’	Initial device revision
‘A’	Second device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

2. Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
ADC.1	Internal sync inputs not operational.	'-', 'A'	Section 3.1
ADC.2	A/D Global Data register should not be used with burst mode or hardware triggering.	'-', 'A'	Section 3.2
ADC.3	Noise caused by nearby I/O pin switching activity or board design/layout could cause the ADC conversion results to be above the expected range.	'-', 'A'	Section 3.3
Ethernet.1[1]	Ethernet TxConsumeIndex register does not update correctly after the first frame is sent.	'-', 'A'	Section 3.4
GPIO.1	Open drain mode cannot be selected when port pin is configured as a non GPIO function.	'-', 'A'	Section 3.5
GPIO.2	Open drain mode is not functional on port pin P4.29.	'-', 'A'	Section 3.6
I2C.1	In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register.	'-', 'A'	Section 3.7
I2S.1[2]	XY divider will not work for PCLK-I2S higher than 74 MHz.	'-', 'A'	Section 3.8
IBAT.1	Typical lots have about 5 % parts with higher than normal I_{BAT} current when only V_{BAT} power is provided (VDD_{REG} is grounded).	'-', 'A'	Section 3.9
MCPWM.1	Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional.	'-'	Section 3.10
PCLKSELx.1	Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.	'-', 'A'	Section 3.11
PLL0.1	PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes.	'-', 'A'	Section 3.12
PWM.1	When updating the duty cycle for PWM1.1 from 100 %, in some cases the output can stay low for a full PWM period before the update takes effect.	'-', 'A'	Section 3.13
RTC.1	The Real Time Clock (RTC) does not work reliably within the temperature specification.	'-'	Section 3.14
USB.1[3]	USB host controller hangs on a dribble bit.	'-', 'A'	Section 3.15
$V_{DD(REG)(3V3)}$.1	The minimum regulator supply voltage is 3.0 V for the temperature range −40 °C to 85 °C.	'-'	Section 3.16

[1] LPC1769/68/67/66/64 only.

[2] LPC1769/68/67/66/65/63 only.

[3] LPC1769/68/66/65 only.

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes table

Errata notes	Short description	Revision identifier	Detailed description
Note.1[1]	On the LPC176x, for USB operation, the supply voltage ($V_{DD(3V3)}$) range must be 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.	'-', 'A'	Section 5.1
Note.2	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.	'-', 'A'	Section 5.2

[1] LPC1769/68/66/65/64 only.

3. Functional problems detail

3.1 ADC.1: External sync inputs not operational

Introduction:

In software-controlled mode (BURST bit is 0), the 10-bit ADC can start conversion by using the following options in the A/D Control Register:

26:24	START		When the BURST bit is 0, these bits control whether and when an A/D conversion is started:	0
		000	No start (this value should be used when clearing PDN to 0).	
		001	Start conversion now.	
		010	Start conversion when the edge selected by bit 27 occurs on the P2.10 / EINT0 / NMI pin.	
		011	Start conversion when the edge selected by bit 27 occurs on the P1.27 / CLKOUT / USB_OVRCRn / CAP0.1 pin.	
		100	Start conversion when the edge selected by bit 27 occurs on MAT0.1. Note that this does not require that the MAT0.1 function appear on a device pin.	
		101	Start conversion when the edge selected by bit 27 occurs on MAT0.3. Note that it is not possible to cause the MAT0.3 function to appear on a device pin.	
		110	Start conversion when the edge selected by bit 27 occurs on MAT1.0. Note that this does not require that the MAT1.0 function appear on a device pin.	
		111	Start conversion when the edge selected by bit 27 occurs on MAT1.1. Note that this does not require that the MAT1.1 function appear on a device pin.	

Fig 1. A/D control register options

Problem:

The external start conversion feature, AD0CR:START = 0x2 or 0x3, may not work reliably and ADC external trigger edges on P2.10 or P1.27 may be missed. The occurrence of this problem is peripheral clock (pclk) dependent. The probability of error (missing a ADC trigger from GPIO) is estimated as follows:

- For PCLK_ADC = 120 MHz, probability error = 12 %
- For PCLK_ADC = 50 MHz, probability error = 6 %
- For PCLK_ADC = 12 MHz, probability error = 1.5 %

The probability of error is not affected by the frequency of ADC start conversion edges.

Work-around:

In software-controlled mode (BURST bit is 0), the START conversion options (bits 26:24 set to 0x1 or 0x4 or 0x5 or 0x6 or 0x7) can be used. The user can also start a conversion by connecting an external trigger signal to a capture input pin (CAPx) from a Timer peripheral to generate an interrupt. The timer interrupt routine can then start the ADC conversion by setting the START bits (26:24) to 0x1. The trigger can also be generated from a timer match register.

3.2 ADC.2: A/D Global Data register should not be used with burst mode or hardware triggering

Introduction:

On the LPC176x, the START field and the BURST bit in the A/D control register specify whether A/D conversions are initiated via software command, in response to some hardware trigger, or continuously in burst ("hardware-scan") mode. Results of the ADC conversions can be read in one of two ways. One is to use the A/D Global Data Register to read all data from the ADC. Another is to use the individual A/D Channel Data Registers.

Problem:

If the burst mode is enabled (BURST bit set to ‘1’) or if hardware triggering is specified, the A/D conversion results read from the A/D Global Data register could be incorrect. If conversions are only launched directly by software command (BURST bit = '0' and START = ‘001’), the results read from the A/D Global Data register will be correct provided the previous result is read prior to launching a new conversion.

Work-around:

When using either burst mode or hardware triggering, the individual A/D Channel Data registers should be used instead of the A/D Global Data register to read the A/D conversion results.

3.3 ADC.3: Noise caused by nearby I/O pin switching activity or board design/layout could cause the ADC conversion results to be above the expected range.

Introduction:

The LPC176x contains a single 12-bit successive approximation ADC with eight input channels and has a conversion rate up to 200 kHz.

Problem:

Noise caused by I/O switching activity on pins close to the ADC input channels or caused by the board design/layout can couple into the ADC input channels. This causes the ADC conversion results to be corrupted up to 0xFFF. The issue occurs more frequently at −45 C and when toggling the I/O pins adjacent to the ADC input channels.

Work-around:

Use the following work-arounds:

1. If possible, avoid toggling the pins adjacent to ADC input channels during conversions.
2. Noise should be minimized by following the design rules in the application note: AN10974 LPC176x/175x 12-bit ADC design guidelines, including the use of two ground planes with recommended decoupling, separate power supplies for analog and digital domains, and use of low pass filtering on the ADC input channels.

3.4 Ethernet.1: Ethernet TxConsumeIndex register does not update correctly after the first frame is sent (LPC1769/68/67/66/64 only)

Introduction:

The transmit consume index register defines the descriptor that is going to be transmitted next by the hardware transmit process. After a frame has been transmitted hardware increments the index, wrapping the value to 0 once the value of TxDescriptorNumber has been reached. If the TxConsumeIndex equals TxProduceIndex the descriptor array is empty and the transmit channel will stop transmitting until software produces new descriptors.

Problem:

The TxConsumeIndex register is not updated correctly (from 0 to 1) after the first frame is sent. After the next frame sent, the TxConsumeIndex register is updated by two (from 0 to 2). This only happens the very first time, so subsequent updates are correct (even those from 0 to 1, after wrapping the value to 0 once the value of TxDescriptorNumber has been reached)

Work-around:

Software can correct this situation in many ways; for example, sending a dummy frame after initialization.

3.5 GPIO.1: Open drain mode cannot be selected when port pin is configured as a non GPIO function

Introduction:

A special open drain mode can be configured via the PINMODE_OD registers for the standard general purpose port pins. Open drain mode can be selected for the standard general purpose port pins regardless of the function selected on the pin.

Problem:

Open drain mode can be selected for every standard general purpose port pin only when configured as a GPIO function.

Work-around:

None.

3.6 GPIO.2: Open drain mode is not functional on port pin P4.29

Introduction:

A special open drain mode can be configured via the PINMODE_OD registers for the standard general purpose port pins.

Problem:

Open drain mode is not functional only on port pin P4.29. Open drain mode works for the rest of the standard general purpose port pins.

Work-around:

None.

3.7 I2C.1: In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register

Introduction:

The I2C monitor allows the device to monitor the I2C traffic on the I^2C-bus in a non-intrusive way.

Problem:

In the slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I^2C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100 % non-intrusive.

Work-around:

When setting the device in monitor mode, enable the ENA_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1); //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to the slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for the slave-transmitter mode:

```
case 0xA8:     // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:     // data byte in DAT transmitted, ACK received
case 0xC0:     // (last) data byte transmitted, NACK received
case 0xC8:     // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER;//Save data. Data can be process in Main loop
    LPC_I2C->DAT = 0xFF;            // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

3.8 I2S.1: The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz (LPC1769/68/67/66/65/63 only)

Introduction:

The transmitter/receiver MCLK (Master clock output) rate is generated using a fractional rate generator, dividing down the frequency of PCLK_I2S. Values of the numerator (X) and the denominator (Y) must be chosen to produce a frequency twice that desired for the receiver MCLK, which must be an integer multiple of the receiver bit clock rate.

Problem:

The XY divider (8-bit Fractional Rate Divider) will not work for PCLK_I2S (Peripheral clock for I2S) higher than 74 MHz.

Work-around:

Do not use PCLK_I2S signal higher than 74 MHz.

3.9 IBAT.1

Introduction:

Two independent power domains (VDD_{REG} domain and V_{BAT} domain) are provided that allow the bulk of the device to have power removed while maintaining operation of the Real Time Clock (RTC). The V_{BAT} pin supplies power only to the RTC domain and is active when V_{BAT} is greater than VDD_{REG}. The RTC requires a minimum of power to operate, which can be supplied by an external battery (V_{BAT}). Whenever the device core power (VDD_{REG}) is greater than V_{BAT}, VDD_{REG} is used to operate the RTC. When VDD_{REG} is grounded, the I_{BAT} is typically around 1 uA.

Problem:

Typical lots have about 5 % parts with I_{BAT} current as high as about 10 uA when only V_{BAT} is applied (VDD_{REG} is grounded). This is due to a leakage current path in a level shifter in the power domain.

Work-around:

The problematic leakage path is disabled when the part is entered into Deep power-down mode. If the application allows, the customer should put the device into Deep power-down mode before the VDD_{REG} power is grounded; the BOD ISR could potentially be used for this purpose.

3.10 MCPWM.1: Input pins (MCI0-2) on the Motor Control PWM peripheral are not functional

Introduction:

On the LPC176x, the Motor Control PWM (MCPWM) peripheral is optimized for three-phase AC and DC motor control applications and can also be used in applications which require timing, counting, capture, and comparison. The MCPWM contains three input pins (MCI0-2) for PWM channels 0, 1, and 2. The inputs can be used as feedbacks for controlling brushless DC motors with Hall sensors, and also can be used to trigger a Timer/Counter's (TC) capture or increment a channel's TC when MCPWM is configured as a timer/counter.

Problem:

The input pins (MCI0-2) are not functional.

Work-around:

The GPIO interrupts on port 0 or port 2 can be used instead of the MCPWM MCI0-2 pins. The GPIO interrupts give the ability to trigger an interrupt on both the rising and falling edge; therefore, all six states of the connected hall sensor can be detected through an interrupt.

3.11 PCLKSELx.1: Peripheral Clock Selection Registers must be set before enabling and connecting PLL0

Introduction:

A pair of bits in the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) controls the rate of the clock signal that will be supplied to APB0 and APB1 peripherals.

Problem:

If the Peripheral Clock Registers (PCLKSEL0 and PCLKSEL1) are set or changed after PLL0 is enabled and connected, the value written into the Peripheral Clock Selection Registers may not take effect. It is not possible to change the Peripheral Clock Selection settings once PLL0 is enabled and connected.

Work-around:

Peripheral Clock Selection Registers must be set before enabling and connecting PLL0.

3.12 PLL0.1: PLL0 (Main PLL) remains enabled and connected in Deep Sleep and Power-down modes

Introduction:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, main PLL (PLL0) automatically turns off and disconnects after the chip enters Deep Sleep mode or Power-down mode leading to reduced power consumption.

Problem:

If the main PLL (PLL0) is enabled and connected before entering Deep Sleep or Power-down modes, it will remain enabled and connected after the chip enters Deep Sleep mode or Power-down mode causing the power consumption to be higher.

Work-around:

In the software, user must disable and disconnect the main PLL (PLL0) before entering Deep Sleep and Power-down modes to reduce the power consumption. This must be done only if the main PLL (PLL0) was enabled and connected before entering Deep Sleep mode or Power-down mode.

The code below demonstrates the steps to disable and disconnect the main PLL0:

```
PLL0CON &= ~(1<<1);                  /* Disconnect the main PLL (PLL0) */

PLL0FEED = 0xAA;                     /* Feed */

PLL0FEED = 0x55;                     /* Feed */

while ((PLL0STAT & (1<<25)) != 0x00); /* Wait for main PLL (PLL0) to disconnect */

PLL0CON &= ~(1<<0);                  /* Turn off the main PLL (PLL0) */

PLL0FEED = 0xAA;                     /* Feed */

PLL0FEED = 0x55;                     /* Feed */

while ((PLL0STAT & (1<<24)) != 0x00); /* Wait for main PLL (PLL0) to shut down */

/************** Then enter into Deep sleep mode or Power-down mode*****************/
```

3.13 PWM.1: When updating the duty cycle for PWM1.1 from 100 %, in some cases the output can stay low for a full PWM period before the update takes effect

Introduction:

On the LPC176x PWM peripheral, two match registers can be used to provide a single edge controlled PWM output. One match register (PWM1MR0) controls the PWM cycle rate, by resetting the count upon match. The other match register controls the PWM edge position. As an example, match register PWM1MR1 controls PWM1's edge position. Multiple single edge controlled PWM outputs will all have a rising edge at the beginning of each PWM cycle, when a PWM1MR0 match occurs.

Problem:

Only in single-edge mode, if the duty cycle for PWM1.1 (Pulse Width Modulator 1, channel 1 output) is updated from 100 % (PWM1MR1 = PWM1MR0), then the output for PWM1.1 could unexpectedly remain low for a full PWM period before the new desired duty cycle takes effect. This problem only affects the output for PWM1.1. Other PWM channels (PWM1.2 to PWM1.6) are not affected by this problem.

Work-around:

A software fix can be implemented where the user can load PWM1MR1 with PWM1MR0 + 1 (at least 1) to avoid any delays in the PWM1.1's output update.

3.14 RTC.1: The Real Time Clock (RTC) does not work reliably within the temperature specification

Introduction:

The RTC is a set of counters for measuring time when system power is on, and optionally when it is off. The RTC is clocked by a separate 32 kHz oscillator that produces a 1 Hz internal time reference. The RTC is powered by its own power supply pin, VBAT, which can be connected to a battery, externally tied to a 3 V supply, or left floating. The RTC can operate over temperature range from −40 °C to 85 °C.

Problem:

The RTC does not work reliably within the temperature specification.

Work-around:

None.

3.15 USB.1: USB host controller hangs on a dribble bit (LPC1769/68/66/65 only)

Introduction:

Full-/low-speed signaling uses bit stuffing throughout the packet without exception. If the receiver sees seven consecutive ones anywhere in the packet, then a bit stuffing error has occurred and the packet should be ignored.

The time interval just before an EOP is a special case. The last data bit before the EOP can become stretched by hub switching skews. This is known as dribble and can lead to a situation where dribble introduces a sixth bit that does not require a bit stuff. Therefore, the receiver must accept a packet for which there are up to six full bit times at the port with no transitions prior to the EOP.

Problem:

The USB host controller will hang indefinitely if it sees a dribble bit on the USB bus. It will hang the first time a dribble bit is seen. Once it is in this state there is no recovery other than a hard chip reset. This problem has no effect on the USB device controller.

Work-around:

None.

3.16 $V_{DD(REG)(3V3)}$.1: The minimum regulator supply voltage is 3.0 V for the temperature range –40 °C to 85 °C

Introduction:

The device has a regulator supply voltage ($V_{DD(REG)(3V3)}$) with a specification of 2.4 V to 3.6 V for the temperature range –40 °C to 85 °C.

Problem:

The device **does not work** when the regulator supply voltage ($V_{DD(REG)(3V3)}$) is lower than 3.0 V for temperature range –40 °C to 85 °C.

Work-around:

Ensure that the $V_{DD(REG)(3V3)}$) is kept above 3.0 V over the temperature range –40 °C to 85 °C.

4. AC/DC deviations detail

4.1 n/a

5. Errata notes detail

5.1 Note.1 (LPC1769/68/66/65/64 only)

On the LPC176x, for USB operation, the supply voltage ($V_{DD(3V3)}$) range must be 3.0 V ≤ $V_{DD(3V3)}$ ≤ 3.6 V.

5.2 Note.2

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the V_{DD} level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V_{DD} supply ramps up.

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