Freescale Semiconductor
Addendum

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MC9328MX21 Mask Differences Between 2L45X and M55B

Reference Manual Addendum for MC9328MX21RM

1 Introduction

This addendum describes the changes between the 2L45X and M55B mask sets of the MC9328MX21 applications processor and the specific changes to the *MC9328MX21 Applications Processor Reference Manual*, Rev. 1.1.

The information is presented first by providing the location of the change within the reference manual and then by providing a summary of the change. Finally, for each change, the actual reference manual content before and after the change is provided.

Contents

2 PCMCIA Chapter Changes

The change to the Chapter 39.1.2, PCMCIA Features, is the fifth bulleted item. Please replace the first five bulleted items with those in this document's Section 2.2, "Mask M55B: Features."

The summary of change is that the M55B mask set provides up to 32 kbytes in memory space, as compared to 2 kbytes in the 2L45X mask set.

2.1 Mask 2L45X: Features

The PCMCIA/CF controller includes these distinctive features:

- A host adapter interface fully compliant with the PCMCIA standard release 2.1 (PC Card -16)
- Supports one PCMCIA socket
- Supports hot-insertion
- Supports card detection
- Mapping to common memory space, attribute memory space and I/O space. Each space is up to 2 kbyte in size

  and so on

2.2 Mask M55B: Features

The PCMCIA/CF controller includes these distinctive features:

- A host adapter interface fully compliant with the PCMCIA standard release 2.1 (PC Card -16)
- Supports one PCMCIA socket
- Supports hot-insertion
- Supports card detection
- Mapping to common memory space, attribute memory space and I/O space. Each space is up to 32 kbyte in size

  and so on

2.3 PCMCIA Base Registers 0-4 (PBR0-PBR4) Change Summary

The change to Section 39.3.4 PCMCIA Base Registers 0–4 (PBR0–PBR4), of the reference manual is the reassignment of the Base Register Address (PBA) bits within the register illustration and register table. Please replace Section 39.3.4 with the information in this document's Section 2.3.2, "Mask M55B: PCMCIA Base Registers 0–4 (PBR0–PBR4)."

The summary of change is the reassignment of the Base Register Address (PBA) bits from [10:0] to [14:4].

2.3.1 Mask 2L45X: PCMCIA Base Registers 0–4 (PBR0–PBR4)

PBA [10:0]—PCMCIA base address. Compared to the address bus to determine if a PCMCIA window is being accessed by an internal bus master. PBA is used in conjunction with POR[BSIZE]. When accessing this register 1-wait state is added by the PCMCIA/CF controller.

PBR0–PBR4 PCMCIA Base Registers 0–4 **Addr 0xDF00 200C ... 0xDF00 201C**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						PBA[10:0]										
TYPE	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1. PCMCIA Base Register Description

Name	Description
PBA Bit 10–0	**Base Register Address**—This contains the base register address used by the PCMCIA device.

2.3.2 Mask M55B: PCMCIA Base Registers 0–4 (PBR0–PBR4)

PBA [14:4]—PCMCIA base address. Compared to the address bus to determine if a PCMCIA window is being accessed by an internal bus master. PBA is used in conjunction with POR[BSIZE]. When accessing this register 1-wait state is added by the PCMCIA/CF controller.

PBR0–PBR4 PCMCIA Base Registers 0–4 **Addr 0xDF00 200C ... 0xDF00 201C**

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		PBA[14:4]														
TYPE	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2. PCMCIA Base Register Description

Name	Description
PBA Bit 14–4	**Base Register Address**—This contains the base register address used by the PCMCIA device.

2.4 PCMCIA Offset Registers 0-4 (POFR0-POFR4) Change Summary

The change to Section 39.3.6, PCMCIA Offset Registers 0-4, of the reference manual is the reassignment of the PCMCIA Offset Address (POFA) bits within the external address calculation example, the register illustration, and register table. Please replace section 39.3.4 with the information in this document's Section 2.4.2, "Mask M55B: PCMCIA Offset Registers 0–4 (POFR0–POFR4)."

The summary of change is the reassignment of the PCMCIA Offset Address (POFA) bits from [10:0] to [14:4]. This change affects the external address calculation example.

2.4.1 Mask 2L45X: PCMCIA Offset Registers 0–4 (POFR0–POFR4)

POFA [10:0]—PCMCIA offset address. The offset address of the window. PBA is used in conjunction with POR[BSIZE]. The external address is ext_addr= POFA + haddr and MASK.

For example, if:

```
haddr = 0x263, MASK = 0x7C0, POFA = 0x161
```

then:

```
ext_addr = 0x161 + 0x263 and (0x7C0) = 0x161 + 0x23 = 0x184
```

When accessing this register 1-wait state is added by the PCMCIA/CF controller.

POFR0–POFR4 PCMCIA Offset Registers 0–4

Addr
0xDF00 2044
...
0xDF00 2054

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						POFA										
TYPE	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1. PCMCIA Offset Register Description

Name	Description	Settings
Reserved Bits 31–11	Reserved—These bits are reserved and should read 0.	
POFA Bits 10–0	**POFA**—PCMCIA Offset Registers Address	N/A

2.4.2 Mask M55B: PCMCIA Offset Registers 0–4 (POFR0–POFR4)

POFA [14:4]—PCMCIA offset address. The offset address of the window. PBA is used in conjunction with POR[BSIZE]. The external address is ext_addr= POFA + haddr and MASK.

For example, if:

```
haddr = 0x2630, MASK = 0x7C00, POFA = 0x1610
```

then:

```
ext_addr = 0x1610 + 0x2630 and (0x7C00) = 0x1610 + 0x230 = 0x1840
```

When accessing this register 1-wait state is added by the PCMCIA/CF controller.

POFR0–POFR4 PCMCIA Offset Registers 0–4

Addr
0xDF00 2044
...
0xDF00 2054

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		POFA[14:4]														
TYPE	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2. PCMCIA Offset Register Description

Name	Description	Settings
Reserved Bits 31–11, 3–0	Reserved—These bits are reserved and should read 0.	
POFA Bits 14–4	**POFA**—PCMCIA Offset Registers Address	N/A

2.5 BSIZE Table Value Changes

The changes to Section 39.3.5, Table 39-9 BSIZE Values, of the reference manual are the units in the Meaning column of the table. Please replace Section 39.3.5, Table 39-9 BSIZE Values, with Section 2.5.2, “Mask M55B: BSIZE Values” in this document.

The summary of change is the window granularity and sizes from 1 byte through 2 kbyte to 16 byte through 32 kbyte.

2.5.1 Mask 2L45X: BSIZE Values

Table 3. BSIZE Values

Value	Meaning	Value	Meaning
00000	1 byte	00101	64 byte
00001	2 byte	00100	128 byte
00011	4 byte	01100	256 byte
00010	8 byte	01101	512 byte
00110	16 byte	01111	1 kbyte
00111	32 byte	01110	2 kbyte

2.5.2 Mask M55B: BSIZE Values

Table 4. BSIZE Values

Value	Meaning	Value	Meaning
00000	16 byte	00101	1 kbyte
00001	32 byte	00100	2 kbyte
00011	64 byte	01100	4 kbyte
00010	128 byte	01101	8 kbyte
00110	256 byte	01111	16 kbyte
00111	512 byte	01110	32 kbyte

2.6 PCMCIA BSIZE Mask Table Changes

The changes to Section 39.3.5, Table 39-10 BSIZE Mask, of the reference manual is the addition of four address columns in the table. Please replace Section 39.3.5, Table 39-10 BSIZE Mask, with Section 2.6.2, “Mask M55B: PCMCIA BSIZE Mask Table Changes” in this document.

The summary of change is the addition of address columns A0-A3.

2.6.1 Mask 2L45X: PCMCIA BSIZE Mask Table Changes

Table 5. BSIZE Mask

BSIZE	Mask									
0000	1	1	1	1	1	1	1	1	1	1
0001	1	1	1	1	1	1	1	1	1	0
0011	1	1	1	1	1	1	1	1	0	0
0010	1	1	1	1	1	1	1	0	0	0
0110	1	1	1	1	1	1	0	0	0	0
0111	1	1	1	1	1	1	0	0	0	0
0101	1	1	1	1	1	0	0	0	0	0
0100	1	1	1	1	0	0	0	0	0	0
1100	1	1	1	0	0	0	0	0	0	0
1101	1	1	0	0	0	0	0	0	0	0
1111	1	0	0	0	0	0	0	0	0	0
1110	0	0	0	0	0	0	0	0	0	0
1001	0	0	0	0	0	0	0	0	0	0
1000	0	0	0	0	0	0	0	0	0	0
11000	0	0	0	0	0	0	0	0	0	0
11001	0	0	0	0	0	0	0	0	0	0
11011	0	0	0	0	0	0	0	0	0	0
11010	0	0	0	0	0	0	0	0	0	0
11110	0	0	0	0	0	0	0	0	0	0
11111	0	0	0	0	0	0	0	0	0	0
11101	0	0	0	0	0	0	0	0	0	0
11100	0	0	0	0	0	0	0	0	0	0
10100	0	0	0	0	0	0	0	0	0	0
10101	0	0	0	0	0	0	0	0	0	0
10111	0	0	0	0	0	0	0	0	0	0

2.6.2 Mask M55B: PCMCIA BSIZE Mask Table Changes

Table 6. BSIZE Mask

BSIZE	A14						Mask							A0
0000	1	1	1	1	1	1	1	1	1	1	0	0	0	0
0001	1	1	1	1	1	1	1	1	1	0	0	0	0	0
0011	1	1	1	1	1	1	1	1	0	0	0	0	0	0
0010	1	1	1	1	1	1	1	0	0	0	0	0	0	0
0110	1	1	1	1	1	1	0	0	0	0	0	0	0	0
0111	1	1	1	1	1	0	0	0	0	0	0	0	0	0
0101	1	1	1	1	0	0	0	0	0	0	0	0	0	0
0100	1	1	1	0	0	0	0	0	0	0	0	0	0	0
1100	1	1	0	0	0	0	0	0	0	0	0	0	0	0
1101	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1111	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1001	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1000	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11000	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11001	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11011	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11010	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11110	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11111	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11101	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11100	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10100	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10101	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10111	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3 Signal Descriptions and Pin Assignments Changes—Addition of EXT_DMAGRANT Multiplexing with CSPI1_SS1 (in the Bin Port)

The changes to the Chapter 2.1 Signal Description, Table 2-1, of the reference manual is the addition of CSPI1_SSI to the External DMA and CSPI signal descriptions within the table. Please replace the portions of Section 2.1, Table 2-1 i.MX21 Signal Descriptions, with the portions of Section 3.2.1, “Mask M55B: Part of Signal Description Table 2-1” in this document.

The change to the Chapter 2.1 Signal Description, Table 2-2, Signal Multiplexing Scheme, of the reference manual adds the External DMA signal to the GPIO BIN column within the table. Please replace the portion of Section 2.1, Table 2-2 i.MX21 Signal Mulitplexing Scheme, with the portion of Section 3.2.2, “Mask M55B: Part of Multiplexing Table 2-2” in this document.

The change summary is the addition of EXT_DMAGRANT multiplexed with CSPI1_SS1 in the BIN port.

3.1 Mask 2L45X: Signal Description and Multiplexing Table Changes

3.1.1 Mask 2L45X: Part of Signal Description Table 2-1

Table 7. External DMA and CSPI Portions of Signal Description Table

External DMA	
$\overline{\text{EXT\_DMAREQ}}$	External DMA Request input signal. This signal is multiplexed with CSPI1_$\overline{\text{RDY}}$.
$\overline{\text{EXT\_DMAGRANT}}$	External DMA Grant output signal. This signal is multiplexed with LD[16].
CSPI	
CSPI1_MOSI	Master Out/Slave In signal
CSPI1_MISO	Master In/Slave Out signal
CSPI1_SS[2:0]	Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT.

3.1.2 Mask 2L45X: Part of Multiplexing Table 2-2

Table 8. NVDD3 Multiplexing Scheme Portion of Signal Multiplexing Table

I/O Supply Voltage	BGA Pins	Primary				Alternate				GPIO							Default
		Signal	Dir	PU	OD	Signal	Dir	PU	OD	Mux	Pull-up	AIN	BIN	CIN	AOUT	BOUT	
NVDD3	F16	CSPI1_SS1	B							PD27	PUEN						PD27

3.2 Mask M55B: Signal Description and Multiplexing Table Changes

3.2.1 Mask M55B: Part of Signal Description Table 2-1

Table 9. External DMA and CSPI Portion of Signal Description Table

External DMA	
$\overline{\text{EXT\_DMAREQ}}$	External DMA Request input signal. This signal is multiplexed with CSPI1_$\overline{\text{RDY}}$.
$\overline{\text{EXT\_DMAGRANT}}$	External DMA Grant output signal. This signal is multiplexed with LD[16] and CSPI1_SS1.
CSPI	
CSPI1_MOSI	Master Out/Slave In signal
CSPI1_MISO	Master In/Slave Out signal
CSPI1_SS[2:0]	Slave Select (Selectable polarity) signal. CSPI1_SS2 is also multiplexed with USBG_RXDAT and CSPI1_SS1 is multiplexed with EXT_DMAGRANT.

3.2.2 Mask M55B: Part of Multiplexing Table 2-2

Table 10. NVDD3 Multiplexing Scheme Portion of Signal Multiplexing Table

I/O Supply Voltage	BGA Pins	Primary				Alternate				GPIO							Default
		Signal	Dir	PU	OD	Signal	Dir	PU	OD	Mux	Pull-up	AIN	BIN	CIN	AOUT	BOUT	
NVDD3	F16	CSPI1_SS1	B							PD27	PUEN		EXT_DMAGRANT				PD27

4 System Control Chapter Changes

The changes to Section 9.1.1 Silicon ID, of the reference manual is the type of address of bit 92 within the register illustration and the setting of the Chip ID (CID) bits in the register table. Please replace section 39.3.4 with the information in Section 4.2, “Mask M55B: Silicon ID Register” of this document.

The summary of change is the type of address of bit 92 (from 0 to 1) and the setting of the Chip ID (CID) bits from 32’h001D101D, to 0x101D101D, in the register table.

4.1 Mask 2L45X: Silicon ID Register

SIDR Silicon ID Register **0x10027804**

BIT	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
	CID															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1
	0x001D															

BIT	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	CID															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1
	0x101D															

TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
BIT	63–48															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0x0000_0000															

Table 4-1. Silicon ID Register Description

Name	Description	Silicon Fuse Setting	Settings
CID Bits 95–64	**Chip ID**—Contains the chip identification number of the i.MX21. Bits 95–92 contains 4 usable bits and it indicates the part version.	Blown[x]=1 Intact[x]= 0	32’h001D101D

4.2 Mask M55B: Silicon ID Register

SIDR Silicon ID Register **0x10027804**

BIT	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
	CID															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1
	0x001D															

BIT	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
	CID															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	1	0	0	0	0	0	0	0	1	1	1	0	1
	0x101D															

TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
BIT	63–48															
TYPE	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
RESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	0x0000_0000															

Table 4-2. Silicon ID Register Description

Name	Description	Silicon Fuse Setting	Settings
CID Bits 95–64	**Chip ID**—Contains the chip identification number of the i.MX21. Bits 95–92 contains 4 usable bits and it indicates the part version.	Blown[x]=1 Intact[x]= 0	0x101D101D

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