MCF5213 Chip Errata

Silicon Revision: All

This document identifies implementation differences between the MCF521*x* processors and the description contained in the *MCF5213 ColdFire® Reference Manual*. Refer to http://www.freescale.com/coldfire for the latest updates.

All current MCF5211/12/13 devices are marked as M30B mask set.

Table 1. Summary of MCF521x Errata

Errata	Module Affected	Date Errata Added	Revision Affected?	
			PCF521x	MCF521x
SECF023	Clock	4/29/05	Yes	No
SECF024	Clock	4/29/05	Yes	No
SECF051	VSTDBY	10/27/05	Yes	Yes
SECF015	Flash	11/17/06	Yes	Yes
SECF018	ADC	2/5/08	Yes	Yes
SECF019	ADC	2/5/08	Yes	Yes
SECF014	BDM	3/20/08	Yes	Yes

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
0	5/2005	Initial release
1	10/2005	Added column toTable 1 showing part numbers affected. Also added statement that ‘MCF ‘prefix devices are not affected.
2	10/2005	Added SECF051 and updated Table 1.
2.1		Added “Part number affected: All devices” to SECF051
3	11/2006	Added SECF015 Updated Table 1. Text changes for grammar and punctuation.
4	3/2008	Added SECF018 and SECF019. Updated Table 1.
5	3/2008	Added SECF014
6	02/2015	Updated SECF015

SECF023: Input Clock is Ignored When the External Oscillator is Configured as the Reference Clock

Errata type: Silicon
Affects: Clock
Description: When configuring the device to use an external oscillator as the reference clock, the input clock is ignored and the clock output is generated from the on-chip oscillator (OCO).

Workaround: Place the device into one of the external crystal modes (CLKMOD[1:0] = 01 or CLKMOD[1:0] = 11) and input an external oscillator on the EXTAL pin.

- If the PLL is enabled (CLKMOD[1:0] = 11), the valid external oscillator range is 2 to 10MHz.
- If the PLL is disabled (CLKMOD[1:0] = 01), the valid external oscillator range is 0 to 80MHz.

Fix plan: Fixed in devices with an MCF prefix in the part number.

SECF024: Clock has Jitter of +/-10 Percent When PLL is Enabled

Errata type: Silicon
Affects: Clock
Description: When the PLL is enabled, the resulting clock has jitter of +/- 10 percent. This behavior is independent of the input clock source.

Workaround: Set bit 2 in the oscillator test register (IPSBAR + 0x120006) after powering on the processor. Do not disturb the other bit settings of this register. Therefore, bit 2 should be ORed into the default register setting.

Fix plan: Fixed in devices with an MCF prefix in the part number.

SECF051: Non-functional RAM Standby Supply

Errata type: Silicon
Affects: VSTDBY
Description: The V_{STDBY} supply is intended to supply power to the on-chip SRAM when the main power supply, V_{DD}, is removed. However, when V_{STDBY} is a higher voltage than V_{DD}, the V_{STDBY} supply sources power to the entire V_{DD} supply rail.

Workaround: V_{STDBY} should be connected to the V_{DD} supply. The STOP low-power mode should be used to conserve RAM contents and meet power savings requirements. V_{STDBY} should not exceed V_{DD} + 0.3V.

Fix plan: Currently, there are no plans to fix this.

SECF015: Internal Flash Speculation Address Qualification Incomplete

Errata type: Silicon
Affects: Flash controller
Description: The flash controller uses a variety of advanced techniques, including two-way 32-bit bank interleaving, address speculation, and pipelining to improve performance. An issue involving a complex series of interactions between the local flash controller and other memory accesses (internal SRAM, EIM, or SDRAM) has been uncovered. In rare instances, the interaction between a non-flash memory access and a flash access can result in incorrect data usage for a read operation. This may produce unexpected exceptions, incorrect execution, or silent data corruption.

The problem requires two accesses where the modulo (flash size) address and address mask configuration are the same for both a flash access and a non-flash access that occur close in time.

Workaround: **Workaround Step 1 (Always do this)**: Use FLASHBAR[6] to disable the address speculation mechanisms of the flash controller. The default configuration (FLASHBAR[6] = 0) enables the address speculation. If FLASHBAR[6] equals 1, address speculation is disabled. Core performance may be degraded from 4% – 9%, depending heavily on application code.

NOTE

FLASHBAR[6] is user accessible via the movec instruction. FLASHBAR[6] always reads back as 0.

NOTE

On MCF528x and MCF521x devices FLASHBAR[6] is already set to 1 for datecodes XXX0327 and later. The bit still reads back as 0.

Workaround Step 2a (Select one of the step 2 options to use): Construct the device memory map so the flash and SRAM spaces are disjoint within the modulo-(flash_size) addresses. In some cases if this approach is selected, the upper portion of the flash memory might be unused and the SRAM be mapped to this unused flash space.

Consider an example where the flash memory size is 256 Kbytes and the on-chip SRAM size is 32 Kbytes. If 224 Kbytes or less of flash are used, the SRAM can be based at the upper 32 Kbytes (within the modulo-256 Kbyte address) of the flash address space:

```
Flash: size = 0x40000, base = 0x0000_0000
RAM: size = 0x08000, base = 0x8003_8000 = RAM_BASE+(256-32) Kbytes
```

where the flash and SRAM base addresses are unique BA[31:16].

In summary, this approach can be applied if the combined size of the used flash and used SRAM is less than the total flash size, with the flash contents justified to the lower address range and the SRAM contents justified to the upper address range.

Workaround Step 2b (Select one of the step 2 options to use): Separate the contents of the SRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR and RAMBAR to restrict accesses. For example, if the flash contains only instructions and the SRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Workaround Step 3a (Select one of the step 3 options to use if external parallel memory is used in the system): Do not enable caching of external memories. With caching disabled the timing requirements for an issue to occur will not be met, so this will prevent conflicts between flash and external parallel memory accesses through the EIM or SDRAMC.

Workaround Step 3b (Select one of the step 3 options to use if external parallel memory is used in the system): Separate the contents of the EIM and/or SDRAM and the flash memory into exclusive categories and use the address space mask bits in FLASHBAR, CSMRn, and DMRn to restrict accesses. For example, if the flash contains only instructions and the SDRAM contains only operands (all data), the appropriate address space mask fields are specified to prevent flash and SRAM accesses from overlapping.

Fix plan: Currently, there are no plans to fix this.

SECF018: ADC Might Give Erroneous Results if V_{REFH} and V_{REFL} are Not at the Same Potential as V_{DDA} and V_{SSA} Respectively

Errata type: Silicon
Affects: ADC
Description: The ADC could produce an error if the ADC reference voltage VREFH is below the analog supply voltage VDDA, or if the ADC reference voltage VREFL is above analog ground VSSA by more than 50 mV. The error is that the ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Connect V_{REFH} directly to V_{DDA}. Similarly, connect V_{REFL} to V_{SSA}.

Fix plan: Currenty, there are no plans to fix this.

SECF019: ADC Might Give Erroneous Results if the ADC Reference Voltage (V_{REFH}) is Below 3.1 V

Errata type: Silicon
Affects: ADC
Description: If the ADC reference voltage V_{REFH} is less than 3.1 V, either of the following error conditions could result:

- Low analog input voltages to the ADC might not be measured properly. (for example, input voltages less than 100 mV might yield measurements equal to 0)
- The ADC digital result might jump randomly to an invalid value before returning to a correct value on the next result. The invalid value could be full scale (for example, 0 or 4095) or mid range.

Workaround: Ensure that V_{REFH} is at or above 3.1 V.

Fix plan: Currenty, there are no plans to fix this.

SECF014: Level 2 Trigger Operation Controlled by TDR[31]

Errata type: Silicon
Affects: BDM
Description: The TDR[L2T] bit (TDR bit 15) has no effect on the level 2 trigger. Bit 31 of the TDR register provides both trigger response control and logical operation of the level 2 trigger.

Workaround: Use the TDR[31] bit to control the logical operation for the level 2 trigger as follows:

- 0 -- Level 2 trigger = PC_condition & Address_range & Data_condition
- 1 -- Level 2 trigger = PC_condition | (Address_range & Data_condition)

Since TDR[31] is also part of the trigger response control, only certain combinations of trigger responses and logical operations are available as shown below:

Table 3. TDR[31:30] Definitions

TDR[31:30]	Level 2 Trigger	Trigger Response
00	PC_cond & (Add_range & Data_cond)	Display on DDATA
01		Processor halt
10	PC_cond | (Add_range & Data_cond)	Debug interrupt
11		Reserved

Fix plan: Currently, there are no plans to fix this.

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