MCF5275 Chip Errata

Silicon Revision: All

This document identifies implementation differences between the MCF5274 and MCF5275 processors and the description contained in the *MCF5275 ColdFire® Reference Manual*. Refer to http://www.freescale.com/coldfire for the latest updates.

All current MCF5274 and MCF5275 devices are marked as L71W mask set. The date code on the marking can be used to determine which errata have been corrected on a particular device, as shown in Table 1. The datecode format is XXXXYYWW, where YY represents the year and WW represents the work week. The four leading digits can be ignored.

Table 1. Summary of MCF5274 and MCF5275 Errata

Errata	Module Affected	Date Errata Added	Date Code Affected?	
			< XXXX0545	≥ XXXX0545
SECF005	Cache	4/25/05	Yes	Yes
SECF001	Cache	4/25/05	Yes	Yes
SECF010	FEC	4/25/05	Yes	Yes
SECF050	USB	4/28/05	Yes	No
SECF131	PLL	9/15/08	Yes	Yes
SECF163	PLL	3/4/10	Yes	Yes
SECF220	CCM	8/20/13	Yes	Yes

The table below provides a revision history for this document.

Table 2. Document Revision History

Rev. No.	Date	Substantive Changes
0		Initial revision
0.1		Added SECF050
1		Updated errata with new revision of silicon and added note regarding errata that never existed.
2	9/2008	Added SECF131
3	4/2010	Added SECF163
4	6/2011	• Updated fix plan for SECF163 • Corrected revision numbers in revision history table • Removed SECF007 and SECF009 errata since they never affected any versions of the MCF5274 and MCF5275 devices
5	9/2013	Added SECF220
6	9/2014	Corrected Fix Plan for SECF163 removing duplicate entries.

SECF001: Incorrect Operation of Cache Freeze (CACR[CFRZ])

Errata type: Silicon
Affects: Version 2 ColdFire Cache
Description: The cache on the V2 ColdFire core is controlled by the cache control register (CACR). When the CACR[CFRZ] bit is set, the cache freeze function is enabled and no valid cache array entry is displaced. However, this feature does not always work as specified, sometimes allowing valid lines to be displaced when CACR[CFRZ] is enabled.

This does not cause any corrupted accesses. However, there could be cache misses for data that was originally loaded into the cache but was subsequently deallocated, even though the CACR[CFRZ] bit was set.

Also, incoherent cache states are possible when a frozen cache is cleared via the CACR[CINV] bit.

Workaround: Unfreeze the cache by clearing CACR[CFRZ] when invalidating the cache using the CACR[CINV] bit

Workaround: Use the internal SRAM to store critical code/data if the system cannot handle a potential cache miss

Fix plan: Currently, there are no plans to fix this.

SECF005: Possible Cache Corruption After Clearing Cache (Setting CACR[CINV])

Errata type: Silicon
Affects: Version 2 ColdFire Cache
Description: The cache on the V2 ColdFire core may function as either:

- a unified data and instruction cache

- an instruction cache
- a data cache

The cache function and organization is controlled by the cache control register (CACR). The CACR[CINV] bit causes a cache clear. If the cache is configured as a unified cache and the CINV bit is set, the scope of the cache clear is controlled by two other bits in the CACR:

- CACR[INVI] invalidates instruction cache only
- CACR[INVD] invalidates data cache only

If a write to the CACR is performed to clear the cache (CACR[CINV] = 1) and only a partial clear is done (CACR[INVI] or CACR[INVD] set), then cache corruption may occur.

Workaround: All loads of the CACR that perform a cache clear operation (CACR[CINV] set) should be followed immediately by a NOP instruction. This avoids the cache corruption problem.

Fix plan: Currently, there are no plans to fix this.

SECF010: FEC Interrupts will not Trigger on Consecutive Transmit Frames

Errata type: Silicon
Affects: FEC
Description: The late collision (LC), retry limit (RL), and underrun (UN) interrupts do not trigger on consecutive transmit frames. For example, if back-to-back frames cause a transmit underrun, only the first frame generates an underrun interrupt. No other underrun interrupts are generated until a frame is transmitted that does not underrun or the FEC is reset.

Workaround: Because late collision, retry limit, and underrun errors are not directly correlated to a specific transmit frame, in most cases a workaround for this problem is not needed. If a workaround is required, there are two independent workarounds:

- Ensure that a correct frame is transmitted after a late collision, retry limit, or underrun errors are detected.
- Perform a soft reset of the FEC by setting ECR[RESET] when a late collision, retry limit, or underrun errors are detected.

Fix plan: Currently, there are no plans to fix this.

SECF050: Corruption of USB Descriptor RAM

Errata type: Silicon
Affects: USB
Description: The USB descriptor RAM stores standard data structures which are used by the USB host to allocate bandwidth and to determine how many and what kind of endpoints are available on the device. This data is returned to the USB host during a GET_DESCRIPTOR request. After the device is connected to the host, it is possible for the descriptor RAM data to be corrupted. This can cause the host to incorrectly respond to the device during the enumeration process.

Workaround: Use the same 48-MHz clock source for the USB_CLK and the EXTAL signals and operate the processor in 1:1 PLL mode. Subsequently, the ColdFire core will run at 96 MHz and the system clock will be 48 MHz. The major drawback to this workaround is that you are not able to use DDR SDRAM memory (the DDR SDRAM runs out of spec at 48 MHz).

Fix plan: Fixed on datecodes XX0545 and later.

SECF131: PLL Does Not Lock in Normal PLL Mode with External Clock Reference

Errata type: Silicon
Affects: PLL
Description: During a power on reset, if the CLKMOD[1:0] equals 10 setting is used (normal PLL mode with external clock reference), the PLL does not lock and the device never comes out of reset.

Workaround:

NOTE

If a workaround for errata SECF163 is implemented, a workaround for this errata is not necessary.

When configuring the PLL for normal PLL mode with external clock reference, tie CLKMOD1 to $\overline{\text{RESET}}$ and not straight to 3.3V. This allows the PLL to correctly detect the desired operating mode and lock.

Fix plan: Currently, there are no plans to fix this.

SECF163: Some Devices May Not Exit Reset After Power On

Errata type: Silicon
Affects: PLL
Description: During power-on reset (POR), the frequency of the PLL's internal oscillator (ICO) may overrun the ability of the ICO's internal feedback to track to that frequency. This results in an open-loop condition where the frequency of the ICO remains at its upper limit. The internal feedback loop recovers, but might not be able to reach the target frequency and exit reset. This affects all PLL-enabled modes, but does not affect bypass mode.

Workaround: After $\overline{\text{RESET}}$ deasserts and before $\overline{\text{RSTOUT}}$ deasserts, change the target clock mode to a PLL-enabled mode in which the input clock is disabled for more than 160us. Then, change back to the target clock mode.

Table 3. Workaround #1

Start in	CLK MOD	After $\overline{\text{RESET}}$ deasserts and before $\overline{\text{RSTOUT}}$ deasserts, switch to	CLK MOD	After 160us, switch back to the target clock mode	CLK MOD
Normal mode with crystal reference	11	Normal mode with external reference	10	Normal mode with crystal reference	11
Normal mode with external reference	10	Normal mode with crystal reference	11	Normal mode with external reference	10
1:1 mode	01	Normal mode with crystal reference	11	1:1 mode	01

Workaround: At POR, start in a PLL-enabled mode in which the input clock is disabled. Keep $\overline{\text{RESET}}$ asserted for at least 160us. After $\overline{\text{RESET}}$ deasserts and before $\overline{\text{RSTOUT}}$ deasserts change to the desired clock mode.

Table 4. Workaround #2

Start in	CLK MOD	After $\overline{\text{RESET}}$ deasserts and before $\overline{\text{RSTOUT}}$ deasserts, switch to target clock mode	CLK MOD
Normal mode with external reference	10	Normal mode with crystal reference	11
Normal mode with crystal reference	11	Normal mode with external reference	10
Normal mode with crystal reference	11	1:1 mode	01

Fix plan: Currently, there are no plans to fix this.

SECF220: CCR[PSTEN] bit not implemented

Errata type: Silicon
Affects: CCM
Description: The CCM_CCR[PSTEN] bit is documented in the reference manual as a PST[3:0]/DDATA[3:0] enable. This bit is not actually implemented on the MCF5275/4 device. The bit cannot be set. The PST and DDATA signals are enabled by default and cannot be disabled using this bit.

Workaround: Do not attempt to use the CCM_CCR[PSTEN] bit. Booting the processor in JTAG mode is the recommended method to disable the PST[3:0] and DDATA[3:0] signals.

Fix plan: Currently, there are no plans to fix this.

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