Mask Set Errata for Mask 0N40H

Introduction

This report applies to mask 0N40H for these products:

- KINETIS_L

Errata ID	Errata Title
6609	I2C1: DMA transfers using certain OUTDIV1 and OUTDIV4 clock divider combinations will result in corrupted data
6395	MCG: Fast IRC Fine Trim bit is not used by the MCG Auto Trim Machine
6665	Operating requirements: Limitation of the device operating range
6580	SPI1: DMA transfers using certain OUTDIV1 and OUTDIV4 clock divider combinations will result in corrupted data
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6396	sLCD: LCD_GCR[RVTRIM] bits are in reverse order

e6609: I2C1: DMA transfers using certain OUTDIV1 and OUTDIV4 clock divider combinations will result in corrupted data

Errata type: Errata

Description: When I2C1 is configured to operate with DMA, data transfers will not complete correctly under the following conditions:

1. SIM_CLKDIV[OUTDIV1] == SIM_CLKDIV[OUTDIV4] and SIM_CLKDIV[OUTDIV1] > 1
2. SIM_CLKDIV[OUTDIV1] != SIM_CLKDIV[OUTDIV4] and SIM_CLKDIV[OUTDIV4] == 0

Workaround: Do not use I2C1 with DMA and the clock divider settings described above.

e6395: MCG: Fast IRC Fine Trim bit is not used by the MCG Auto Trim Machine

Errata type: Errata

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Description: The Fast IRC fine trim bit, MCG_C2[FCFTRIM], is not used by the Auto Trim Machine. This means that when the Auto Trim Machine is used to set the Fast IRC frequency, it will not be trimmed with the finest resolution. If the finer resolution is required, the MCG_C2[FCFTRIM] bit must be manually changed and the resulting fast IRC frequency must then be measured to determine whether this bit should be set or cleared to be closest to the target frequency.

Workaround: If the finest resolution of the Fast IRC trim is not required, then no workaround is required. However, if the finest resolution is required, the following steps must be performed:

1) After the auto trim machine has completed running, measure the Fast IRC frequency.

2) Clear the MCG_C2[FCFTRIM] and re-measure the Fast IRC frequency.

3) Determine which value of MCG_C2[FCFTRIM] provided the closest frequency to the desired target frequency.

4) Store the MCG_C4[FCTRIM] and MCG_C2[FCFTRIM] values in a suitable flash location. Refer to the individual device reference manual for the recommended flash location.

e6665: Operating requirements: Limitation of the device operating range

Errata type: Errata
Description: Some devices, when power is applied, may not consistently begin to execute code under certain voltage and temperature conditions. Applications that power up with either VDD >= 2.0 V or temperature >= -20C are not impacted. Entry and exit of low-power modes is not impacted.

Workaround: To avoid this unwanted behavior, one or both of these conditions must be met:

a) Perform power on reset of the device with a supply voltage (VDD) equal-to or greater-than 2.0 V , or

b) Perform power on reset of the device at a temperature at or above -20 C.

e6580: SPI1: DMA transfers using certain OUTDIV1 and OUTDIV4 clock divider combinations will result in corrupted data

Errata type: Errata
Description: When SPI1 is configured to operate with DMA, data transfers will not complete correctly under the following conditions:

1. SIM_CLKDIV[OUTDIV1] == SIM_CLKDIV[OUTDIV4] and SIM_CLKDIV[OUTDIV1] > 1

2. SIM_CLKDIV[OUTDIV1] != SIM_CLKDIV[OUTDIV4] and SIM_CLKDIV[OUTDIV4] == 0

Workaround: When using the clock divider settings above, enable the SPI1 FIFO, SPI1_C3[FIFOMODE] = 1, before performing DMA transfers. Note that if DMA cycle steal mode is enabled, DMA_DCRn[CS] = 1, the DMA will not need to be reconfigured by software after every transfer.

e6060: TSI: Out of Range interrupt shows incorrect behavior with some configurations.

Errata type: Errata
Description: Out of Range interrupt does not work correctly in the following cases:

1)When using LPTMR as the trigger source and using LPO clock source, only when counter values of TSI scan are less than 7000.

2)When using LPTMR as the trigger source and the clock source is external oscillator(32.768khz), if the prescaler value and number of scan setup is less than 12.

Workaround: Use one of the following two methods for out of range interrupt:

1)If using LPTMR with LPO as the trigger source, ensure that the counter value reaches above 10,000 counts by fine-tuning the EXTCHRG, REFCHRG, NSCN and PS registers.

2)If using LPTMR with external oscillator as the trigger source, ensure that the NSCN and PS setup gives a value of higher than 12 scans. The number of scans formula is: (NSCN +1)*(2^PS).

e6396: sLCD: LCD_GCR[RVTRIM] bits are in reverse order

Errata type: Errata

Description: The four bits of LCD_GCR[RVTRIM] are in reverse order, in such a way that the LSB corresponds to bit 27 and the MSB corresponds to bit 24 of the LCD_GCR. The RVTRIM adjustment from lower voltage to higher voltage does not follow a linear increase in the LCD_GCR[RVTRIM] value. The RVTRIM adjustment should follow this sequence:

0,8,4,12,2,10,6,14,1,9,5,13,3,7,11,15

to achieve a linear increase from lower voltage to higher voltage.

The reset value of this field is still 8, which corresponds to a low voltage value of the VIREG.

Workaround: You can use a lookup table with the correct order of RVTRIM values for a linear change on the VIREG voltage (contrast). If planning to use a user-selectable contrast, a memory buffer is required to keep track of the logic value of the RVTRIM. When required to increase or decrease the contrast of the LCD, the buffer pointer should be increased or decreased accordingly and the corresponding value from the lookup table should be written to the LCD_GCR[RVTRIM].

To avoid a low voltage on VIREG after reset, LCD_GCR[RVTRIM] must be updated during the LCD initialization routine.

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