Freescale Semiconductor
Application Note

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Quad Flat Package (QFP)

1 Introduction

This document provides guidelines for handling and assembly of Freescale QFP packages during Printed Circuit Board (PCB) assembly.

Guidelines for PCB design, rework, and package performance information such as Moisture Sensitivity Level (MSL) rating, board level reliability, mechanical and thermal resistance data are included for reference.

2 Scope

This document contains generic information that encompasses various Freescale QFP packages assembled internally or at external subcontractors. It should be noted that the specific information about each device is not provided. This document serves only as a guideline to help users develop a specific solution. Actual experience and development efforts are still required to optimize the assembly process and application design per individual device requirements, industry standards such as IPC and JEDEC, and prevalent practices in user's assembly environment.

For assistance for more details or questions about the specific devices contained in this note, visit www.freescale.com or contact the appropriate product application team.

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3 Quad Flat Package (QFP)

Figure 1 shows the standard QFP offerings through Freescale. The exposed pad (denoted as – EP) version is also discussed.

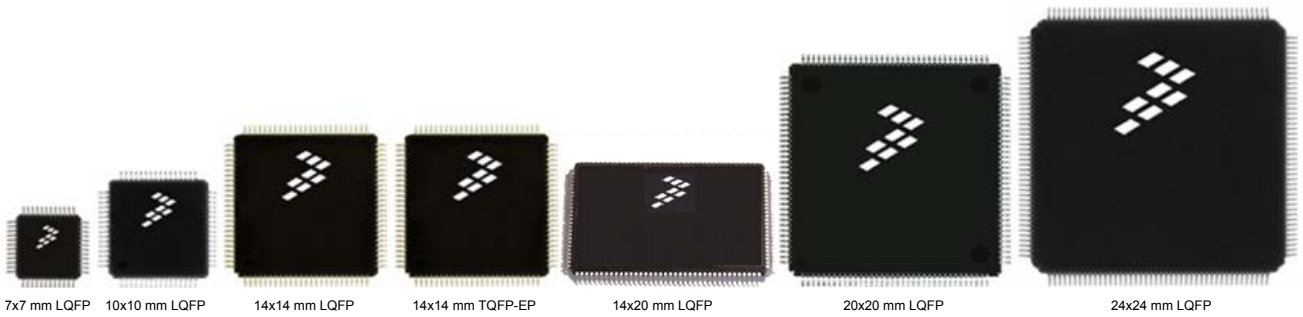


Figure 1. Standard Freescale QFP Offerings

3.1 Package Description

The QFP is a surface mount integrated circuit package. The standard form is a flat rectangular body, usually square, with leads extending from all four sides. The leads are formed in a gull wing shape to allow solid footing during assembly to a PCB. Standard Pb-free lead finish is Matte Tin.

Thermally enhanced QFPs may be offered with an exposed die pad and is denoted with the suffix '-EP'. The exposed pad is on the bottom of the QFP and acts as a ground connection and/or a heat sink for the package. The pad can be soldered to the PCB to dissipate heat.

3.2 Package Dimensioning

QFP are offered in industry standard sizes and thicknesses with various options of lead quantity and pitch. See Table 1. Refer to Freescale package case outline drawings to obtain detailed dimensions and tolerances.

Table 1. Standard Freescale QFP Offerings[(1)]

Units in mm		Package Dimensions										
Package	**Thickness**	**4x4**	**5x5**	**7x7**	**10x10**	**12x12**	**14x14**	**14x20**	**20x20**	**24x24**	**28x28**	**32x32**
LQFP	1.4	X	X	X	X	X	X	X	X	X	X	
LQFP-EP	1.4			X	X			X		X		
TQFP-EP	1.0					X	X					
QFP	>1.6				X		X	X			X	X
PQFP	3.6									X		

Notes

1. This table lists all the Freescale packages this application note applies to. However, some types of packages listed above may not be available for new product use. Check with FSL sales team.

3.3 Package Cross-section

The cross-section drawings in Figure 2 are included to show representative internal leadframe design differences between QFP and EP packages. Standard QFP packages have mold compound which encompasses the entire bottom side of the package, while the EP design exposes the die pad, which increases thermal performance.

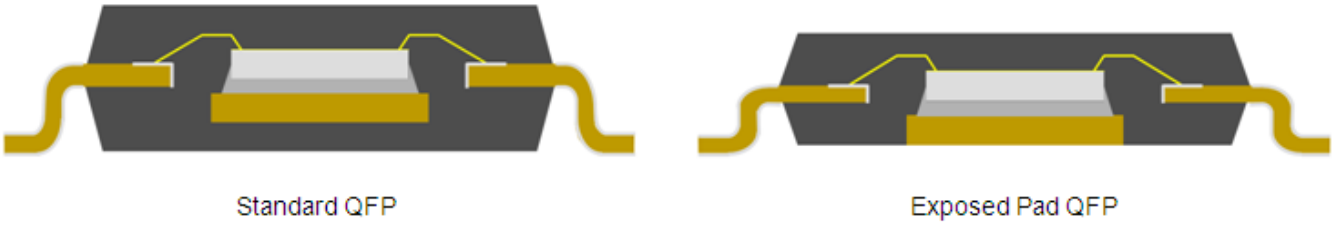


Figure 2. Difference Between Standard and Exposed Pad QFP

4 Printed Circuit Board Guidelines

4.1 PCB Design Guidelines and Requirements

As the package size shrinks and the lead count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Special care must be taken when preparing for test, especially in the test contactor cavity design and contactor pin location. Part interchangeability is also a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier may have issues (manufacturing yield and/or solder joint life) with the other supplier's parts. When more than one source is expected, the PCB layout should be optimized for both parts. Additional information of this topic is provided in PCB Design Guidelines.

A proper PCB footprint and stencil designs are critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package Case Outline drawings are available at www.freescale.com. Follow the procedures in Case Outline Drawing, MCDS and MSL Information Download. An example 14 x 14 mm LQFP Case Outline drawing is shown in Figure 3. The goal is a well soldered QFP gull wing lead as is shown in Figure 4.

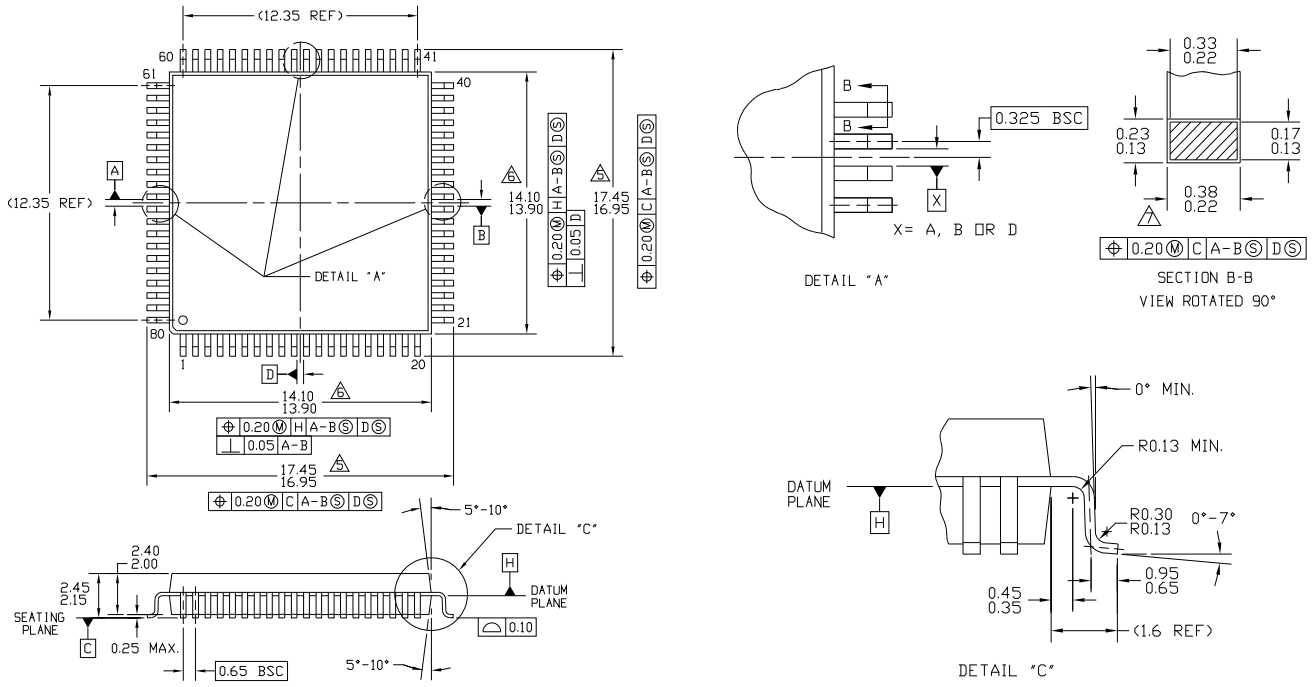


Figure 3. Example of 14 x 14 mm LQFP Case Outline Drawing

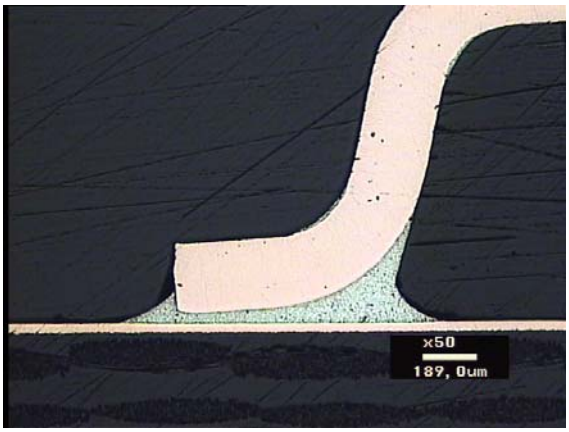


Figure 4. 50x Magnified Optical Microscope Image of a Well Soldered QFP Lead Based on a Robust Pad Design

4.2 PCB Pad Design

4.2.1 General Pad Guidelines

Freescale follows the Generic Requirements for Surface Mount Design and Land Pattern Standards from the Institute for Printed Circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the IPC's web site landpatterns.ipc.org and include guidelines for most QFPs, based on assumed package dimensions. Some general guidelines for QFP footprints are:

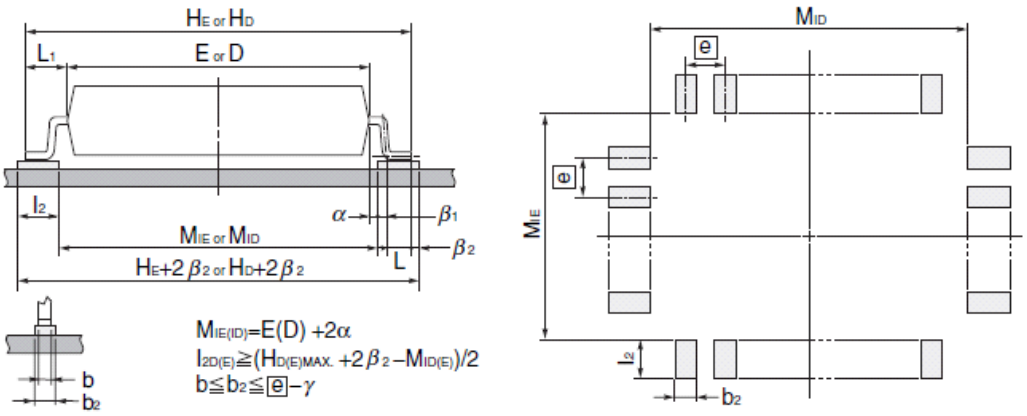
- Lead foot should be approximately centered on the pad with equal pad extension from the toe and the foot
- Typically, the pad is extended 0.5 mm beyond the QFP foot at both the heel and the toe
- Care should taken that PCB pads do not extend under the QFP body, which can cause issues in assembly
- Pad width should be approximately 60% of the lead pitch – See Table 2.
- Pitch needs to be designed in metric using the exact dimensions of 0.40, 0.50, 0.65, and 0.80 mm

Note: Some legacy products may have alternate pitches.

Table 2. Recommended Pad Widths as a Function of Lead Pitch

Lead Pitch (mm)	Pad Width (mm)
0.40	0.26
0.50	0.30
0.65	0.38
0.80	0.50

Using the example of the 14 x 14 mm QFP in Figure 3, the PCB pad width should be designed at 0.38 mm for this 0.65 mm lead pitch package. To determine the placement and length of the pads, obtain the tip to tip dimension from the package drawing (Figure 3). It has a range of 16.95 to 17.45 mm or a nominal dimension of 17.20 mm. Similarly, the foot length has a range of 0.65 to 0.95 mm with a nominal of 0.80 mm. So, the pad should be 1.80 mm in length which is the 0.80 mm nominal foot length with a 0.50 mm extension on the heel and toe sides. See Figure 5.



○ Dimension Parameter (Unit : mm)

e	1.00	0.80	0.65	Remark
α	0.20	0.20	0.20	Washability of the printed-circuit board
β1	0.50	0.50	0.50	Soldering strength
β2	0.20	0.20	0.20	Pattern accuracy of the solder mask and visual inspection soldering.
γ	0.30	0.30	0.30	Determined by the margin of safety taken into consideration as a measure for coping with the soldering bridge.

(The reference value according to EIAJ ED-7404 (old standard))

Figure 5. QFP Land Pattern Dimensions

4.2.2 Thermal/Electrical Pad Guidelines

Exposed pad QFP packages are thermally/electrically enhanced leadframe technology based, and the bottom of the package provides the primary heat removal path as well as excellent electrical grounding to the PCB. In an EP package the die attach paddle is down-set within the package such that the pad is exposed during the mold process, as shown in Figure 6. White arrows here stand for heat flow. To optimize thermal performance, the PCB design should include a thermal plane, as shown in Figure 6.

Although the land pattern design for EP lead attachment on the PCB should be the same as that for conventional, non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled packages may involve some extra steps, depending upon the current rework practice within the company.

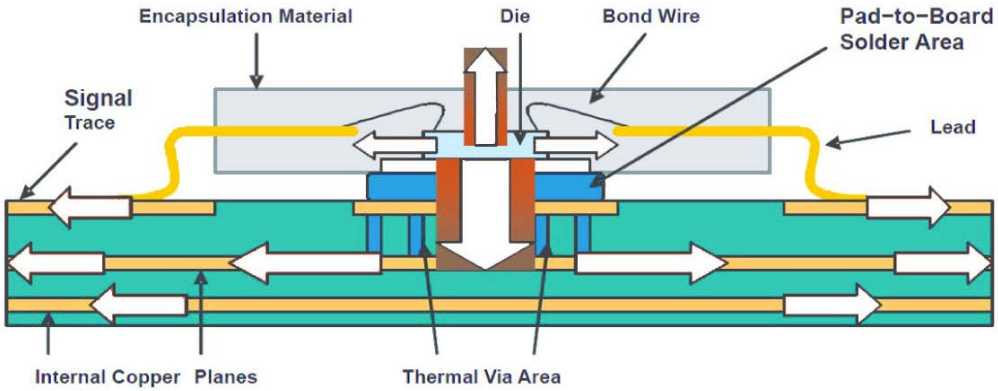


Figure 6. Cross-section of EP Package with Heat Transfer Schematic

4.2.3 Spacing between PCB PADs for Leads and Exposed Pad

To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 7. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the solderable area, as defined by the solder mask, should be at least the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the land pattern and the inner edges of leads pad pattern to avoid any shorts. This topic is discussed in more detail in Solder Stencil/Solder Paste.

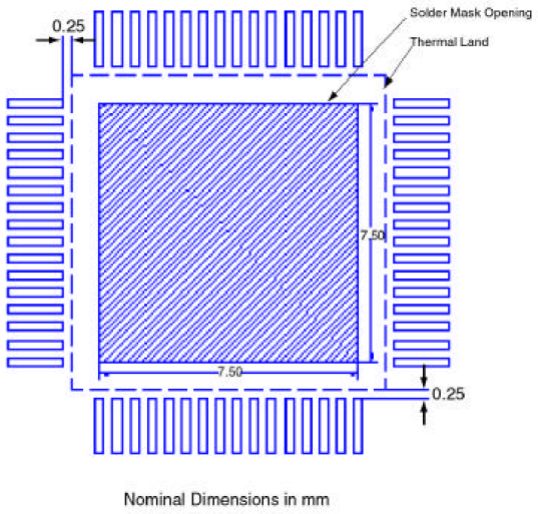


Figure 7. Example of Exposed Pad Land Pattern

4.2.4 Vias in the PCB EP Pad

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 1.2 mm grid, as shown in Figure 8.

It is also recommended that the via diameter should be 0.30 to 0.33 mm with 1.0 oz. copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad and the thermal land. If the copper plating does not plug the vias, the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.1 mm (4.0 mils) larger than the via diameter.

Note: These recommendations are to be used as a guideline only.

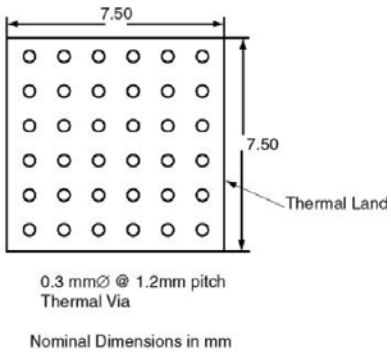


Figure 8. PCB Exposed Pad Via Grid

4.2.5 Via Pad Finishes

Almost all PCB finishes are compatible with QFPs including Hot Air Solder Leveled (HASL), Organic Solderability Protectant (OSP), Electroless Nickel Immersion Gold (ENIG), Immersion Sn and Immersion Ag.

4.2.6 Solder Mask Layer

In general, solder mask should be pulled away from both the Input/Output pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads may be too thin for the solder mask resulting in the solder mask lifting off from the PCB. A potential solution is modification of the solder mask along the pad-to-pad spacing so only the “toes” of the pads are covered with solder mask for better PCB strength.

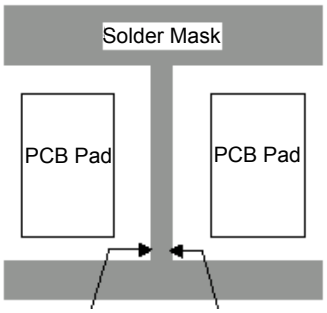


Figure 9. Pad and Solder Mask with Thin Webbing

5 Board Assembly

5.1 Assembly Process Flow

A typical Surface Mount Technology (SMT) process flow is depicted in the SMT Process Flow in Figure 10.

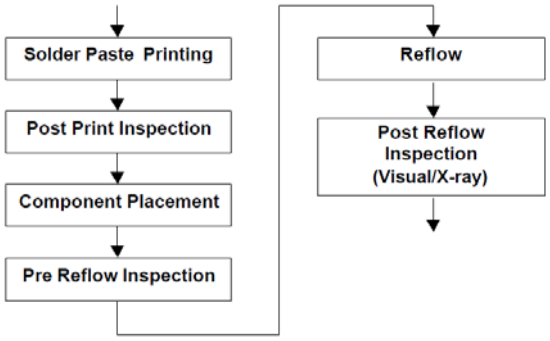


Figure 10. SMT Process Flow

5.2 Solder Stencil/Solder Paste

For maximum thermal/electrical performance, it is required that the exposed pad on the package be soldered to the land pattern on the PCB. This can be achieved by applying solder paste on both the pattern for lead attachment as well as on the land pattern for the exposed pad. While for standard (non-thermally/electrically enhanced) leadframe based packages the stencil thickness depends on the lead pitch and package co-planarity, the package standoff must also be considered for the thermally/electrically enhanced packages to determine the stencil thickness. For a nominal standoff of 0.1 mm, the stencil thickness of 0.13 – 0.20 mm, depending upon the pitch, is recommended. The EP stencil aperture openings should be 0.25mm smaller than the copper pads on PCB, as shown in Figure 11. This will allow for proper registration of the stencil to the pad pattern. A large stencil opening may result in poor release. To overcome this, the aperture opening should be subdivided into an array of smaller openings, similar to the thermal land pattern shown in Figure 12. These guidelines will result in the solder joint area to be about 80 to 90% of the exposed pad area.

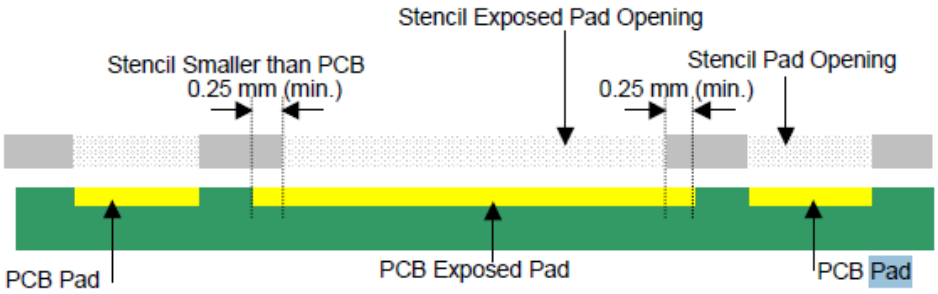


Figure 11. Reduced Solder Stencil Aperture for Exposed Pad

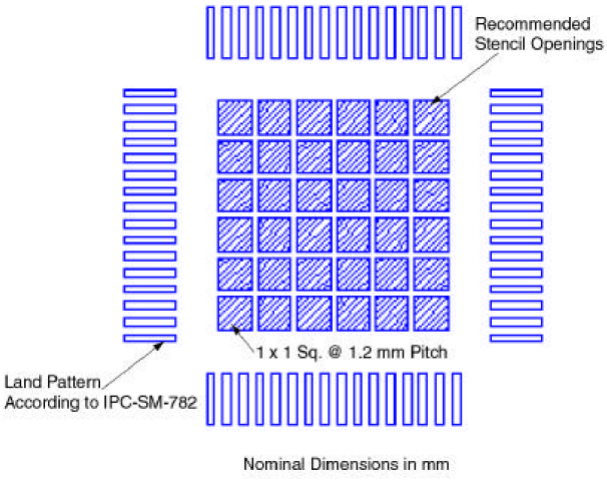


Figure 12. Recommended Stencil Design

An array design pattern is recommended in the stencil opening for the large thermal pad region. A large opening or aperture in the thermal region allows “scooping” to occur during screen printing. Other reasons for segmenting the thermal regions include minimizing solder standoff mismatch with terminal pads, minimizing solder voids in the thermal region, and minimizing chances of bridging with terminal pads.

Several different array patterns are being recommended in this section. Smaller QFP package sizes do not require any thermal pad pattern on the PCB and stencil, unless to minimize solder voids. On larger packages, stencil thermal openings should be segmented in smaller regions. Examples are shown in Figure 13. The spacing between segments either on the stencil or on the PCB should be 0.15 mm or more. Narrower spacing between segments can become a manufacturing issue.

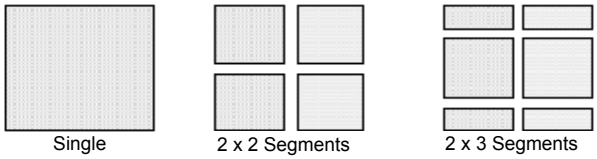


Figure 13. Segmented Stencil Openings

The stencil opening should be approximately 50% – 80% of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering by removing minor surface contamination and oxidation. There are two different flux systems commonly available. The first type requires cleaning such as standard rosin chemistries and water soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions or aqueous/saponifier solutions while the water soluble chemistries are cleaned with pure water. The second flux system type requires no cleaning, but normally a little residue will remain on the PCB after soldering. In general, it is recommended to use a no-clean solder paste. However, the end user should evaluate their entire process and usage to ensure desired results.

The spread of solder paste during reflow partially depends upon the solder paste alloy. SnPb solder alloys spread significantly better than the many lead-free pastes (i.e., SnAgCu, SnAgBiCu, etc.), given the same reflow temperature.

5.3 Component Placement

The high lead interconnection and insertion density suggests that precise and accurate placement machines are preferred. To meet this tight requirement, the placement machine should be equipped with optical recognition systems, i.e., vision system, for the centering of the PCB as well as the components during the pick and place motion. A placement accuracy study is recommended to calculate compensations required. Freescale follows EIA-783 standard for tape and reel orientation as is shown in Figure 14.

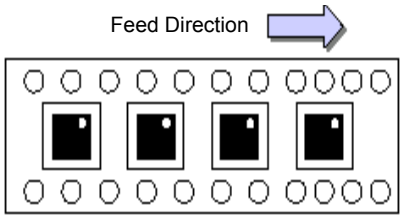


Figure 14. QFP Orientation in Tape and Reel

5.4 Soldering

A typical profile band is shown in Figure 15. The actual profile parameters depend upon the solder paste used and recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine tuned to establish a robust process. In most cases, thermocouples should be placed under the heaviest thermal mass device on the PCB to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB will reach reflow temperatures as well.

Nitrogen reflow is recommended to improve solderability and to reduce defects such as solder balls.

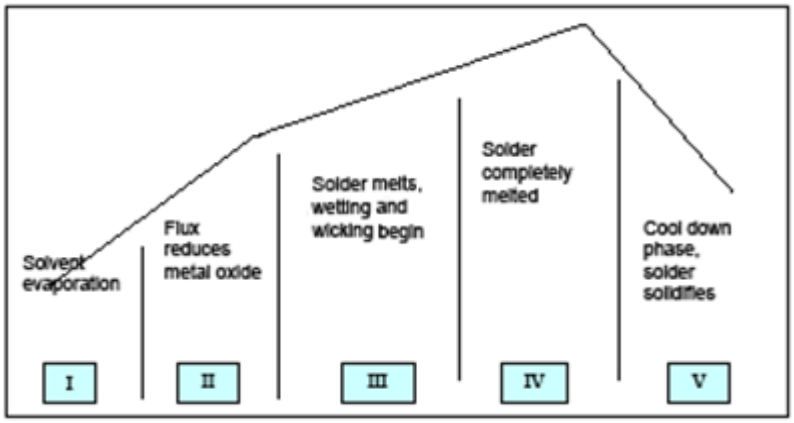


Figure 15. General Solder Reflow Phases

It is also recommended to monitor the temperature profile of package top surfaces to validate the package peak temperature does not exceed MSL classification of individual devices.

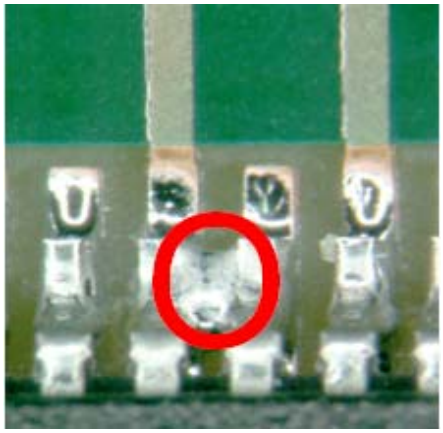
For all devices on the PCB, the solder paste needs to be taken into account for the reflow profile. Every paste has a flux, and the flux dominates the reflow profile for steps like soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus a “safety” margin to ensure that all solder paste on the PCB reflows. The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

The reflow profile should follow the paste supplier's "recommended" profile. Deviation from the recommended profile should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as "x" and "y" lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or "x" and "y". The goal is have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use to remove Cu-oxide build up.

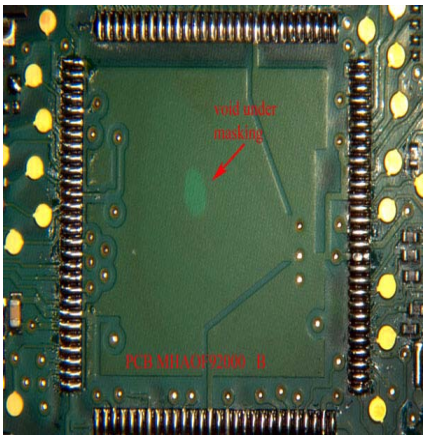
5.5 Inspection

Whenever possible, non-destructive vision/optical inspection and X-ray inspection are recommended to verify any open or short-circuit after reflow soldering.

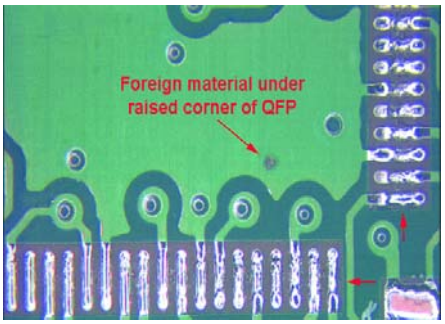
5.6 Common QFP Defects



Solder Short (fine pitch)



Blister in solder mask
which caused an open lead



Foreign matter under QFP
causing open corner leads

Figure 16. Three Common QFP Defects

6 Repair and Rework Procedure

The following items must be observed when performing the repair and rework

- The influence of the heating on adjacent packages must be minimized. Care should be taken to not exceed the temperature rating of the adjacent package.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- Freescale follows industry standard component level qualification requirements which include three solder reflow passes. The three reflow passes simulate board level attach to a double sided board and includes one rework pass. The removed QFP package should be properly disposed of so that they will not mix in with new components.

6.1 Repairing

Repair of single solder joints is generally possible but requires proper tools. A soldering iron can be used to repair soldering defects for packages that have leads which extend beyond the package periphery, including the QFP package. Difficulty with fine pitch applications may be observed with the use of soldering irons. The soldering iron temperature and usage must be set so that the package surface temperature does not exceed its maximum allowable temperature.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the heating methods described in the below section.

A typical QFP rework flow process is:

1. Tooling preparation
2. Package removal
3. Site redressing
4. Solder paste printing
5. Remount package
6. Reflow soldering
7. Visual check

Note: Freescale product quality guaranty/warranty does not apply to products that have been removed, thus, component reuse should be avoided if at all possible.

In any rework, the PCB will be heated. The thermal limits of PCB and components (e.g. MSL information) have to be followed. During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. To prevent moisture induced failures, it is recommended that the PCBs and components have had strict storage control with a controlled environment such as dry air or Nitrogen. In addition, a prebake (e.g. 125 °C for 24 hours for boards with SMT components or 95 °C for 24 hours for boards with temperature sensitive components) is recommended to remove the moisture from components and PCB prior to removal of the QFP, if the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly.

Individual process steps for reworking a QFP package are as follows:

6.2.1 Tooling Preparation

Various rework systems are available on the market – In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing QFP packages, a system should meet the following requirements:

- Heating – Controlled hot air transfer (temperature and air flow) to both the QFP package and its mounted PCB is strongly recommended. The heating should be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side (component side). Nitrogen can be used instead of air. Additional information can be found in Package Removal.
- Vision system – The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- Moving and additional tools – Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

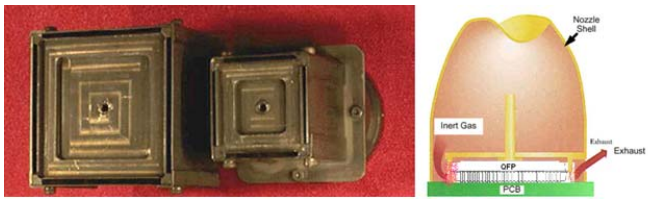


Figure 17. Examples of Typical QFP Heating Nozzles

6.2.2 Package Removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB as this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- Moisture removal: Dry bake components before removal at 125 °C for 16 – 24 hours for boards with SMT components or 95 °C for 16 – 24 hours for boards with temperature sensitive components.
- Temperature profile: During de-soldering, ensure the package peak temperature is not higher and temperature ramps are not steeper than the standard assembly reflow process.
- Mechanics: Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB which may limit failure analysis of the package. For large packages, pipettes can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, hot air should be applied from the top and bottom heaters. An air nozzle of correct size should be used to conduct the heat to the QFP component leads such that a vacuum pick up tool can properly remove the component. The temperature setting for the top heater and the bottom heater is dependent on the component rating. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed to allow heating of the entire printed circuit board to raise work efficiency.

6.2.3 Site Redressing

After the component is removed, the PCB pads have to be cleaned to remove solder residue to prepare for the new component placement. This may be complete by vacuum de-soldering, solder sucker, solder wick braid, etc. after applying flux. Remaining solder residue and projections cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transfer, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This is typically a manual operation which is directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes can contribute to bad solder joints (e.g. steel brushes). Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

6.2.4 Solder Paste Printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 18. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are at close proximity with the QFP components, and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

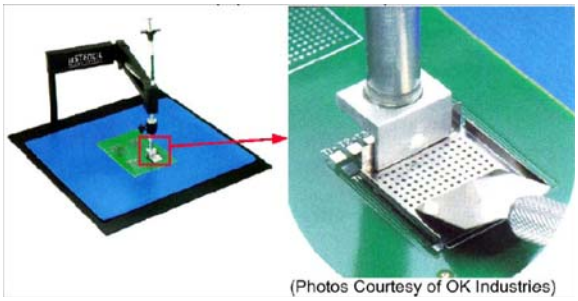
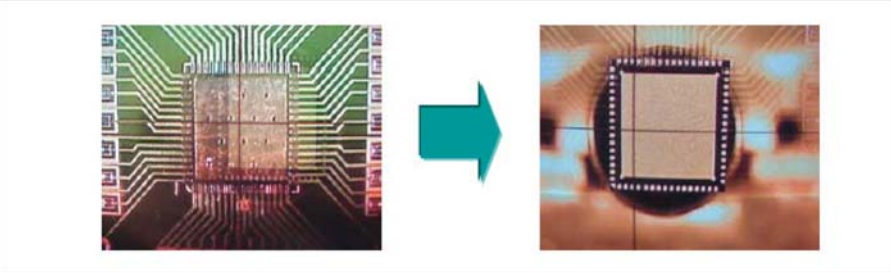


Figure 18. Mini Stencil and Mini Squeegee

6.2.5 Package Remount

After preparing the site, the new package can be placed onto the PCB. When remounting the package, it is recommended to use rework equipment that has good optical or video vision capability. A split light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY which enables correct soldering. See Figure 19.

Regular lead array QFP exhibits self-alignment in any direction including X-axis shift, Y-axis shift, and rotational misplacement. Exposed pad may not exhibit a strong self-alignment capability and precise placement of the component on the PCB is required.



PCB Image Superimposed QFP on PCB

Figure 19. Split Light Placement Images

6.2.6 Reflow Soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in Soldering. During soldering, the package peak temperature and temperature ramps cannot exceed those of the standard assembly reflow process.

In IR or convection processes the temperature can vary greatly across the PC board depending on the furnace type, size, and mass of components, and the location of components on the assembly. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework do have a higher potential to create conductive traces /corrosion etc. compared to standard materials, PCB might need to be cleaned if they do not clean in the “normal” process, or the rework was not done using “no clean” materials.

7 Board Level Reliability

7.1 Testing Details

Solder Joint Reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. Information provided here is based on experiments executed on QFP device using a daisy chain bond configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution. For automotive grade product applications, Freescale typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40 °C to +125 °C. Consumer SJR temperature cycling conditions may vary widely depending on the application and specific user. Typically, Freescale consumer SJR testing is performed from 0 °C to +100 °C.

Table 3. shows the Freescale standard test set-up for performing board level solder joint reliability testing.

Table 3. Board Level Reliability Setup

Board Level Reliability Testing: Material and Test Setup	
PCB Board	• 1.58 mm thickness • Four Cu layer • OSP surface finish
Test Board Assembly	• Pb-free solder paste SAC387 • Reflow peak temperature for SAC assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 - 0.150 mm thickness (depending on the device pitch), Ni plated, laser cut and electro-polished stainless steel stencil
Cycling conditions	• Continuous in-situ daisy chain monitoring per IPC-9701A • Air-Temperature Cycling (ATC) for Automotive — -40 °C / +125 °C — 15 minute ramp/ 15 minute dwell — 1.0 hour cycle time • Air-Temperature Cycling (ATC) for Commercial & Industrial — 0 °C / +100 °C — 10 minute ramp/ 20 minute dwell — 1.0 hour cycle time
Package Test Vehicle	• Production BOM package including die (die mechanically present, without wire bond connection) • Daisy chain bond pattern on lead frame to allow continuous monitoring

7.2 Solder Joint Reliability Results

Freescale experimentally gathers board-level reliability data for a variety of packages. Results from these experiments, including Weibull plots, may be requested by customers by contacting the Freescale sales team.

8 Thermal Characteristics

8.1 General Thermal Performance

Since the thermal performance of the package in the final application will depend on a number of factors (i.e. board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by Freescale should only serve as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, Freescale recommends to run application specific thermal calculations in the design phase to confirm the on-board thermal performance.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific and will depend on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package Thermal Characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors that need be considered in PCB design and thermal rating of the final application amongst others are:

- Thermal resistance of the PCB (thermal conductivity of PCB traces, number of thermal vias, thermal conductivity of thermal vias)
- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are usually given in the Freescale product data sheets as appropriate. Product data sheets are available under www.freescale.com. More detailed thermal properties may be requested by customers.

8.3 Package Thermal Properties – Definition

The thermal performance of QFP packages with and without exposed pad is typically specified by definition of thermal properties such as $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W). Thermal characterization is performed by physical measurement and running complex simulation models under the following conditions:

- Two thermal board types: Single layer board (1s) per JEDEC JESD51-3 & JESD51-5 (exposed pad packages only), four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Four boundary conditions: Natural convection (still air) per JEDEC JESD51-2, forced convection per JEDEC JESD51-6, thermal test board on ring style cold plate method per JEDEC JESD51-8 and cold plate method per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: Theta Junction-to-Ambient Natural Convection (Still Air)

Junction-to-ambient thermal resistance (Theta-JA or RθJA per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths: (1) convection and radiation off the exposed surface of the package and (2) conduction into and through the test board followed by convection and radiation off the exposed board surfaces.

8.3.2 $R_{\theta JMA}$: Theta Junction-to-Moving-Air Forced Convection

Junction-to-Moving-Air (Theta-JMA or RθJMA per JEDEC JESD51-6) is similar to $R_{\theta JMA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: Theta Junction-to-Board

Junction-to-board thermal resistance (Theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement is done using a high effective thermal conductivity four layer test board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only) on a ring style cold plate. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: Theta Junction-to-Case

Junction-to-Case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case is defined as either the temperature at the top of the package (for non-exposed pad packages), or the temperature at the bottom of the exposed pad surface (for exposed pad packages). For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 Ψ_{JT} (Psi JT): Junction-to-Package Top

Junction-to-Package top (Psi JT or Ψ_{JT}) is indicating the temperature difference between package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) or forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be mixed up with the parameter $R_{\theta JC}$:

$R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while Ψ_{JT} is the value of the temperature difference between package surface and junction temperature, usually in natural convection.

8.4 Package Thermal Properties – Example

An example of the thermal characteristics as typically shown in the Freescale product data sheet is shown in Table 4. The example applies to a package size 20 mm x 20 mm x 1.4 mm, pitch 0.5 mm, die size ~ 6.0 mm x 6.3 mm.

Table 4. Thermal Resistance Example

Rating	Board Type	Type	Value	Units	Notes
Junction to Ambient (Natural Convection)	Single Layer Board (1s)	$R_{\theta JA}$	44	°C/W	(2) (3)
Junction to Ambient (Natural Convection)	Four Layer Board (2s2p)	$R_{\theta JA}$	36	°C/W	(2) (4)
Junction to Ambient (@200 ft.min)	Single Layer Board (1s)	$R_{\theta JMA}$	35	°C/W	(2) (4)
Junction to Ambient (@200 ft.min)	Four Layer Board (2s2p)	$R_{\theta JMA}$	30	°C/W	(2) (4)
Junction to Board	---	$R_{\theta JB}$	24	°C/W	(5)
Junction to Case	---	$R_{\theta JB}$	8	°C/W	(6)
Junction to Package Top	Natural Convection	Ψ_{JT}	2	°C/W	(7)

Notes

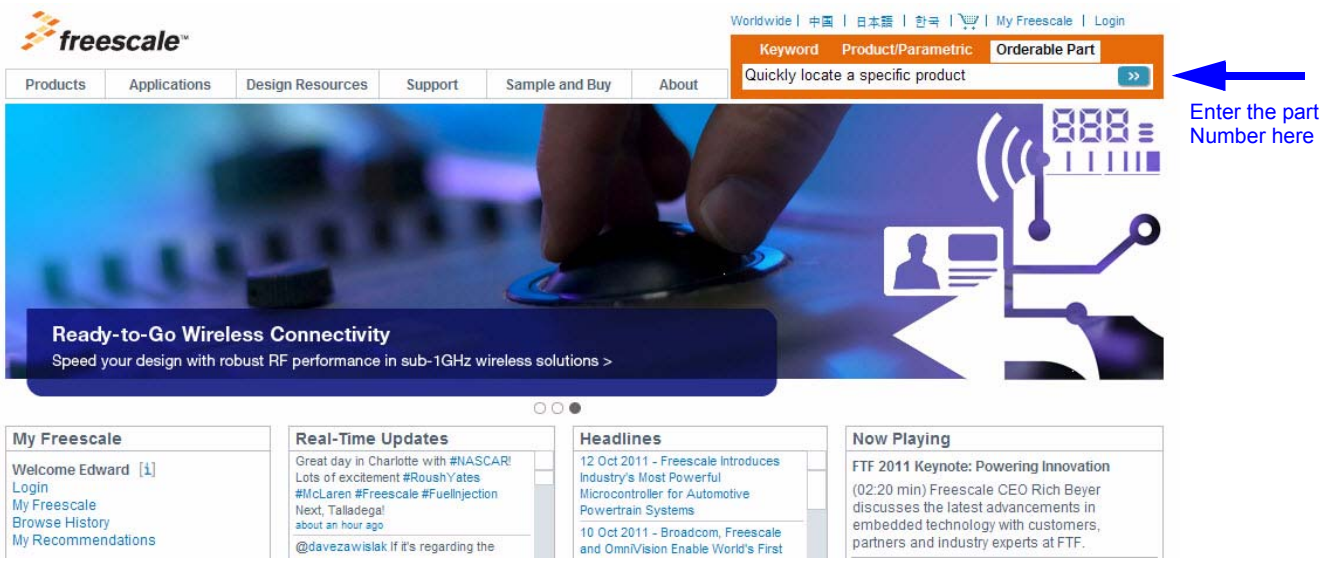
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.
3. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
4. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
7. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT

9 Case Outline Drawing, MCDS and MSL Rating

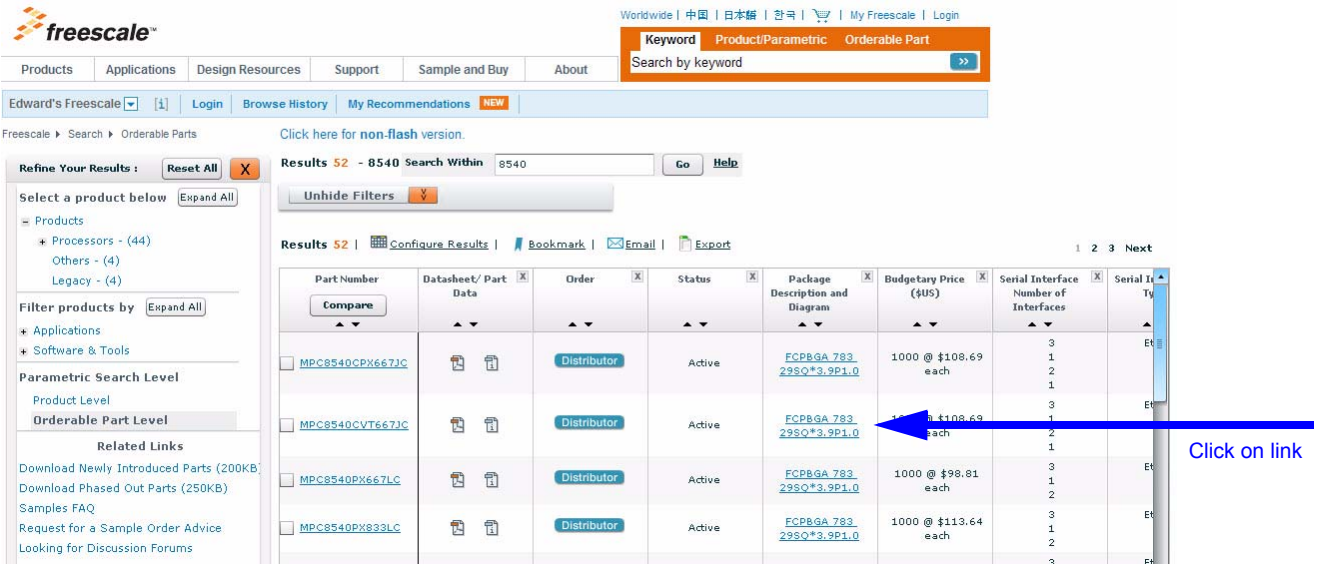
9.1 Case Outline Drawing, MCDS and MSL Information Download

The complete case outline drawing and the Material Composition Declaration Sheet (MCDS), following the IPC-1752 reporting format, can be downloaded from the Freescale web site as PDF file. Information on product specific Moisture Sensitivity Level (MSL) is also available on the web side. To download the documents, use the following instructions:

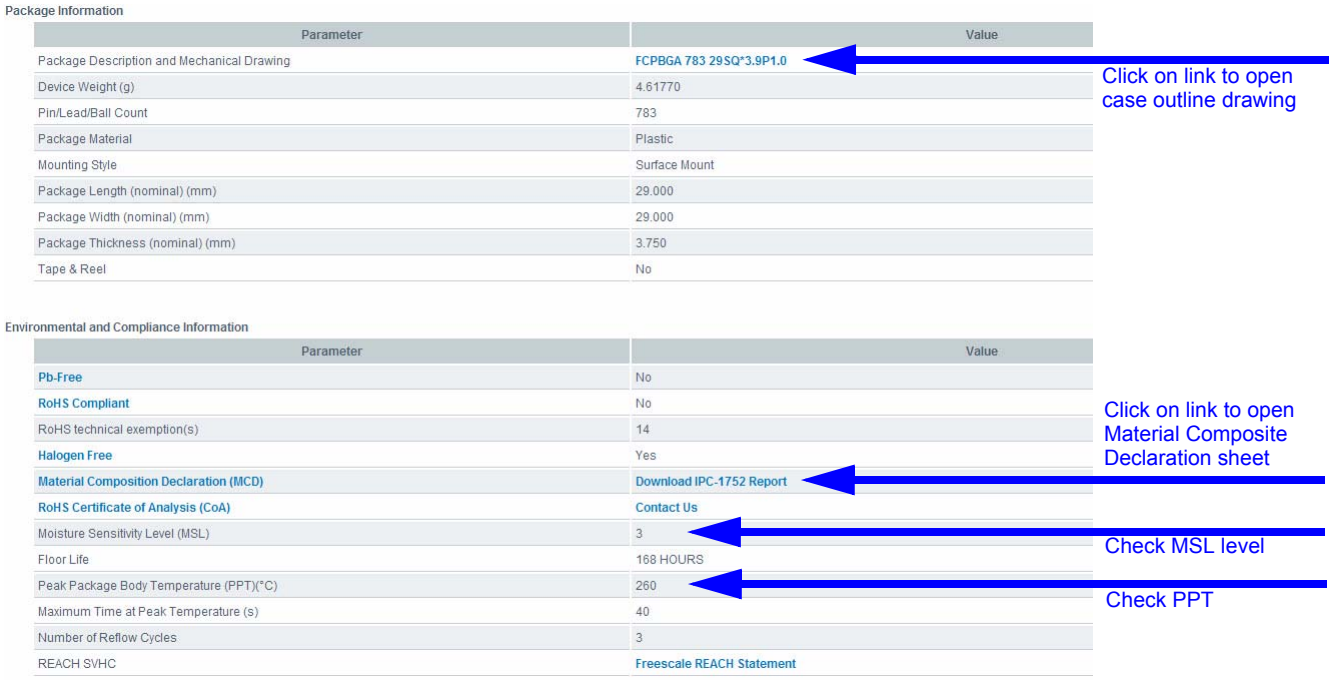
1. Go to http://www.freescale.com
2. Click on “ORDERABLE PART” in the orange box on the upper right of the screen
3. Enter the Freescale product part number in the upper right entry box “Enter Part Number”.



4. The next screen will be a return of search results if anything, and list all formal and existing part numbers related to the search term. On the search results screen, identify the row that contains the desired part number. Click on the package description link in the “Package Description and Diagram” column on the row of part number of interest.



5. The next screen shows the “Product Summary Page”.
   a) Click on the package description link in the “Package Information” table (FCPBGA 783 29SQ*3.7P1.0 in the following example) to open the case outline pdf file or
   b) Click on the “Download IPC-1752 Report” link in the “Environmental and Compliance Information” table to open the material composition declaration sheet pdf file or
   c) Check out the moisture sensitivity level (MSL) and the maximum allowed peak package body temperature (PPT) shown in the related columns:



9.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) indicates the floor life of the component and its storage conditions and handling precautions after the original container has been opened. The permissible time (from opening the moisture barrier bag until the final soldering process) that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component that are high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or lead-frame, wire bond damage, die damage, and internal cracks. In the most severe cases the component will bulge and pop, known as the “popcorn” effect.

Thus it is necessary to dry moisture-sensitive components, seal them in a moisture barrier antistatic bag with a desiccant and a moisture indicator card which is vacuum sealed according to IPC/JEDEC J-STD-033, and only remove them immediately prior to assembly to the PCB.

Table 5. presents the MSL definitions per IPC/JEDEC's J-STD-20. Refer to the “Moisture Sensitivity Caution Label” on the packing material, which contains information about the moisture sensitivity level of Freescale products. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and the maximum reflow temperature that shall not be exceeded during board assembly at the customer’s facility.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a Moisture Barrier Bag (MBB), the components are required to be baked prior to the assembly process. Refer to imprints/labels on the respective packing to determine allowable maximum temperature.

The lower the MSL value, the less care is needed to store the components. The QFP package MSL reliability is dependent upon the different supplier material set and package size. Table 6. depicts the best case MSL for each package size at the time of this document’s release. Freescale packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 5. MSL Descriptions

Level Rating	Floor Life	
	Time	Conditions
1	Unlimited	30°C/85% RH
2	1 Year	30°C/60% RH
2a	4 Weeks	30°C/60% RH
3	168 Hours	30°C/60% RH
4	72 Hours	30°C/60% RH
5	48 Hours	30°C/60% RH
5a	24 Hours	30°C/60% RH
6	TOL (8)	30°C/60% RH

Notes
8.TOL = Time on Label

Table 6. MSL Capability of QFP Packages[8]

Package type	Body Size L x W	Lead Count	MSL	PPT
TQFP-EP 1.0 mm body thickness	12x12	80	3	260
	14x14	100/128	3	260
	4x4	24	3	260
	5x5	32	3	260
	7x7	32/48	3	260
	10x10	44/52/64	3	260
LQFP 1.4 mm body thickness	12x12	80	3	260
	14x14	64/80/100/128	3	260
	14x20	128	3	260
	20x20	112/144	3	260
	24x24	160/176	3	260
	28x28	208	3	260
LQFP-EP 1.4 mm body thickness	7x7	48	3	260
	10x10	64	3	260
QFP >1.6 mm body thickness	10x10	44	3	260
	14x14	64/80/100	3	245/250
	14x20	100/128	3	245
	28x28	144/160/208	3	245
	32x32	240	3	245
PQFP 3.6 mm body thickness	29x24	132	3	245

Notes

9. This table and application note list all the FSL packages this application note applies to, but some types of packages listed above may not be available for new product use. Check with FSL sales team

10 Package Handling

10.1 Handling Electrostatic Discharge Sensitive Devices

Semiconductor Integrated Circuits (ICs) and components are Electrostatic Discharge Sensitive devices (ESDS) and proper precautions are required for handling and processing them. Electrostatic Discharge (ESD) is one of significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing should be considered. Following industry standards describe detailed requirements of proper ESD controls and Freescale recommends users to meet the standards before handling and processing ESDS.

- JESD615-A – Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-101/61340-5 – Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling Moisture Sensitive Surface Mount Devices

QFPs are Moisture/Reflow Sensitive Surface Mount Devices (SMD) and proper precautions are required for Handling, Packing, Shipping and Use. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in Moisture Sensitivity Level, during solder reflow, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concern, and proper handling of SMDs should be considered.

Dried Moisture Sensitive SMDs are placed in Tray or Tape and Reel, and dry packed for proper transportation and storage. SMDs are sealed with desiccant material and a Humidity Indicator Card inside of a MBB. Shelf life of dry packed SMDs are 12 months from the dry pack seal date when stored in $\leq$40 °C/90%RH environment.

Proper use and storage of Moisture Sensitive SMDs are required after MBB is opened. Improper use and storage will increase various quality and reliability risks. SMDs that will be subjected to reflow solder or other high temperature process must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033B standard. Baking of SMDs is required before mounting if any of followings are experienced.

- SMDs exposed to specified floor environment greater than specified period
- Humidity Indicator Card reading >10% for level 2a – 5a or >60% for level 2 devices when read at 23 ±5.0 °C environment.
- SMDs not stored according to J-STD-033B standard

Baking procedure, and more detailed requirements and procedures of handling Moisture Sensitive SMDs can be found in following industry standard.

- IPC/JEDEC J-STD-033B – Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

10.3 Packing of Devices

QFP devices are contained in Tray or Tape-and-Reel configuration, and Trays and Tape-and-Reel are dry packed for transportation and storage. Packing media are design to protect devices from electrical, mechanical and chemical damages as well as moisture absorption, but proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90%RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

- Tray
  - Freescale complies with standard JEDEC tray design configuration – See Figure 20
  - Pin one of devices will be oriented with lead one toward the chamfered corner of the tray
  - Trays designed to be baked for moisture sensitive SMDs, but temperature rating of tray should NOT be exceeded when devices are baked. Temperature rating can be found at end-tab of tray. Recommended baking temperature of trays is 125 °C.
  - Trays are typically banded together with 5+1 (five fully loaded trays and one cover tray) stacking and dry packed in Moisture Barrier Bag. Partial stacking (1+1, 2+1, etc.) is also available depending on individual requirements.

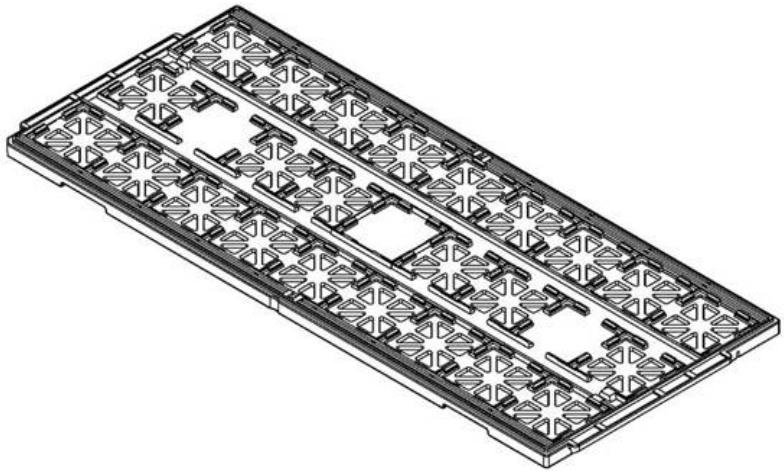


Figure 20. JEDEC Tray Example

- Tape and Reel
  - Freescale complies with EIA-481B and EIA-481C for carrier tape and reel configuration – See Figure 21
  - Freescale complies Pin one orientation of devices with EIA-481
  - Tape and Reels are NOT designed to be baked at high temperature
  - Each Tape and Reel is typically dry packed in Moisture Barrier Bag

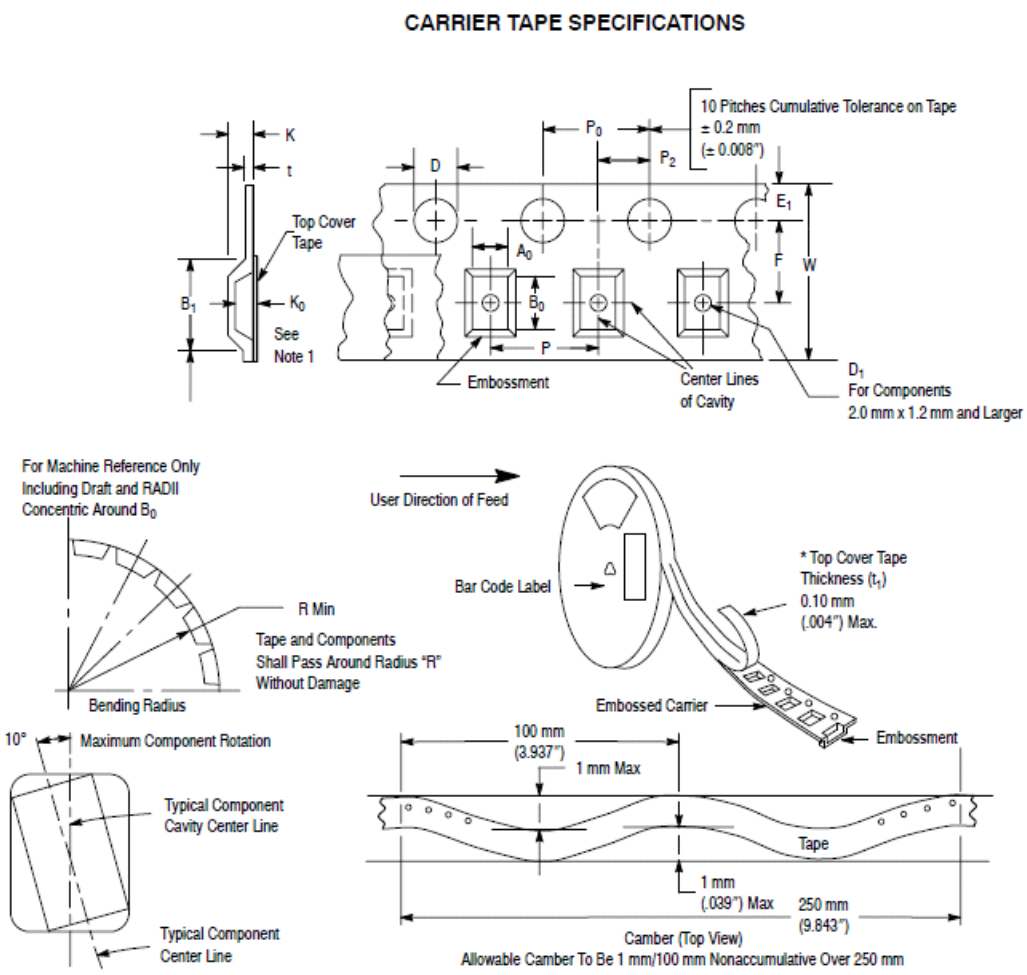


Figure 21. Tape and Reel Example

- Dry Packing
  - Trays and Tape-and-Reels, loaded with devices, are sealed in a moisture barrier bag which are labeled and packed in dedicated boxes with dunnage for the final shipment
  - Each dry pack bag contains a desiccant pouch as well as a humidity indicator card
  - Freescale encourages the recycling and reuse of materials whenever possible.
  - Freescale will not use packing media items processed with or containing class 1 Ozone Depleting Substances
  - Whenever possible, Freescale shall design its packing configurations to optimize volumetric efficiency and package density to minimize the amount packing that enters the industrial waste stream
  - Freescale shall comply with following Environmental Standards Conformance guidelines / directives:
  - ISPM 15: Guidelines for regulating wood packaging material in international trade
  - European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste.

11 References

Ref.	Name	Title	Date
[1]	IPC/JEDEC's J-STD-20C	Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices	January 2004
[2]	IPC/JEDEC J-STD-033B	Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices	January 2007
[3]	EIA-783	Guideline Orientation Standard for Multi-Connection Package (Design Rules for Tape and Reel Orientation)	November 1998
[4]	EIA/JESD51-2	Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)	December 1995
[5]	EIA/JESD51-3	Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages	August 1996
[6]	EIA/JESD51-5	Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms	February 1999
[7]	EIA/JESD51-7	High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages	February 1999
[8]	EIA/JESD51-8	Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board	October 1999
[9]	EIA/JESD 51-6	Integrated Circuits Thermal Test Method Environment Conditions – Forced Convection (Moving Air)	March 1999
[10]	MIL SPEC-883 Method 1012.1	Thermal Characteristics	February 2006
[11]	IPC-7351	Generic Requirements for Surface Mount Design and Land Pattern Standards	June 2010
[12]	EIA-783	Component Orientation	
[13]	EIA-481	Standards − Excerpts used to assure complete alignment	
[14]	JESD615-A	Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices	
[15]	IEC-101/61340-5	Specification for the Protection of Electronic Devices from Electrostatic Phenomena	
[16]	Åström, Anders	The Effect of Nitrogen Reflow Soldering in a Lead-Free Process	September 2003

12 Revision History

REVISION	DATE	DESCRIPTION OF CHANGES
1.0	10/2011	Initial release
2.0	2/2014	Updated Figure 16

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