NX18P3001

Bidirectional high-side power switch for charger and USB-OTG combined applications

Rev. 1 — 24 September 2013 **Product data sheet**

1. General description

The NX18P3001 is an advanced bidirectional power switch and ESD- protection device for combined USB-OTG and charger port applications. It includes undervoltage lockout, overvoltage lockout and overtemperature protection circuits designed to automatically isolate the power switch terminals when a fault condition occurs.

The device features two power switch input/output terminals (VBUSI and VBUSO), an open-drain acknowledge output ($\overline{\text{ACK}}$), an enable input which includes logic level translation ($\overline{\text{EN}}$) and low capacitance Transient Voltage Suppression (TVS) type ESD clamps for USB data and ID pins.

When $\overline{\text{EN}}$ is set HIGH the device enters a low-power mode, disabling all protection circuits. When used in combined charger and USB-OTG applications the 30 V tolerant VBUSI switch terminal is used as the supply and switch input when charging, for USB-OTG the VBUSO switch terminal is used as the supply and switch input.

Designed for operation from 3.2 V to 17.5 V, it is used in battery charging and power domain isolation applications to reduce power dissipation and extend battery life.

2. Features and benefits

- 30 V tolerant VBUSI supply pin
- Wide supply voltage range from 3.2 V to 17.5 V
- Automatic switch operation for charging within the supply range
- I_{SW} maximum 3 A continuous current
- Low ON resistance: 62 mΩ (typical) at a supply voltage of 5.0 V
- 1.8 V control logic input to open the switch
- Soft start turn-on slew rate
- Protection circuitry
  - Overtemperature protection
  - Overvoltage lockout
  - Undervoltage lockout
- ESD protection:
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E)
  - IEC61000-4-2 contact discharge exceeds 8 kV for pins VBUSI, D–, D+ and ID
- Specified from –40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	**Name**	**Description**	**Version**
NX18P3001UK	–40 °C to +85 °C	WLCSP12	wafer level chip-scale package, 12 bumps; body 1.36 × 1.66 × 0.51 mm (Backside Coating included)	NX18P3001

5. Marking

Table 2. Marking codes

Type number	Marking code
NX18P3001UK	X18P3

6. Functional diagram

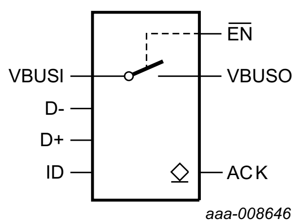


Fig 1. Logic symbol

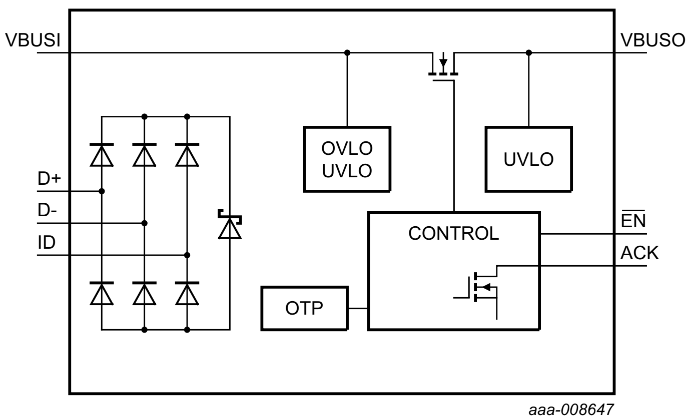


Fig 2. Logic diagram (simplified schematic)

7. Pinning information

7.1 Pinning

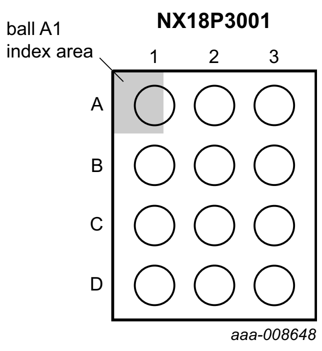


Fig 3. Pin configuration WLCSP12 package

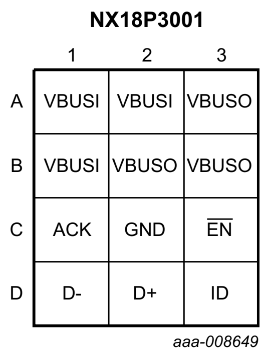


Fig 4. Ball mapping for WLCSP12

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBUSO	A3, B2, B3	VBUSO (output/input supply)
VBUSI	A1, A2, B1	VBUSI (input supply/output)
ACK	C1	acknowledge condition indicator (open-drain output)
GND	C2	ground (0 V)
EN	C3	enable input (active LOW)
D-	D1	ESD-protection I/O
D+	D2	ESD-protection I/O
ID	D3	ESD-protection I/O

8. Functional description

Table 4. Function table[1]

EN	VBUSI	VBUSO	ACK	Operation mode
L	< 3.2 V	< 3.2 V	Z	undervoltage lockout; switch open
L	3.2 V < VBUSI < 17.5 V	< 3.2 V	Z	enabled; switch closed; charging mode
L	< 3.2 V	> 3.2 V	Z	enabled; switch closed; OTG mode
L	X	X	0	overtemperature protection; switch open
L	> 17.5 V	X	0	overvoltage lockout; switch open
H	X	X	Z	disabled; switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.1 EN-input

A HIGH on EN disables the N-channel MOSFET and all protection circuits putting the device into a low-power mode. A LOW on EN enables the protection circuits and then the N-channel MOSFET.

8.2 Undervoltage lockout

When EN is LOW and VBUSI and VBUSO < 3.2 V, the UnderVoltage LockOut (UVLO) circuits disable the N-channel MOSFET. Once VBUSI or VBUSO > 3.3 V and no other protection circuits are active, the state of the N-channel MOSFET is controlled by the EN pin.

8.3 Overvoltage lockout

When EN is LOW and VBUSI > 17.5 V, the OverVoltage LockOut (OVLO) circuit disables the N-channel MOSFET and set the ACK output LOW. Once VBUSI < 17.35 V and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the EN pin.

8.4 Overtemperature protection

When EN is LOW and the device temperature exceeds 125 °C the OverTemperature Protection (OTP) circuit disables the N-channel MOSFET and sets the ACK output LOW. Once the device temperature decreases to below 115 °C and no other protection circuits are active, ACK is set high impedance and the state of the N-channel MOSFET is controlled by the EN pin.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. If OVLO or OTP circuits are activated the ACK output is set LOW to indicate that a fault has occurred. The ACK output returns to high impedance state automatically once the fault condition is removed or EN is HIGH.

9. Application diagram

The NX18P3001 typically connects a USB port in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level it is connected to.

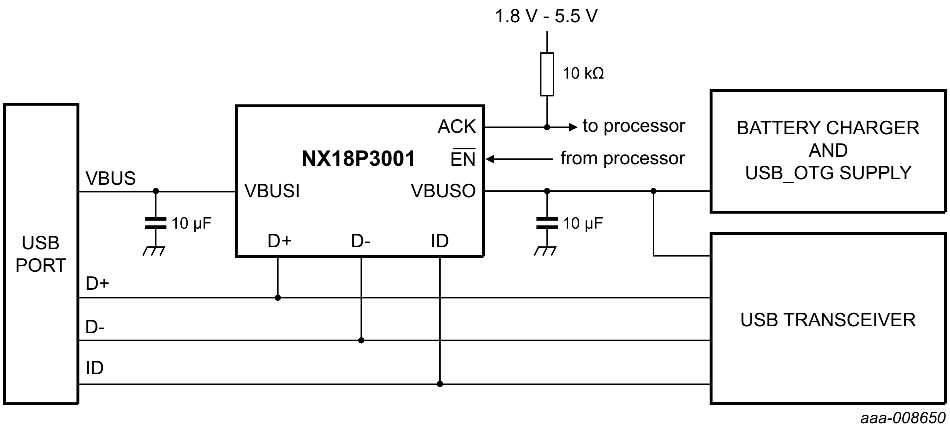


Fig 5. NX18P3001 application diagram

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUSI [1]	–0.5	+32	V
		VBUSO [1]	–0.5	+6.75	V
		$\overline{EN}$ [2]	–0.5	+6.0	V
		D-, D+, ID [1]	–0.5	+6.0	V
V_O	output voltage	ACK	–0.5	+6.0	V
I_{IK}	input clamping current	$\overline{EN}$: $V_I < –0.5$ V	–50	-	mA
I_{SK}	switch clamping current	VBUSI; VBUSO; $V_I < –0.5$ V	–50	-	mA
I_{SW}	switch current	T_{amb} = 85 °C	-	3	A
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C

Table 5. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
P_{tot}	total power dissipation	T_{amb} = –40 °C to +85 °C				
		WLCSP12 package	[3]		1.44	W

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

[3] For WLCSP12 package: P_{tot} derates linearly with 13.7 mW/K above 20 °C.

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUSI	3.0	30	V
		VBUSO	3.0	5.5	V
		$\overline{EN}$	0	5.5	V
$V_{I/O}$	input/output voltage	D-, D+, ID	0	5.5	V
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	73	K/W

[1] The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply. Try not to use any solder-stop varnish under the chip.

[2] Please rely on the measurement data given for a rough estimation of the $R_{th(j-a)}$ in your application. The actual $R_{th(j-a)}$ value may vary in applications using different layer stacks and layouts

13. Static characteristics

Table 8. Static characteristics

$V_{I(VBUSI)}$ = 4.0 V to 16.0 V or $V_{I(VBUSO)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\overline{EN}$	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	ACK; I_O = 8 mA	-	-	0.5	-	0.5	V
R_{pu}	pull-up resistance	ACK	10	-	200	10	200	kΩ
V_{pu}	pull-up voltage	ACK	1.65	-	5.5	1.65	5.5	V

Table 8. Static characteristics *...continued*

$V_{I(VBUSI)}$ = 4.0 V to 16.0 V or $V_{I(VBUSO)}$ = 4.0 V to 5.5 V; unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
				Min	Typ[1]	Max	Min	Max	
I_{GND}	ground current	$\overline{EN}$ = LOW; I_O = 0 A; see Figure 6 to Figure 13		-	280	-	-	450	μA
		$\overline{EN}$ = HIGH; $V_{I(VBUSx)}$ = 5.5 V; I_O = 0 A; see Figure 6 to Figure 13	[2]	-	8	-	-	16	μA
		$\overline{EN}$ = HIGH; $V_{I(VBUSI)}$ = 16 V; I_O = 0 A; see Figure 6 to Figure 13		-	20	-	-	33	μA
$I_{S(OFF)}$	OFF-state leakage current	$V_{I(VBUSI)}$ = 30 V; $V_{I(VBUSO)}$ = 0 V to 5 V; see Figure 14	[3]	-	0.1	-	-	6.5	μA
		$V_{I(VBUSO)}$ = 5.5 V; $V_{I(VBUSI)}$ = 0 V to 5 V; see Figure 15	[4]	-	0.1	-	-	8.5	μA
V_{UVLO}	undervoltage lockout voltage	VBUSI; VBUSO; $\overline{EN}$ = LOW		3.0	3.2	3.4	3.0	3.4	V
$V_{hys(UVLO)}$	undervoltage lockout hysteresis voltage	VBUSI; VBUSO; $\overline{EN}$ = LOW		-	100	-	-	-	mV
V_{OVLO}	overvoltage lockout voltage	VBUSI; $\overline{EN}$ = LOW		16.5	17.5	18.5	16.5	18.5	V
$V_{hys(OVLO)}$	overvoltage lockout hysteresis voltage	VBUSI; $\overline{EN}$ = LOW		-	105	-	-	-	mV
$C_{I/O}$	input/output capacitance	D-; D+; ID; $V_{I(VBUSx)}$ = 5.5 V	[2]	-	3	-	-	-	pF
C_I	input capacitance	$\overline{EN}$		-	3	-	-	-	pF
$C_{S(ON)}$	ON-state capacitance	VBUSI; VBUSO		-	-	0.5	-	0.5	nF

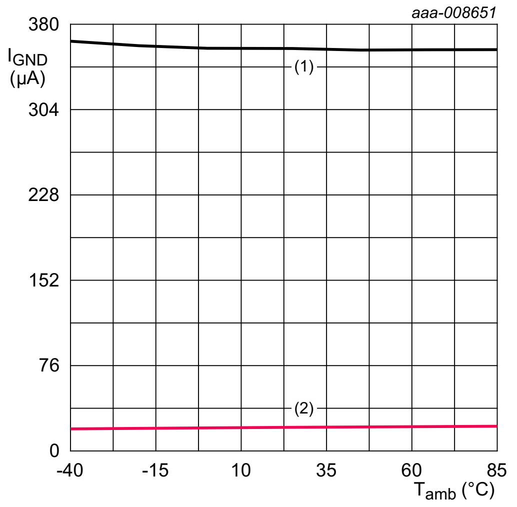
[1] All typical values are measured at $V_{I(VBUSx)}$ = 5.0 V unless otherwise specified.

[2] VBUSx is the supply voltage associated with the input, either VBUSI or VBUSO.

[3] Typical value is measured at $V_{I(VBUSO)}$ = 0 V.

[4] Typical value is measured at $V_{I(VBUSI)}$ = 0 V.

13.1 Graphs

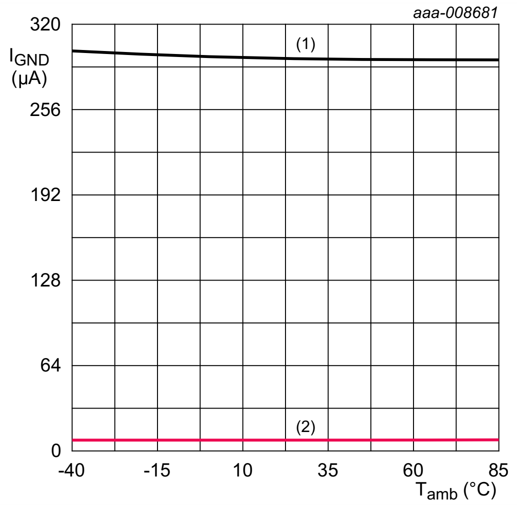


$V_{I(VBUSI)}$ = 16 V

(1) Enabled

(2) Disabled

Fig 6. Ground current versus temperature

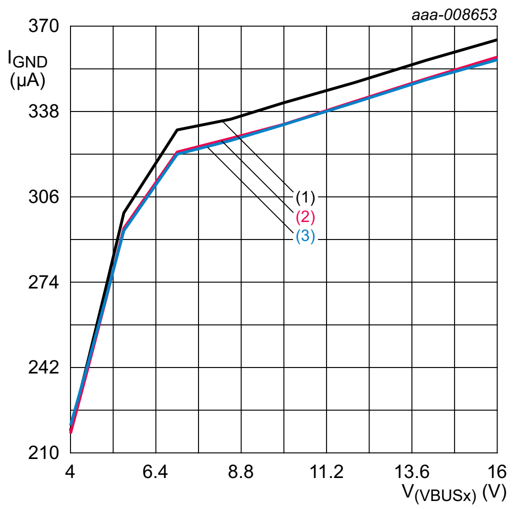


$V_{I(VBUSO)}$ = 5.5 V

(1) Enabled

(2) Disabled

Fig 7. Ground current versus temperature



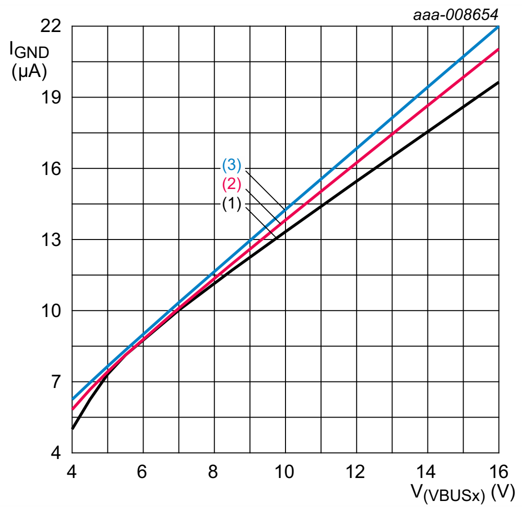
$\overline{EN}$ = L

(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 8. Ground current versus input voltage on pin VBUSI



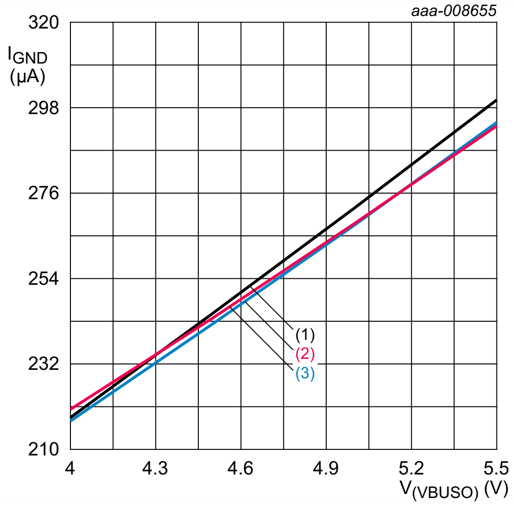
$\overline{EN}$ = H

(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 9. Ground current versus input voltage on pin VBUSI



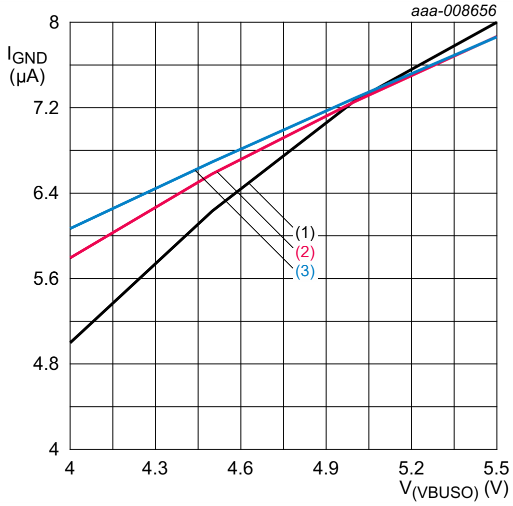
$\overline{EN}$ = L

(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 10. Ground current versus input voltage on pin VBUSO



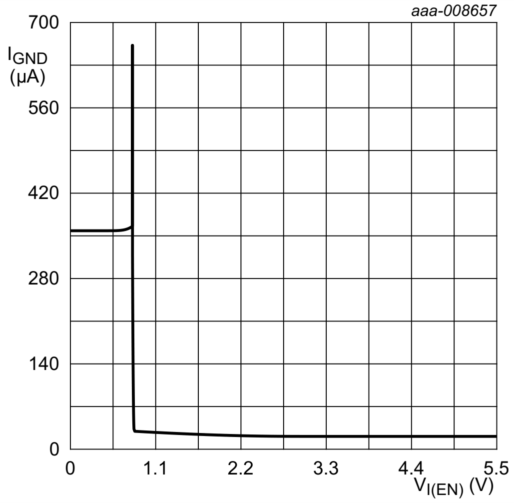
$\overline{EN}$ = H

(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

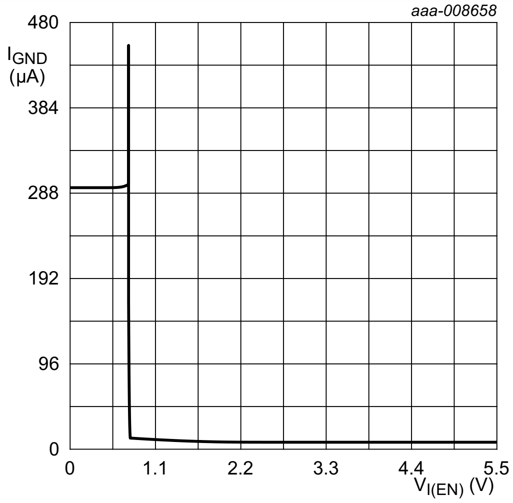
(3) T_{amb} = 85 °C.

Fig 11. Ground current versus input voltage on pin VBUSO



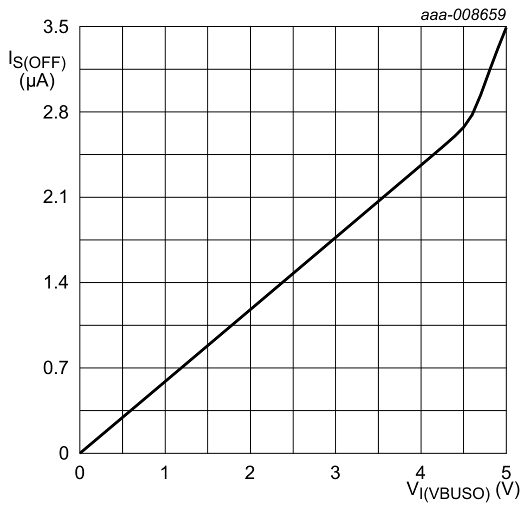
$V_{I(VBUSI)}$ = 16 V

Fig 12. Ground current versus input voltage on pin $\overline{EN}$



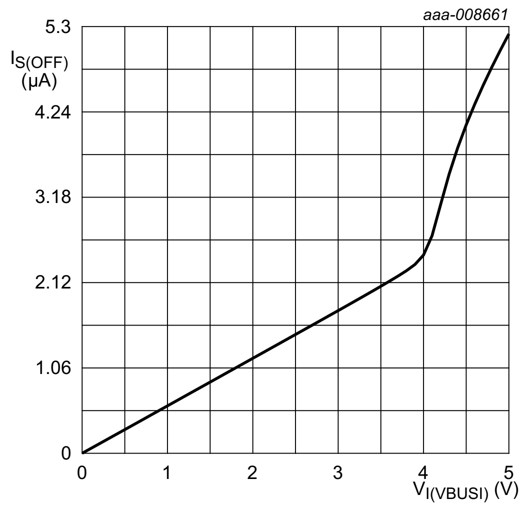
$V_{I(VBUSO)}$ = 5.5 V

Fig 13. Ground current versus input voltage on pin $\overline{EN}$



$V_{I(VBUSI)}$ = 16 V

Fig 14. OFF-state leakage current versus input voltage on pin VBUSO



$V_{I(VBUSO)}$ = 5.5 V

Fig 15. OFF-state leakage current versus input voltage on pin VBUSI

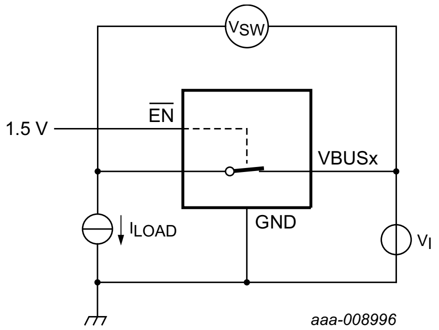
13.2 ON resistance

Table 9. ON resistance

At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

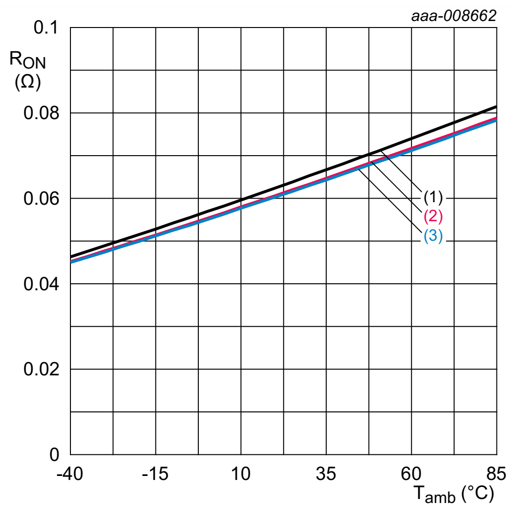
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	$V_{I(VBUSI)}$ = 4.0 V to 16 V; see Figure 16 to Figure 20						
		I_{LOAD} = 200 mA	-	62	-	40	100	mΩ
		I_{LOAD} = 1.5 A	-	62	-	40	100	mΩ
		$V_{I(VBUSO)}$ = 4.0 V to 5.5 V; see Figure 16 to Figure 20						
		I_{LOAD} = 200 mA	-	62	-	40	100	mΩ
		I_{LOAD} = 1.5 A	-	62	-	40	100	mΩ

13.3 ON resistance test circuit and graphs



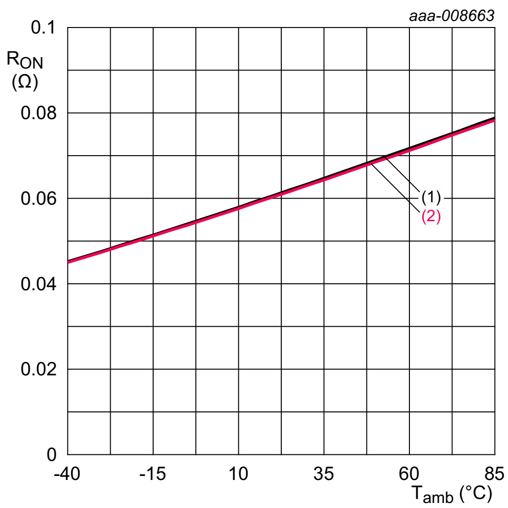
$R_{ON} = V_{SW} / I_{LOAD}$

Fig 16. Test circuit for measuring ON resistance



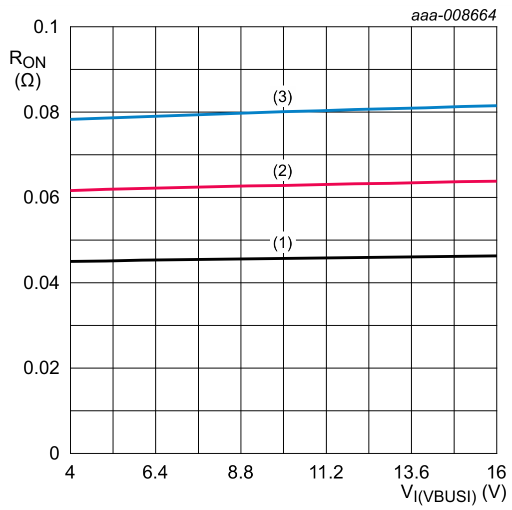
$V_{I(VBUSI)}$ = 4.0 V and 16 V

Fig 17. ON resistance versus temperature



$V_{I(VBUSO)}$ = 4.0 V and 5.5 V

Fig 18. ON resistance versus temperature

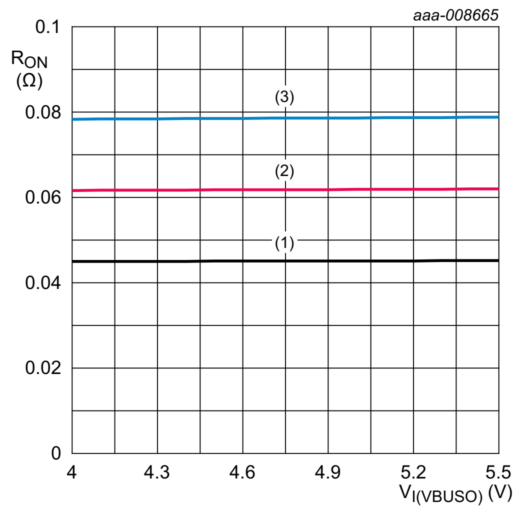


(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 19. ON resistance versus input voltage on pin VBUSI



(1) T_{amb} = –40 °C.

(2) T_{amb} = 25 °C.

(3) T_{amb} = 85 °C.

Fig 20. ON resistance versus input voltage on pin VBUSO

14. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 22.

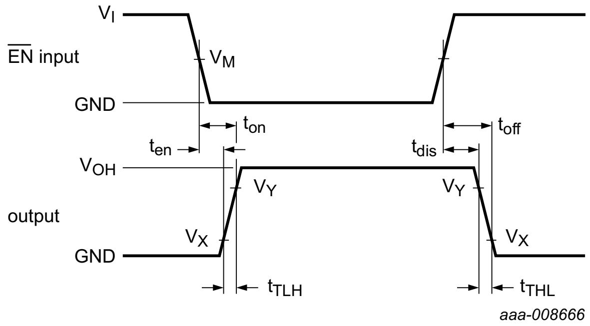
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	enable time	$\overline{EN}$ to VBUSO; see Figure 21 and Figure 23 to Figure 26						
		$V_{I(VBUSI)}$ = 4.0 V	-	500	-	210	-	µs
		$V_{I(VBUSI)}$ = 16 V	-	500	-	250	-	µs
		$\overline{EN}$ to VBUSI; see Figure 21 and Figure 23 to Figure 26						
		$V_{I(VBUSO)}$ = 4.0 V	-	500	-	310	-	µs
		$V_{I(VBUSO)}$ = 5.5 V	-	500	-	290	-	µs
t_{dis}	disable time	$\overline{EN}$ to VBUSO; see Figure 21 and Figure 27 to Figure 30						
		$V_{I(VBUSI)}$ = 4.0 V	-	1.6	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	1.6	-	-	-	ms
		$\overline{EN}$ to VBUSI; see Figure 21 and Figure 27 to Figure 30						
		$V_{I(VBUSO)}$ = 4.0 V	-	1.6	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	1.6	-	-	-	ms

Table 10. Dynamic characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 22.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{on}	turn-on time	$\overline{EN}$ to VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	1500	-	880	-	μs
		$V_{I(VBUSI)}$ = 16 V	-	2000	-	1130	-	μs
		$\overline{EN}$ to VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	1500	-	820	-	μs
		$V_{I(VBUSO)}$ = 5.5 V	-	1500	-	880	-	μs
t_{off}	turn-off time	$\overline{EN}$ to VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	34.6	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	34.6	-	-	-	ms
		$\overline{EN}$ to VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	34.6	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	34.6	-	-	-	ms
t_{TLH}	LOW to HIGH output transition time	VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	1000	-	670	-	μs
		$V_{I(VBUSI)}$ = 16 V	-	1500	-	880	-	μs
		VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	1000	-	510	-	μs
		$V_{I(VBUSO)}$ = 5.5 V	-	1000	-	590	-	μs
t_{THL}	HIGH to LOW output transition time	VBUSO; see Figure 21						
		$V_{I(VBUSI)}$ = 4.0 V	-	33.0	-	-	-	ms
		$V_{I(VBUSI)}$ = 16 V	-	33.0	-	-	-	ms
		VBUSI; see Figure 21						
		$V_{I(VBUSO)}$ = 4.0 V	-	33.0	-	-	-	ms
		$V_{I(VBUSO)}$ = 5.5 V	-	33.0	-	-	-	ms

14.1 Waveforms and test circuit



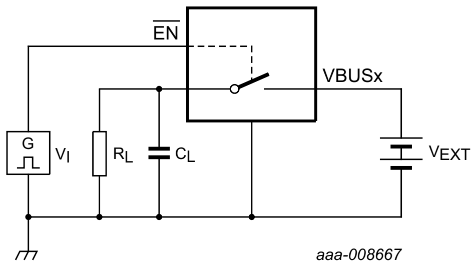
Measurement points are given in Table 11.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Fig 21. Switching times

Table 11. Measurement points

Supply voltage V_I		$\overline{EN}$ Input	Output	
VBUSI	VBUSO	V_M	V_X	V_Y
4.0 V to 16 V	4.0 V to 5.5 V	0.5 × $V_{I(EN)}$	0.1 × V_{OH}	0.9 × V_{OH}



Test data is given in Table 12.

Definitions test circuit:

R_L = Load resistance.

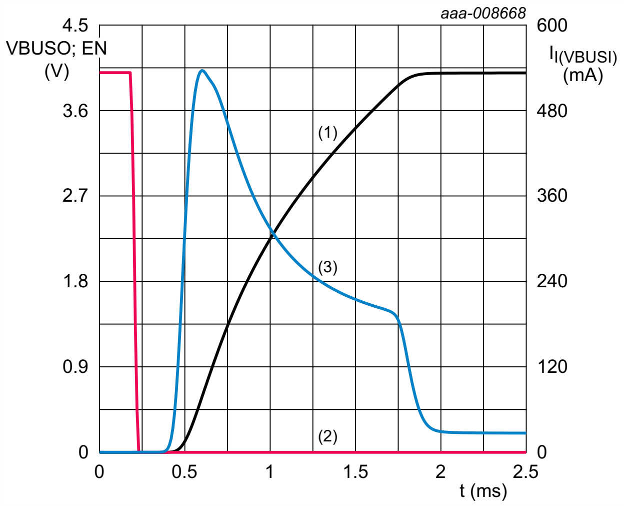
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 22. Test circuit for measuring switching times

Table 12. Test data

Supply voltage V_{EXT}		Input	Load	
VBUSI	VBUSO	V_I	C_L	R_L
4.0 V to 16 V	4.0 V to 5.5 V	1.5 V	100 μF	150 Ω



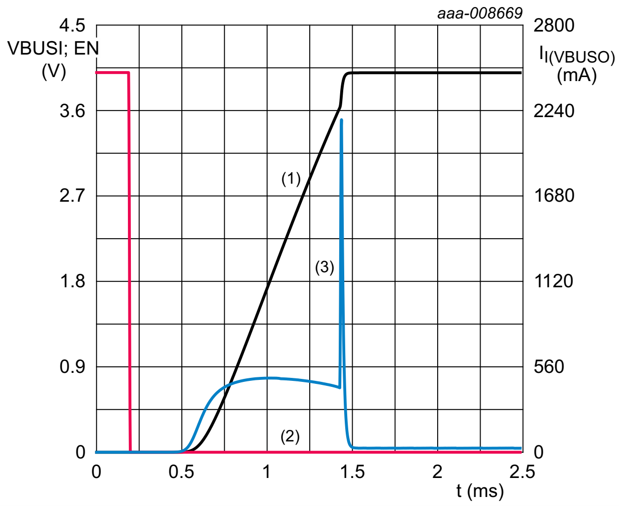
$V_{I(VBUSI)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 23. Enable time and in-rush current



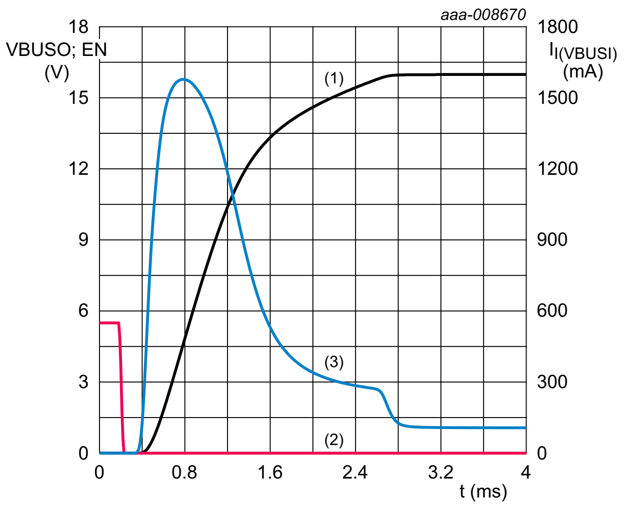
$V_{I(VBUSO)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

Fig 24. Enable time and in-rush current



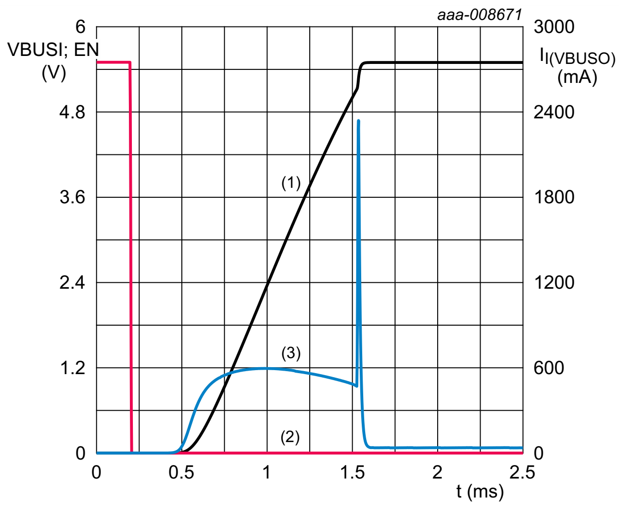
$V_{I(VBUSI)}$ = 16 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 25. Enable time and in-rush current



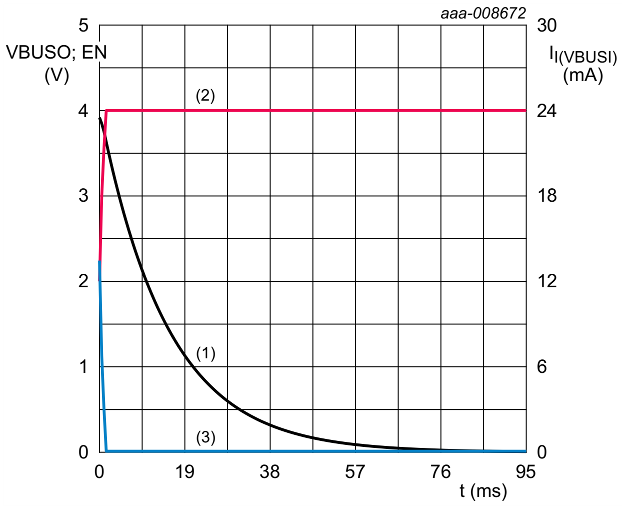
$V_{I(VBUSO)}$ = 5.5 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

Fig 26. Enable time and in-rush current



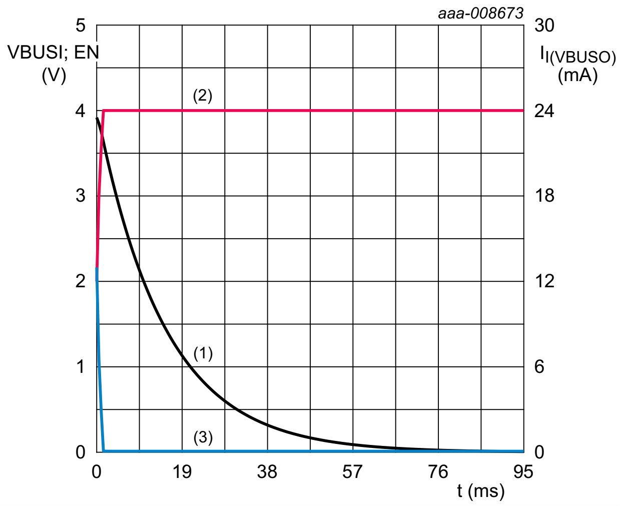
$V_{I(VBUSI)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 27. Disable time



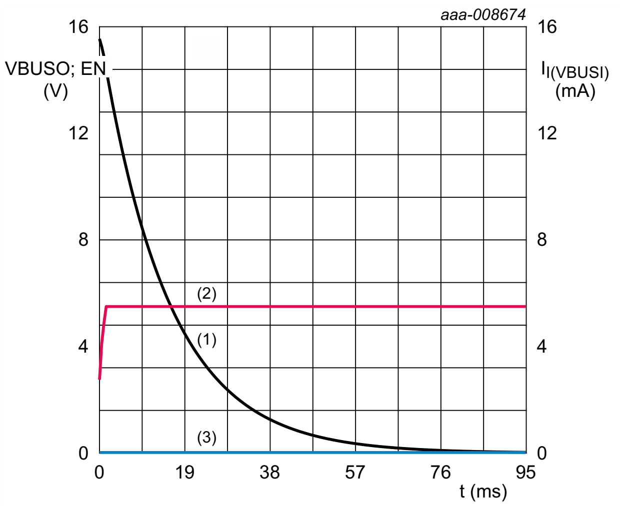
$V_{I(VBUSO)}$ = 4.0 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSI

(2) EN

(3) $I_{I(VBUSO)}$

Fig 28. Disable time



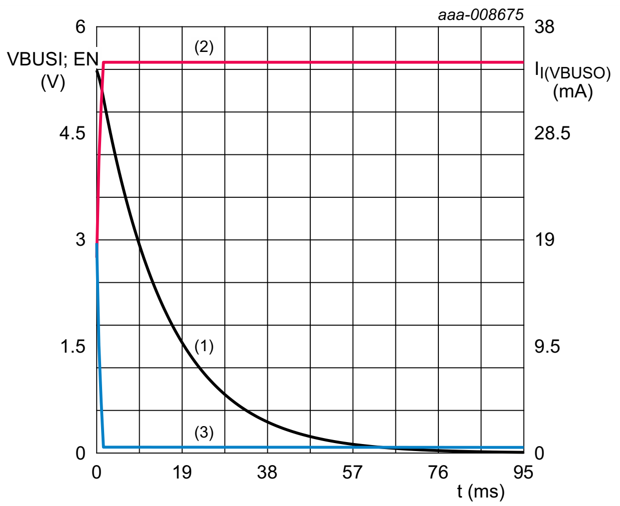
$V_{I(VBUSI)}$ = 16 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSO

(2) EN

(3) $I_{I(VBUSI)}$

Fig 29. Disable time



$V_{I(VBUSO)}$ = 5.5 V; R_L = 150 Ω; C_L = 100 μF; T_{amb} = 25 °C

(1) VBUSI

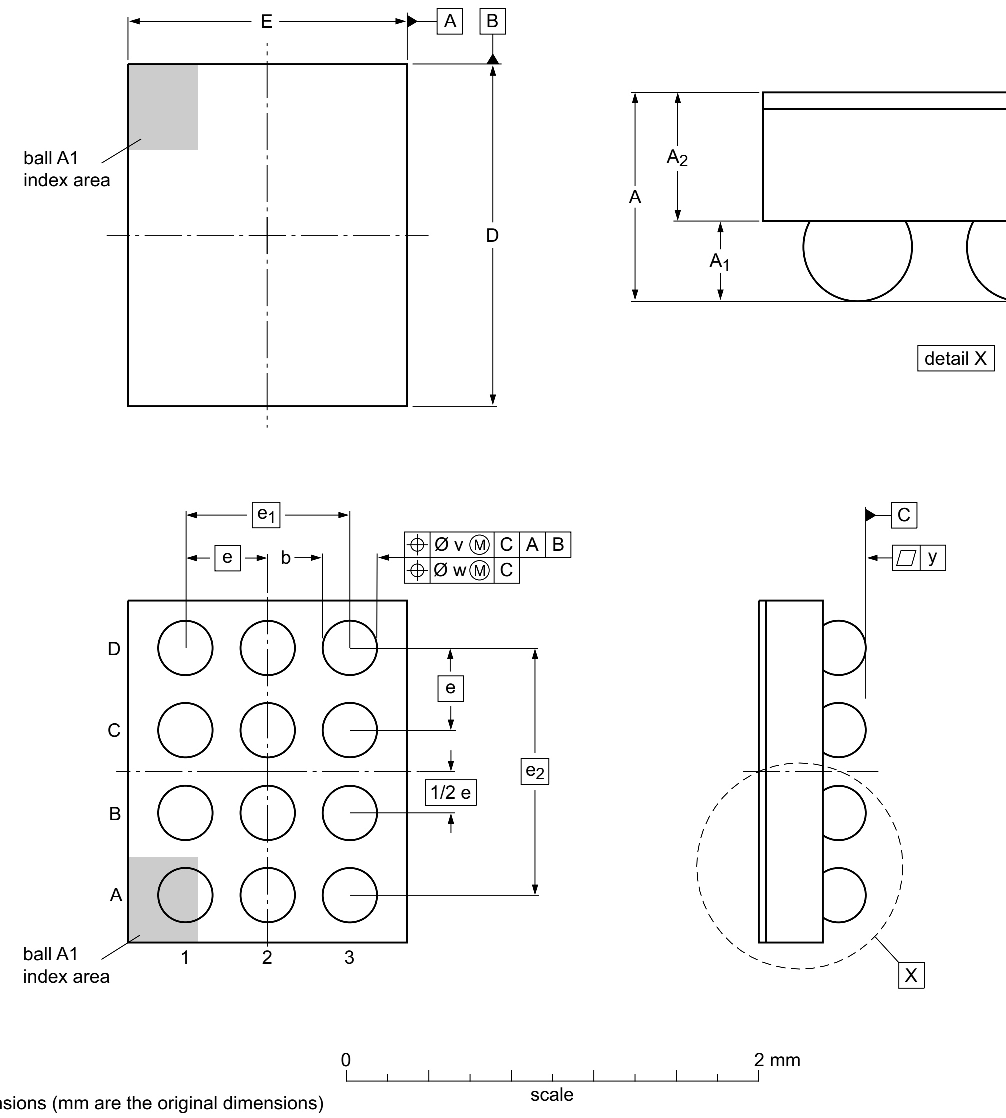
(2) EN

(3) $I_{I(VBUSO)}$

Fig 30. Disable time

15. Package outline

WLCSP12: wafer level chip-scale package; 12 bumps; 1.36 x 1.66 x 0.51 mm, 0.4 mm pitch (Backside coating included) **NX18P3001**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.55	0.23	0.34	0.29	1.69	1.39						
	nom	0.51	0.20	0.31	0.26	1.66	1.36	0.4	0.8	1.2	0.05	0.15	0.03
	min	0.47	0.17	0.29	0.23	1.63	1.33						

wlcsp12_nx18p3001_po

Outline version	References IEC	References JEDEC	References JEITA		European projection	Issue date
NX18P3001						~~13-03-29~~ 13-05-23

Fig 31. Package outline WLCSP12 package

16. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
OTP	OverTemperature Protection
USB-OTG	Universal Serial Bus On-The-Go
UVLO	UnderVoltage LockOut
OVLO	OverVoltage LockOut

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX18P3001 v.1	20130924	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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Date of release: 24 September 2013

Document identifier: NX18P3001