



# PCA9536

## 4-bit I<sup>2</sup>C-bus and SMBus I/O port

Rev. 05 — 25 January 2010

Product data sheet

## 1. General description

The PCA9536 is an 8-pin CMOS device that provides 4 bits of General Purpose parallel Input/Output (GPIO) expansion for I<sup>2</sup>C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I<sup>2</sup>C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push buttons, LEDs, fans, etc.

The PCA9536 consists of a 4-bit Configuration register (input or output selection), 4-bit Input Port register, 4-bit Output Port register and a 4-bit Polarity Inversion register (active HIGH or active LOW operation). The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the read register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The power-on reset sets the registers to their default values and initializes the device state machine.

The I<sup>2</sup>C-bus address is fixed and allows only one device on the same I<sup>2</sup>C-bus/SMBus.

## 2. Features

- 4-bit I<sup>2</sup>C-bus GPIO
- Operating power supply voltage range of 2.3 V to 5.5 V
- 5 V tolerant I/Os
- Polarity Inversion register
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power-up
- Internal power-on reset
- 4 I/O pins which default to 4 inputs with 100 k $\Omega$  internal pull-up resistor
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: SO8, TSSOP8 (MSOP8), HVSON8

### 3. Ordering information

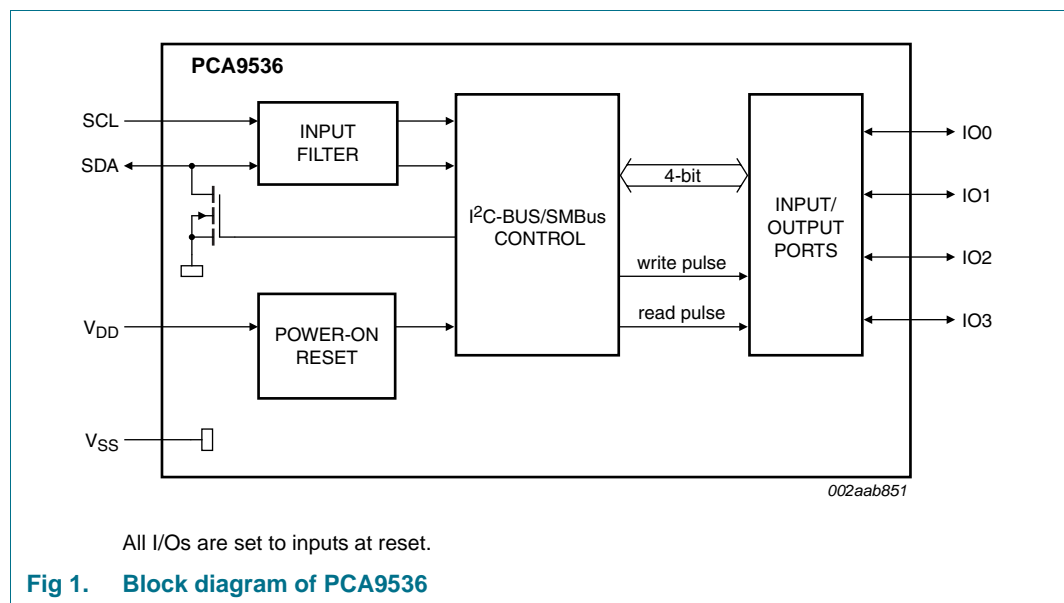
**Table 1. Ordering information**

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$

Type number	Topside mark	Package		Version
		Name	Description	
PCA9536D	PCA9536	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
PCA9536DP	9536	TSSOP8 <sup>[1]</sup>	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PCA9536TK	9536	HVSON8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 × 3 × 0.85 mm	SOT908-1

[1] Also known as MSOP8.

### 4. Block diagram



## 5. Pinning information

### 5.1 Pinning

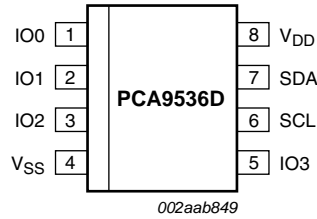


Fig 2. Pin configuration for SO8

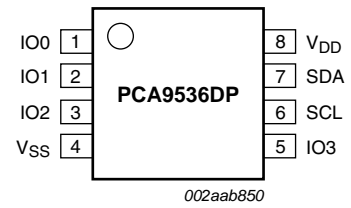


Fig 3. Pin configuration for TSSOP8

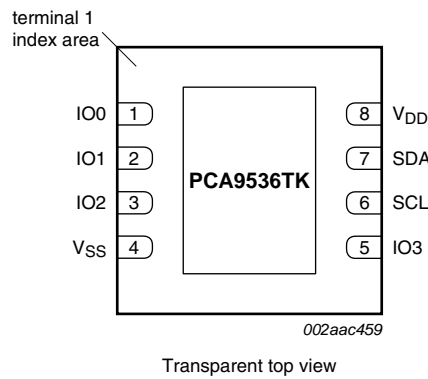


Fig 4. Pin configuration for HVSON8

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
IO0	1	input/output 0
IO1	2	input/output 1
IO2	3	input/output 2
V <sub>SS</sub>	4	supply ground
IO3	5	input/output 3
SCL	6	serial clock line
SDA	7	serial data line
V <sub>DD</sub>	8	supply voltage

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9536”](#).

### 6.1 Registers

#### 6.1.1 Command byte

**Table 3. Command byte**

Command	Protocol	Function
0	read byte	Input Port register
1	read/write byte	Output Port register
2	read/write byte	Polarity Inversion register
3	read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

#### 6.1.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally logic 1 when no external signal externally applied because of the internal pull-up resistors.

**Table 4. Register 0 - Input Port register bit description**

Legend: \* default value

Bit	Symbol	Access	Value	Description
7	I7	read only	1*	not used
6	I6	read only	1*	
5	I5	read only	1*	
4	I4	read only	1*	
3	I3	read only	X	determined by externally applied logic level
2	I2	read only	X	
1	I1	read only	X	
0	I0	read only	X	

### 6.1.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 5. Register 1 - Output Port register bit description**

Legend: \* default value

Bit	Symbol	Access	Value	Description
7	O7	R	1*	not used
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	reflects outgoing logic levels of pins defined as outputs by Register 3
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

### 6.1.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with '1'), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a '0'), the Input Port data polarity is retained.

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 6. Register 2 - Polarity Inversion register bit description**

Legend: \* default value

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	not used
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	inverts polarity of Input Port register data
2	N2	R/W	0*	0 = Input Port register data retained (default value)
1	N1	R/W	0*	1 = Input Port register data inverted
0	N0	R/W	0*	

### 6.1.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to  $V_{DD}$ .

'Not used' bits can be programmed with either logic 0 or logic 1.

**Table 7. Register 3 - Configuration register bit description**

Legend: \* default value

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	not used
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	configures the directions of the I/O pins
2	C2	R/W	1*	0 = corresponding port pin enabled as an output
1	C1	R/W	1*	1 = corresponding port pin configured as input (default value)
0	C0	R/W	1*	

## 6.2 Power-on reset

When power is applied to  $V_{DD}$ , an internal Power-On Reset (POR) holds the PCA9536 in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that point, the reset condition is released and the PCA9536 registers and state machine will initialize to their default states. Thereafter,  $V_{DD}$  must be lowered below 0.2 V to reset the device.

For a power reset cycle,  $V_{DD}$  must be lowered below 0.2 V and then restored to the operating voltage.

## 6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input with a weak pull-up (100 k $\Omega$  typical) to  $V_{DD}$ . The input voltage may be raised above  $V_{DD}$  to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care should be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either  $V_{DD}$  or  $V_{SS}$ .

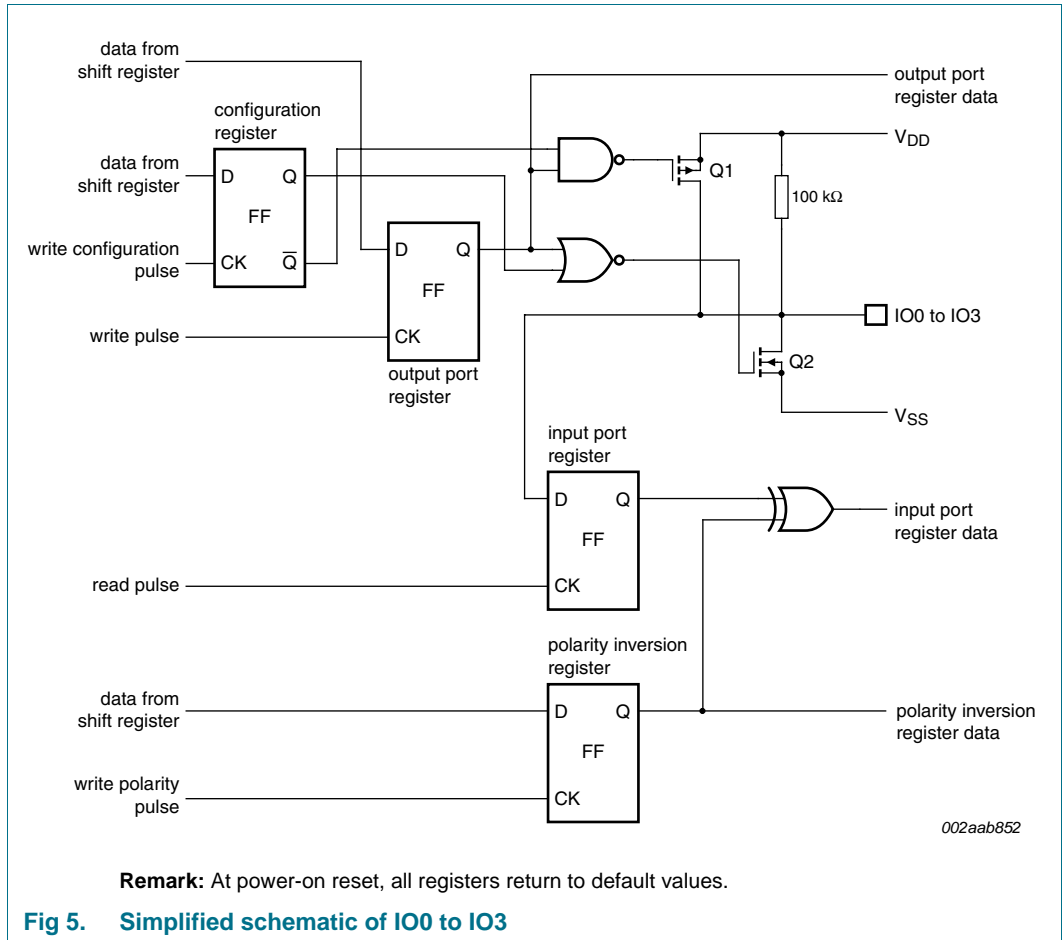


Fig 5. Simplified schematic of IO0 to IO3

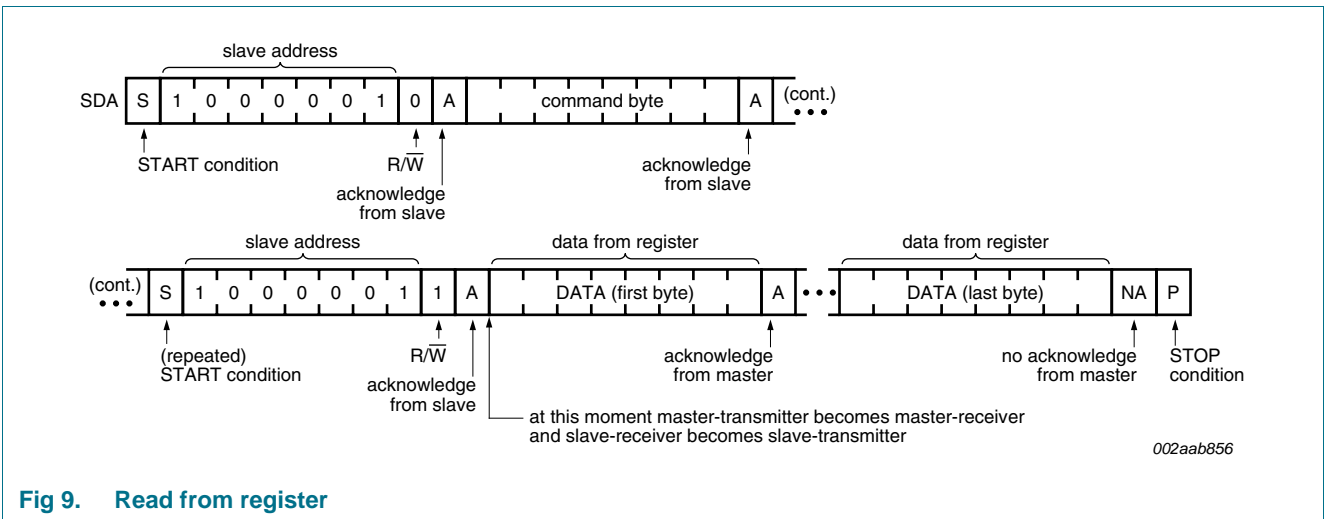
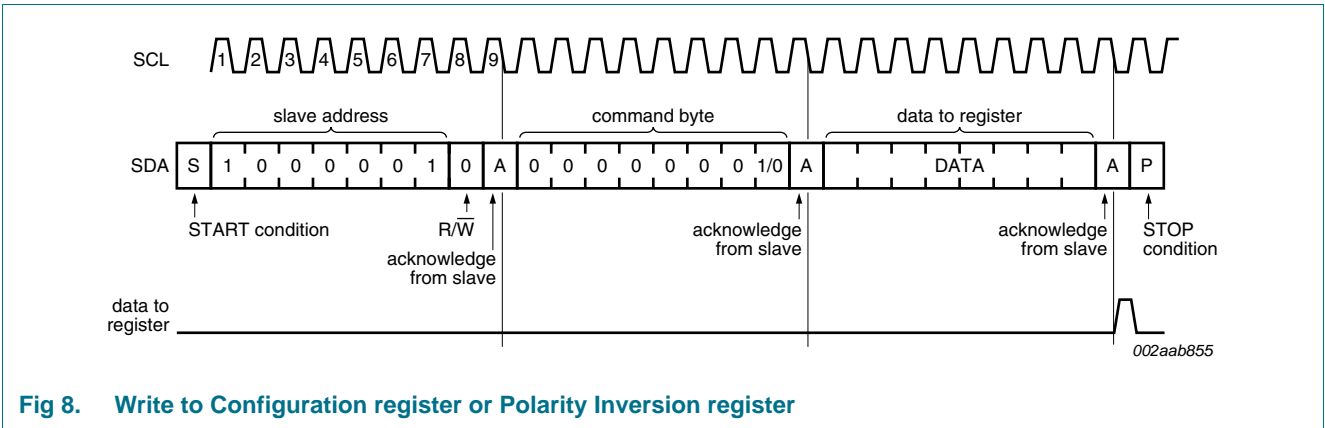
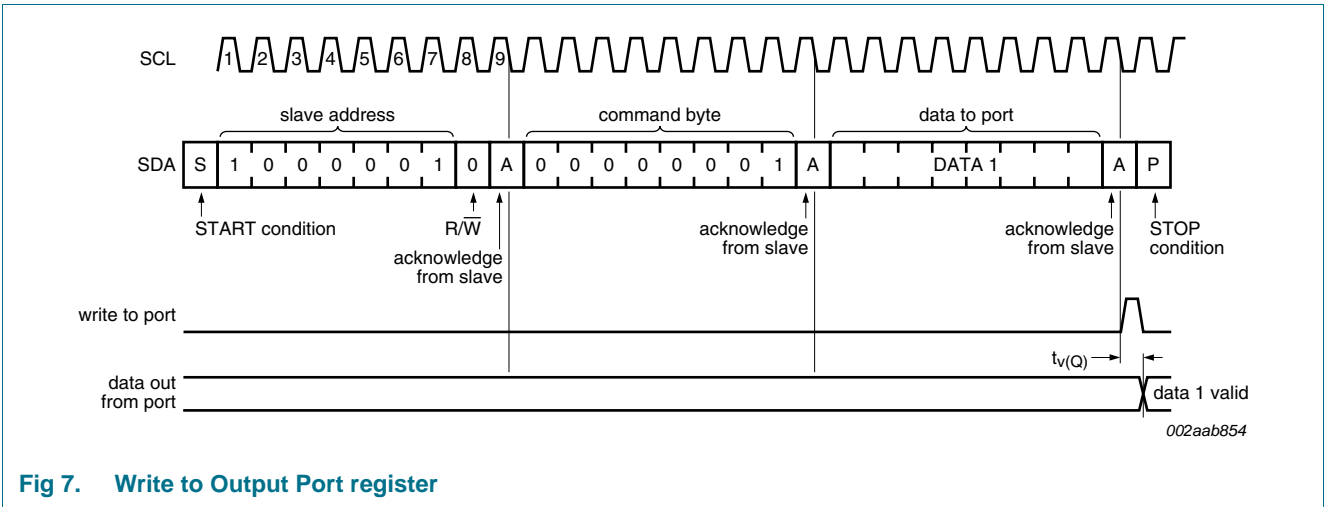
### 6.4 Device address



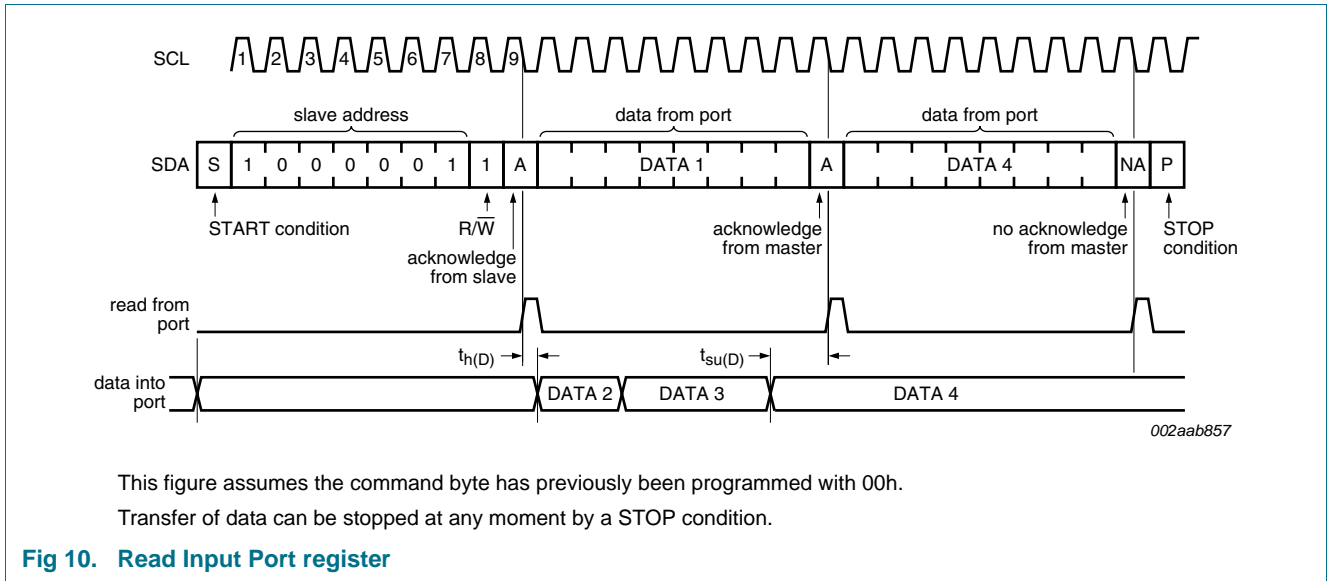
Fig 6. PCA9536 device address

### 6.5 Bus transactions

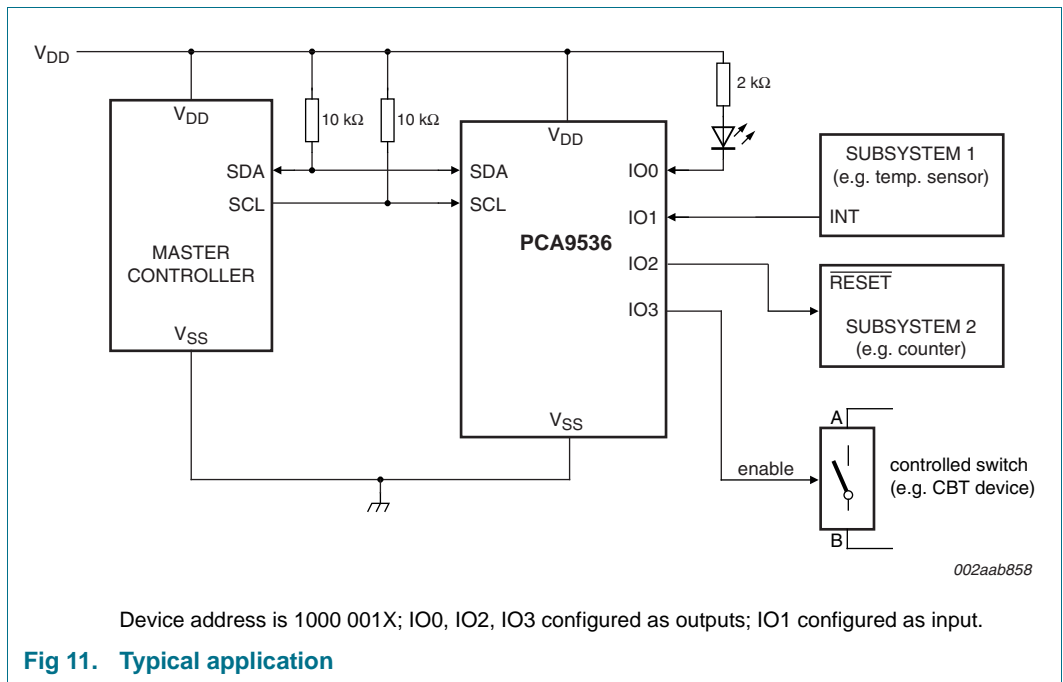
Data is transmitted to the PCA9536 registers using the Write mode as shown in [Figure 7](#) and [Figure 8](#). Data is read from the PCA9536 registers using the Read mode as shown in [Figure 9](#) and [Figure 10](#). These devices do not implement an auto-increment function, so once a command byte has been sent, the register which was addressed will continue to be accessed by reads until a new command byte has been sent.







## 7. Application design-in information



## 8. Limiting values

**Table 8. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+6.0	V
I <sub>I</sub>	input current		-	±20	mA
V <sub>I/O</sub>	voltage on an input/output pin		V <sub>SS</sub> - 0.5	5.5	V
I <sub>O(IOn)</sub>	output current on pin IOn		-	±50	mA
I <sub>DD</sub>	supply current		-	85	mA
I <sub>SS</sub>	ground supply current		-	100	mA
P <sub>tot</sub>	total power dissipation		-	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
T <sub>j(max)</sub>	maximum junction temperature		-	+125	°C

## 9. Static characteristics

**Table 9. Static characteristics**
 $V_{DD} = 2.3\text{ V to }5.5\text{ V}; V_{SS} = 0\text{ V}; T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C};$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
$V_{DD}$	supply voltage		2.3	-	5.5	V
$I_{DD}$	supply current	operating mode; $V_{DD} = 5.5\text{ V}$ ; no load; $f_{SCL} = 100\text{ kHz}$	-	290	400	$\mu\text{A}$
$I_{stb}$	standby current	Standby mode; $V_{DD} = 5.5\text{ V}$ ; no load; $V_I = V_{SS}$ ; $f_{SCL} = 0\text{ kHz}$ ; I/O = inputs	-	225	350	$\mu\text{A}$
		Standby mode; $V_{DD} = 5.5\text{ V}$ ; no load; $V_I = V_{DD}$ ; $f_{SCL} = 0\text{ kHz}$ ; I/O = inputs	-	0.25	1	$\mu\text{A}$
$V_{POR}$	power-on reset voltage		[1] -	1.5	1.65	V
<b>Input SCL; input/output SDA</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.3 $V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		0.7 $V_{DD}$	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	6	-	mA
$I_L$	leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	$\mu\text{A}$
$C_i$	input capacitance	$V_I = V_{SS}$	-	6	10	pF
<b>I/Os</b>						
$V_{IL}$	LOW-level input voltage		-0.5	-	+0.8	V
$V_{IH}$	HIGH-level input voltage		2.0	-	5.5	V
$I_{OL}$	LOW-level output current	$V_{OL} = 0.5\text{ V}; V_{DD} = 2.3\text{ V}$	[2] 8	10	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 2.3\text{ V}$	[2] 10	13	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 3.0\text{ V}$	[2] 8	14	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 3.0\text{ V}$	[2] 10	19	-	mA
		$V_{OL} = 0.5\text{ V}; V_{DD} = 4.5\text{ V}$	[2] 8	17	-	mA
		$V_{OL} = 0.7\text{ V}; V_{DD} = 4.5\text{ V}$	[2] 10	24	-	mA
$V_{OH}$	HIGH-level output voltage	$I_{OH} = -8\text{ mA}; V_{DD} = 2.3\text{ V}$	[3] 1.8	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 2.3\text{ V}$	[3] 1.7	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 3.0\text{ V}$	[3] 2.6	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 3.0\text{ V}$	[3] 2.5	-	-	V
		$I_{OH} = -8\text{ mA}; V_{DD} = 4.75\text{ V}$	[3] 4.1	-	-	V
		$I_{OH} = -10\text{ mA}; V_{DD} = 4.75\text{ V}$	[3] 4.0	-	-	V
$I_{LIH}$	HIGH-level input leakage current	$V_{DD} = 3.6\text{ V}; V_I = V_{DD}$	-	-	1	$\mu\text{A}$
$I_{LIL}$	LOW-level input leakage current	$V_{DD} = 5.5\text{ V}; V_I = V_{SS}$	-	-	-100	$\mu\text{A}$
$C_i$	input capacitance		-	3.7	5	pF
$C_o$	output capacitance		-	3.7	5	pF

[1]  $V_{DD}$  must be lowered to 0.2 V in order to reset part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

## 10. Dynamic characteristics

Table 10. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I <sup>2</sup> C-bus		Fast-mode I <sup>2</sup> C-bus		Unit
			Min	Max	Min	Max	
f <sub>SCL</sub>	SCL clock frequency		0	100	0	400	kHz
t <sub>BUF</sub>	bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t <sub>HD;STA</sub>	hold time (repeated) START condition		4.0	-	0.6	-	μs
t <sub>SU;STA</sub>	set-up time for a repeated START condition		4.7	-	0.6	-	μs
t <sub>SU;STO</sub>	set-up time for STOP condition		4.0	-	0.6	-	μs
t <sub>HD;DAT</sub>	data hold time		0	-	0	-	μs
t <sub>VD;ACK</sub>	data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	μs
t <sub>VD;DAT</sub>	data valid time	[2]	300	-	50	-	ns
t <sub>SU;DAT</sub>	data set-up time		250	-	100	-	ns
t <sub>LOW</sub>	LOW period of the SCL clock		4.7	-	1.3	-	μs
t <sub>HIGH</sub>	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t <sub>r</sub>	rise time of both SDA and SCL signals		-	1000	20 + 0.1C <sub>b</sub> [3]	300	ns
t <sub>f</sub>	fall time of both SDA and SCL signals		-	300	20 + 0.1C <sub>b</sub> [3]	300	ns
t <sub>SP</sub>	pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns

### Port timing

t <sub>v(Q)</sub>	data output valid time	-	200	-	200	ns
t <sub>su(D)</sub>	data input set-up time	100	-	100	-	ns
t <sub>h(D)</sub>	data input hold time	1	-	1	-	μs

[1] t<sub>VD;ACK</sub> = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] t<sub>VD;DAT</sub> = minimum time for SDA data output to be valid following SCL LOW.

[3] C<sub>b</sub> = total capacitance of one bus line in pF.

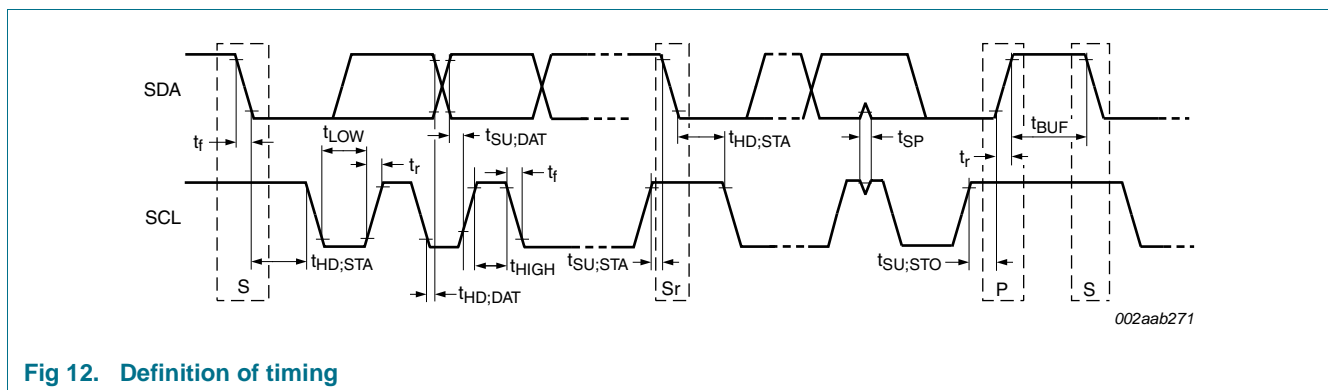
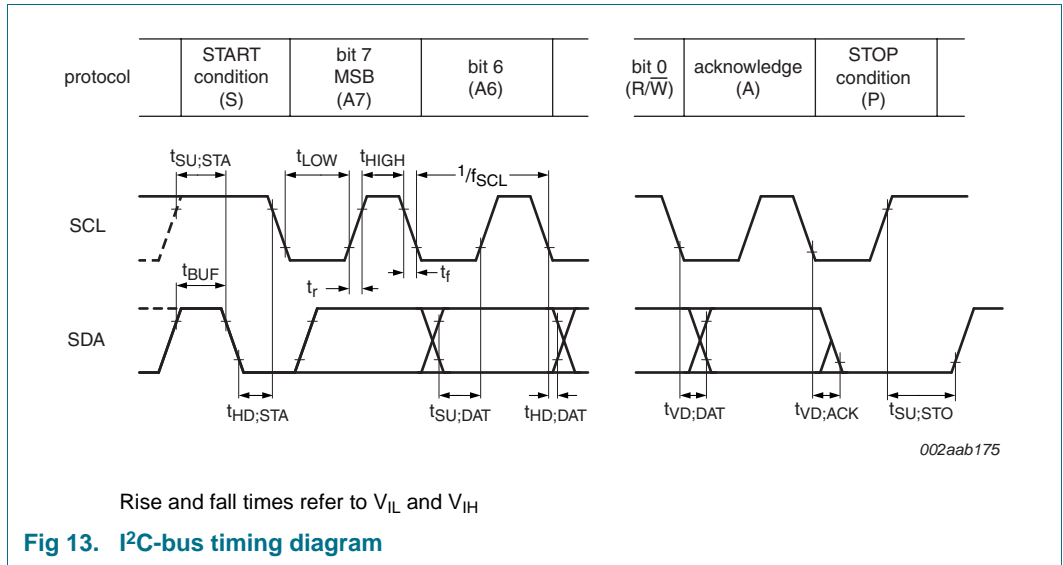


Fig 12. Definition of timing



## 11. Test information

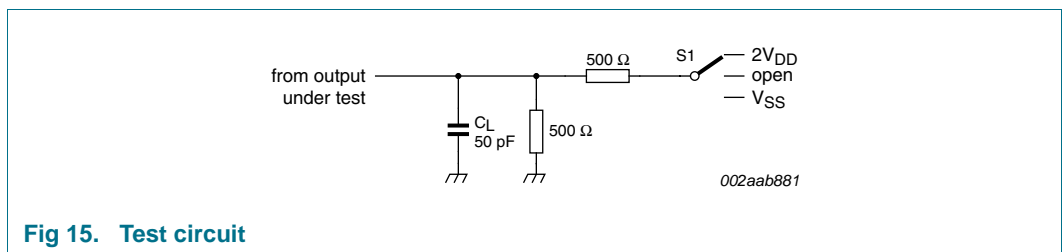
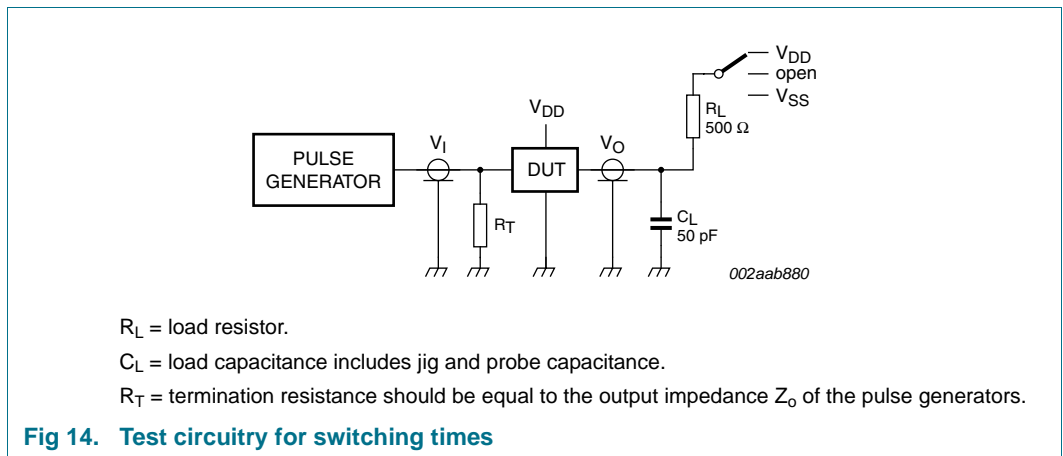


Table 11. Test data

Test	Load		Switch
	$C_L$	$R_L$	
$t_{V(Q)}$	50 pF	500 $\Omega$	$2V_{DD}$

## 12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

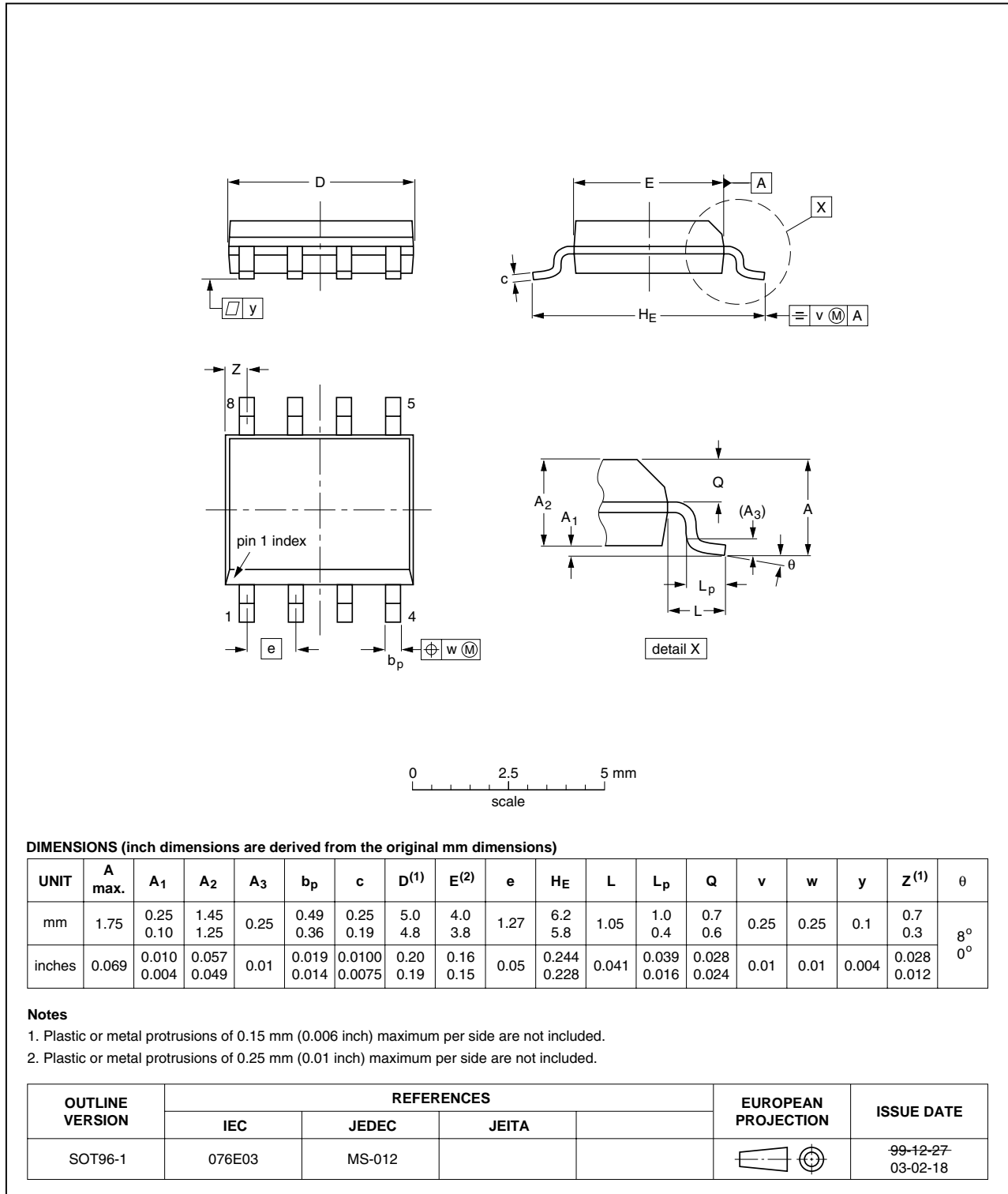


Fig 16. Package outline SOT96-1 (SO8)

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

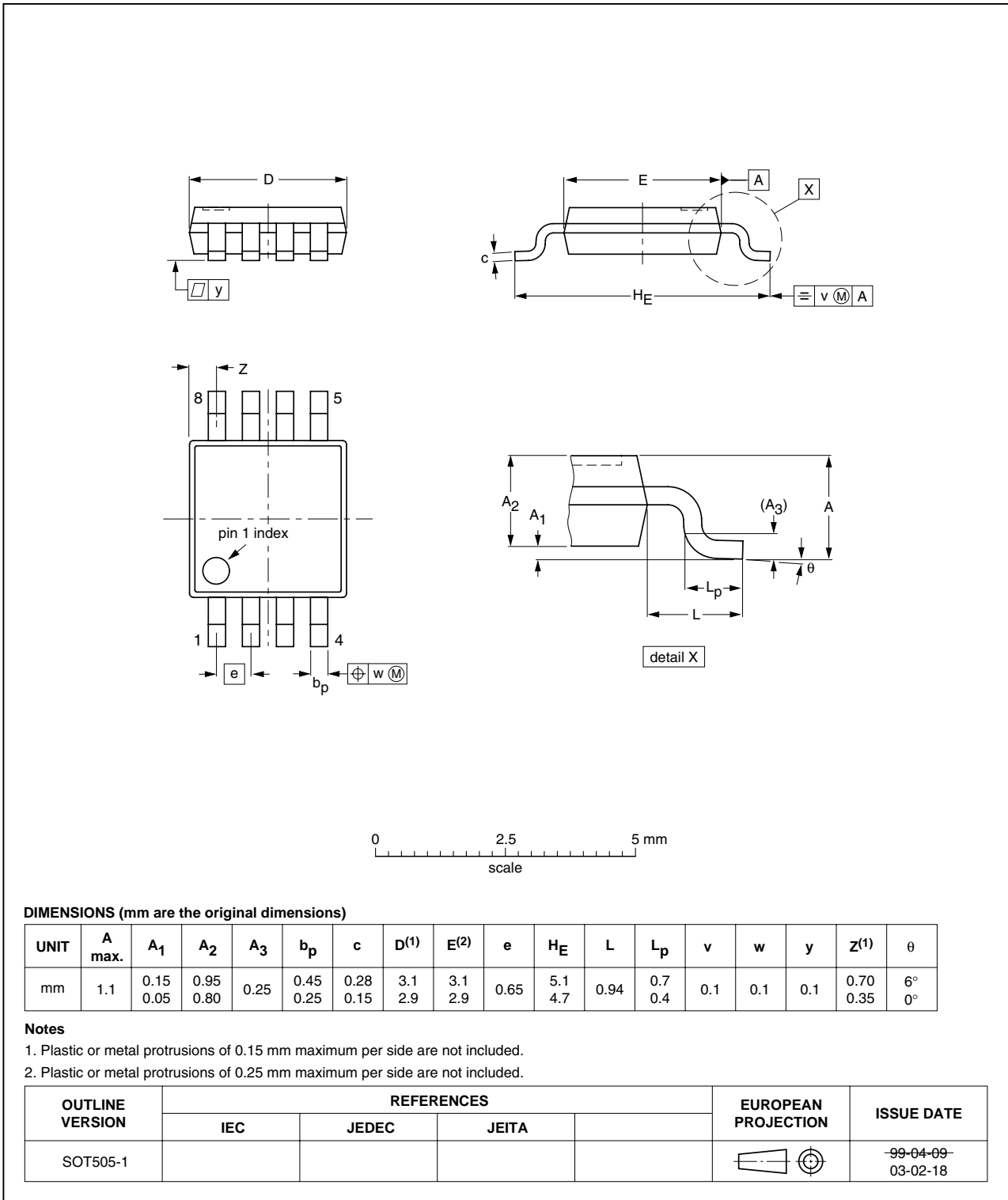
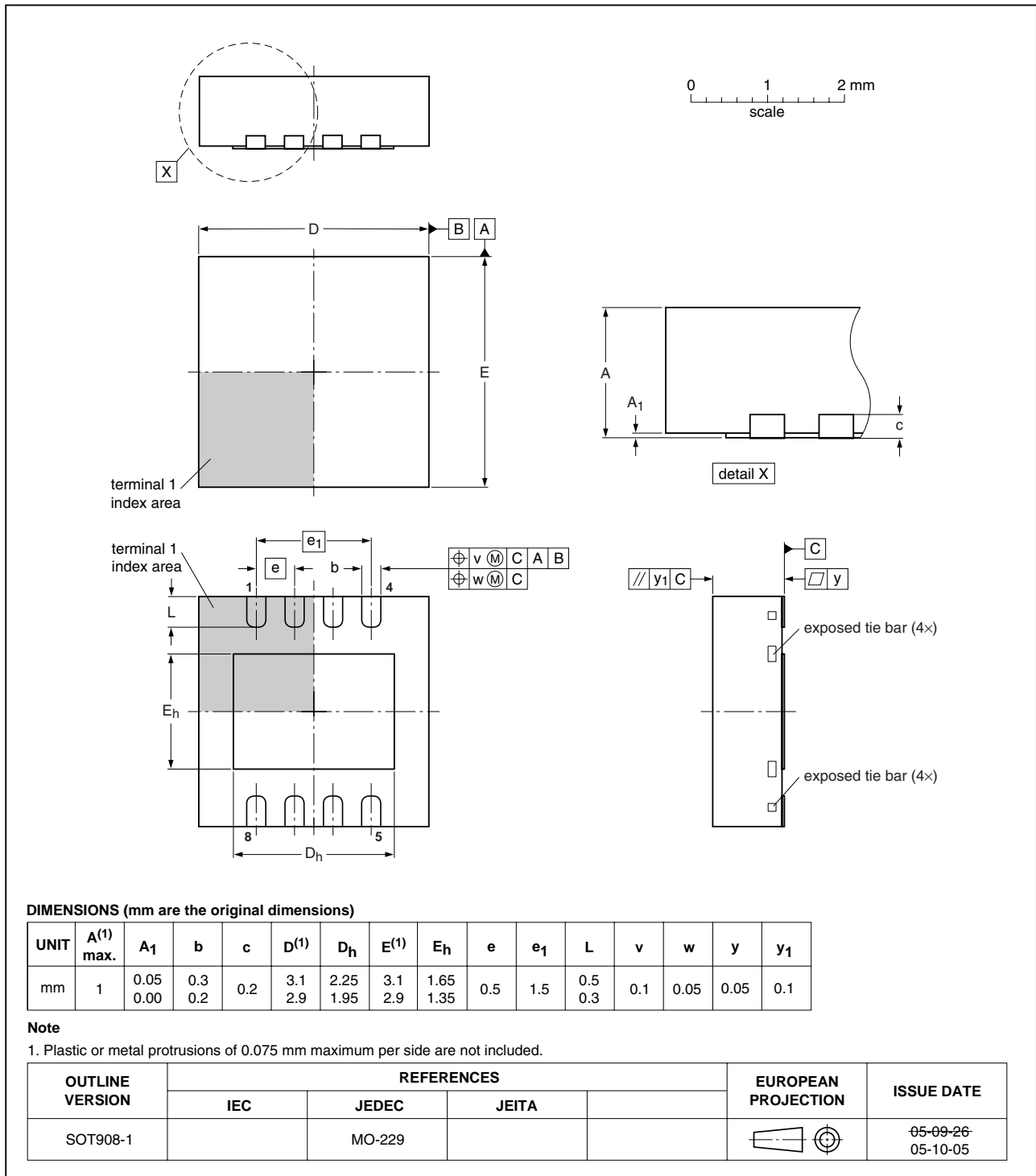


Fig 17. Package outline SOT505-1 (TSSOP8)

**HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 3 x 3 x 0.85 mm**

**SOT908-1**



**Fig 18. Package outline SOT908-1 (HVSON8)**



## 13. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 19](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 12](#) and [13](#)

**Table 12. SnPb eutectic process (from J-STD-020C)**

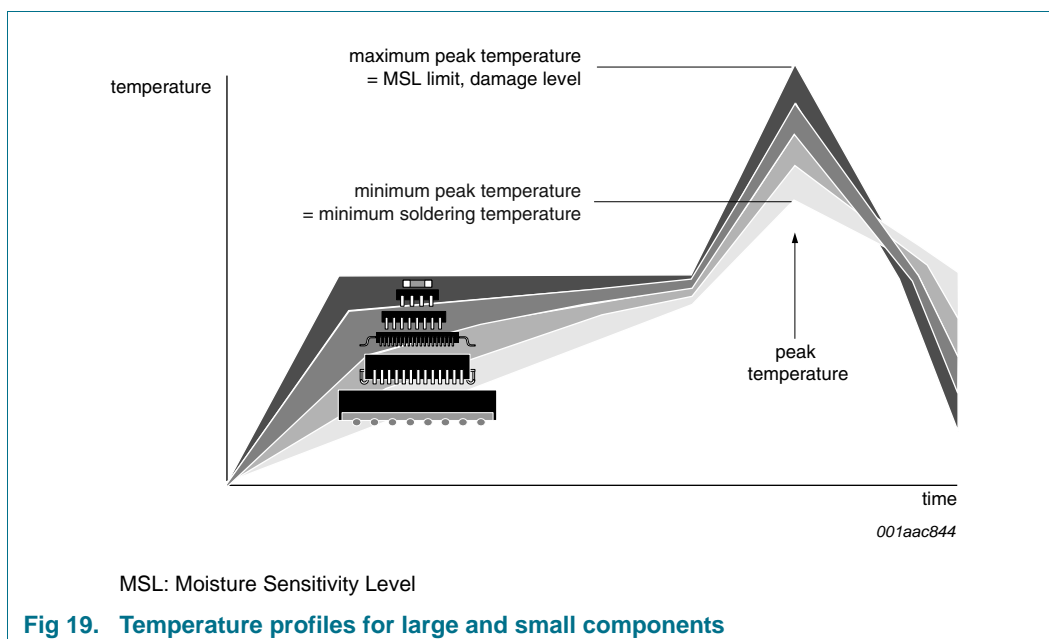
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 13. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 19](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 15. Abbreviations

**Table 14. Abbreviations**

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
GPIO	General Purpose Input/Output
HBM	Human Body Model
I <sup>2</sup> C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light-Emitting Diode
MM	Machine Model
POR	Power-On Reset
SMBus	System Management Bus

## 16. Revision history

Table 15. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9536_5	20100125	Product data sheet	-	PCA9536_4
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 9 “Static characteristics”</a>, sub-section “Supplies”:               <ul style="list-style-type: none"> <li>– I<sub>DD</sub> Typical value changed from “104 μA” to “290 μA”</li> <li>– I<sub>DD</sub> Maximum value changed from “175 μA” to “400 μA”</li> </ul> </li> <li>• <a href="#">Table 10 “Dynamic characteristics”</a>: Unit for “t<sub>f</sub>, fall time of both SDA and SCL signals” changed from “μs” to “ns”</li> </ul> <p><b>Remark:</b> The changes made in this revision are to correct typographical errors only. There is no change in the performance of the device.</p>			
PCA9536_4	20070911	Product data sheet	-	PCA9536_3
PCA9536_3	20061009	Product data sheet	-	PCA9536_2
PCA9536_2 (9397 750 14124)	20040930	Objective data sheet	-	PCA9536_1
PCA9536_1 (9397 750 12895)	20040820	Objective data sheet	-	-

## 17. Legal information

### 17.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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