

TDA18274

Hybrid (analog and digital) silicon tuner for terrestrial and cable TV reception

Rev. 1 — 11 February 2013

Product short data sheet

1. General description

The TDA18274 is a high performance silicon tuner designed for terrestrial and cable TV reception for both analog and digital signals.

The TDA18274 supports all analog and digital TV standards and delivers a Low IF (LIF) signal to a demodulator for analog TV and/or a channel demodulator for digital TV.

The TDA18274 facilitates TV design by:

- Allowing on-board integration
- · Drastically reducing the tuner Bill Of Material (BOM)
- Providing flexibility in system solution development
- Allowing straightforward and cost effective multi-tuner applications optimization

2. Features and benefits

- Single 3.3 V supply voltage
- Worldwide multistandard terrestrial and cable capabilities
- Alignment free
- RoHS compliant
- I²C-bus interface compatible with 3.3 V microcontrollers
- Crystal oscillator output buffer as well as Slave Tuner Output (STO) for multiple tuner applications
- Fully integrated oscillators
- Fully integrated RF selectivity (no need for RF tracking filters coils) (TDA18274HD only)
- 2 programmable General-Purpose Outputs (GPO)
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz and 10 MHz channel bandwidths
- LIF channel center frequency output ranging from 0.8 MHz to 7.5 MHz
- Fully integrated IF selectivity; eliminating the need for external SAW filters
- Large flexibility in the IF filtering stage to ease the matching with various demodulators circuits
- Single-ended RF input, no need for external balun
- Up to 1 GHz RF input capability
- Excellent return loss compatible with cable requirements
- Power Level Detector (PLD) embedded
- Integrated gain control
- Self-AGC synchronization mode (VSync) for analog reception



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- Very fast tuning time
- Strong immunity to LTE interferers in the digital dividend bandwidth
- Strong immunity to WLAN interferers

3. Quick reference data

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Тур | Max | Unit |
|----------------------|-----------------------------------|--|--------------|-----|------|--------|
| f_{RF} | RF frequency | full range of RF input | 42 | - | 1002 | MHz |
| NF _{tun} | tuner noise figure | 75 Ω impedance source; maximum gain | - | | | |
| | | LNA $Z_i = 1$ and RF < 870 MHz | | 4.0 | 4.6 | dB |
| | | LNA $Z_i = 1$ and 870 MHz < RF < 1 GHz | | 5.4 | 6 | dB |
| Φjit | phase jitter | integrated from 250 Hz to 4 MHz | - | 0.4 | 0.6 | degree |
| $lpha_{	ext{image}}$ | image rejection | worst case, measured at 4 MHz IF frequency and for image levels above 60 dB $\!\mu\text{V}$ | 57.5 | 63 | - | dB |
| CSO | composite second-order distortion | worst interferer over RF frequency with respect to wanted carrier | <u>[1]</u> - | -60 | -50 | dBc |
| СТВ | composite triple beat | worst interferer over RF frequency with respect to wanted carrier for frequency ≤ 550 MHz | [1] - | -65 | -60 | dBc |
| | | worst interferer over RF frequency with respect to wanted carrier for frequency > 550 MHz | [1] - | - | -55 | dBc |
| ICP _{1dB} | 1 dB input compression point | at the tuner input and minimum gain | 120 | - | - | dBμV |
| | | | | | | |

^[1] Test scenario: 129 channels each 75 dB μ V.

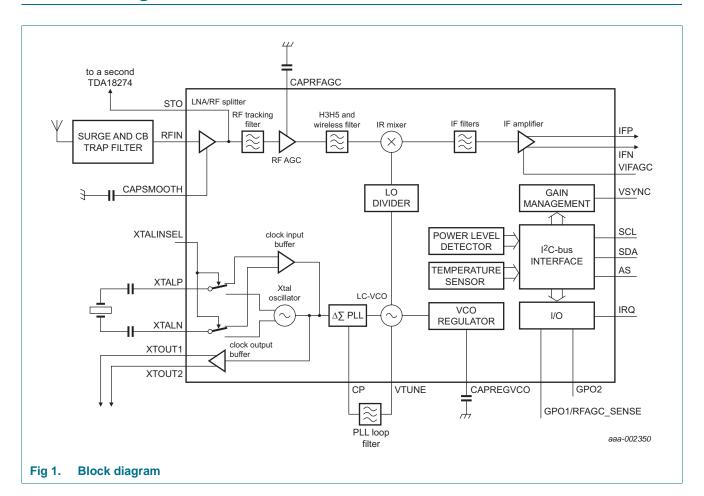
4. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|---------------|----------|--|----------|
| | Name | Description | Version |
| TDA18274HN/C1 | HVQFN40 | plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body $6\times6\times0.85$ mm | SOT618-6 |
| TDA18274HD/C1 | HLQFN48R | plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body $7 \times 7 \times 1.15$ mm | SOT995-2 |

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5. Block diagram



6. Limiting values

Table 3. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

| Parameter | Conditions | Min | Max | Unit |
|-------------------------------------|--|---|--|--|
| supply voltage | 2 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - | -0.3 | +3.6 | ٧ |
| input voltage | V _{CC} < 3.3 V | -0.3 | $V_{CC} + 0.3$ | 3 V |
| | V _{CC} > 3.3 V | -0.3 | +3.6 | V |
| storage temperature | | -40 | +150 | °C |
| junction temperature | | - | 150 | °C |
| ambient temperature | | -20 | <u>[1</u> | <u>∏</u> ∘C |
| electrostatic discharge voltage | EIA/JESD22-A114 (HBM) | -2 | +2 | kV |
| | EIA/JESD22-C101-C (FCDM) class III ² | 750 | - | V |
| GPO pins: GPO1/RFAGC_SENSE and GPO2 | | | | |
| supply voltage | $0 \text{ V} < \text{V}_{\text{pu}} < 5.5 \text{ V}; R_{\text{pu}} > 390 \Omega$ | -0.3 | +5.5 | V |
| supply current | corresponding GPO ON | -20 | 0 | mA |
| | input voltage storage temperature junction temperature ambient temperature electrostatic discharge voltage s: GPO1/RFAGC_SENSE and G supply voltage | $\begin{array}{lll} \text{supply voltage} & & & & & & & \\ & \text{input voltage} & & & & & & \\ & & & & & & & \\ & & & & $ | $\begin{array}{c} \text{supply voltage} & -0.3 \\ \text{input voltage} & V_{\text{CC}} < 3.3 \text{ V} & -0.3 \\ \hline V_{\text{CC}} > 3.3 \text{ V} & -0.3 \\ \text{storage temperature} & -40 \\ \text{junction temperature} & -20 \\ \text{electrostatic discharge voltage} & EIA/JESD22-A114 (HBM) & -2 \\ \hline EIA/JESD22-C101-C (FCDM) class III $ | $\begin{array}{c} \text{supply voltage} & -0.3 & +3.6 \\ \text{input voltage} & V_{\text{CC}} < 3.3 \text{ V} & -0.3 & V_{\text{CC}} + 0.3 \\ \hline V_{\text{CC}} > 3.3 \text{ V} & -0.3 & +3.6 \\ \end{array}$ $\begin{array}{c} \text{storage temperature} & -40 & +150 \\ \text{junction temperature} & - & 150 \\ \hline \text{ambient temperature} & -20 & \boxed{1} \\ \hline \text{electrostatic discharge voltage} & \boxed{\text{EIA/JESD22-A114 (HBM)}} & -2 & +2 \\ \hline \text{EIA/JESD22-C101-C (FCDM) class III} \boxed{2} & 750 & - \\ \hline \text{s: GPO1/RFAGC_SENSE and GPO2} \\ \hline \text{supply voltage} & 0 \text{ V < V}_{\text{pu}} < 5.5 \text{ V; R}_{\text{pu}} > 390 \Omega & -0.3 & +5.5 \\ \hline \end{array}$ |

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- [1] The maximum allowed ambient temperature $T_{amb(max)}$ depends on the assembly conditions of the package and especially on the design of the Printed-Circuit Board (PCB) and die connection. The application mounting must be done in such a way that the maximum junction temperature is never exceeded. The junction temperature can be obtained by reading the temperature sensor bit via I^2C -bus. The junction temperature: $T_j = T_{amb} + \Delta T_{j-c}$. where $\Delta T_{j-c} = power \times R_{th}$.
- [2] Class III: 500 V to 1000 V.

7. Abbreviations

Table 4. Abbreviations

| Acronym | Description |
|---------|--|
| AGC | Automatic Gain Control |
| BOM | Bill Of Material |
| FCDM | Field-induced Charged-Device Model |
| GPO | General Purpose Outputs |
| H3H5 | Harmonic 3 and Harmonic 5 |
| HBM | Human Body Model |
| IF | Intermediate Frequency |
| I/O | Input/Output |
| LC-VCO | Inductors and Capacitors - Voltage Controlled Oscillator |
| LIF | Low IF |
| LNA | Low-Noise Amplifier |
| LO | Local Oscillator |
| LTE | Long-Term Evolution |
| LTO | Loop-Through Output |
| PLD | Power Level Detector |
| PLL | Phase-Locked Loop |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| SAW | Surface Acoustic Wave |
| STB | Set-Top Box |
| STO | Slave Tuner Output |
| VCO | Voltage Controlled Oscillator |
| Xtal | Crystal |
| WLAN | Wireless Local Area Network |

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8. Revision history

Table 5. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------------|---------------|------------|
| TDA18274_SDS v.1 | 20130211 | Product short data sheet | - | - |

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|--------------------------------|-------------------|---|
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