UM10349

Contact smart card reader chips evaluation with CAKE80xx_MBA

Rev. 1.0 — 1 October 2014   **User manual**

Document information

Info	Content
Keywords	TDA Eval board, Smart card reader
Abstract	This document describes the way to use the Cake80xx_MBA mother board: power supply, protocols, plug of the daughter boards, firmware

Revision history

Rev	Date	Description
1.0	20141001	First official release
0.3	20131008	Add TDA8037
0.2	20101116	Add EMV Loopback mechanism
0	20090313	Draft

Contact information

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1. Board presentation

The Cake80xx_MBA is a mother board dedicated to the evaluation of the NXP smart card reader front end devices.

The following devices are compliant with the mother board:

- TDA8025 with the Cake8025_01_D daughter board
- TDA8026 with the Cake8026_02_D daughter board
- TDA8034 with the Cake8034_0X_D daughter boards (one for each package)
- TDA8024 with the Cake8024_11_D (TDA8024TT) and Cake8024_12_D (TDA8024T) daughter boards
- TDA8020 with the Cake8020_07_D daughter board
- TDA8023 with the Cake8023_06_D daughter board
- TDA8035 with the Cake8035_01_D daughter board
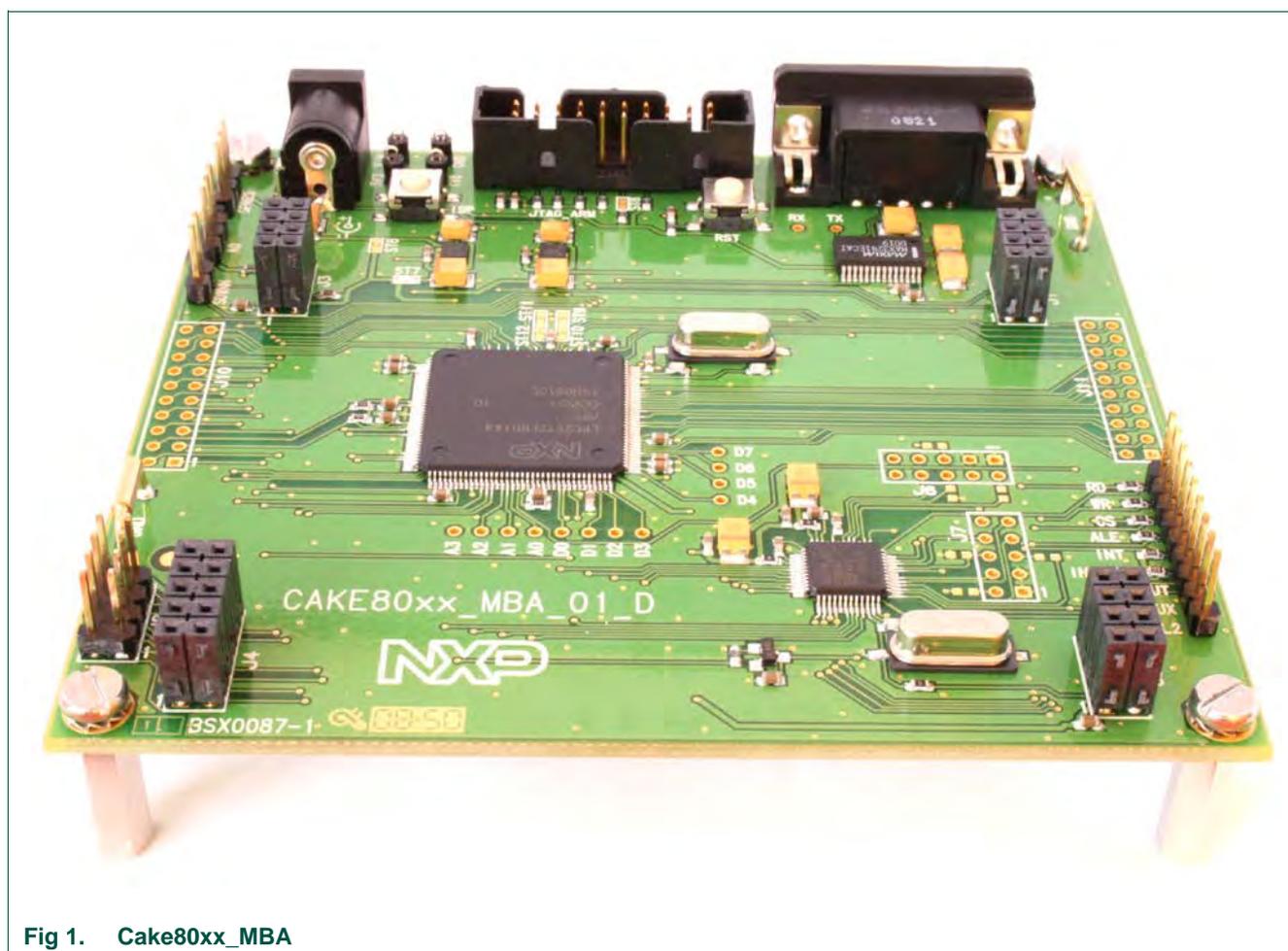- TDA8037 with the Cake8037T and Cake8037TT daughter board

Fig 1.   Cake80xx_MBA

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1.1 Board architecture

The following figure shows how the Cake80xxMBA drives TDA daughter boards.
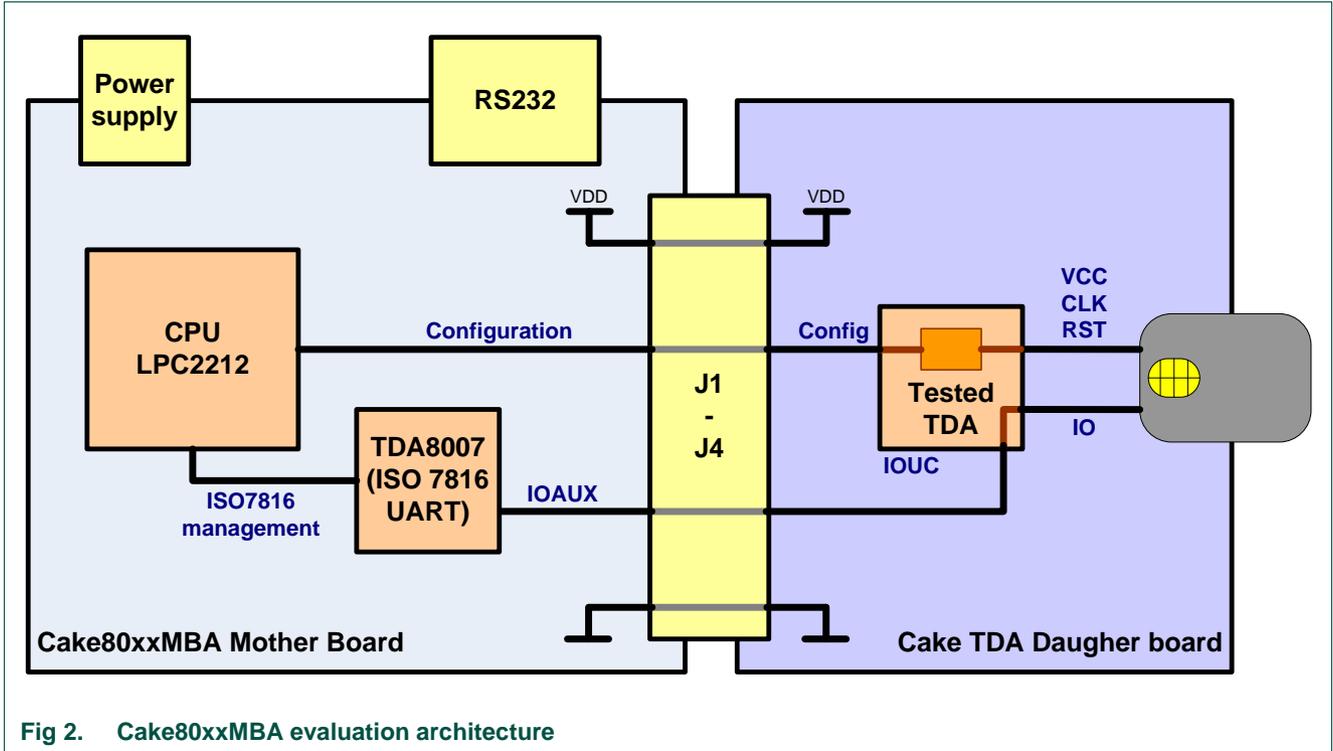

Fig 2.   Cake80xxMBA evaluation architecture

The TDA8007 on the mother board is used as an ISO7816 UART interface. Then the host CPU drives the evaluated TDA directly for the configuration and activation management, and through the TDA8007 for the smart card communication (data over IO line).

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1.2 Board connections

The Mother board must be supplied and connected to the host to be used.

1.2.1 Power supply

The power is supplied through the Jack connector J12.

This board must be supplied with 5V. On the Jack connector the 5V must be inside the connector while the ground is on the external connection.

1.2.2 Computer connection

The connection to the computer is made through an RS232 straight serial cable connected on J5.

1.2.3 Daughter boards connections

The daughter boards must be plugged on the HE10 connectors J1 to J4.

The daughter boards must always be placed so that the main smart card connector is available from the side opposed to the RS232 connector, as shown in the next figure.
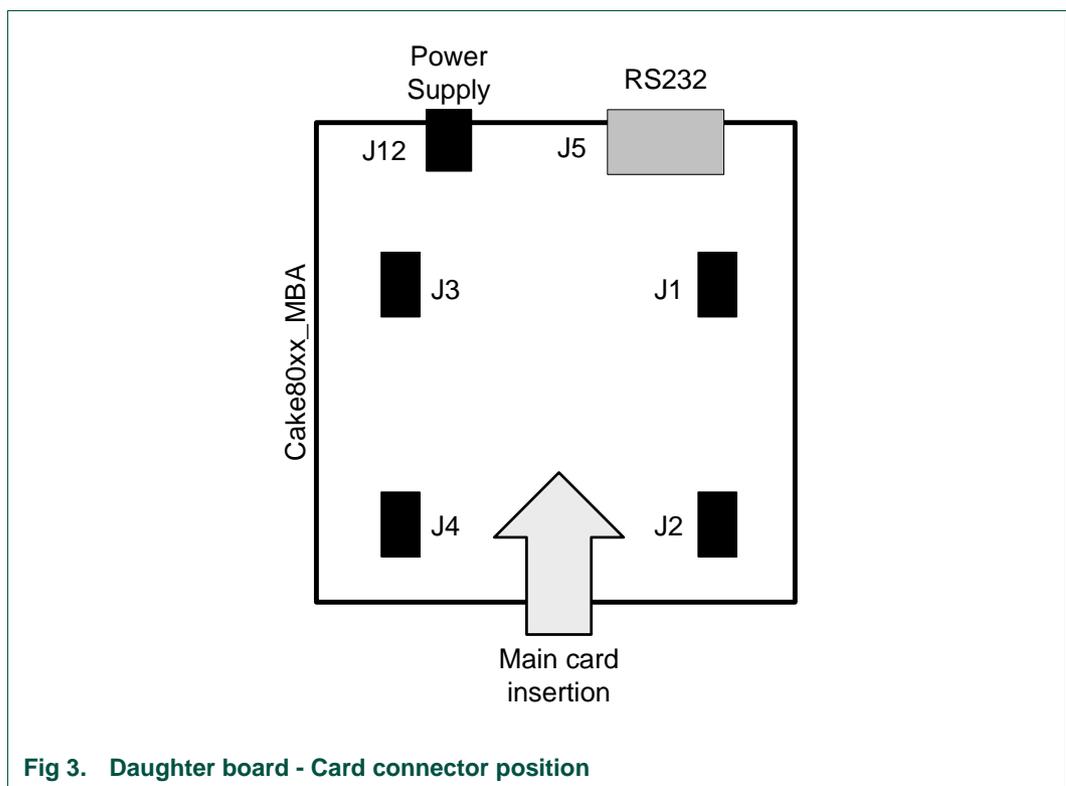

Fig 3.   Daughter board - Card connector position

With respect to this card connector position, the following figures give the position of the different daughter boards.

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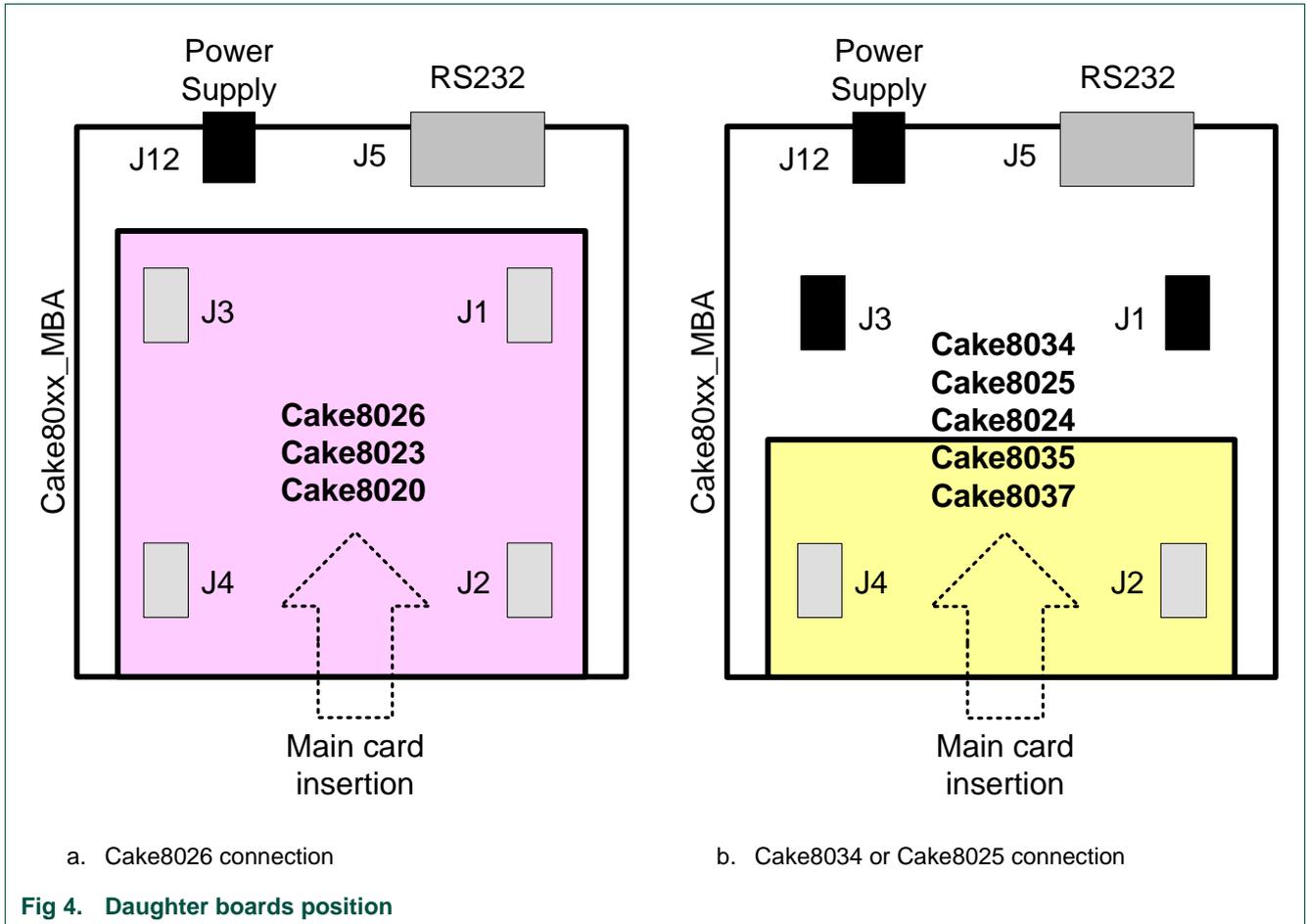a. Cake8026 connection   b. Cake8034 or Cake8025 connection

Fig 4.   Daughter boards position

- The Cake8034 and Cake8024 use only two connectors: J2 and J4. J4 is a 10 pins connector while the other (J1 to J3) are only 8 pins.
- Cake8025, Cake8035 and Cake8037 use J2 and J4 as well, but only the 8 lower pins of J4 are needed.
- Cake8026, Cake8023 and Cake8020 must be plugged on the 4 connectors J1 to J4.
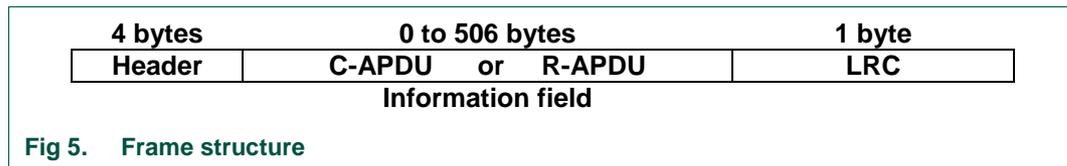
2. Communication

2.1 ALPAR Protocol

The communication between the host controller and the Cake80xx_MBA obeys to a protocol named ALPAR.
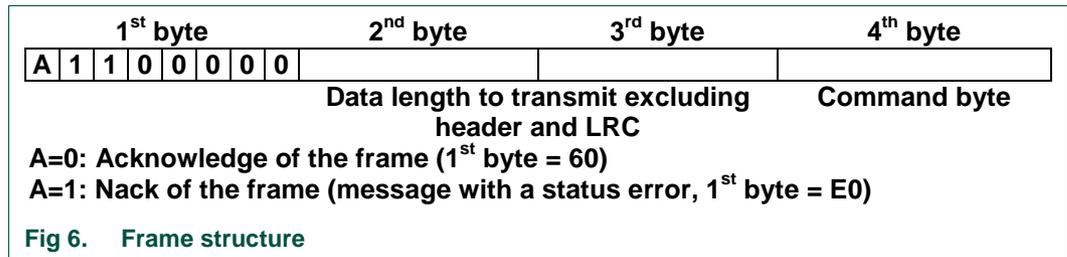
This protocol encapsulates the useful data of a message in an invariant frame structure and defines a dialog structure of messages exchanges.

Data is exchanged between the host controller and the mother board in blocks, each made up of binary characters on one byte:

   4 header characters

   0 to 506 data characters (C-APDU or R-APDU)

   1 LRC character

4 bytes	**0 to 506 bytes**	**1 byte**
Header	**C-APDU or R-APDU**	**LRC**
	Information field	

Fig 5.   Frame structure

The 4 header bytes include the following bytes:

1st byte	**2nd byte**	**3rd byte**	**4th byte**
A 1 1 0 0 0 0 0			
	Data length to transmit excluding header and LRC		**Command byte**
A=0: Acknowledge of the frame (1st byte = 60)			
A=1: Nack of the frame (message with a status error, 1st byte = E0)			

Fig 6.   Frame structure

The LRC (Longitudinal Redundancy Check) byte is such that the exclusive-oring of all bytes including LRC is null.

2.1.1 General dialog structure

The host controller is the master for the transmission; each command from the master is followed by an answer from TDACake80xx_MBA including the same command byte as the input command.

However, in some cases (card insertion or extraction, a time out detection on Rx line or an automatic emergency deactivation of the card) the Cake80xx_MBA is able to initiate an exchange.

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2.1.1.1 Successful command

System to TDA8029:

60	XX XX	YY	nnnnnnnnnnnnnnnnnn	ZZ
ACK	**length**	**code**	**Data (C-APDU)**	**LRC**

TDA8029 to System:

60	UU UU	YY (1)	mmmmmmmmmmmmmm	TT
ACK	**length**	**code**	**Data (R-APDU)**	**LRC**

(1) The same command byte YY is returned in the answer from TDA8029.

Fig 7. Successful command frame description

2.1.1.2 Unsuccessful command

System to TDA8029:

60	XX XX	YY	nnnnnnnnnnnnnnnnnn	ZZ
ACK	**length**	**code**	**Data (C-APDU)**	**LRC**

TDA8029 to System:

E0	UU UU	YY	SS (1)	TT
NACK	**length**	**code**	**Status**	**LRC**

(1) In that case, the status contains the error code information (see error list)

Fig 8. Unsuccessful command frames

2.1.1.3 Answer with an acknowledge (power_off, idle_mode, power_down_mode)

System to TDA8029 (example: power_off):

60	00 00	4D	2D
ACK	**Length**	**code**	**LRC**

TDA8029 to System:

60	00 00	4D	2D
ACK	**Length**	**code**	**LRC**

(1) In the case where the answer is an acknowledge of the command, the TDA8029 sends back a frame with the same content of the command.

Fig 9. Acknowledge frame

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2.2 Commands

2.2.1 General commands

The following command bytes are available (listed in numerical order):

Table 1. Command summary

Command	Code	Description
card_command (APDU)	00$_H$	Sends an APDU to the activated smart card
check_pres_card	09$_H$	Check the selected card presence
send_num_mask	0A$_H$	Reads the firmware version
set_card_baud_rate	0B$_H$	Sets the baudrate of the activated smart card
ifsd_request	0C$_H$	Request an IFSD change for the activated smart card communication
Set_serial_baud_rate	0D$_H$	Changes the baudrate for host communication
show_fidi	0E$_H$	Displays the current FiDi
set_serial_timeout	0F$_H$	Sets the timeout for the serial connexion
negotiate (PPS)	10$_H$	Initiates a parameter change for t=0
set_clock_card	11$_H$	Selects the division for the smart card clock
tda_write_i2c	2B$_H$	Write to a TDA connected to the CPU through I²C interface
tda_read_i2c	2C$_H$	Reads from a TDA connected to the CPU through I²C interface
start_EMV_loopback	2F$_H$	Launch the EMV loopback process. Blocking function that does not return
power_off	4D$_H$	Deactivates the current smart card
select_device	67$_H$	Selects the connected TDA daughter board
power_up_1.8V	68$_H$	Activates the card with VCC=1.8V
select_card	6A$_H$	Selects the smart card to access
power_up_3V	6D$_H$	Activates the card with VCC=3V
power_up_5V	6D$_H$	Activates the card with VCC=5V
set_nad	A5$_H$	Sets the NAD parameter for T=1 communication
idle_mode	A9$_H$	Sets the smart card in idle mode (activated with lower consumption)
get_reader_status	AA$_H$	Displays information about the current state of the reader

Table 2. Outgoing commands (only)

Command	Code	Parameter	Description
Card_extraction	A0$_H$	X0$_H$	These commands are sent as soon as a card is inserted or extracted without any command coming from the system. These commands use the same operating code but the extra parameter gives the additional information.
Card_insertion	A0$_H$	X1$_H$	
			The 'X' in the parameter (high nibble) is the number of the card that has been inserted or extracted.
Card deactivated	XX$_H$	40$_H$	The card is deactivated due to a hardware problem (short on Vcc, overcurrent)
Time out	XX$_H$	FF$_H$	Time out problem on (Cake80xx_MBA) Rx line
			This command is used in order to warn the host controller that the last communication has broken down (time out problem) so that the Rx line of Cake80xx_MBA does not remain blocked.
			The time out condition is a silence greater than 10 ms in the host command frame.
Frame lost	XX$_H$	F1$_H$	An unexpected host controller command frame has been received by the Cake80xx_MBA while it was busy to process a previous command frame.

In the last three commands, the code value is the previous code value used during a normal exchange.

2.3 Error list

The error list gives the status code identification and a brief signification of the status error code.

Table 3. List of error codes

Status code	Meaning
08$_H$	Length of the data buffer too short
20$_H$	Wrong APDU
21$_H$	Too short APDU
22$_H$	Card mute now (during T=1 exchange)
24$_H$	Bad NAD
25$_H$	Bad LRC
26$_H$	Resynchronized
27$_H$	Chain aborted
29$_H$	Overflow from card
30$_H$	Non negotiable mode (TA2 present)
31$_H$	Protocol is neither T=0 nor T=1 (negotiate command)
32$_H$	T=1 is not accepted (negotiate command)

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Status code	Meaning
33$_H$	PPS answer is different from PPS request
34$_H$	Error on PCK (negotiate command)
35$_H$	Bad parameter in command
38$_H$	TB3 absent
39$_H$	PPS not accepted (no answer from card)
3B$_H$	Early answer of the card during the activation
40$_H$	Card Deactivated
55$_H$	Unknown command
80$_H$	Card mute (after power on)
81$_H$	Time out (waiting time exceeded)
83$_H$	4 parity errors in reception
84$_H$	4 parity errors in transmission
86$_H$	Bad FiDi
88$_H$	ATR duration greater than 19200 etus (E.M.V.)
89$_H$	CWI not supported (E.M.V.)
8A$_H$	BWI not supported (E.M.V.)
8B$_H$	WI (Work waiting time) not supported (E.M.V.)
8C$_H$	TC3 not accepted (E.M.V.)
8D$_H$	Parity error during ATR
92$_H$	Specific mode byte TA2 with b5 byte=1
93$_H$	TB1 absent during a cold reset (E.M.V.)
94$_H$	TB1different from 00 during a cold reset (E.M.V.)
95$_H$	IFSC<10H or IFSC=FFH
96$_H$	Wrong TDi
97$_H$	TB2 is present in the ATR (E.M.V.)
98$_H$	TC1 is not compatible with CWT
99$_H$	IFSD not accepted
A0$_H$	Procedure byte error
C0$_H$	Card absent
C3$_H$	Checksum error

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Status code	Meaning
$C6_H$	ATR not supported
$E0_H$	Card error (bad card selected)
$E1_H$	Card clock frequency not accepted (after a set_clock_card command)
$E2_H$	UART overflow
$E3_H$	Supply voltage drop-off
$E4_H$	Temperature alarm
$E9_H$	Framing error
$F0_H$	Serial LRC error
$F1_H$	At least one command frame has been lost
FF_H	Serial time out

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2.4 Commands description

2.4.1 General commands

2.4.1.1 send_num_mask

This command is used to identify the software version which is flashed in the Cake80xx_MBA CPU.

For example the current software can be coded as: "`ARMTDA 1.0 TDA8026`"

The first string represents the firmware name, then the version is given, and finally the name of the current used daughter board is displayed.

System to CAKE80XX: 60   00 00   0A   6A

CAKE80XX to System: 60   00 01   0A   41 52 4D 54 44 41 20 31 2E 30 20 54 4D 41 38 30 32 36   LRC

2.4.1.2 Select_device

This command selects the device type plugged with the daughter board. When executed, this command changes the device to the one chosen and performs an initialization of the microcontroller and the TDA plugged.

The result of the device switch can be seen in the mask version: After the firmware version, the used device is displayed.

The following parameters are used by this command:

- 00_H: Selects the TDA8026
- 01_H: Selects the TDA8025
- 02_H: Selects the TDA8034T (SO16 package)
- 03_H: Selects the TDA8034HN (HVQFN24 package)
- 04_H: Selects the TDA8020
- 05_H: Selects the TDA8023
- 06_H: Selects the TDA8024
- 07_H: Selects the TDA8035
- 08_H: Selects the TDA8037

System to CAKE80XX: 60   00 01   67   01   06

CAKE80XX to System: 60   00 00   67   07

2.4.1.3 check_card_presence

This command is used to check the presence of a card.

System to CAKE80XX: 60   00 00   09   69

CAKE80XX to System: 60   00 01   09   PRES   LRC

Where PRES indicates the presence of the selected slot (00 if there is no card, 01 if a card is present).

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2.4.1.4 get_reader_status

This command is used to check the status of the reader.

System to CAKE80XX: 60   00 00   AA   CA

CAKE80XX to System: 60   00 01   AA   EMV PRO FIDI UX CS VER MTH YR LRC

Where:

- EMV: emv state
- PRO: protocol type.
- FIDI: current FiDi
- UX: UX parameter
- CS: Cards 1 to 4 state. High nibble=Presence, low nibble=activation
- VER: Actual version number.
- MTH: Month of the actual version
- YR: Year of the actual version

2.4.1.5 set_serial_baud_rate

This command is used for changing the baud rate onto the serial link between the host and the interface card. The default value is set to 38400 baud.

A parameter has to be transmitted in order to choose the baud rate:

System to CAKE80XX: 60   00 01   0D   PAR   LRC
CAKE80XX to System: 60   00 00   0D   6D

Table 4.   Baud rate parameter

Baud rate (Baud)	Parameter
4800	00
9600	01
19200	02
38400	03
57600	04
76800	05
115200	06

After a baud rate change, the new value takes place for the next command sent by the host.

2.4.1.6 serial_time_out

This command is sent from CAKE80XX to the host controller if, during a transmission from the host controller to CAKE80XX, the time interval between 2 characters exceeds 10ms. This timing is calculated between each character of a frame, starts after the first character, and is disabled after the last character of the frame. This feature has been implemented in order to avoid any blocking of the transmission line between the host controller and CAKE80XX.

CAKE80XX to System: E0   00 01   6F   FF   71

2.4.2 power_up commands

There are three different power up commands (5V, 3V , 1.8V). Two of them (power_up_3V and power_up_5V) have to be followed by a parameter:

- 00_H indicates that all the parameters of the ATR of the card compliant with ISO7816-3 will be taken into account.

- 01_H indicates that only the ATR of cards whose parameters are inside the E.M.V. 4.2 specification scope will be taken into account; cards having an ATR which does not comply with E.M.V. 4.2 requirements will be rejected.

2.4.2.1 power_up_5V

This command allows activating the card at a VCC of 5V. All the signals going to the card will be referenced to this VCC.

An activation sequence is processed following the ISO7816-3 normalization (VCC is rising, I/O is enabled, CLK is started, and RST is processed). If the card answers to this command, the answer will content all the ATR parameters; these parameters are memorized in CAKE80XX and will be taken into account during the whole card session (till the card is deactivated or till a warm reset is processed). The structure of the answer is the following:

System to CAKE80XX

60	00 01	6E	01	0F
ACK	Length	code	E.M.V.	LRC

CAKE80XX to System

60	XX XX	6^E	nnnnnnnnnnnnnnnnnnn	ZZ
ACK	Length	code	ATR parameters	LRC

Fig 10.   power_up_5V frame exchange

If the card is in specific mode, CAKE80XX will process the next command directly using the new interface parameters of this specific mode. If the card proposes a different Fi/Di in the ATR than the default value (Fi/Di=372), it is up to the application to make a PPS command by using the negotiate command. If the card proposes 2 different protocols in its ATR, it is up to the application to make a PPS command by using the negotiate command.

If the card does not answer to the reset, a status giving an error code is returned to the application.

In the case of E.M.V. compliant power up, if the card is using T=1 protocol, just after having received the ATR, CAKE80XX sends an IFSD request to the card indicating that the reader can manage a data buffer of 254 bytes (FEH).

The power_up_5V command can be used to generate a warm reset if the card is already activated.

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2.4.2.2 power_up_3V

This command allows activating the card at a VCC of 3V. Every signal going to the card will be referenced to this VCC.

See power_up_5V for the other characteristics.

2.4.2.3 power_up_1.8V

This command allows activating the card at a VCC of 1.8V. Every signal going to the card will be referenced to this VCC.

See power_up_5V for the other characteristics.

2.4.3 power_off

This command is used to deactivate the card whatever it has been activated for 3V or 5V operation. A deactivation sequence is processed following the ISO 7816-3 normalization in about 100µs.

System to CAKE80XX: 60   00 00   4D   2D

CAKE80XX to System: 60   00 00   4D   2D

2.4.4 card_command (APDU)

This command is used to transmit card commands under APDU format from system to CAKE80XX whatever T=0 or T=1 protocol are used. Short or extended commands (see limitations in §8.1) can be used.

An answer to such a command is also made in APDU format from CAKE80XX to the system.

Example:

System to CAKE80XX: 60   00 07   00   00 A4 00 00 02 4F 00   8E

CAKE80XX to System: 60   00 02   00   90 00   F2

2.4.5 negotiate

This command is used to make a PPS (Protocol and Parameter Selection) to the card, if in its ATR the card proposes a different Fi/Di or 2 different protocols. By using this command a PPS will be made to the card with the Fi or Di and protocol type entered as a parameter (PP). It is up to the host to make the correct Fi/Di submission to the card.

Example:

System to CAKE80XX: 60   00 02   10   PP FD   LRC

CAKE80XX to System: 60   00 00   10   70

Where FD is the ratio Fi/Di given by TA1 parameter of the ATR and PP is the protocol to be used.

If the command is acknowledged, any subsequent exchanges between the card and CAKE80XX will be made by using the new parameters.

2.4.6 Ifsd_request

This command is used to send a S(IFS request) block to the card indicating the maximum length of information field of blocks which can be received by the interface device in T=1 protocol. The initial size following the answer to reset is 32 bytes and this size shall be used throughout the rest of the card session or until a new value is negotiated by the terminal by sending a S(IFS request) block to the card.

In E.M.V. mode, the IFSD size is automatically negotiated to 254 just after the ATR has been received.

System to CAKE80XX: 60   00 01   0C   PAR   LRC

CAKE80XX to System: 60   00 00   0C   6C

Where PAR is the IFSD size.

2.4.7 set_clock_card

This command is used for changing the card clock frequency. The default value is set to FXTAL/4 which is 3.68625 MHz.

A parameter has to be transmitted in order to choose the card clock frequency:

System to CAKE80XX: 60   00 01   11   PAR   LRC

Table 5.   set_clock_card parameter
Based on a crystal with a frequency equal to 14.745MHz

Frequency	Parameter
Fxtal =14.745MHz	00
Fxtal/2=7.37MHz	02
Fxtal/4=3.68MHz	04
Fxtal/8=1.84MHz	06

After a card clock frequency change, all the waiting times are internally set to the new value.

Before applying the requested clock, the compatibility of the frequency with the current Fi used by the card is checked as described in ISO7816-3. For example, if the card has answered in its ATR a Fi parameter of 372 or 558 (fmax $\leq$ 6MHz), a change of the card clock frequency to Fxtal (14.745MHz) or Fxtal/2 (7.37MHz) will not be processed and an error status will be sent to the application.

2.4.8 card_take_off and card_insertion

These two commands are sent directly to the system processor as soon as a card extraction or insertion has occurred.

CAKE80XX to System: 60   00 01   A0   10   C1   for a card 1 extraction

60   00 01   A0   11   C0   for a card 1 insertion.

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2.4.9 set_card_baud_rate

This command is used mainly for cards which are not fully ISO 7816-3 compliant with specific and negotiable modes. As a matter of fact some cards are in specific mode but they do not give TA2 parameter in their answer to reset. So the UART has to be set to the right baud rate by means of this specific command which programs the baud rate. For non ISO baud rates there is a possibility to increase the capability of the reader by setting the bit CKU which divides by 2 the number of clock cycles of the etu and thus doubles the baud rate of the ISO UART.

Example:

System to CAKE80XX: 60 00 02 0B XX CKU LRC

CAKE80XX to System: 60 00 00 0B LRC

Where XX is the value of FiDi

if CKU=0, the baud rate is defined by FiDi

if CKU=1, the baud rate is 2 * the baud rate is defined by FiDi

For an etu of 372 clock cycles: XX=FiDi=0x11

prescaler = 31, divider = 12; 31 * 12 = 372, CKU=0.

Table 6.   Supported baudrates

As the baud rates in dark boxes are using CKU bit, they are not reachable when $f_{CLK} = f_{XTAL}/1$

TA1	CLK/ETU	TA1	CLK/ETU	TA1	CLK/ETU	TA1	CLK/ETU	TA1	CLK/ETU
0x01	372	0x31	744	0x54	186	0x95	32	0xC1	1536
0x02	186	0x32	372	0x55	93	0x96	16	0xC2	768
0x03	93	0x33	186	0x56	46.5	0xA1	768	0xC3	384
0x04	46.5	0x34	93	0x58	124	0xA2	384	0xC4	192
0x08	31	0x35	46.5	0x61	1860	0xA3	192	0xC5	96
0x11	372	0x38	62	0x62	930	0xA4	96	0xC6	48
0x12	186	0x41	1116	0x63	465	0xA5	48	0xC8	128
0x13	93	0x42	558	0x64	232.5	0xA8	64	0xD1	2948
0x14	46.5	0x43	279	0x68	155	0xB1	1024	0xD2	1024
0x18	31	0x44	139.5	0x69	93	0xB2	512	0xD3	512
0x21	558	0x48	93	0x91	512	0xB3	256	0xD4	256
0x22	279	0x51	1488	0x92	256	0xB4	128	0xD5	128
0x23	139.5	0x52	744	0x93	128	0xB5	64	0xD6	64
0x28	46.5	0x53	372	0x94	64	0xB6	32		

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2.4.10 set_nad

This command is used from the application layer in order to specify a SAD (source address) and a DAD (destination address) for a logical connection using T=1 protocol as defined in ISO7816-3. The default value is 00 and will be kept until the send NAD command has been notified to the CAKE80XX. Any NAD submission where SAD and DAD are identical (except 00) will be rejected. If bits b4 or b8 of the NAD required are set to 1 (VPP programming) the NAD will be rejected.

The NAD shall be initialized before any information exchange with the card using T=1 protocol, otherwise and error message will be generated.

System to CAKE80XX: 60   00 01   A5   NAD   LRC

CAKE80XX to System: 60   00 00   A5   LRC

Where   NAD is the new value of NAD immediately taken into account.

2.4.11 TDA_write_i2c

This command writes a value on an I²C address if a TDA with I²C interface is connected on the board (e.g.: TDA8026).

The answer from the board is an acknowledge.

Example:

System to CAKE80XX: 60   00 02   2B   ADD VAL   LRC

CAKE80XX to System: 60   00 00   2B   LRC

Where ADD is the I²C address, and VAL is the value to write.

2.4.12 TDA_write_i2c

This command reads a value on an I²C address if a TDA with I²C interface is connected on the board (e.g.: TDA8026).

The answer from the board is the read value.

Example:

System to CAKE80XX: 60   00 01   2C   ADD LRC

CAKE80XX to System: 60   00 01   2C   VAL   LRC

Where ADD is the I²C address, and VAL is the read value returned.

2.4.13 Start_EMV_Loopback

These commands launch the EMV Loopback mechanism. This is a loop which tries to activate the smart card (slot 1) every second. If the card activation is success, then the EMV loopback starts and the full test is performed automatically.

At the end, the loop restarts, trying to activate again the smart card.

This commands never returns and works by itself. It allows passing a full EMV protocol certification without any action from the user. (But it can display data on the serial link)

System to CAKE80XX: 60   00 01   2F LRC

CAKE80XX to System: ASCII DATA

3. Embedded firmware

The mother board Cake80xxMBA is supplied with a loaded firmware with a protocol interface described in the communication chapter.

The loaded firmware may not be the one described in this file but a previous version. If the latest one is required, it must be compiled and loaded using the following description.

The source code of this mother board is available as a MSVC solution, provided with an installer: Cake80xxMBAFW_setup.exe.

This solution is based on MSVC 2003 for the text editor, but as it's an ARM embedded software, it uses GNUARM compiler and linker.

3.1 Compiler

The GNUARM Compiler can be downloaded from the GNUARM website:

www.nxp.com/redirect/gnuarm.com/

The package that has been used to build the Firmware is the GCC-4.1 toolchain for cygwin:

http://www.gnuarm.com/bu-2.17_gcc-4.1.1-c-c++_nl-1.14.0_gi-6.5.exe

For the project to be built, the GNUARM compilers must be installed in the C:\GNUARM folder.

If another folder is chosen, then the GNUARM dir in the Build.mak file must be updated.
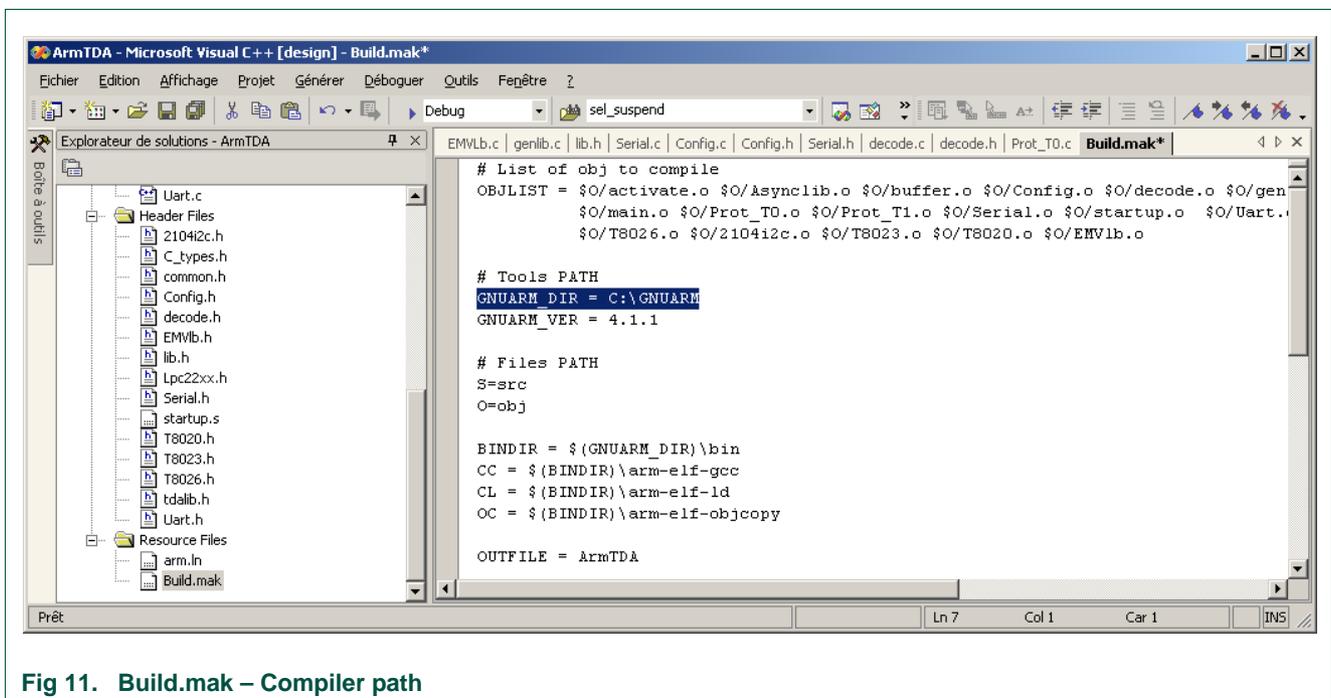
Fig 11. Build.mak – Compiler path

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3.2 Loader

Once the Firmware has been built, it can be loaded using LPC2000 Flash Utility which can be downloaded from the NXP website:

http://www.nxp.com/documents/other/lpc2000_flash_isp_utility.zip

The loader must be configured as follows:
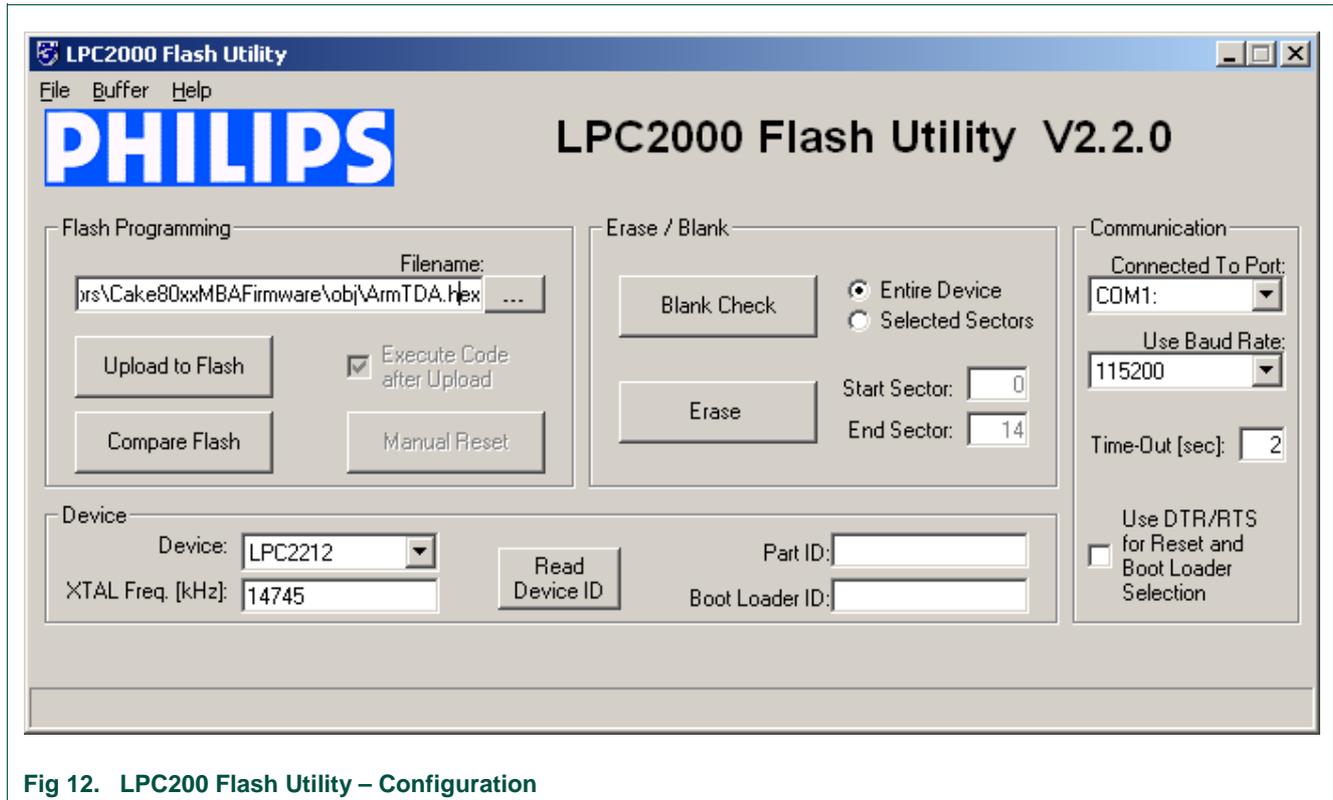
Fig 12. LPC200 Flash Utility – Configuration

The COM port must be adapted to the one used to connect the Cake80xx_MBA board.

The filename is the built hex file. By default, after source code installation, the path is:

C:\Program Files\NXP Semiconductors\Cake80xxMBAFirmware\obj\ArmTDA.hex

To load the software, follow the steps:

- Supply the Cake80xxMBA board, and connect the serial port to the PC COM port
- Click on the "Upload to Flash" button under the Flash Utility tool
- When the tool asks to reset the board, press and hold the ISP switch of the Cake80xxMBA, then press and release the RST switch, and finally release ISP
- Click on OK in the message box of Flash Utility
- The load starts

After the load is completed, reset the board by pressing the RST switch only, the board restarts with the new FW.

4. Special comments

4.1 Remarks for CAKE8037T and CAKE8037TT Support

If you get the Motherboard is not marked CAKE80xx_MBA_01_v2 (or has a blue sticker) on it, the quartz Y1 needs to be changed in order to be able to use the CAKE8037T or the CAKE8037TT. This is because the TDA8037 can only divide the frequency by 1 or 2.

The new quartz Y1 needs to be between 4 and 5 MHz.
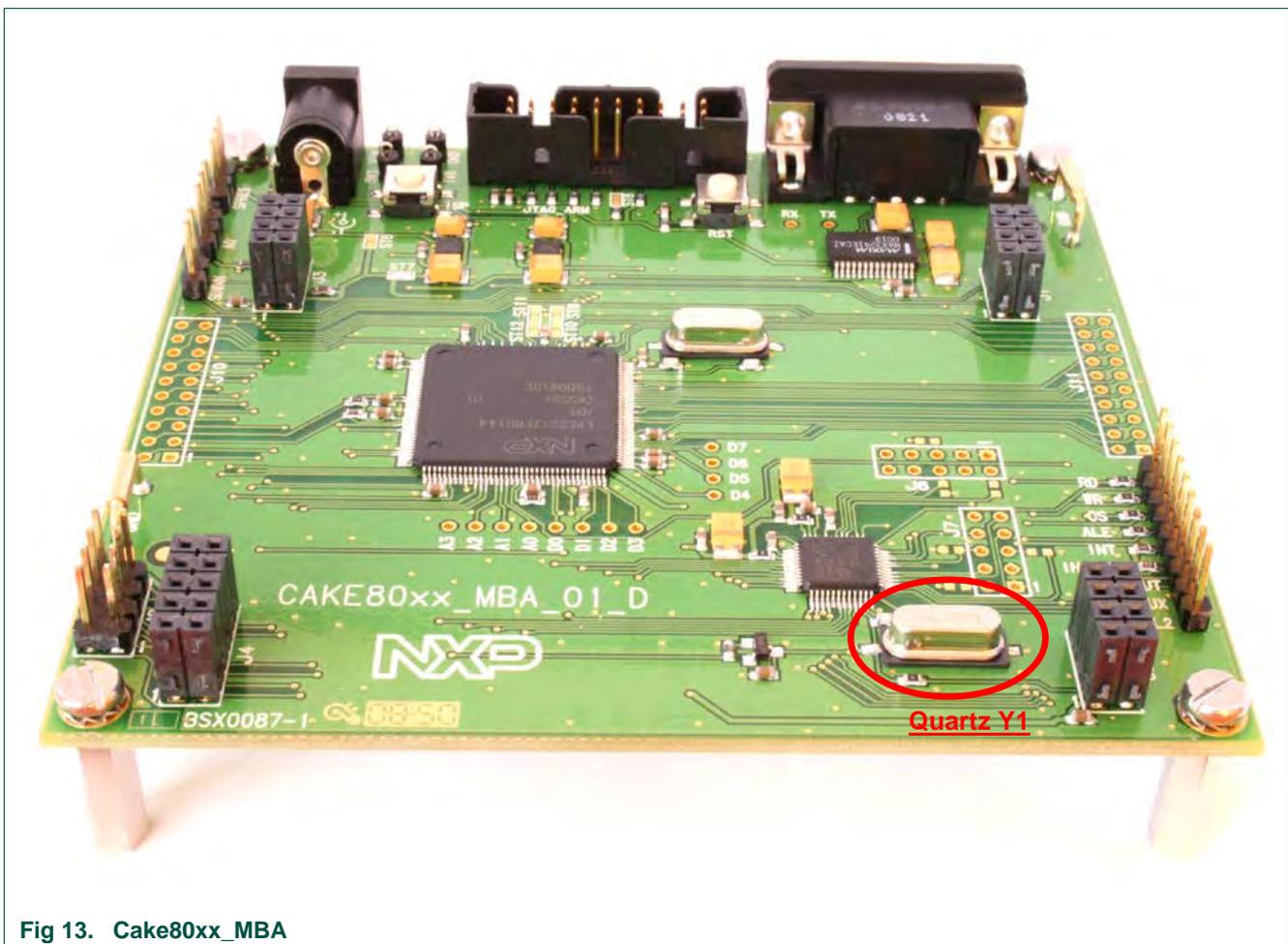
Fig 13.   Cake80xx_MBA

5. Schematic and layout

5.1 Schematic
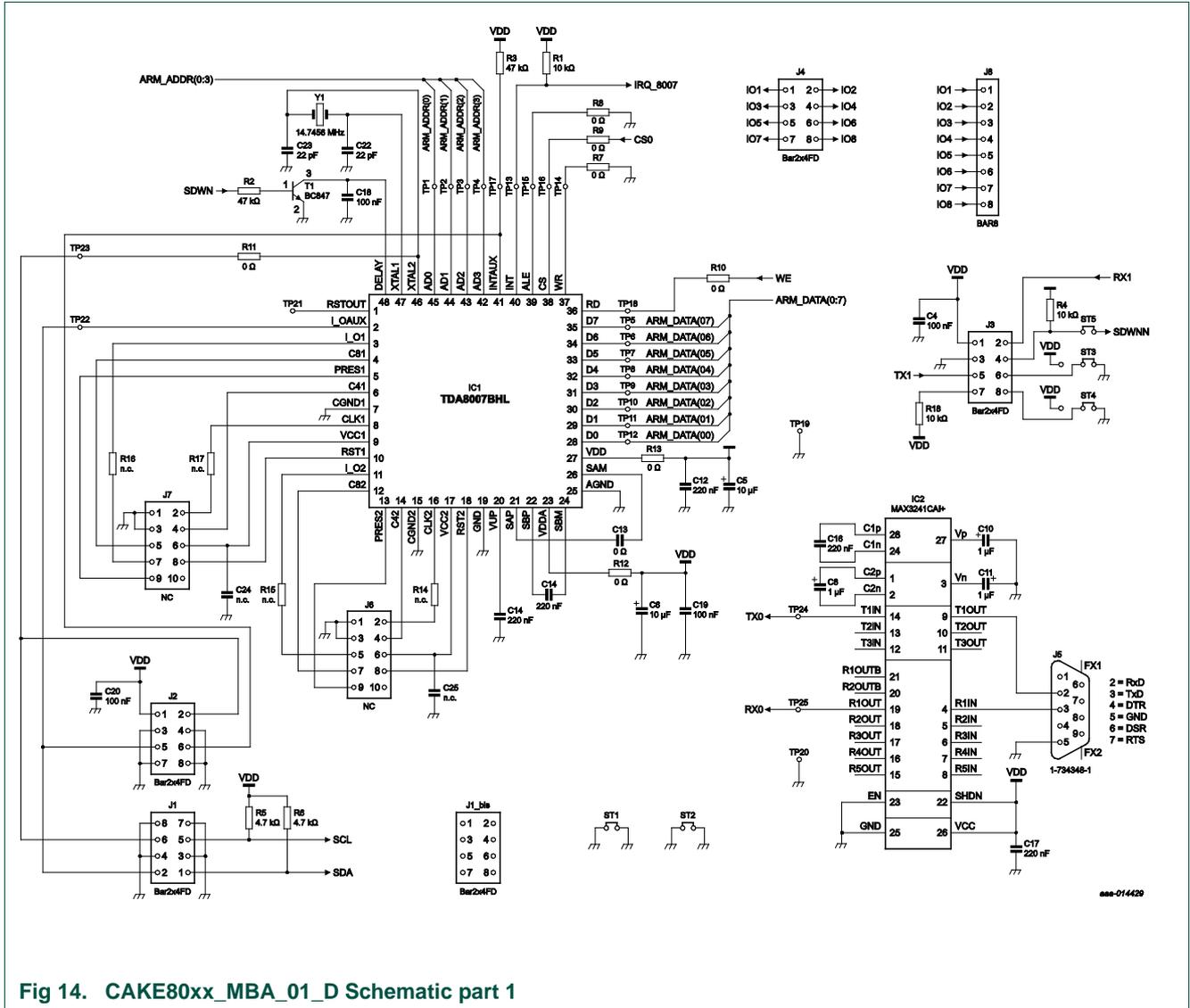
Fig 14. CAKE80xx_MBA_01_D Schematic part 1

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Fig 15. CAKE80xx_MBA_01_D Schematic part 2

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Fig 16.   CAKE80xx_MBA_01_D Schematic part 3

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5.2 Layout

BSX0087-1 Cuivre Top

Fig 17. Layout - Top Layer

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BSX0087-1 Cuivre Bottom

Fig 18.   Layout – Bottom Layer

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5.3 BOM

COMPANY PART NO.	COUNT	REFERENCE	GEOMETRY	DESCRIPTION	Fournisseur
pnsx_b3s_1000	2	BP1 BP2	sw_b3s	B3S-1000, OMRON:B3S-1000 Bouton poussoir CMS 6x6	
pnsx_bar2_cav	1	ST5	cav_254_bar2md	BAR2_CAV, Barrette male droite, pas:2.54mm, h:7mm, 2 points + cavalier	
pnsx_bar2x10mdNC	2	J10 J11	con_bar_254_2x10_md	NC, ***NON CABLE*** Barrette male droite double rangee, 2x10 points, Pas:2.54mm, H=7mm	
pnsx_bar2x4fd	3	J1 J2 J3	con_bar_254_2x4_fd	Bar2x4FD, Barrette femelle droite double rangee, 2x4 points, Pas:2.54mm, H=8.5mm, ex:KONTEK:4773541108470	
pnsx_bar2x4md	1	J8	con_bar_254_2x4_md	Bar2x4, Barrette male droite double rangee, 2x4 points, Pas:2.54mm, H=7mm	
pnsx_bar2x5fd	1	J4	con_bar_254_2x5_fd	Bar2x5FD, Barrette femelle droite double rangee, 2x5 points, Pas:2.54mm, H=8.5mm, ex:KONTEK:4773541110470	
pnsx_bar2x5mdNC	2	J6 J7	con_bar_254_2x5_md	NC, ***NON CABLE*** Barrette male droite double rangee, 2x5 points, Pas:2.54mm, H=7mm	
pnsx_bar3_cav	2	ST3 ST4	cav_254_bar3md	BAR3_CAV, Barrette male droite, pas:2.54mm, h:7mm, 3 points + cavalier	
pnsx_bc847	1	T1	sot23	BC847, NXP: BC847, Transistor NPN general purpose, 45V 100mA	
pnsx_c0603_100nf_50V	26	C4 C18 C19 C20 C31	c0603	100nF, Capacite X7R 0603 50V, 10%	
		C32 C33 C34 C35			
		C36 C37 C38 C39			
		C40 C41 C42 C43			
		C44 C45 C46 C47			
		C48 C49 C50 C51			
		C52			
pnsx_c0603_220nf_25V	6	C12 C13 C14 C15	c0603	220nF, Capacite X7R 0603 25V, 10%	
		C16 C17			
pnsx_c0603_22pf_50V	4	C22 C23 C53 C54	c0603	22pF, Capacite COG 0603 50V, 5%	
pnsx_c0603_nc	2	C24 C25	c0603	N.C., Capacite type 0603 ***NON CABLE***, -	
pnsx_cav_1016	2	ST1 ST2	cav_1016	CAV_10.16, Cavalier dore 10.16mm KONTEK:3130676000500	
pnsx_chev_citr_s	1	ST7	chev_citr_o_bom	A_SOUDER, Chevron Citroen 0603 !!! A SOUDER !!!	
pnsx_dc10a	1	J12	con_jack_alim_dc10	DC-10A, CLIFF:DC-10A Connecteur Jack DC power diam:2.1mm	
pnsx_hc49_sm_14.7456mh	2 2	Y1 Y2	xtal_hc49_sms	14.7456MHz, Quartz package HC49/4H-SMD 14.7456MHz, 30ppm, ex:CITIZEN_AMERICA: HCM49 14.7456MABJ-UT	
pnsx_he10bpr_2x10md	1	J9	con_he10bp_2x10_md	N2520-6002RB, HE10 bas profil 20 points, male droit, ex:3M:N2520-6002RB	
pnsx_lp38693sd_1.8	1	IC4	llp6	LP38693SD-1.8, NATIONAL_SEMICONDUCTOR:LP38693SD-1.8 Low drop CMOS regulator 500mA 1.8V	
pnsx_lp38693sd_3.3	1	IC3	llp6	LP38693SD-3.3, NATIONAL_SEMICONDUCTOR:LP38693SD-3.3 Low drop CMOS regulator 500mA 3.3V	
pnsx_lpc2212	1	IC5	lqfp144_sot486_1	LPC2212FBD144, NXP: LPC2212FBD144 Microcontroleur 16-32bits, 128kB Flash, 10-bit ADC, package:lqfp144	NXP
pnsx_max3241cai	1	IC2	ssop28_sot341_1	MAX3241CAI+, MAXIM:MAX3241CAI+, Transceiver RS232, 3.0 to 5.5V, ESD protected, 1Mbps, Package:ssop28	NXP
pnsx_r0603_0	7	R7 R8 R9 R10 R11	r0603	0, Resistance Package CMS 0603 1% 0.1W	
		R12 R13			
pnsx_r0603_10k	9	R1 R4 R18 R19 R20	r0603	10k, Resistance Package CMS 0603 1% 0.1W	
		R21 R22 R23 R24			
pnsx_r0603_47k	2	R2 R3	r0603	47k, Resistance Package CMS 0603 1% 0.1W	
pnsx_r0603_4k7	4	R5 R6 R25 R26	r0603	4k7, Resistance Package CMS 0603 1% 0.1W	
pnsx_r0603_nc	4	R14 R15 R16 R17	r0603	N.C., Resistance Package CMS 0603 1% 0.1W ***NON CABLE***	
pnsx_subd_09fc_tyco	1	J5	con_subd_09_fc_tyco	1-734348-1, TYCO:1-734348-1, SubD 9 points, femelle coude, serie AMPLIMITE	
pnsx_taja_10u_10v	2	C29 C30	cap_320x160x160_a	10uF, Capacite Tantalium Package TAJA AVX:TAJA106K010R, 10%, 10V-85 degres / 7V-125 degres	
pnsx_tajb_10u_16v	2	C5 C6	cap_350x280x190_b	10uF, Capacite Tantalium Package TAJB AVX:TAJB106K016R, 10%, 16V-85 degres / 10V-125 degres	
pnsx_tajb_1u_35v	3	C8 C10 C11	cap_350x280x190_b	1uF, Capacite Tantalium Package TAJB AVX:TAJB105K035R, 10%, 35V-85 degres / 23V-125 degres	
pnsx_tajb_33u_10v	3	C26 C27 C28	cap_350x280x190_b	33uF, Capacite Tantalium Package TAJB AVX:TAJB336K010R, 10%, 10V-85 degres / 7V-125 degres	
pnsx_tda8007b	1	IC1	lqfp48_sot313_2	TDA8007BHL, NXP: TDA8007BHL Double multiprotocol IC card interface package:lpfq48	NXP
pnsx_tp_bar1	11	TP13 TP14 TP15	tp_bar1	TP_Bar1, Barrette male droite, h:7mm 1 point, SAMTEC:HTSW-1-01-07-G-S	
		TP16 TP17 TP18			
		TP21 TP22 TP23			
		TP24 TP25			
pnsx_tp_bar1_nc	12	TP1 TP2 TP3 TP4	tp_bar1	N.C., ***NON CABLE***	
		TP5 TP6 TP7 TP8			
		TP9 TP10 TP11 TP12			
pnsx_tp_boucle1_n	4	TP26 TP27 TP28	tp_boucle_d100	5001, TestPoint:KEYSTONE:5001 Noir	
		TP29			
zbulle01	1			Circuit_imprime:BSX0087-1	
zbulle02	4			BULLE02:Entretoise_Hexag_fem_M3x15_laiton-ETL305015	
zbulle03	4			BULLE03:Vis_C_M3x6_Inox	
zbulle04	4			BULLE04:INTER_INOX:A2M320_rondelle_eventaille_inox	
zcav254snt	3			cavalier_2.54mm:SAMTEC:SNT-100-BK-G	

Fig 19. Bill of materials

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