AN11458

Design guideline for TDA8037

Rev. 1.1 — 1 October 2014 **Application note**

Document information

Info	Content
Keywords	TDA8037, Smart Card Interface, Pay TV, STB, CISCO, ISO 7816-3
Abstract	This application note describes the smart card interface integrated circuit TDA8037. This document helps to design the TDA8037 in an application. The general characteristics are presented and different application examples are described.

Revision history

Rev	Date	Description
1.1	20141001	First official release
1.0	20140109	Initial version

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1. Introduction

1.1 Presentation

The TDA8037 is a smart card interface device forming the electrical interface between a micro controller and a smart card. This device mainly supports asynchronous cards (micro controller-based IC cards).

The electrical characteristics of the TDA8037 are in accordance with CISCO technology requirements (IRD Electrical Interface Specifications doc n° LC-T056) and also comply with ISO7816-3 for class B.

The TDA8037 can be used in various applications such as pay-TV, Point-Of-Sale terminals (POS), public phones, vending machines, and many conditional access applications (i.e. Internet...).

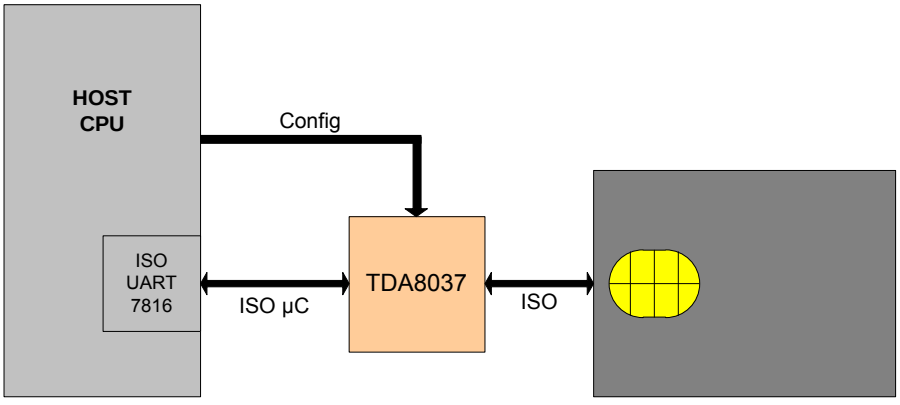


Fig 1. Simplified interfacing view

In the whole document, TDA8037T and TDA8037TT will be referred as TDA8037 for the commons features.

2. Power supply

2.1 Power supply pins

V_{DD} input pins is used to supply the TDA8037. V_{DD} is dedicated to the interface supply. All signals which are interfaced with the host are referenced to this voltage supply.

The next table describes all the pins that must be referenced to $V_{DD.}$

Table 1. V_{DD} referenced pins

Pin name	Comment
IOUC	Smart card data. Controlled by the microcontroller
PORADJ	External configuration of V_{DDhost} supervision threshold
CMDVCCN	Smart card activation. Controlled by a microcontroller GPIO
CLKDIV	Control of the clock division. Can be controlled by the microcontroller or connected directly to GND or $V_{DD(HOST)}$
RSTIN	RST pin management. Controlled by a microcontroller GPIO
OFFN	Output to the host. Must be connected to the microcontroller and therefore have the same level
CLKIN	External oscillator
CS	Chip select signal
PRESN	Not connected to the microcontroller but reference to V_{DD} The smart card connector presence switch must use V_{DD}
AUX1UC	Management of AUX1UC. Controlled by the microcontroller
AUX2UC	Management of AUX2UC. Controlled by the microcontroller

A voltage V_{REG} is internally generated by the TDA8037 and used for the internal digital part. V_{DD} is used to supply the internal regulator that generates V_{REG}.

V_{REG} supplies the core of the TDA8037. Its value is always 1.8 V.

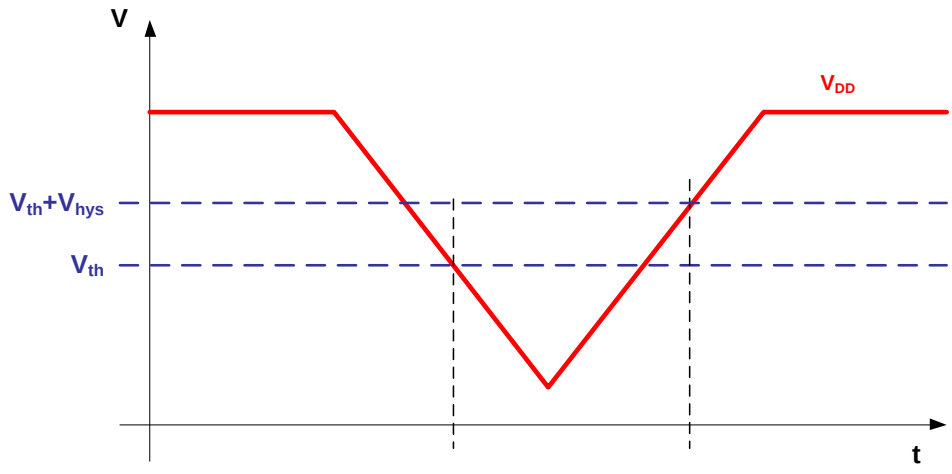
2.2 Supply supervisor

2.2.1 Main principles

The TDA8037 supervises the voltage level of V_{REG}, V_{DD} and V_{DDhost}. For V_{REG} and V_{DD} supervision, the threshold is internally fixed. For V_{DDhost}, the threshold is set by using the PORAdj pin. If you don't want to specify a threshold, connect PORAdj to V_{DD}.

The following figure explains the supervision for all the supplies.

Then the table gives the threshold values for each input.



(1) When one power supply input falls below its corresponding threshold, the TDA8037 is in reset mode. When all the levels are above their threshold + the hysteresis, the TDA8037 is ON.

Fig 2. Supply supervisor principles

2.2.2 Supervision with PORAdj used

The TDA8037T allows to fix externally the threshold on V_{DDhost}. This can be done by using an external resistor bridge on the PORAdj pin.

The supervision principle is given in the next two pictures:

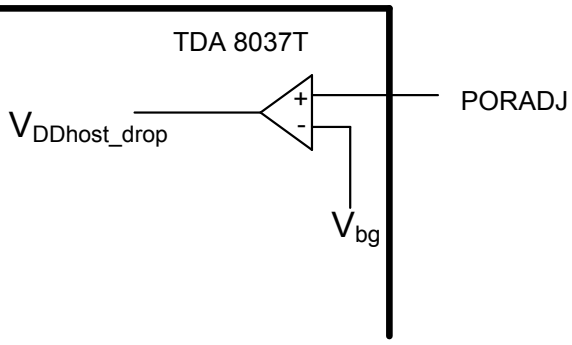


Fig 3. V_{DDhost} supervision – PORADJ level detector

The TDA8037 compares the pin voltage level on pin PORADJ to an internal Reference voltage called Vbg (for Bandgap voltage).

When PORADJ falls below Vbg, the TDA8037 is reset:

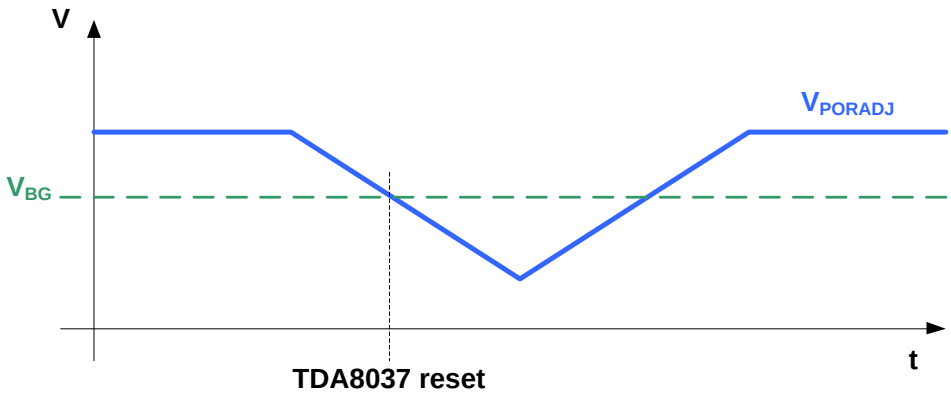


Fig 4. V_{DDhost} supervision – Reset when PORADJ falls

In order to set a specific supply supervisor value on V_{DDhost}, a resistor bridge referred to V_{DDhost} must be connected to PORADJ:

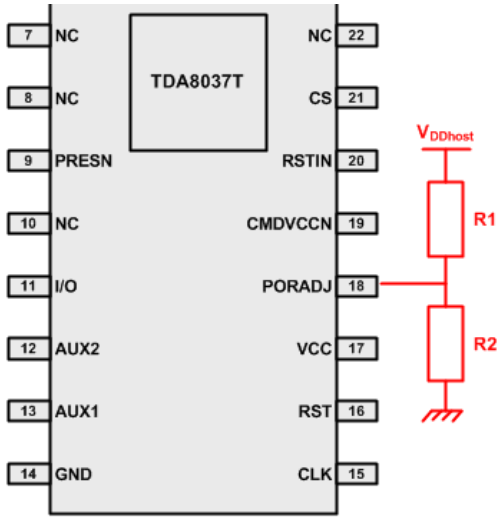


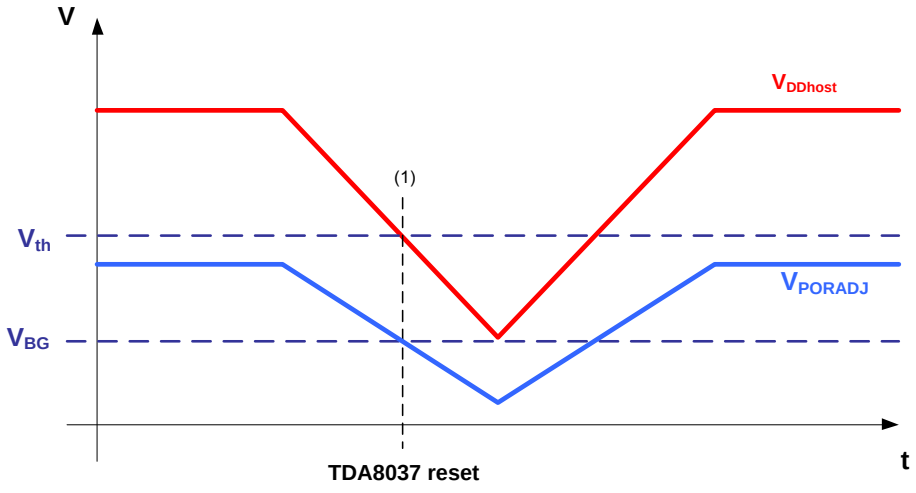
Fig 5. V_{DDhost} supervision – Resistor bridge

In this case $V_{PORADJ} = V_{DDhost}.R2/(R1+R2)$ and V_{DDhost} is monitored indirectly: the TDA8037 enters the reset mode when $V_{DDhost}.R2/(R1 + R2)$ falls below V_{bg}.

This corresponds to a "virtual" threshold on V_{DDhost} which value is obtained when

$Vbg = V_{DDhost}.R2/(R1+R2) \rightarrow V_{DDhost} = V_{bg}.(1+R1/R2)$

This virtual threshold is the Vth corresponding to V_{DDhost}. This is called virtual as V_{DDhost} is never compared to V_{th}. Only V_{PORADJ} is compared to V_{bg}. The following drawing shows this behavior:



(1) When V_{DDhost} falls below $V_{th,}$ V_{PORADJ} falls below V_{bg} then the drop-off is detected

Fig 6. V_{DDhost} supervision – Virtual V_{DDhost} threshold Vth

The resistor bridge is needed only in the case a specific threshold on V_{DDhost} must be chosen for the application, but in the general case, V_{DDhost} can be input directly on PORADJ.

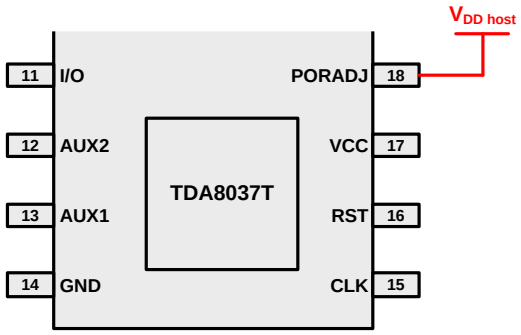


Fig 7. V_{DDhost} supervision – No resistor bridge

This is a particular case of the previous description with R1 = 0Ω and R2 = ∞.

Here Vth = Vbg.(1+R1/R2) = Vbg.

2.2.3 Summary

The following table gives the different threshold values for each supply input pin.

Table 2. Supply supervisor - Typical threshold values

	V_{REG}	V_{DD}	V_{DDhost} (No PORADJ bridge)	V_{DDhost} (PORADJ bridge used)
Typ. V_{th}	1,35	2.6V	0.84V	0.86 x (1+R1/R2)
Typ. V_{hys}	75mV	50mV	65mV	65mV

2.3 Shutdown mode

The shutdown mode is the default mode when the card is not active (CMDVCCN HIGH). The max consumption in this mode is 400 µA.

Due to this mode, the activation timing changes a bit compared to the TDA8024. Refer to the “Activation” chapter to see the exact difference induced by this mode.

In this mode the supervisors are active, card presence detection is available.

3. Input Clock

3.1 Clock and clock selection

An external clock on CLKIN is required. At start, it can be from 1 MHz to 10MHz for TDA8037T and 1MHz to 5MHz for TDA8037TT. (Avoid the very max frequency at start, in particularly for certification)

The input clock must be referenced to V_{DD}.

The clock is not mandatory outside of the card session. However, it is mandatory to start it before CMDVCCN is LOW, but it is not necessary to apply it when the card must not be activated.

The following figures represent the two configurations and the way they are used.

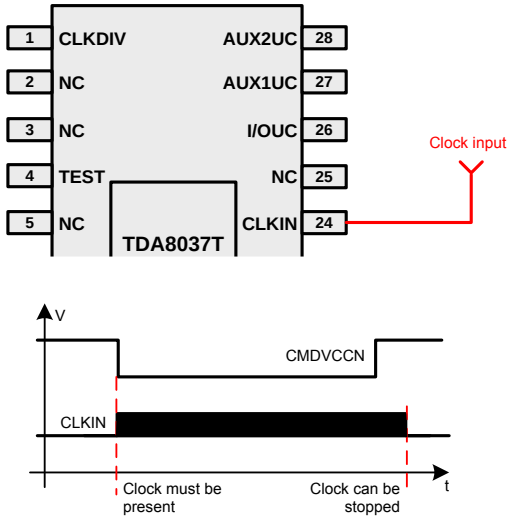


Fig 8. TDA8037 clock

The clock frequency can be managed by the host on CLKIN. On the TDA8037T, CLKDIV can also be used to switch the frequency. However on the TDA8037T, be sure the CLKDIV pin is set to low level before changing the frequency on CLKIN.

3.2 Duty cycle

On the card side, the duty cycle of the clock line must be in the range 45 % to 55 % to be compliant with most of the standards.

This duty cycle is guaranteed by the TDA8037 for any clock generated by the TDA with a division by 2.

Therefore, whatever the input clock frequency, duty cycle, voltage levels on the host side, as long as they respect the input specification, the card CLK duty cycle will be in the range.

4. Chip select

The TDA8037T implements a functionality that allows cascading several devices using the same connection pins. The following signals can be multiplexed:

- CMDVCCN
- RSTIN
- CLKIN
- IOUC
- AUX1UC
- AUX2UC
- OFFN
- CLKDIV

4.1 Active device

To drive a TDA8037, its corresponding CS pin must be tied to high level. Then all the configuration pins behaves as expected.

If the CS pin is pulled to low, then all the pins are high impedance and the TDA8037 keeps internally its last configuration.

The following figure shows the behavior, when the TDA8037 is fixed in its state when CS is low. Whatever the value of any configuration pin, the behavior is always the same. The figure shows this behavior with CMDVCCN. The value on CMDVCCN only has an action on the chip when CS is high, or becomes high.

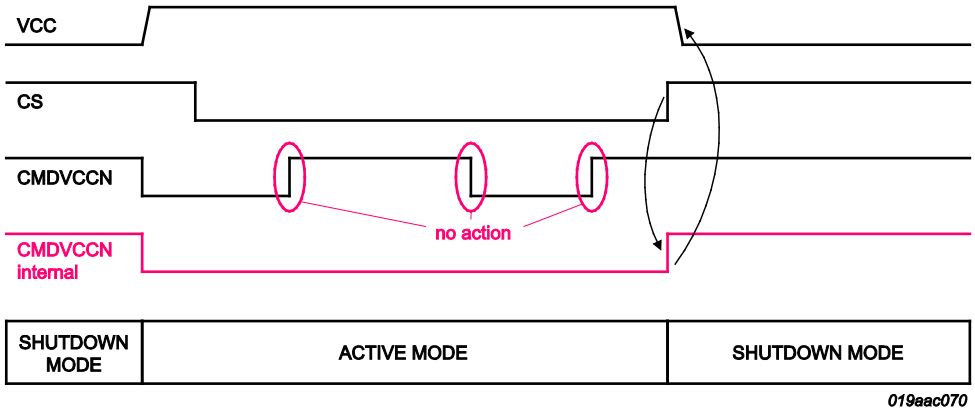


Fig 9. CS action on CMDVCCN behavior

The signal CMDVCCN Internal represents the value that is seen by the TDA8037: the value is latched as soon as CS goes low, and can only change after CS goes back high.

In this case, when CS rises, CMDVCCN internal become high, which causes the deactivation.

The behavior of OFFN is affected in the same way by CS. OFFN from any unactive device will always be kept to high level. Then the host must regularly check each device to know its state.

The following figure gives an example with a card removal when the device is not active:

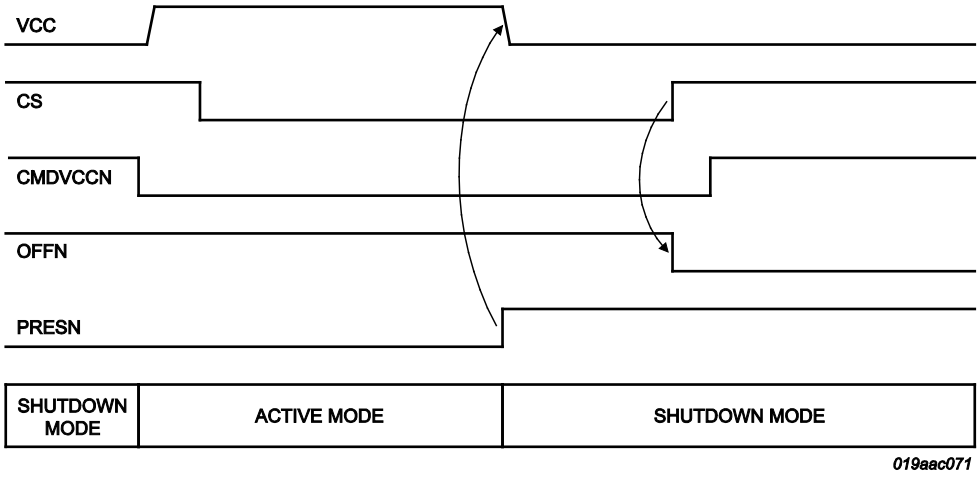


Fig 10. CS action on OFFN behavior

This shows that when the card is removed (or by extension when any fault is detected), the TDA automatically deactivate the card, in order to protect it.

But the host is not warned if the CS pin is low. It will only know that the fault occurred after it has pulled the CS pin high.

4.2 Schematics

The following schematics give an example on how to connect 2 TDA8037 to a host.

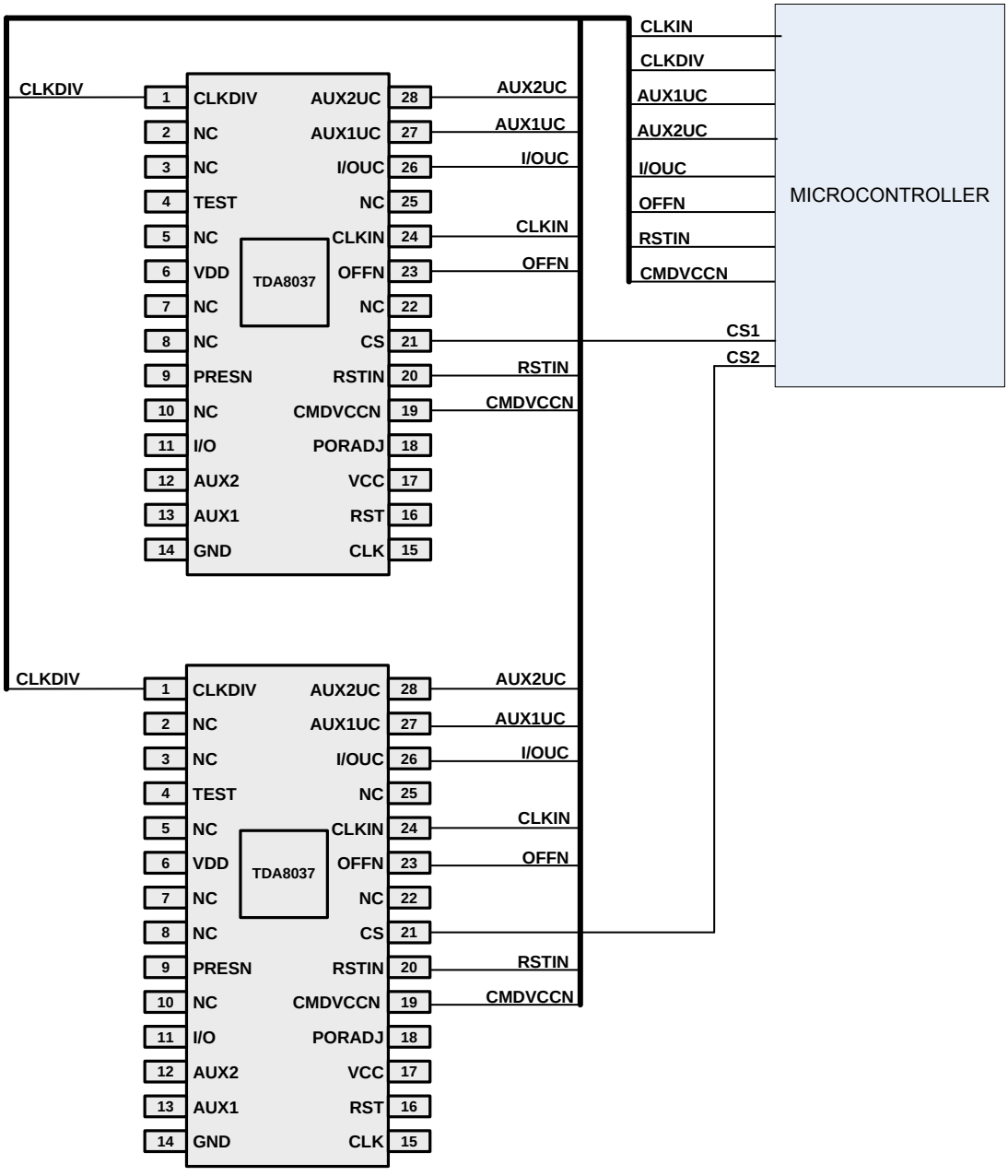


Fig 11. 2 cascaded TDA8037 devices

4.3 Device switch

Using the previous design, some precautions must be taken when switching from one device to another:

Only one CSx signal must be active at the same time

The configuration signals must be saved before clearing the CSx pin, and restored before raising the CSx pin.

The following picture shows the sequence that must be followed to activate smart card from device 1, then activate smart card from device 2, and finally send APDU to device 1.

Only CMDVCCN behavior is shown here, but all input signals must be handled in the same way (save and restore).

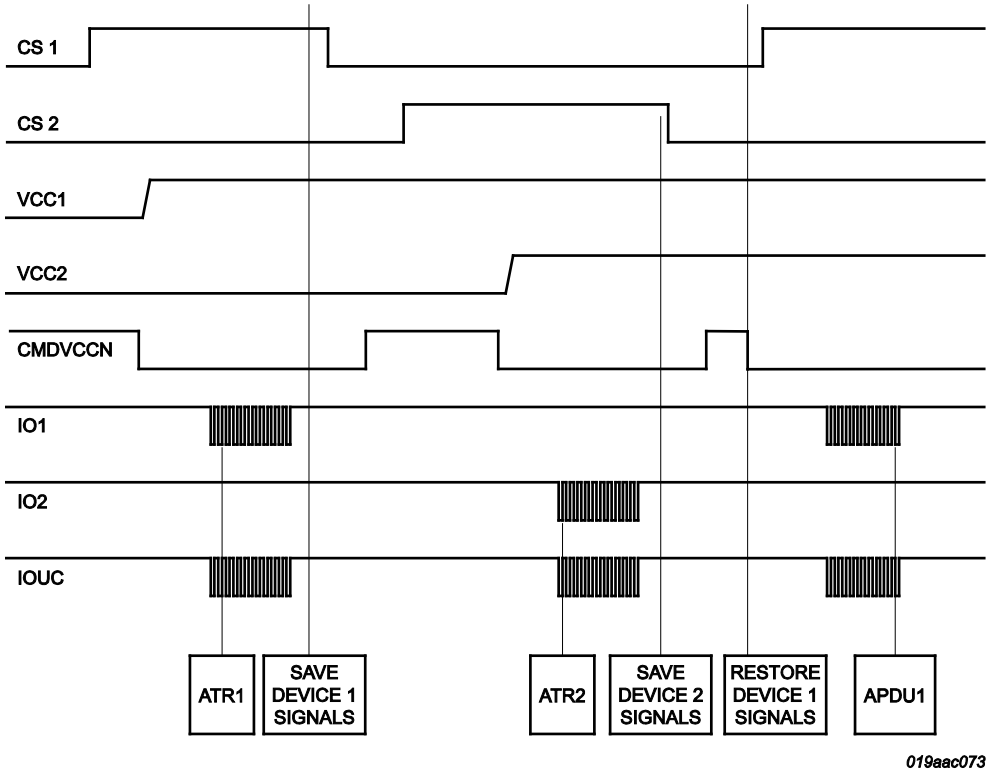


Fig 12. 2 devices management with CS

5. Card connector

5.1 Presence pin

One input pin is available to detect the card presence: PRESN.

This pin is active LOW and embeds an internal resistor to GND. Therefore, when the pin is left open, the card is assumed to be present.

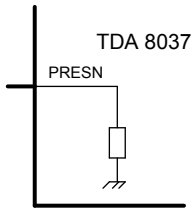


Fig 13. Presence input pin

The way to connect the switch of a smart card connector depends on its gender (normally open or normally closed).

5.1.1 Normally closed presence switch

The TDA8037 is planned to be used with this type of card connector without any external component. The connection of this card connector presence switch is shown in the next figure:

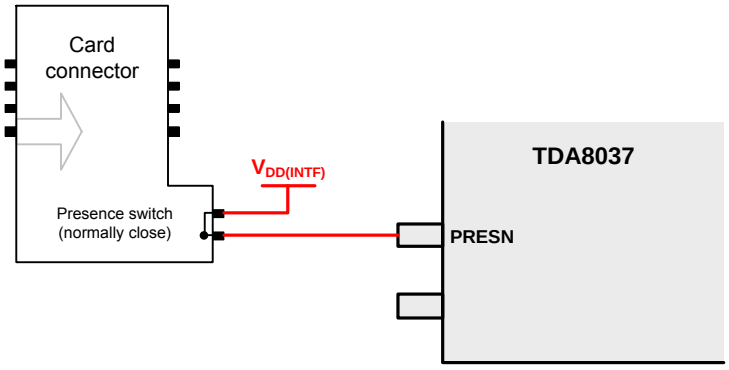


Fig 14. Normally closed card connector connection

When the card is not inserted, the switch is closed, and the PRESN pin is not active and the card is assumed to be absent.

When the card is inserted, the switch is opened and the PRESN pin is driven to low by its internal resistor connected to the ground. The pin is active and the card is seen as present.

5.1.2 Normally open presence switch

5.1.2.1 Schematics

To use this type of card connector, an external resistor is mandatory, and the schematics must be used as shown hereafter:

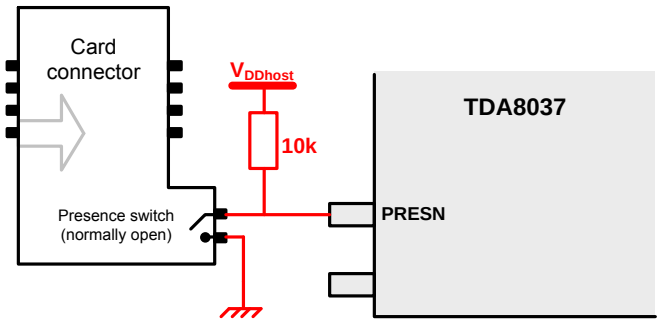


Fig 15. Normally closed card connector connection

When the card is not inserted, the switch is open and PRESN is pulled-up to HIGH level. The pin is not active so the card is seen as absent.

When the card is inserted, the switch is closed. Then the PRESN pin is directly connected to ground. PRESN is then active and the card is seen as present.

The circuit is optimized to work with a normally closed switch. Although fully functional, a design with a normally open switch consumes more power than a design with a normally closed switch.

5.1.2.2 Pull-up resistor calculation

The PRESN is internally connected to GND through a pull-down resistor.

Depending on the PRESN level, the pull-down resistor can have different value:

- When PRESN is high (not active), the resistor value is 1MΩ (to reduce current consumption)
- When PRESN is low (active), the resistor value is 30kΩ

To choose the pull-up resistor, the 30kΩ value must be taken into account. Indeed, the goal is to pull the PRESN line to V_{DD} when the card is removed and the switch opened.

The 30kΩ pull-down has a 20% precision, then the minimum value can be 24kΩ.

If R_{ext} is the external pull-up and R_{int} the internal pull-down, then the PRESN voltage level is:

$V_{PRESN} = V_{DD} \times R_{int} / (R_{int} + R_{ext})$

To be detected as high, V_{PRESN} must be greater than V_{IH}. Then the constraint on R_{ext} is:

$R_{ext} > R_{int} \times (V_{DD} - V_{IH}) / V_{IH}$

For instance, if V_{DD} = 3.3V, then VIH = 0.7*3.3V = 2.31V

As Rint min is 24kΩ, Rext max = 10.28 kΩ.

A maximum value of 10kΩ must be used in this case.

5.1.3 Debouncing

With some card connectors, depending on the mechanical characteristics of the switch, bouncing may be seen on the PRESN pin when a card is inserted or extracted. This bouncing is managed by the TDA8037 which does not transfer exactly the PRESN state to the OFFN pin.

When the card is inserted, the TDA8037 waits for the PRESN pin to be stable for several milliseconds before assuming that the card is inserted. When the card is extracted, the chip acts as soon as the presence is not active. This behavior is summarized in Fig 16:

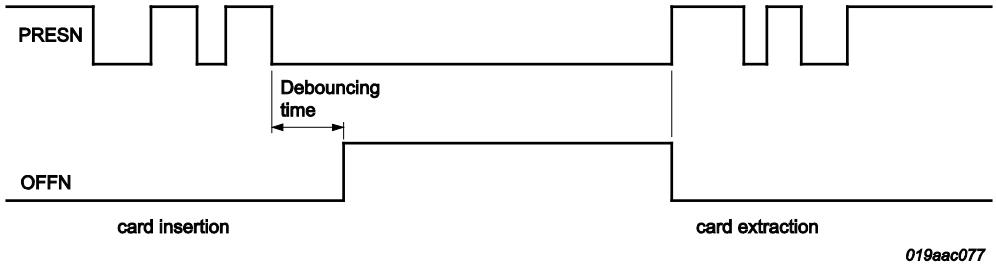


Fig 16. Debouncing feature

5.2 Schematics

To connect the smart card connector to the TDA8037, only two capacitors are mandatory as external components. The schematic reference is given in Fig 17.

The C1 capacitor must be placed near the TDA8037 and C2 must be connected close to the card connector.

The advised values for C1 and C2 are respectively 220 nF and 220 nF. These values are mandatory to have a ripple on VCC in the specified limits.

Pins C4 and C8 of the card connector (connected to pins AUX1 and AUX2) are optional. They can be left unconnected unless some specific operation using these pins is required.

Depending on the application, VPP (C6) can be connected directly to VCC or GND or not connected. Connecting it to VCC allows it to be compliant with older cards which might not support VPP connected to the Ground.

For more flexibility, the design should include a not connected serial resistor between VPP and VCC. Then the application can be easily adapted if needed.

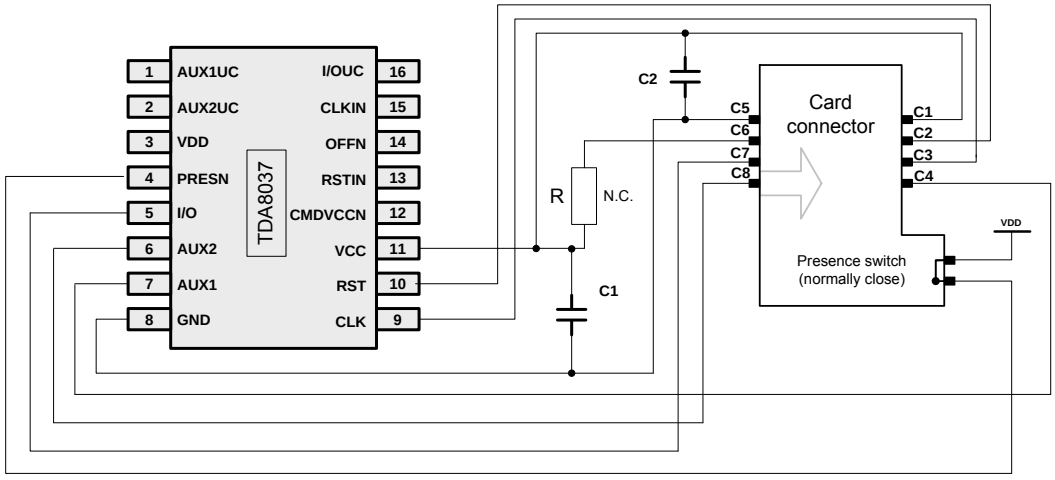


Fig 17. Card connector schematics

6. Card configuration

6.1 Card voltage

The TDA 8037 only handles class B cards. The only card voltage level handled is 3.3V

6.2 Card clock

6.2.1 Frequency selection

Only the TDA8037T can change the card clock. This clock can be selected by CLKDIV

This signal must be connected to the host and determine the division ratio of the input frequency in the clock which is sent to the card when activated.

The following table describes the frequency corresponding to CLKDIV value. f_{CLKIN} is the frequency of the signal applied to CLKIN.

Table 3. TDA8037 - Clock division selection

CLKDIV	CLK
0	f_{CLKIN}
1	$f_{CLKIN}/2$

6.2.2 Frequency switch

6.2.2.1 General behavior

CLKDIV can be changed freely when the card is not active. The value will be adopted on activation.

When the card is active, the frequency applied to the card can be switched by changing CLKDIV as shown in the following figure:

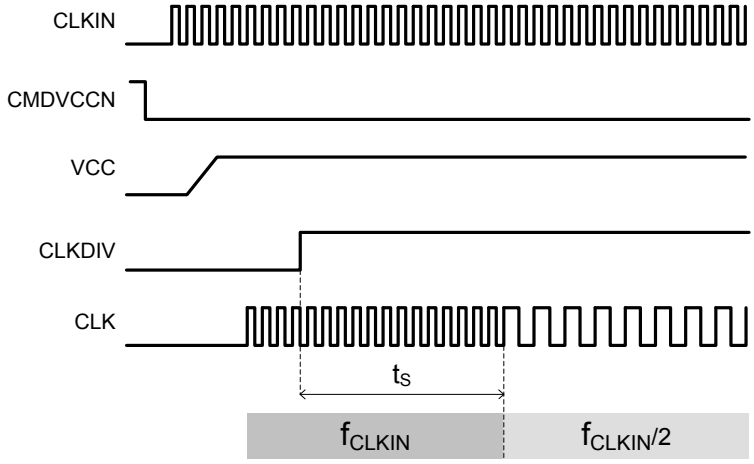


Fig 18. Clock switch during activation

The clock starts with the value specified at activation. Then the clock frequency switch occurs after a maximum of 4 CLKIN periods after a change is seen on CLKDIV ($t_s < t_{smax}$ = 4 clock cycles).

7. Card Activation / Deactivation

7.1 Differences TDA8024 – TDA8037T

7.1.1 Activation timing

The electrical interface between the host and the TDA is based on GPIOs and is exactly the same for TDA8037 as for TDA8024, as soon as the CS pin of the TDA8037 is High.

In the card management, the only difference between the TDA8024 and TDA8037 is the delay between CMDVCCN Low and VCC High.

This time is very low for the TDA8024 while it is at maximum 416 µs (with Clkin=10MHz) in the TDA8037. (See next chapter)

Important notice: Because the TDA8037T can only divide the frequency by 2 at maximum, be sure that the CLKIN frequency is still adapted to your application. Considering the ISO7816 norm specifies that the clock has to be between 1MHz and 5MHz at initialization, the CLKIN clock should be between 1MHz and 10MHz for TDA8037T.

7.1.2 Test Mode

Due to the test mode on TDA8037T it is mandatory for the host to keep the Test pin to ground.

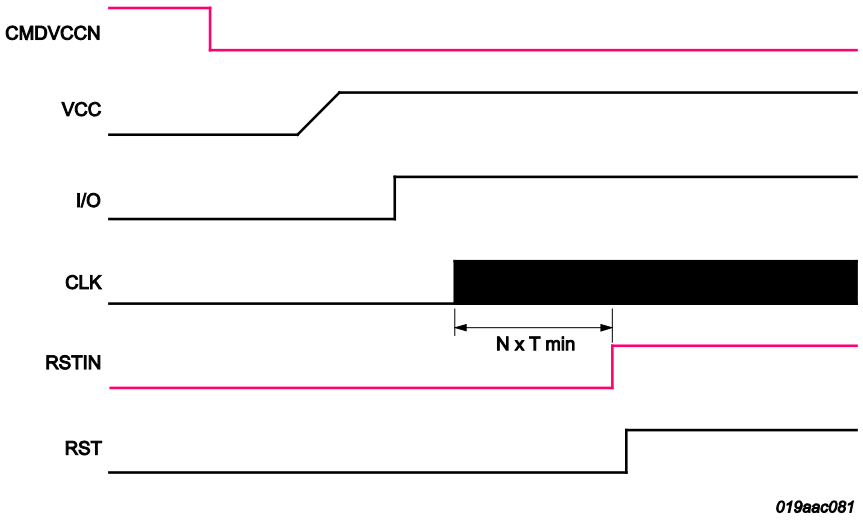
The TDA8024 does not use this test mode but the pin used for test mode on TDA8037T is the same used for PGND on the TDA8024T, so the pinning is compatible between the two.

7.2 Activation timings

To activate the card, two signals are controlled by the host: CMDVCCN and RSTIN.

The first signal sets the card power supply, the second controls the reset pin of the card.

In the simplest mode, two actions are required from the host to activate the card: reset CMDVCCN and then set RSTIN. The activation sequence is shown in Fig 19.



(1) N = 400 for ISO, 40000 for CISCO/EMV, T = Card clock period

Fig 19. Card activation sequence

The input clock must be OK for this sequence to occur. As the clock is supplied externally, the clock must be present and stable before the falling edge of CMDVCCN.

The only constraint on the host is due to the standard specifications:

For the ISO 7816, the host must wait at least 400 clock cycles after the clock is active, before asserting RST.

In CISCO and EMV specifications, the delay must be 40000 clock cycles

However in this mode, the host has no way of knowing when the clock starts. So it is not possible to count precisely the number of cycles.

To be sure that the right number of clock cycles are respected, the host must know the timing between CMDVCCN fall, VCC rise and CLK start.

These timings are given in the following figure

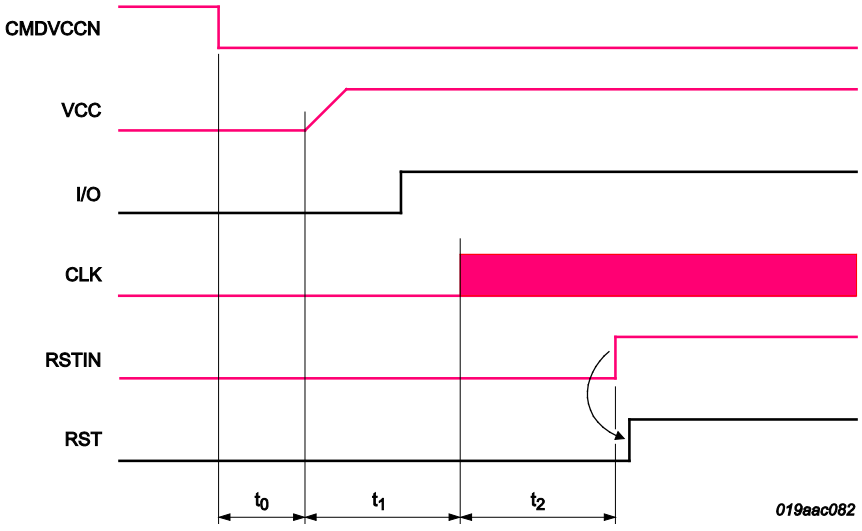


Fig 20. Activation timing

t_0 is the time between CMDVcc High and the start of the rise of Vcc. It lasts around 50 µs.

t_1 is the time between the beginning of the activation and the start of the clock on the smart card side. This time depends on the internal oscillator frequency and lasts at maximum 450 µs.

To set RSTIN, the host must wait at least 400 (ISO) or 40000 (CISCO/EMV) clock cycles after the start of CLK. Therefore t_2 depends on the input clock and on the division applied to supply the clock to the smart card and must be managed by the host.

7.3 Deactivation

The deactivation is managed entirely by the TDA8037 sequencer. Deactivation occurs when one of the following events happens:

- Rising edge of CMDVCCN (normal host deactivation)
- A fault is detected:
  - Card removal
  - Overheating
  - Short-circuit or high current on VCC
  - V_{DDhost}, V_{DD} or V_{REG} drop

The deactivation sequence is automatic and fully compliant with the standard. For more details on the activation or deactivation sequence and their timings, refer to the TDA8037 data sheet and ISO 7816-3 standard.

8. Card operation

8.1 I/O, Aux1, Aux2

The TDA8037 acts as a simple transceiver incorporating a voltage level shifting adaptation for these signals, once the card is activated.

As there is no other conversion, the host must manage entirely the protocol defined by ISO 7816 (Baudrate, timing, frame…).

The TDA8037 only limits the current on the pins. There is a limitation of 15 mA in both directions.

- I/O is linked to I/OUC,
- AUX1 to AUX1UC
- AUX2 to AUX2UC.

I/OUC must be connected directly to an I/O of the host. AUX1UC and AUX2UC can as well be connected to the host or left open if C4 and C8 pin are not used on the card.

8.2 Warm reset

The host can operate a warm reset with the TDA8037: as the RST card pin is the copy of the RSTIN pin, the host just needs to apply a falling edge on RSTIN, followed by a rising edge, and the card shall send its ATR again.

9. OFFN Behavior

9.1 Fault detection

The TDA8037 supervises several parameters and warns the host when a problem occurs. The OFFN pin is used to manage this communication with the host. The table below gives the state of the chip in accordance with CMDVCCN and OFFN values.

In this table it is assumed that CS pin is HIGH.

Table 4. Chip state regarding CMDVCCN and OFFN

CMDVCCN	OFFN	State	Comment
HIGH	HIGH	Card is present and not active	
HIGH	LOW	Card is absent	
LOW	HIGH	Card is active and no fault has been detected	This is the state of all card sessions
LOW	LOW	A fault has been detected (card has been deactivated)	The cause of the deactivation is not yet known.
Rising edge	Stays LOW	The fault detected was the card removal	Setting CMDVCCN allows checking if the deactivation is due to card removal. In this case the OFFN pin will stay low after CMDVCCN is high. If OFFN follows CMDVCCN, the fault is due to a supply voltage drop, a VCC over-current detection or overheating.
Rising edge	Rising edge	The fault detected was not a card removal (card is still present)	

10. Electrical design recommendations

10.1 Decoupling

To ensure proper behavior of the TDA8037, some external components have to be used. All supply pins must be protected against noise.

VCC pin (card contact) needs to be connected to two capacitors: twice 220 nF as described in chapter 5.2: one near the TDA8037 chip and one near the card connector. These capacitors type must be low ESR.

VDD must be protected by two capacitors: one 100nF to protect particularly against high frequency noise and one 10 µF to absorb slower variations.

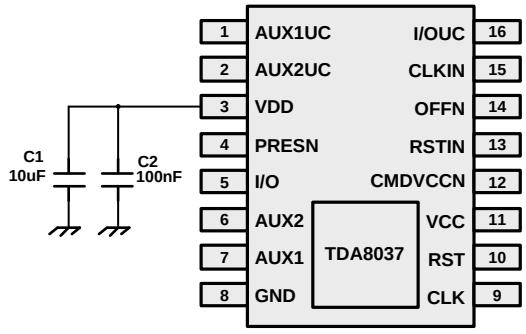


Fig 21. Power supply decoupling strategy

10.2 Layout

For noise reduction optimization, the layout of the design must adhere to the following guidelines.

10.2.1 Decoupling capacitors

Capacitors are mandatory to protect the supply pins as well as the VCC pin (TDA8037 pin and Card connector pin).

Place decoupling capacitors as close as possible to the pin that they protect.

This means that the capacitor must be physically soldered near the chip or the card connector pin, but also with a short and good connection (low resistance) between the protected pin and its capacitor.

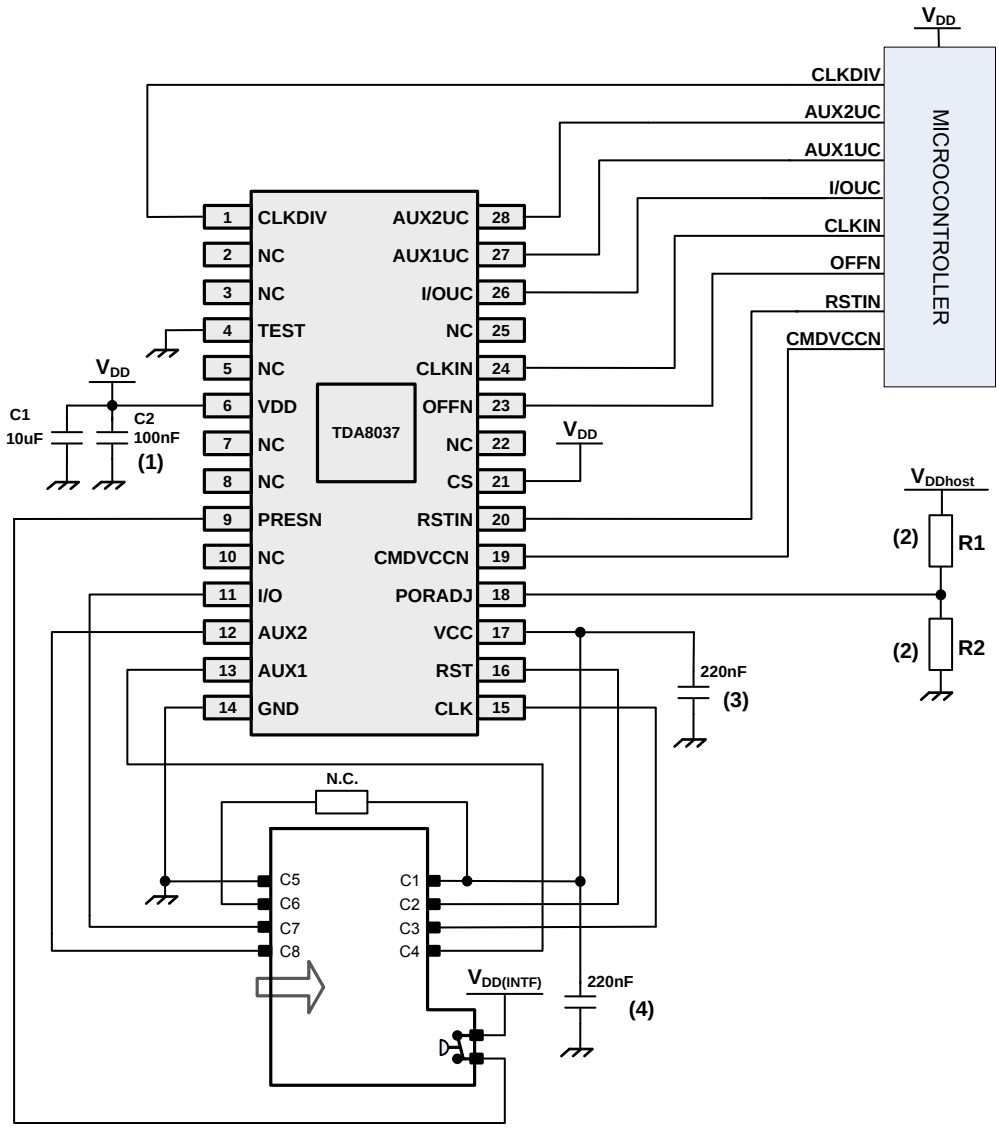
The connection between the capacitor pin and the ground must be short low resistive as well.

10.2.2 Clock wires

Clock (card) can cause crosstalk to other signals. It is advised to isolate these signals: make the connections as short as possible and keep them far from other signals.

The best is to shield these signals with ground when possible.

10.3 Summary



(1) Place close to the protected pin with good (low resistive) and straight connection to the main ground

(2) Optional resistor bridge. If this bridge is not required, connect PORAdj pin to V_{DDhost}

(3) Low ESR 220nF capacitor. Must be placed close to the chip's VCC pin

(4) Low ESR 220nF capacitor. Must be placed close to the C1 contact of the card connector

Fig 22. Reference design with TDA8037HN

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