DATA SHEET

TDA8787A
10-bit, 3.0 V, up to 18 Msps analog-to-digital interface for CCD cameras

Product specification
Supersedes data of 2000 Nov 14

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Philips
Semiconductors

PHILIPS

10-bit, 3.0 V, up to 18 Msps analog-to-digital interface for CCD cameras

TDA8787A

FEATURES

- Correlated Double Sampling (CDS), Programmable Gain Amplifier (PGA), 10-bit Analog-to-Digital Converter (ADC) and reference regulator included
- Fully programmable via a 3-wire serial interface
- Sampling frequency up to 18 MHz
- PGA gain range of 36 dB (in steps of 0.1 dB)
- Low power consumption of only 170 mW at 2.7 V
- Power consumption in standby mode of 4.5 mW (typical value)
- 3.0 V operation; 2.5 to 3.6 V operation for the digital outputs
- Active control pulses polarity selectable via serial interface
- 8-bit DAC included for analog settings
- TTL compatible inputs, CMOS compatible outputs.

APPLICATIONS

- Low-power, low-voltage CCD camera systems.

GENERAL DESCRIPTION

The TDA8787A is a 10-bit analog-to-digital interface for CCD cameras. The device includes a correlated double sampling circuit, a PGA, clamp loops and a low-power 10-bit ADC, together with its reference voltage regulator.

The PGA gain and the ADC input clamp level are controlled via the serial interface.

An additional DAC is provided for additional system controls. Its output voltage range is 1.0 V peak-to-peak which is available at pin OFDOUT.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8787AHL	LQFP48	plastic low profile quad flat package; 48 leads; body $7 \times 7 \times 1.4$ mm	SOT313-2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs stages supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active; f_{pix} = 18 MHz	–	50	60	mA
I_{CCD}	digital supply current	f_{pix} = 18 MHz	–	13	17	mA
I_{CCO}	digital outputs supply current	f_{pix} = 18 MHz; C_L = 20 pF; input ramp response time is 800 μs	–	1	2	mA
ADC_{res}	ADC resolution		–	10	–	bits
$V_{i(CDS)(p-p)}$	CDS input amplitude (video signal) (peak-to-peak value)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$f_{pix(max)}$	maximum pixel frequency		18	–	–	MHz
$f_{pix(min)}$	minimum pixel frequency		2	–	–	MHz
DR_{PGA}	PGA dynamic range		–	36	–	dB
$N_{tot(rms)}$	total noise (RMS value) at CDS input to ADC output	PGA code = 0; see Fig.8	–	0.15	–	LSB
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	PGA code = 383	–	70	–	μV
P_{tot}	total power consumption	$V_{CCA} = V_{CCD} = V_{CCO}$ = 3 V	–	190	–	mW
		$V_{CCA} = V_{CCD} = V_{CCO}$ = 2.7 V	–	170	–	mW

BLOCK DIAGRAM

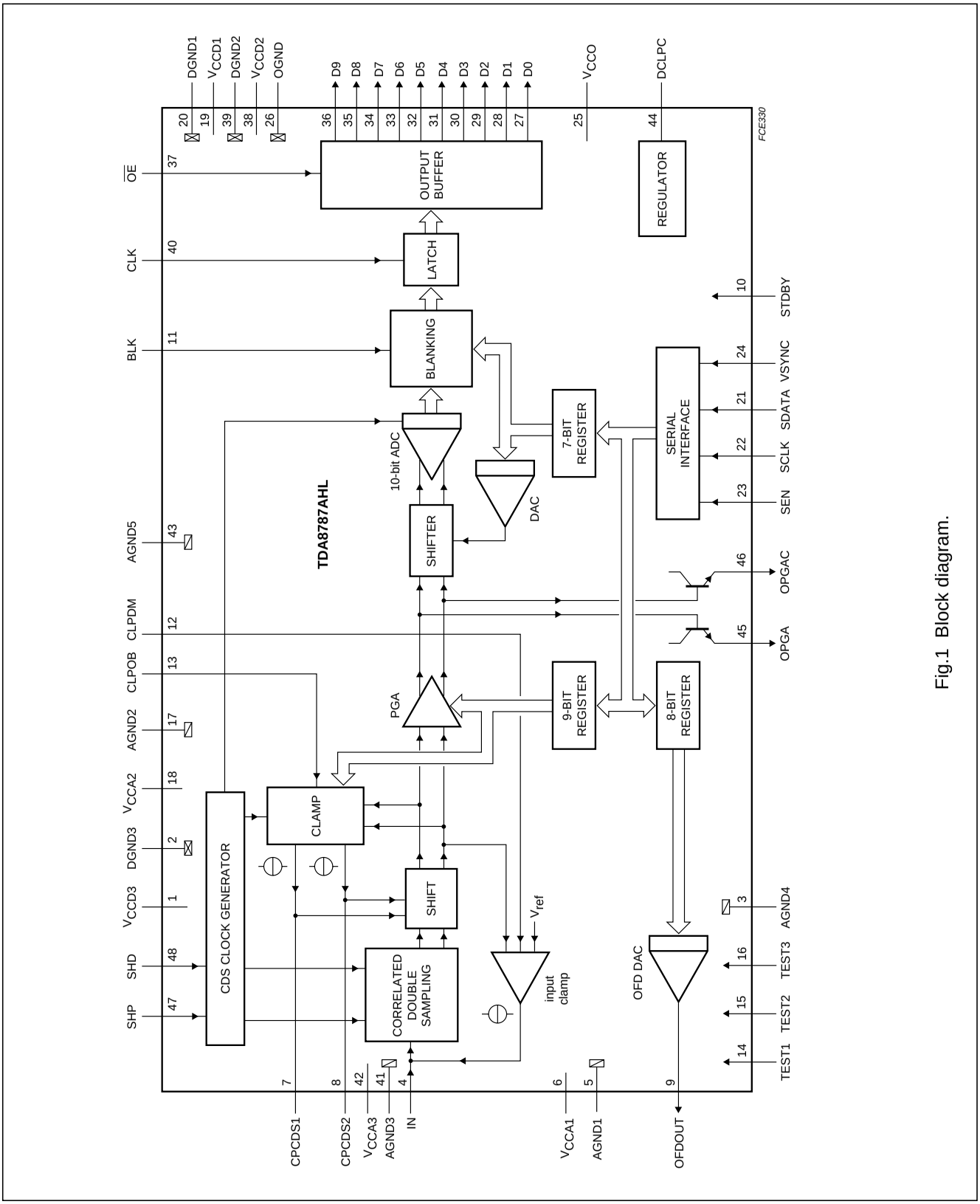


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCD3}	1	digital supply voltage 3
DGND3	2	digital ground 3
AGND4	3	analog ground 4
IN	4	input signal from CCD
AGND1	5	analog ground 1
V_{CCA1}	6	analog supply voltage 1
CPCDS1	7	clamp storage capacitor 1
CPCDS2	8	clamp storage capacitor 2
OFDOUT	9	analog output of the additional 8-bit control DAC
STDBY	10	standby mode control input (LOW: TDA8787A active; HIGH: TDA8787A standby)
BLK	11	blanking control input
CLPDM	12	clamp pulse input at dummy pixel (should be connected to ground)
CLPOB	13	clamp pulse input for optical black
TEST1	14	test pin input 1 (should be connected to AGND2)
TEST2	15	test pin input 2 (should be connected to AGND2)
TEST3	16	test pin input 3 (should be connected to AGND2)
AGND2	17	analog ground 2
V_{CCA2}	18	analog supply voltage 2
V_{CCD1}	19	digital supply voltage 1
DGND1	20	digital ground 1
SDATA	21	serial data input for serial interface control
SCLK	22	serial clock input for serial interface control
SEN	23	strobe pin for serial interface control
VSYNC	24	vertical sync pulse input
V_{CCO}	25	output stages supply voltage
OGND	26	digital output ground
D0	27	ADC digital output 0 (LSB)
D1	28	ADC digital output 1
D2	29	ADC digital output 2
D3	30	ADC digital output 3
D4	31	ADC digital output 4
D5	32	ADC digital output 5
D6	33	ADC digital output 6
D7	34	ADC digital output 7
D8	35	ADC digital output 8
D9	36	ADC digital output 9 (MSB)
$\overline{OE}$	37	output enable control input (LOW: outputs active; HIGH: outputs in high impedance)
V_{CCD2}	38	digital supply 2
DGND2	39	digital ground 2
CLK	40	data clock input

SYMBOL	PIN	DESCRIPTION
AGND3	41	analog ground 3
V_{CCA3}	42	analog supply 3
AGND5	43	analog ground 5
DCLPC	44	regulator decoupling pin
OPGA	45	PGA output (test pin)
OPGAC	46	PGA complementary output (test pin)
SHP	47	preset sample-and-hold pulse input
SHD	48	data sample-and-hold pulse input

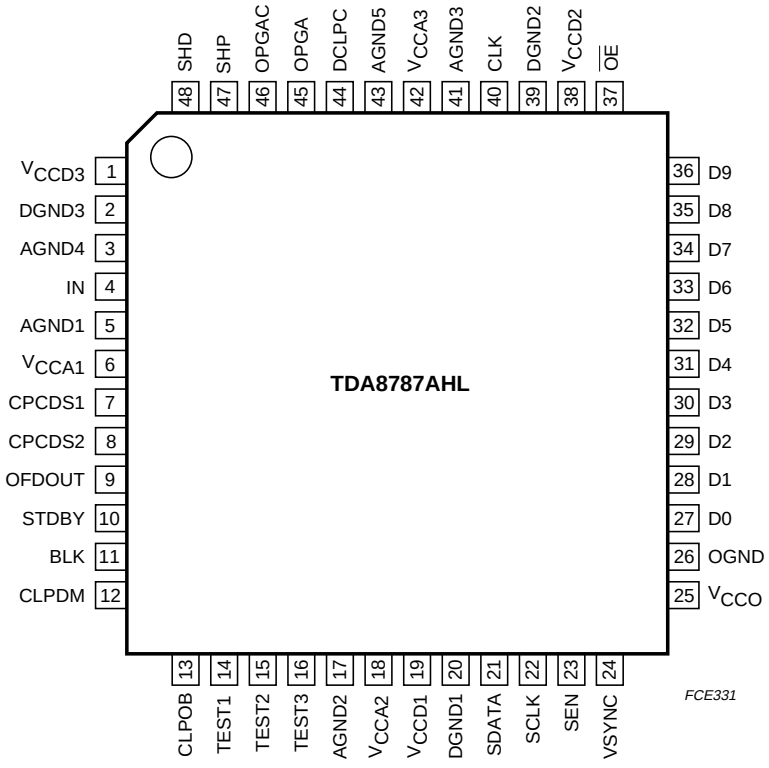


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	–0.3	+5.0	V
V_{CCD}	digital supply voltage	note 1	–0.3	+5.0	V
V_{CCO}	output stages supply voltage	note 1	–0.3	+5.0	V
ΔV_{CC}	supply voltage difference				
	between V_{CCA} and V_{CCD}		–0.5	+0.5	V
	between V_{CCA} and V_{CCO}		–0.5	+1.2	V
	between V_{CCD} and V_{CCO}		–0.5	+1.2	V
V_i	input voltage	referenced to AGND	–0.3	+5.0	V
I_o	data output current		–	±10	mA
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature		–	150	°C

Note

1. The supply voltages V_{CCA}, V_{CCD} and V_{CCO} may have any value between –0.3 and +5.0 V provided that the supply voltage difference ΔV_{CC} remains as indicated.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	76	K/W

CHARACTERISTICS

V_{CCA} = V_{CCD} = 3.0 V; V_{CCO} = 2.6 V; f_{pix} = 18 MHz; T_{amb} = –20 to +75°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		2.7	3.0	3.6	V
V_{CCD}	digital supply voltage		2.7	3.0	3.6	V
V_{CCO}	digital outputs stages supply voltage		2.5	2.6	3.6	V
I_{CCA}	analog supply current	all clamps active	–	50	60	mA
I_{CCD}	digital supply current		–	13	17	mA
I_{CCO}	digital outputs supply current	C_L = 20 pF on all data outputs; input ramp response time is 800 µs	–	1	2	mA
P_{tot}	total power consumption	V_{CCA} = V_{CCD} = V_{CCO} = 3 V	–	190	–	mW
		V_{CCA} = V_{CCD} = V_{CCO} = 2.7 V	–	170	–	mW
Digital inputs						
INPUTS: PINS STDBY, CLPDM, CLPOB, SCLK, SDATA, SEN, VSYNC, $\overline{OE}$, CLK AND BLK						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	5.0	V
I_i	input current	$0 \leq V_i \leq V_{CCD}$	–2	–	+2	µA
INPUTS: PINS SHP AND SHD						
V_{IL}	LOW-level input voltage		0	–	0.6	V
V_{IH}	HIGH-level input voltage		2.2	–	5.0	V
I_i	input current	$0 \leq V_i \leq V_{CCD}$	–10	–	+10	µA
Clamps						
GLOBAL CHARACTERISTICS OF THE CLAMP LOOPS						
$t_{W(clamp)}$	clamp active pulse width in numbers of pixels	PGA input code = 255 for maximum 4 LSB error	12	–	–	pixels
INPUT CLAMP: PIN CLPDM						
$g_{m(CDS)}$	CDS input clamp transconductance		1.5	2.7	3.5	mS
OPTICAL BLACK CLAMP: PIN CLPOB						
G_{shift}	gain from CPCDS1 and 2 to PGA inputs		–	0.27	–	
$I_{LSB(cp)}$	charge pump current for ±1 LSB error at ADC output	PGA input code = 0	–	±20	–	µA
		PGA input code = 383	–	±0.60	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Correlated Double Sampling (CDS): pin IN						
$V_{i(CDS)(p-p)}$	CDS input amplitude (video signal) (peak-to-peak value)	V_{CC} = 2.85 V	650	–	–	mV
		$V_{CC} \geq$ 3.0 V	800	–	–	mV
$V_{i(rst)(max)}$	maximum CDS input reset pulse amplitude		500	–	–	mV
I_i	input current	at floating gate level	–1	–	+1	µA
C_i	input capacitance		–	2	–	pF
$t_{CDS(min)}$	CDS control pulses minimum active time	$V_{i(CDS)(p-p)}$ = 800 mV; black-to-white transition in 1 pixel (±2 LSB typical); T_{amb} = 25 °C; note 1	11	15	–	ns
$t_{h(IN-SHP)}$	hold time SHP to IN	T_{amb} = 25 °C; see Figs 3 and 4	–	1	2	ns
$t_{h(IN-SHD)}$	hold time SHD to IN	T_{amb} = 25 °C; see Figs 3 and 4	–	1	2	ns
Amplifier						
DR_{PGA}	PGA dynamic range		–	36	–	dB
ΔG_{PGA}	PGA gain step		–0.3	–	+0.3	dB
Analog-to-Digital Converter (ADC)						
$LE_{(i)}$	integral non-linearity error	f_{pix} = 18 MHz; ramp input	–	±1.3	±2.5	LSB
$LE_{(d)}$	differential non-linearity error	f_{pix} = 18 MHz; ramp input	–	±0.5	±0.9	LSB
Total chain characteristics (CDS, PGA and ADC)						
$f_{pix(max)}$	maximum pixel frequency		18	–	–	MHz
$f_{pix(min)}$	minimum pixel frequency		2	–	–	MHz
t_{CLKH}	clock HIGH time		15	–	–	ns
t_{CLKL}	clock LOW time		15	–	–	ns
$t_{d(SHD-CLK)}$	time delay SHD to CLK	see Fig.3	10	–	–	ns
$t_{su(BLK-CLK)}$	set-up time of BLK compared to CLK		10	–	–	ns
$V_{i(IN)}$	video input dynamic signal for ADC full-scale output	PGA input code = 0	800	–	–	mV
		PGA input code = 383	12.7	–	–	mV
$N_{tot(rms)}$	total noise from CDS input to ADC output (RMS value)	see Fig.8				
		PGA input code = 0	–	0.15	–	LSB
		PGA input code = 96	–	0.8	–	LSB
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	PGA input code = 383	–	70	–	µV
		PGA input code = 0	–	120	–	µV
$O_{CCD(max)}$	maximum offset between CCD floating level and CCD dark pixel level		–80	–	+80	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital-to-Analog Converter (OFDOUT DAC)						
$V_{OFDOUT(p-p)}$	additional 8-bit control DAC (OFD) output voltage (peak-to-peak value)	R_L = 1 MΩ	–	1.0	–	V
V_{OFDOUT}	DC output voltage	OFD input code 0	–	AGND	–	V
		OFD input code 255	–	AGND + 1.0	–	V
TC_{OFD}	OFD output range temperature coefficient		–	250	–	ppm/K
Z_{OFDOUT}	OFD output impedance		–	2000	–	Ω
I_{OFDOUT}	OFD output drive current	static	–	–	100	µA
Digital outputs (f_{pix} = 18 MHz; C_L = 10 pF); see Figs 3 and 4						
V_{OH}	HIGH-level output voltage	I_{OH} = –1 mA	V_{CCO} – 0.5	–	V_{CCO}	V
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	0	–	0.5	V
I_{OZ}	OFF-state output current	0.5 V < V_{OZ} < V_{CCO}	–20	–	+20	µA
$t_{h(o)}$	output hold time		9	–	–	ns
$t_{d(o)}$	output delay time	V_{CCO} = 3.0 V	–	17	23	ns
		V_{CCO} = 2.7 V	–	19	25	ns
C_L	load capacitance		–	–	22	pF
Serial interface						
$f_{SCLK(max)}$	maximum frequency pin SCLK		5	–	–	MHz

Note

1. Depending on application environments and especially in case of high gain operation and digital supply with jitter, it is preferable to apply 12 ns or higher CDS pulses.

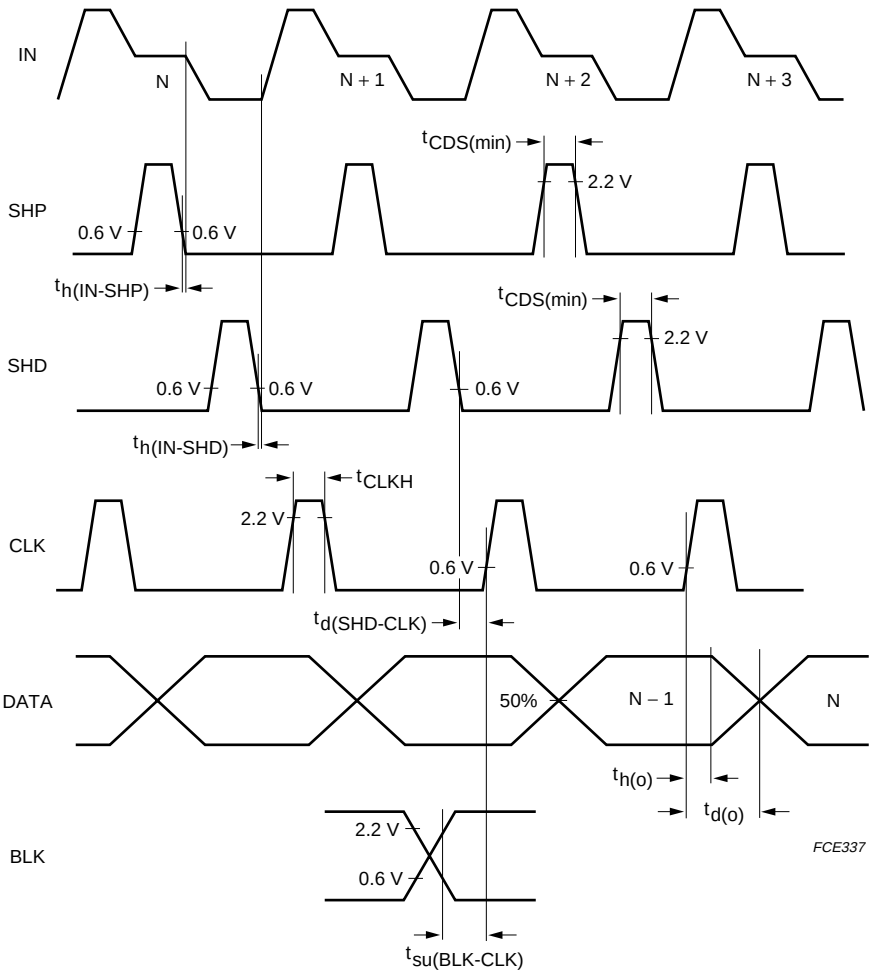


Fig.3 Pixel frequency timing diagram with active HIGH-level polarities.

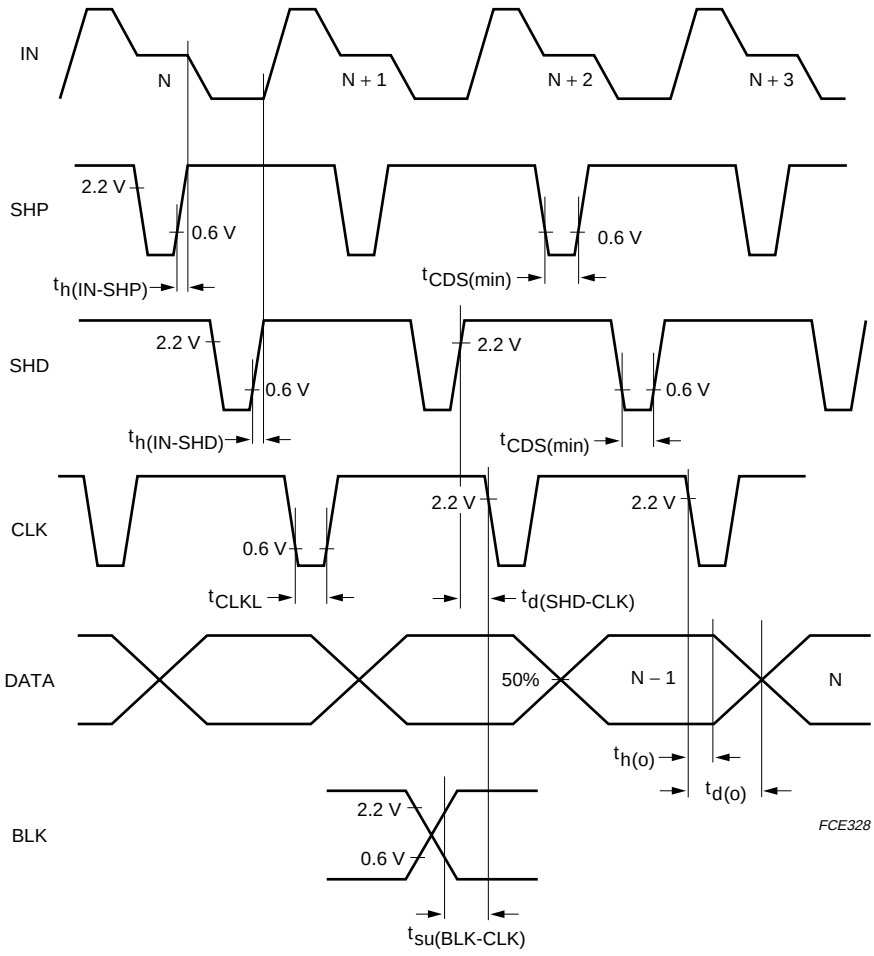


Fig.4 Pixel frequency timing diagram with active LOW-level polarities.

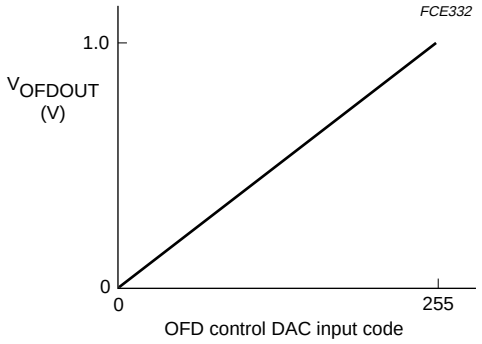
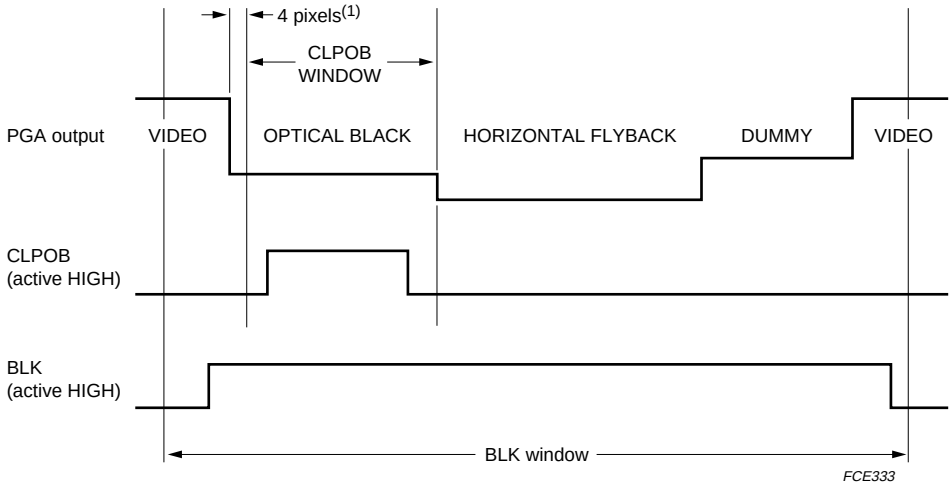
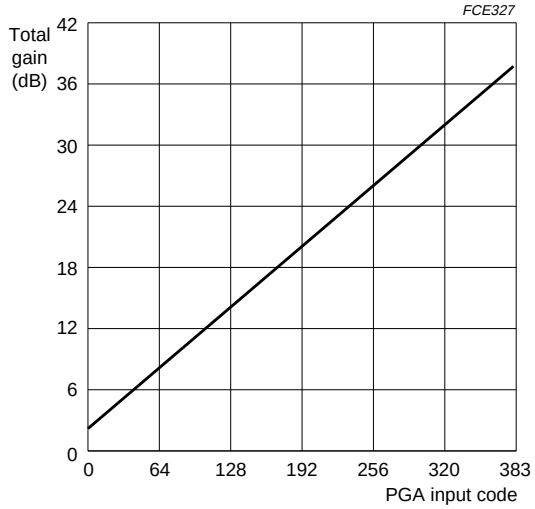


Fig.5 DAC output voltage output as a function of DAC input code.



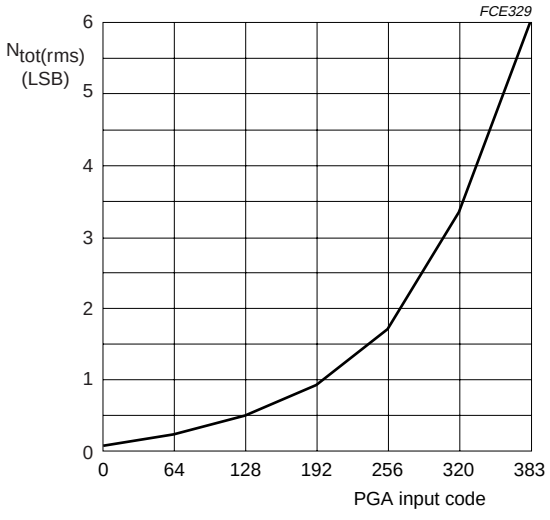
(1) In this case the number of clamp pixels is limited to $18 \times (t_{W(clamp)})$; otherwise this timing interval can be

Fig.6 Line frequency timing diagram.



ADC input range is 1 V_{pp}.

Fig.7 Total gain as a function of PGA input code.



Noise measurement at ADC outputs; coupling capacitor at input is grounded, so only noise contribution of the front-end is evaluated. Front-end works at 18 Mpixels with line of 1024 pixels whose first 40 are used to run CLPOB and the last 40 for CLPDM. Data at the ADC outputs are measured during the other pixels. As a result of this, the standard deviation of the codes statistic is computed, resulting in the noise.

Fig.8 Typical total noise performance as a function of PGA gain.

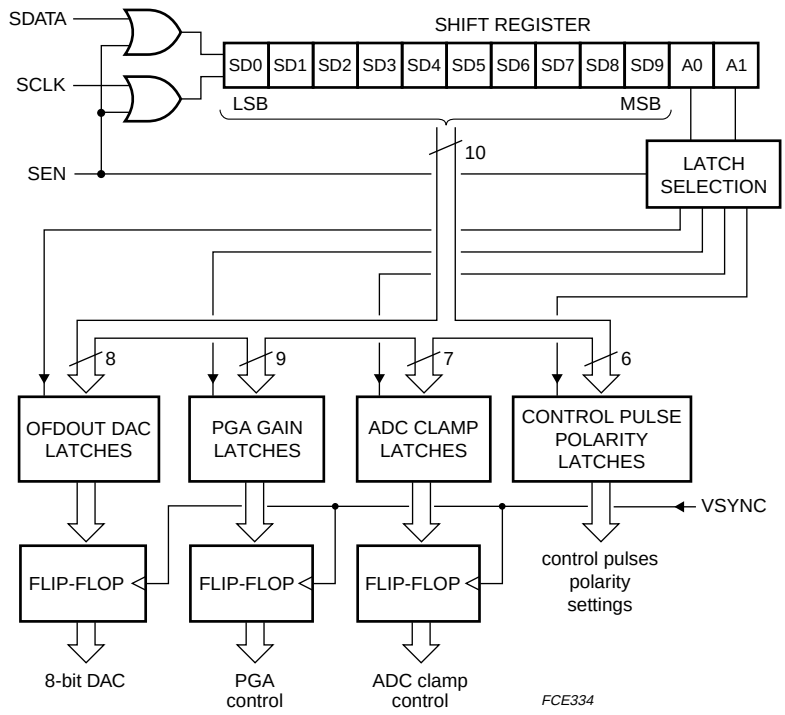
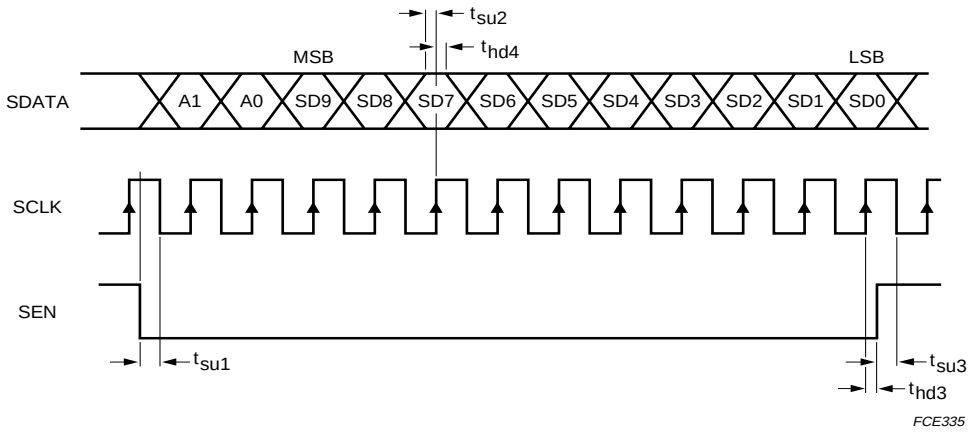


Fig.9 Serial interface block diagram.



$t_{su1} = t_{su2} = t_{su3} = 10$ ns (minimum); $t_{hd3} = t_{hd4} = 10$ ns (minimum).

Fig.10 Loading sequence of control input data via the serial interface.

Table 1 Serial interface programming; see Figs 9 and 10

ADDRESS BITS		DATA BITS SD9 TO SD0
A1	**A0**	
0	0	PGA gain control (bits SD8 to SD0); bit SD9 should be set to logic 0
0	1	DAC OFDOUT output control (bits SD7 to SD0); bits SD8 and SD9 should be set to logic 0
1	0	ADC clamp reference control (SD6 to SD0); from code 0 to 127; bits SD7, SD8 and SD9 should be set to logic 0
1	1	control pulses polarity settings (pins SHP, SHD, CLPDM, CLPOB, BLK and CLK)

Table 2 Polarity settings

SYMBOL	PIN	SERIAL CONTROL BIT[1]	ACTIVE EDGE OR LEVEL
SHP and SHD	47 and 48	SD0	1 = HIGH; 0 = LOW
CLK	40	SD1	1 = HIGH; 0 = LOW
CLPDM	12 (connected to ground)	SD2	always 0 = LOW
CLPOB	13	SD3	1 = HIGH; 0 = LOW
BLK	11	SD5	1 = HIGH; 0 = LOW
VSYNC	24	SD6	0 = rising; 1 = falling

Note

1. Bit SD4 is not used.

Table 3 Standby mode selection; pin STDBY

STDBY	ADC DIGITAL OUTPUTS; PINS D9 TO D0	$I_{CCA} + I_{CCO} + I_{CCD}$ (typical)
1	logic state LOW	1.5 mA
0	active	64 mA

Table 4 Output enable ($\overline{OE}$) pin 37

$\overline{OE}$	ADC DIGITAL OUTPUTS; PINS D9 TO D0
0	active, binary
1	high impedance

APPLICATION INFORMATION

Power and grounding recommendations

When designing a printed-circuit board for applications such as PC cameras, surveillance cameras, camcorders and digital still cameras, care should be taken to minimize the noise.

For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as additional operational amplifiers) must be respected, particularly with respect to power and ground connections.

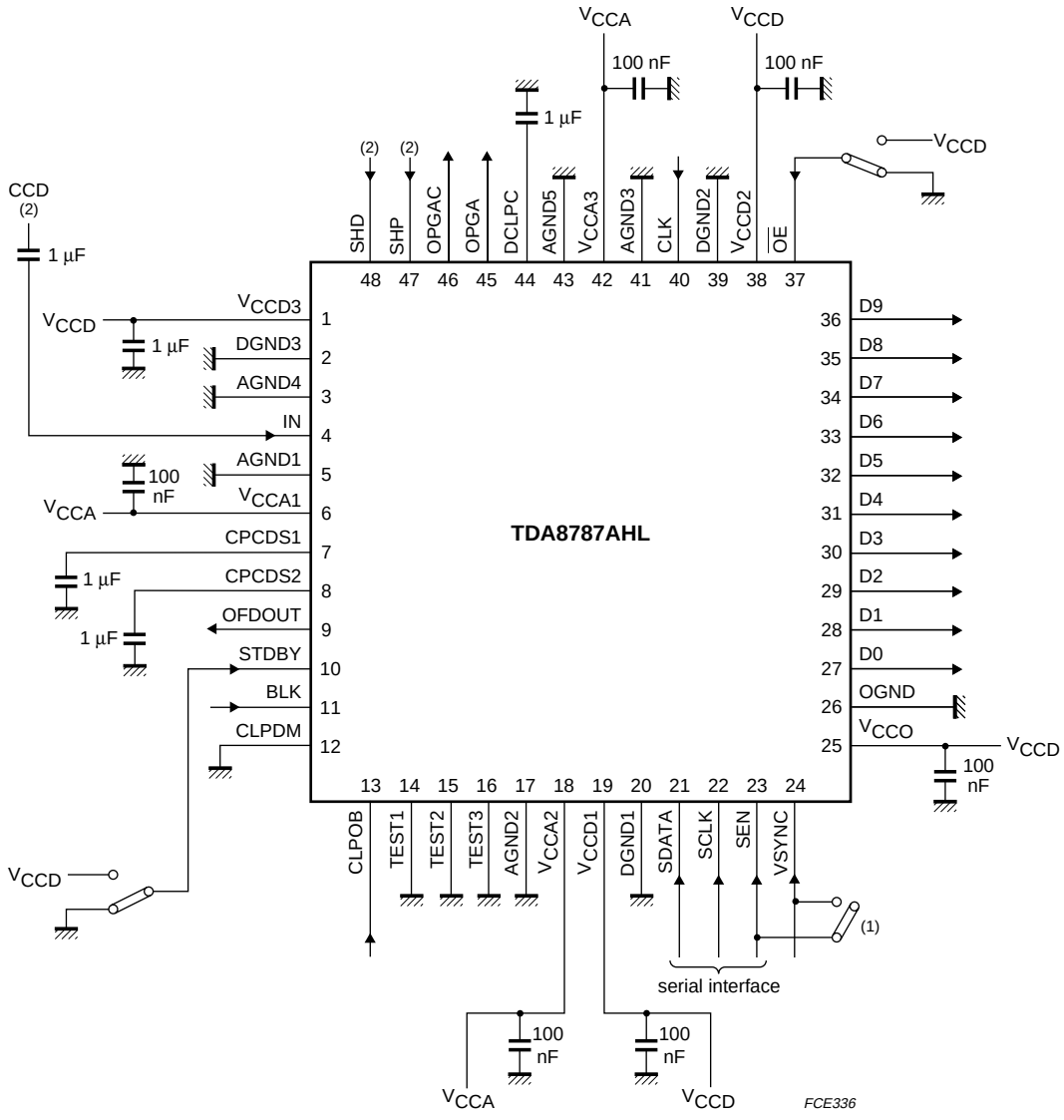
The following additional recommendation is given for the CDS input pin(s) which is /are internally connected to the programmable gain amplifier.

The connections between the CCD interface and CDS input should be as short as possible and a ground ring protection around these connections can be beneficial. Separate analog and digital supplies provide the best solution. If this is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins. If the same power supply and ground are used for all the pins then the decoupling capacitors must be placed as close as possible to the IC package.

In order to minimize the noise due to package and die parasitics in a two-ground system, the following measures must be implemented:

- All the analog and digital supply pins must be decoupled to the analog ground plane. Only the ground pin associated with the digital outputs must be connected to the digital ground plane. All the other ground pins should be connected to the analog ground plane. The analog and digital ground planes must be connected together at one point as close as possible to the ground pin associated with the digital outputs.
- The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as a return path for digital signals.

Application diagram



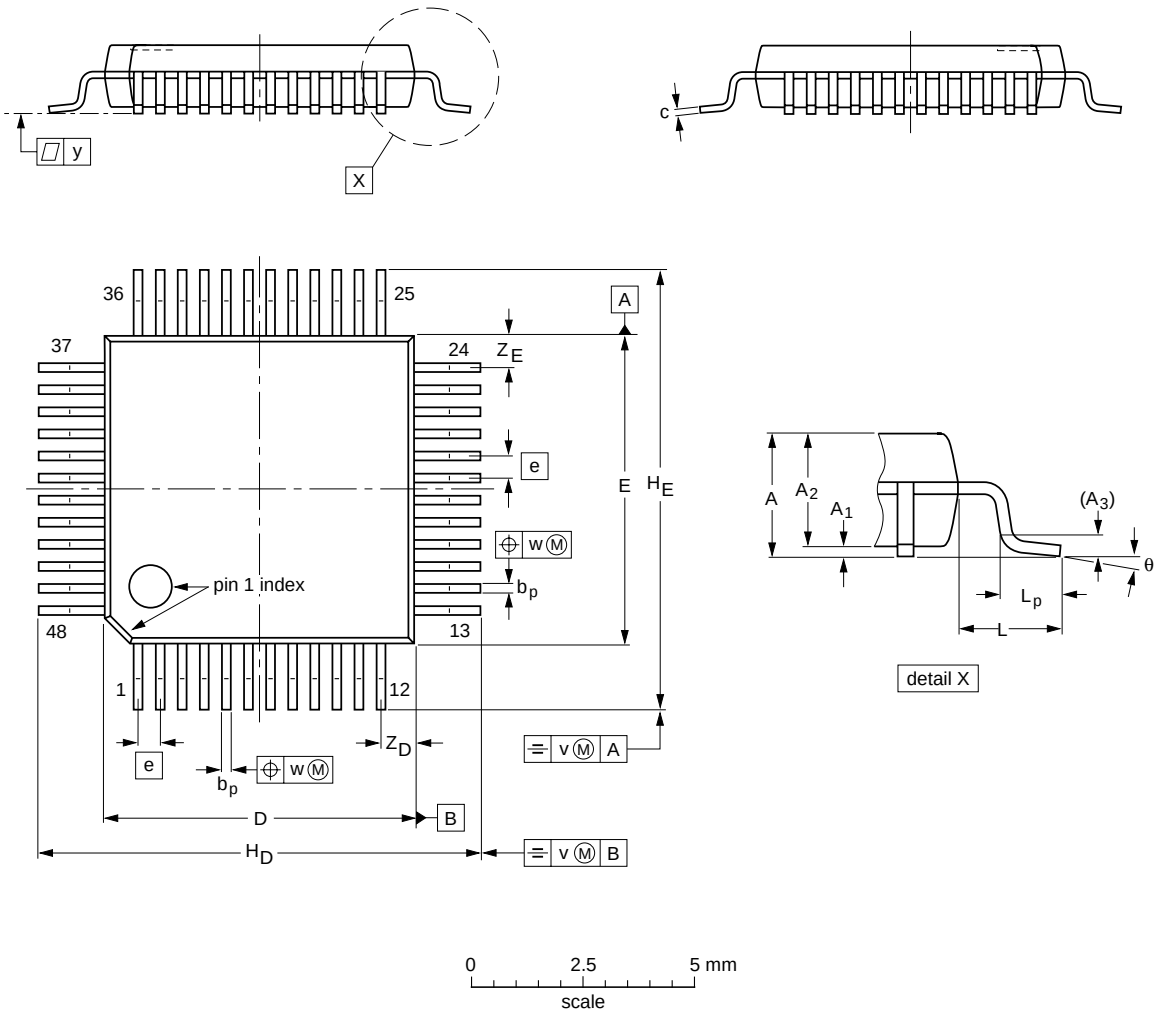
(1) Pins SEN and VSYNC should be interconnected when no vertical synchronization signal is available, while control pin VSYNC should be programmed by serial interface as LOW-level active.

(2) The timing of the signals on pins IN, SHD and SHP has to comply with the hold times $t_{h(IN-SHP)}$ and $t_{h(IN-SHD)}$ (see Fig.3).

Fig.11 Application diagram.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
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