CS8120

5.0 V, 300 mA Linear Regulator with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$

The CS8120 is a 5.0 V, 300 mA precision linear regulator with two microprocessor compatible control functions and protection circuitry included on chip. The composite NPN–PNP output pass transistor assures a lower dropout voltage (1.0 V @ 200 mA) without requiring excessive supply current (2.5 mA).

The CS8120's two logic control functions make this regulator well suited to applications requiring microprocessor–based control at the board or module level. $\overline{\text{ENABLE}}$ controls the output stage. A high voltage (> 2.9 V) on the $\overline{\text{ENABLE}}$ lead turns off the regulator's pass transistor and sends the IC into Sleep mode where it draws only 250 μA. The $\overline{\text{RESET}}$ function sends a $\overline{\text{RESET}}$ signal when the IC is powering up or whenever the output voltage moves out of regulation. The $\overline{\text{RESET}}$ signal is valid down to V_{OUT} = 1.0 V.

The CS8120 design optimizes supply rejection by switching the internal bandgap reference from the supply input to the regulator output as soon as the nominal output voltage is achieved. Additional on chip filtering enhances rejection of high frequency transients on all external leads.

The CS8120 is fault protected against short circuit, over voltage and thermal runaway conditions.

Features

- 5.0 V ±4.0% Output Voltage 300 mA
- Low Dropout Voltage (1.0 V @ 150 mA)
- Low Quiescent Current (2.5 mA @ I_{OUT} = 150 mA)
- μP Compatible Control Functions
  - $\overline{\text{RESET}}$
  - $\overline{\text{ENABLE}}$
- Low Current Sleep Mode
  - I_Q = 250 μA
- Fault Protection
  - Thermal Shutdown
  - Short Circuit
  - 60 V Load Dump

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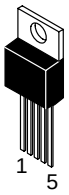
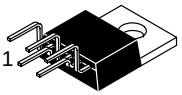
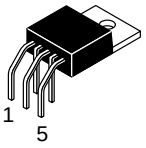


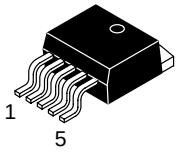
TO–220
FIVE LEAD
T SUFFIX
CASE 314D



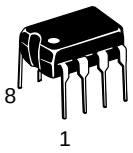
TO–220
FIVE LEAD
TVA SUFFIX
CASE 314K



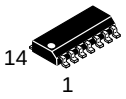
TO–220
FIVE LEAD
THA SUFFIX
CASE 314A



D²PAK
5–PIN
DP SUFFIX
CASE 936F



DIP–8
N SUFFIX
CASE 626



SO–14
D SUFFIX
CASE 751A

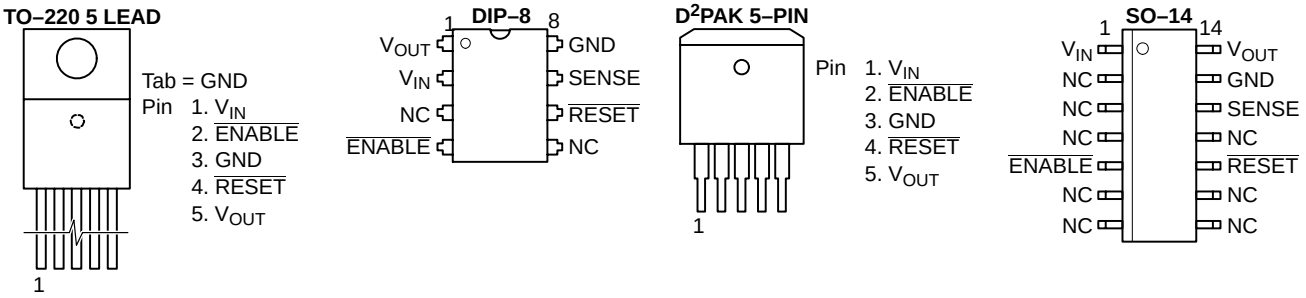
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 10 of this data sheet.

PIN CONNECTIONS



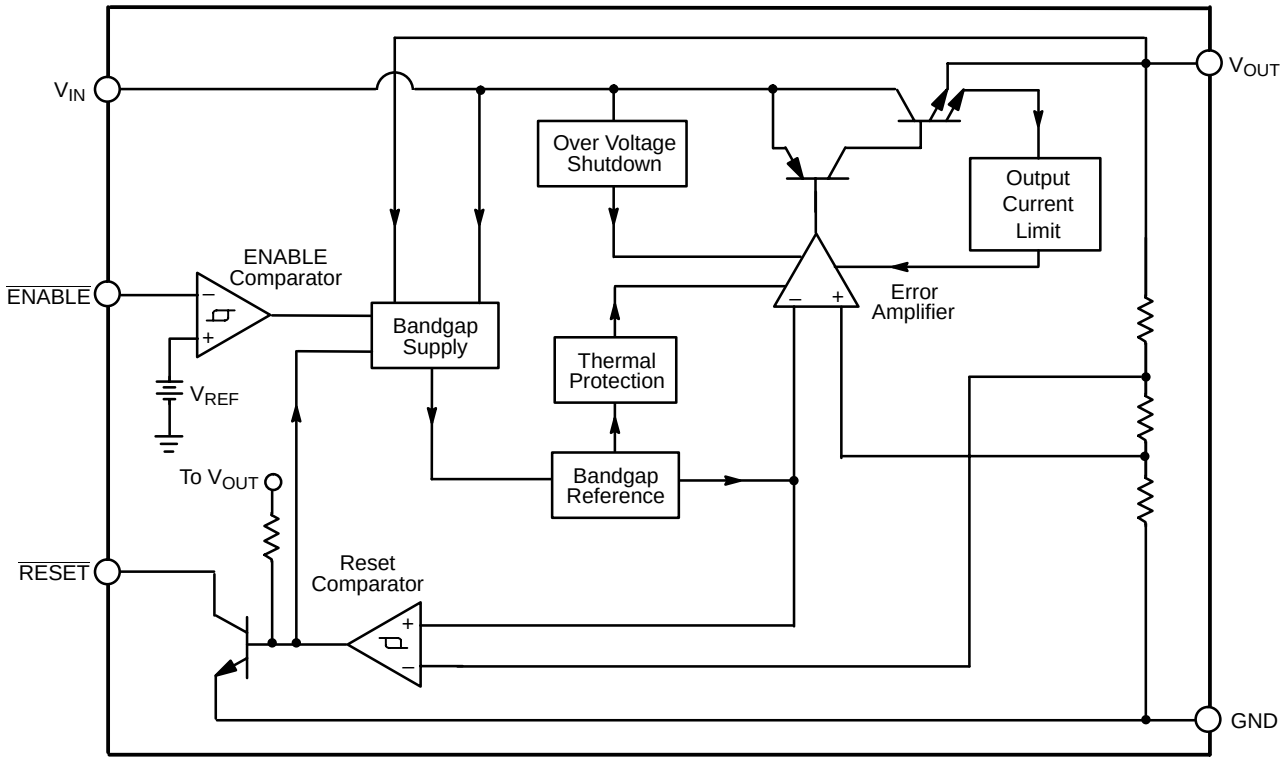


Figure 1. Block Diagram – TO–220

ABSOLUTE MAXIMUM RATINGS*

Rating		Value	Unit
DC Input Voltage		–0.7 to 26	V
Load Dump		60	V
Output Current		Internally Limited	–
Electrostatic Discharge (Human Body Model)		2.0	kV
Operating Temperature		–40 to +125	°C
Junction Temperature		–40 to +150	°C
Storage Temperature Range		–55 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1.) Reflow (SMD styles only) (Note 2.)	260 peak 230 peak	°C °C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V, I_{OUT} = 5.0 mA; –40 ≤ T_J ≤ 150°C, –40°C ≤ T_C ≤ 125°C, unless otherwise noted.) Note 3.

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage, V_{OUT}	7.0 V ≤ V_{IN} ≤ 26 V, 1.0 mA ≤ I_{OUT} ≤ 300 mA	4.8	5.0	5.2	V
Line Regulation	7.0 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 200 mA	–	–	50	mV
Load Regulation	1.0 mA ≤ I_{OUT} ≤ 300 mA	–	–	50	mV
Supply Voltage Rejection	V_{IN} = 14 V_{DC} + 1.0 V_{RMS} @ 120Hz $_{LOAD}$ = 25 Ω	40	70	–	dB
Dropout Voltage	I_{OUT} = 200 mA	–	1.0	1.5	V
Quiescent Current	$\overline{ENABLE}$ = High, V_{IN} = 12 V $\overline{ENABLE}$ = Low, I_{OUT} = 200 mA	– –	0.25 2.5	0.65 15	mA mA
Protection Circuits					
Short Circuit Current	–	300	600	–	mA
Thermal Shutdown	–	150	190	–	°C
Overvoltage Shutdown	–	26	40	–	V
$\overline{RESET}$					
$\overline{RESET}$ Saturation Voltage	1.0 V < V_{OUT} < $V_{RT(OFF)}$, 3.1 kΩ Pull–Up to V_{OUT}	–	0.1	0.4	V
$\overline{RESET}$ Output Leakage Current	$\overline{ENABLE}$ = Low, V_{OUT} > $V_{RT(ON)}$, $V_{\overline{RESET}}$ = V_{OUT}	–	0	25	μA
Power ON/OFF $\overline{RESET}$ Peak Output Voltage	3.1 kΩ Pull–Up to V_{OUT}	–	0.7	1.0	V
$\overline{RESET}$ Threshold HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 – 4.75	 V_{OUT} – 0.10 V_{OUT} – 0.14	 V_{OUT} – 0.04 –	 V V
$\overline{RESET}$ Threshold Hysteresis	–	10	40	–	mV
$\overline{ENABLE}$					
Input High Voltage	7.0 V < V_{IN} < 26 V	–	2.9	3.9	V
Input Low Voltage	7.0 V < V_{IN} < 26 V	1.1	2.1	–	V
Input Hysteresis	7.0 V < V_{IN} < 26 V	0.4	0.8	2.8	V
Input Current	GND < $V_{IN(HI)}$ < V_{OUT}	–10	0	+10	μA

3. To have safe operating junction temperatures, low duty cycle pulse testing is used on tests where applicable.

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #				LEAD SYMBOL	FUNCTION
TO–220 5 LEAD–	DIP–8	SO–14	D^2Pak 5 PIN		
1	2	1	1	V_{IN}	Supply voltage to IC, usually direct from the battery.
2	4	5	2	$\overline{\text{ENABLE}}$	CMOS compatible logical input. V_{OUT} is disabled i.e. placed in a high impedance state when $\overline{\text{ENABLE}}$ is high.
3	8	13	3	GND	Ground Connection.
4	6	10	4	$\overline{\text{RESET}}$	CMOS compatible output lead. $\overline{\text{RESET}}$ goes low whenever V_{OUT} falls out of regulation. The $\overline{\text{RESET}}$ delay is externally programmed.
5	1	14	5	V_{OUT}	Regulated output voltage, 5.0 V (typ).
N/A	7	12	–	SENSE	Kelvin Connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not desired, connect to V_{OUT}.
–	3, 5	2, 3, 4, 6, 7, 8, 9, 11		NC	No Connection.

TYPICAL PERFORMANCE CHARACTERISTICS

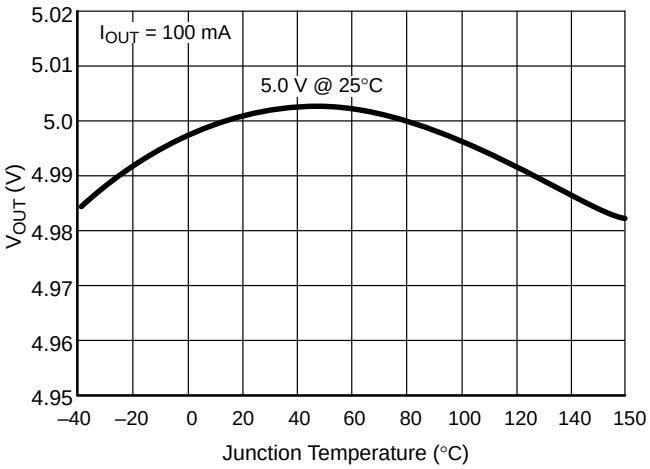


Figure 2. Output Voltage vs. Temperature

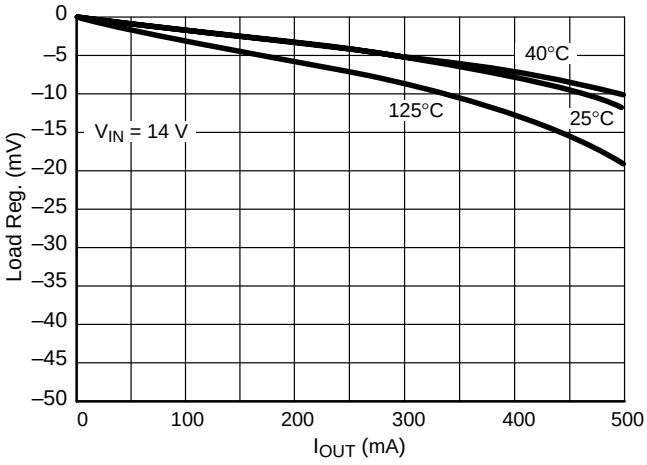


Figure 3. Load Regulation vs. Output Current Over Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

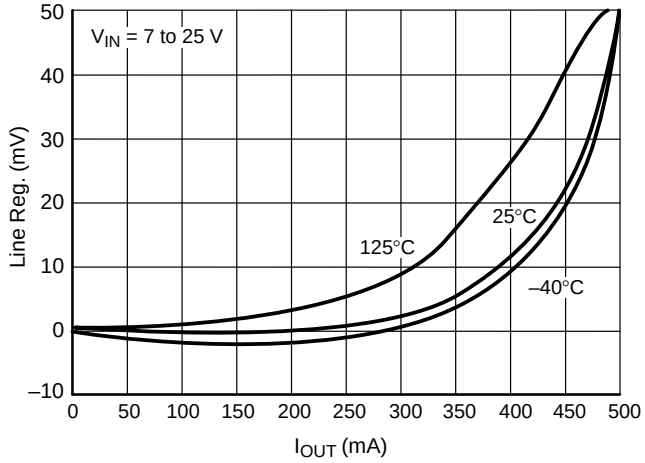


Figure 4. Line Regulation vs. Output Current Over Temperature

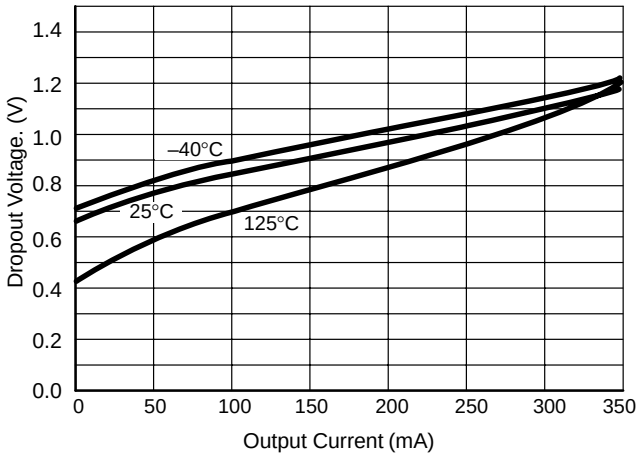


Figure 5. Dropout Voltage vs. Output Current Over Temperature

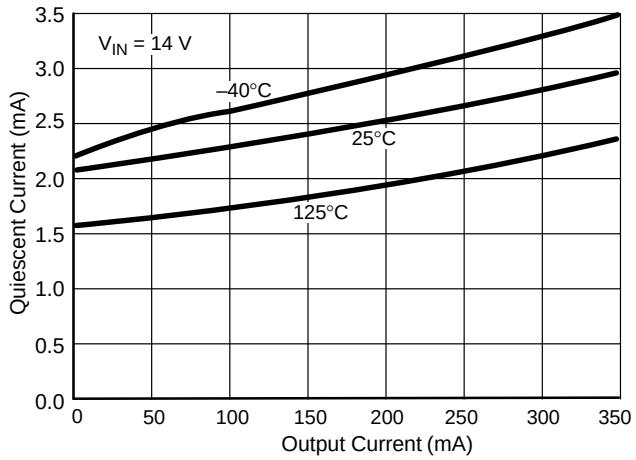


Figure 6. Quiescent Current vs. Output Current Over Temperature

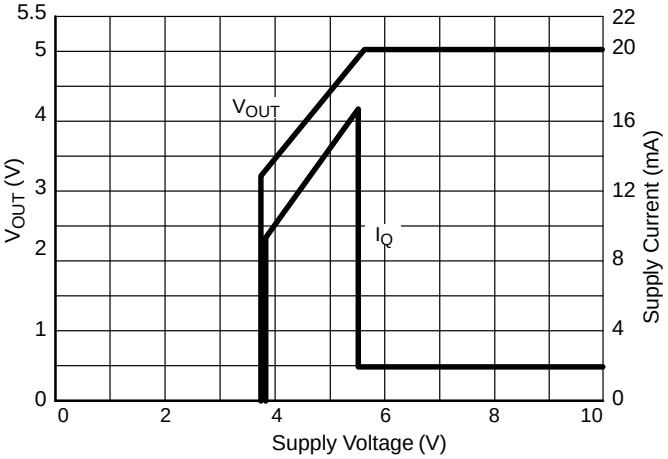


Figure 7. Output Voltage and Supply Current vs. Input Voltage

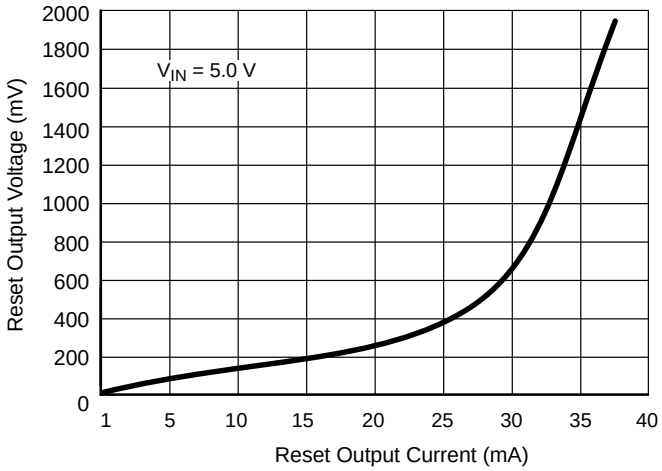


Figure 8. $\overline{\text{RESET}}$ Output Voltage vs. Output Voltage

CIRCUIT DESCRIPTION

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Precision Voltage Reference

The regulated output voltage depends on the precision band gap voltage reference in the IC. By adding an error amplifier into the feedback loop, the output voltage is maintained within ±4.0% over temperature and supply variation.

Output Stage

The composite PNP–NPN output structure (Figure 9) provides 300 mA (typ) of output current while maintaining a low drop out voltage (1.00 V, typ) and drawing little quiescent current (2.5 mA). The NPN pass device prevents deep saturation of the output stage which in turn improves the IC's efficiency by preventing excess current from being used and dissipated by the IC.

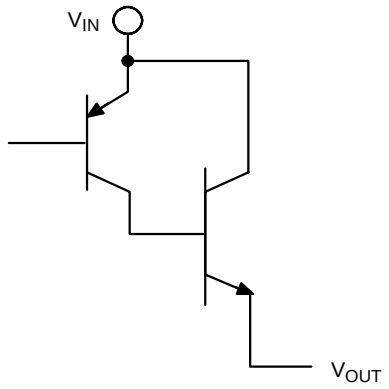


Figure 9. Composite Output Stage of the CS8120

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 10).

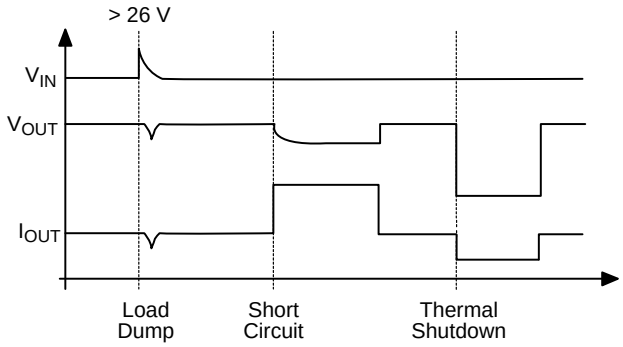


Figure 10. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 26 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Using an emitter sense scheme, the amount of current through the NPN pass transistor is monitored. Feedback circuitry insures that the output current never exceeds a preset limit.

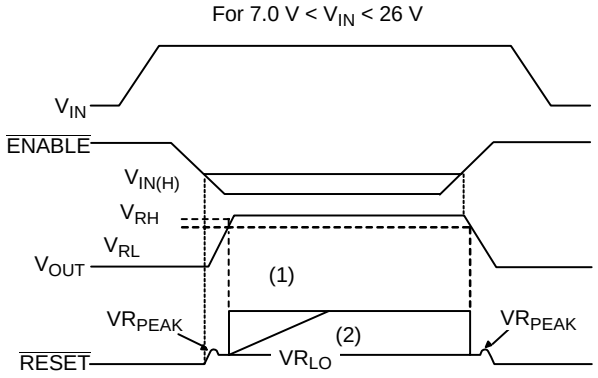
Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS

The CS8120 contains two microprocessor compatible control functions: $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ (Figure 11).

$\overline{\text{ENABLE}}$ Function

The $\overline{\text{ENABLE}}$ function switches the output transistor. When the voltage on the $\overline{\text{ENABLE}}$ lead exceeds 2.9 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 250 μA, until the voltage on the lead drops below 2.1 V typ. Hysteresis (800 mV) is built into the $\overline{\text{ENABLE}}$ function to provide good noise immunity.



(1) = No Reset Delay Capacitor
(2) = With Reset Delay Capacitor

Figure 11. Circuit Waveform for CS8120

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up ($V_{OUT} > V_{OUT} - 100$ mV) or when V_{OUT} drops out of regulation ($V_{OUT} < V_{OUT} - 140$ mV, typ). 40 mV of hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby

guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

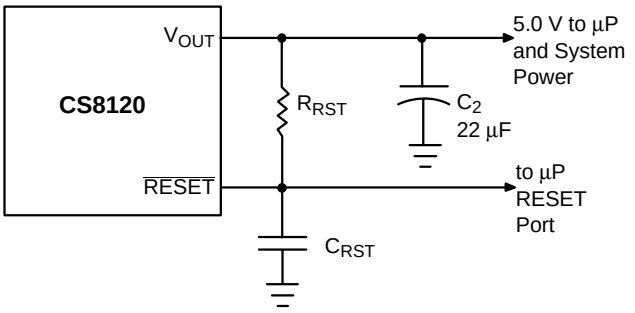


Figure 12. RC Network for $\overline{\text{RESET}}$ Delay Circuitry

An external RC network on the $\overline{\text{RESET}}$ lead (Figure 12) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT} \times C_{RST} = \left[\frac{-t_{Delay}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)}\right]$$

where:

$R_{TOT} = R_{RST}$ in parallel with R_{IN},
R_{IN} = µP port impedance,
$C_{RST} = \overline{\text{RESET}}$ delay capacitor,
t_{Delay} = desired delay time,
$V_{RST} = V_{SAT}$ of $\overline{\text{RESET}}$ lead (0.7 V @ turn – ON), and
V_T = µP logic threshold voltage.

APPLICATION NOTES

The circuit depicted in Figure 13 lets the microprocessor control its power source, the CS8120 regulator. An I/O port on the µP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text{ENABLE}}$ lead falls below its lower threshold. The regulator's output is switched out. When the drive current is removed, the voltage on the $\overline{\text{ENABLE}}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws 250 µA.

By coupling these two controls with the $\overline{\text{ENABLE}}$, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.

Table 1. Logic Control of CS8120 Output

Microprocessor I/O Drive	SWITCH	$\overline{\text{ENABLE}}$	Output
ON	Closed	LOW	ON
	Open	LOW	ON
OFF	Closed	LOW	ON
	Open	HIGH	OFF

The I/O port of the microprocessor typically provides 50 µA to Q1. In automotive applications the SWITCH is connected to the ignition switch.

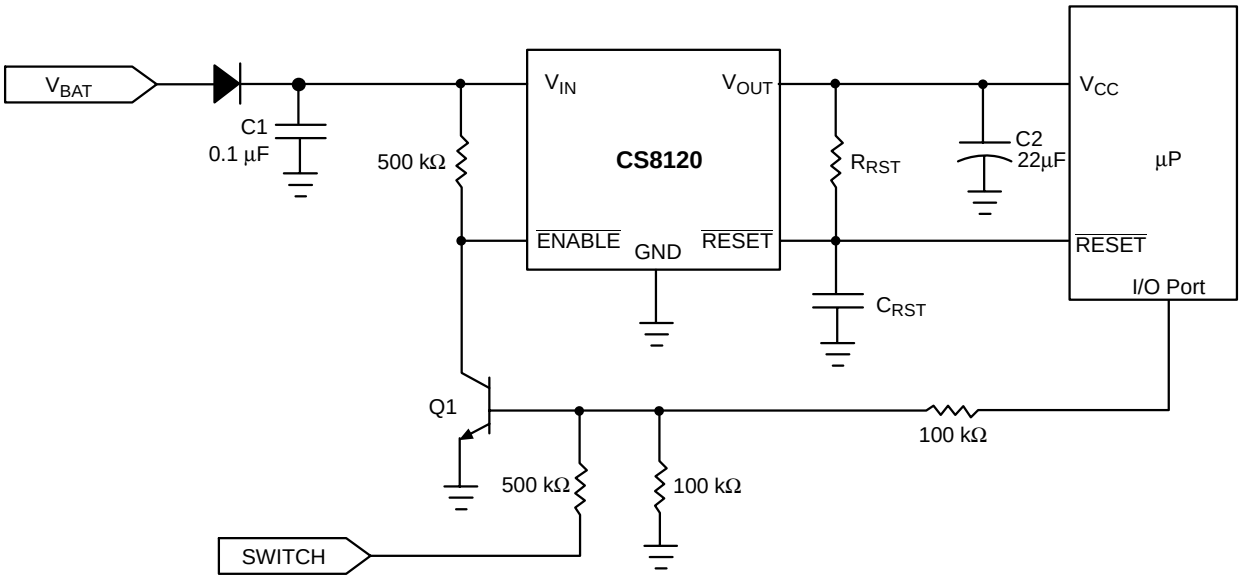


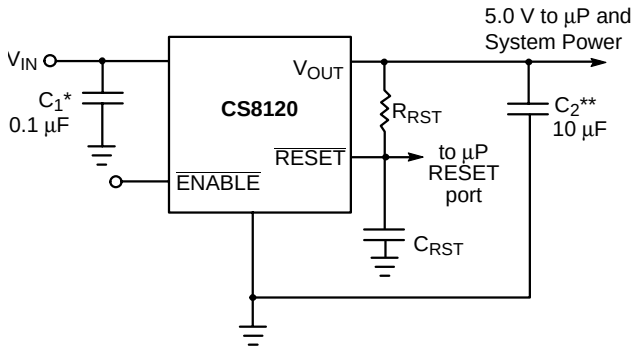
Figure 13. Microprocessor Control of CS8120 Using External Switching Transistor Q1

STABILITY CONSIDERATIONS

The output or compensation capacitor, C_2, helps determine three main characteristics of a linear regulator: start–up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_2 shown in Figure 14 should work for most applications, however it is not necessarily the optimized solution.



*C_1 is required if regulator is far from the power source filter.

**C_2 is required for stability.

Figure 14. Circuit Showing Output Compensation Capacitor

To determine an acceptable value for C_2 for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 15) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\Theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\Theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\Theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

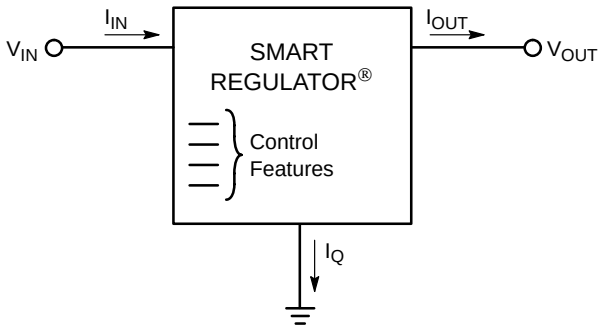


Figure 15. Single Output Regulator With Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\Theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\Theta JC}$ = the junction–to–case thermal resistance,

$R_{\Theta CS}$ = the case–to–heatsink thermal resistance, and

$R_{\Theta SA}$ = the heatsink–to–ambient thermal resistance.

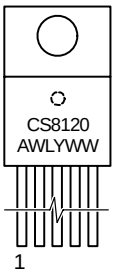
$R_{\Theta JC}$ appears in the package section of the data sheet. Like $R_{\Theta JA}$, it too is a function of package type. $R_{\Theta CS}$ and $R_{\Theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION

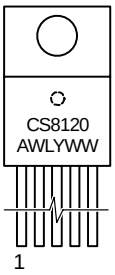
Device	Description	Shipping
CS8120YT5	TO–220 FIVE LEAD STRAIGHT	50 Units/Rail
CS8120YTVA5	TO–220 FIVE LEAD VERTICAL	50 Units/Rail
CS8120YTHA5	TO–220 FIVE LEAD HORIZONTAL	50 Units/Rail
CS8120YN8	DIP–8	50 Units/Rail
CS8120YDP5	D^2PAK, 5–Pin	50 Units/Rail
CS8120YDPR5	D^2PAK, 5–Pin	750 Tape & Reel
CS8120YD14	SO–14	55 Units/Rail
CS8120YDR14	SO–14	2500 Tape & Reel

MARKING DIAGRAMS

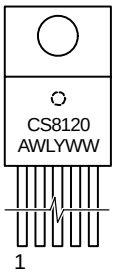
TO–220 FIVE LEAD T SUFFIX CASE 314D



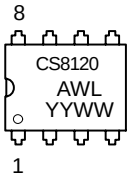
TO–220 FIVE LEAD TVA SUFFIX CASE 314K



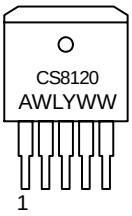
TO–220 FIVE LEAD THA SUFFIX CASE 314A



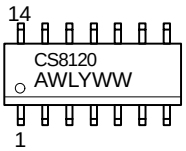
DIP–8 N SUFFIX CASE 626



D^2PAK 5–PIN DP SUFFIX CASE 936F



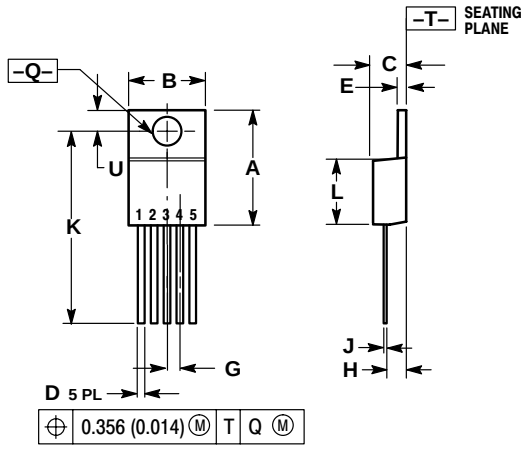
SO–14 D SUFFIX CASE 751A



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

PACKAGE DIMENSIONS

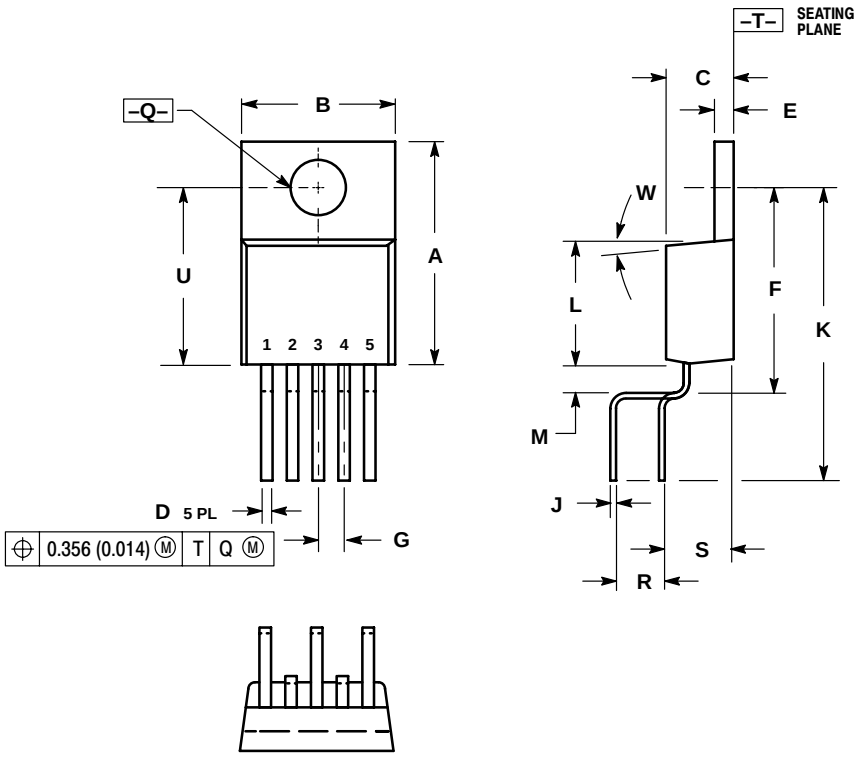
TO–220
FIVE LEAD
T SUFFIX
CASE 314D–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
G	0.067 BSC		1.702 BSC	
H	0.087	0.112	2.210	2.845
J	0.015	0.025	0.381	0.635
K	0.990	1.045	25.146	26.543
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
U	0.105	0.117	2.667	2.972

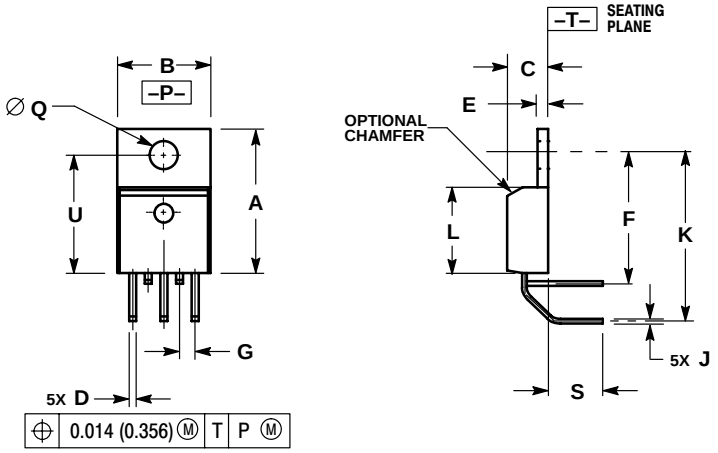
TO–220
FIVE LEAD
TVA SUFFIX
CASE 314K–01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 10.92 (0.043) MAXIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.560	0.590	14.22	14.99
B	0.385	0.415	9.78	10.54
C	0.160	0.190	4.06	4.83
D	0.027	0.037	0.69	0.94
E	0.045	0.055	1.14	1.40
F	0.530	0.545	13.46	13.84
G	0.067 BSC		1.70 BSC	
J	0.014	0.022	0.36	0.56
K	0.785	0.800	19.94	20.32
L	0.321	0.337	8.15	8.56
M	0.063	0.078	1.60	1.98
Q	0.146	0.156	3.71	3.96
R	0.271	0.321	6.88	8.15
S	0.146	0.196	3.71	4.98
U	0.460	0.475	11.68	12.07
W	5 °		5 °	

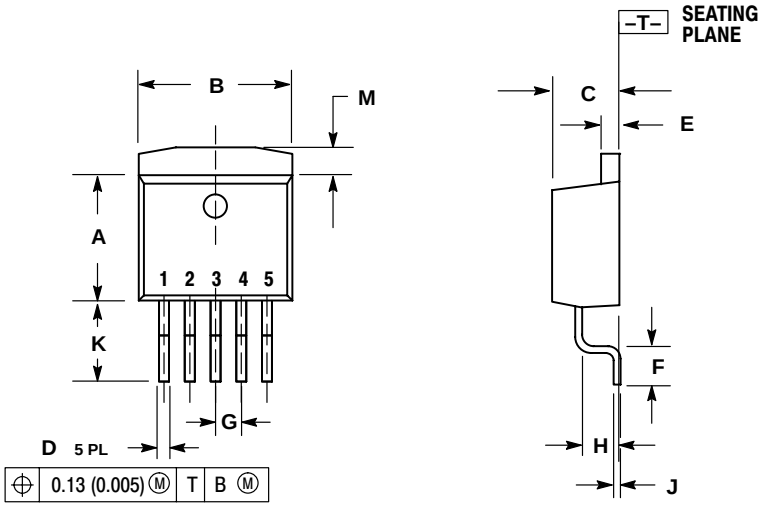
TO–220
FIVE LEAD
THA SUFFIX
CASE 314A–03
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE INTERCONNECT BAR (DAMBAR) PROTRUSION. DIMENSION D INCLUDING PROTRUSION SHALL NOT EXCEED 0.043 (1.092) MAXIMUM.

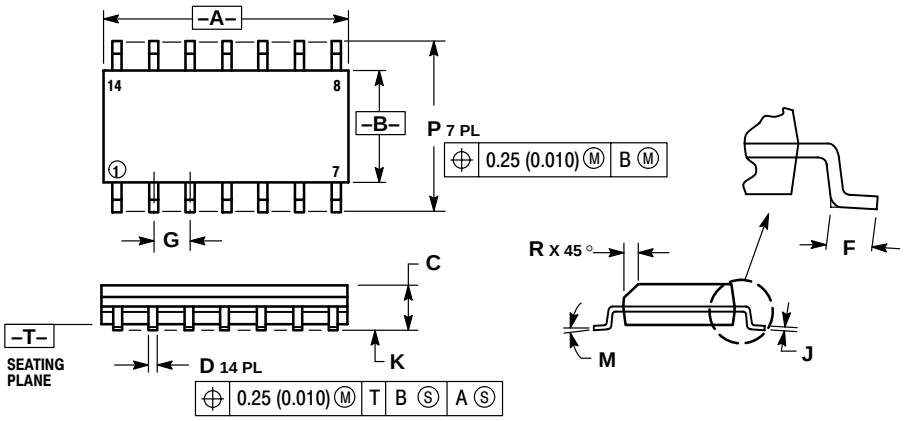
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.572	0.613	14.529	15.570
B	0.390	0.415	9.906	10.541
C	0.170	0.180	4.318	4.572
D	0.025	0.038	0.635	0.965
E	0.048	0.055	1.219	1.397
F	0.570	0.585	14.478	14.859
G	0.067 BSC		1.702 BSC	
J	0.015	0.025	0.381	0.635
K	0.730	0.745	18.542	18.923
L	0.320	0.365	8.128	9.271
Q	0.140	0.153	3.556	3.886
S	0.210	0.260	5.334	6.604
U	0.468	0.505	11.888	12.827

D^{2}PAK
5–PIN
DP SUFFIX
CASE 936F–01
ISSUE O



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.326	0.336	8.28	8.53
B	0.396	0.406	10.05	10.31
C	0.170	0.180	4.31	4.57
D	0.026	0.035	0.66	0.91
E	0.045	0.055	1.14	1.40
F	0.090	0.110	2.29	2.79
G	0.067 BSC		1.70 BSC	
H	0.098	0.108	2.49	2.74
J	0.018	0.025	0.46	0.64
K	0.204	0.214	5.18	5.44
M	0.055	0.066	1.40	1.68
N	0.000	0.004	0.00	0.10

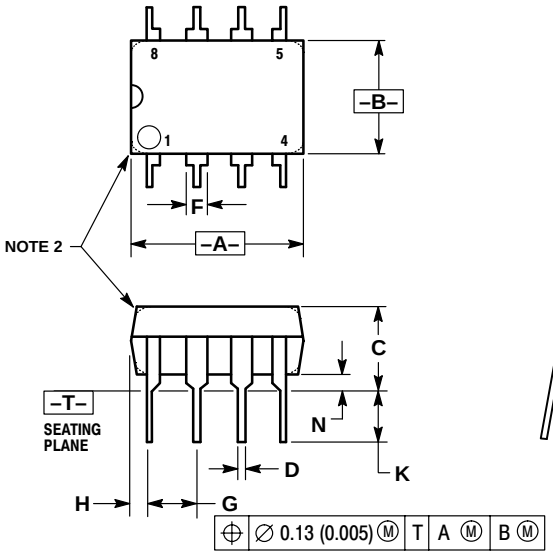
SO–14
D SUFFIX
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

DIP–8
N SUFFIX
CASE 626–05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10 °	---	10 °
N	0.76	1.01	0.030	0.040

PACKAGE THERMAL DATA

Parameter		TO–220 FIVE LEAD	D^2PAK FIVE LEAD	DIP–8	SO–14	Unit
$R_{\Theta JC}$	Typical	3.1	3.1	52	30	°C/W
$R_{\Theta JA}$	Typical	50	10–50*	100	125	°C/W

* Depending on thermal properties of substrate. $R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CA}$

Notes

Notes

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