May 2016

FAN5355
1.1 A / 1 A / 0.8 A, 3 MHz Digitally Programmable Regulator

Features

- 93% Efficiency at 3 MHz
- 800 mA, 1 A, or 1.1 A Output Current
- I^2C™-Compatible Interface up to 3.4 Mbps
- 6-bit V_{OUT} Programmable from 0.75 V to 1.975 V
- 2.7 V to 5.5 V Input Voltage Range
- 3 MHz Fixed-Frequency Operation
- Excellent Load and Line Transient Response
- Small Size, 1 µH Inductor Solution
- ±2% PWM DC Voltage Accuracy
- 35 ns Minimum On-Time
- High-Efficiency, Low-Ripple, Light-Load PFM
- Smooth Transition between PWM and PFM
- 37 µA Operating PFM Quiescent Current
- Pin-Selectable or I^2C™ Programmable Output Voltage
- On-the-Fly External Clock Synchronization
- 10-lead MLP (3 x 3 mm) or 12-bump CSP Packages

Applications

- Cell Phones, Smart Phones
- 3G, WiFi®, WiMAX™, and WiBro® Data Cards
- Netbooks®, Ultra-Mobile PCs
- SmartReflex™-Compliant Power Supply
- Split Supply DSPs and µP Solutions OMAP™, XSCALE™
- Mobile Graphic Processors (NVIDIA®, ATI)
- LPDDR2 and Memory Modules

Description

The FAN5355 device is a high-frequency, ultra-fast transient response, synchronous step-down DC-DC converter optimized for low-power applications using small, low-cost inductors and capacitors. The FAN5355 supports up to 800 mA, 1 A, or 1.1 A load current.

The device is ideal for mobile phones and similar portable applications powered by a single-cell Lithium-Ion battery. With an output-voltage range adjustable via I^2C™ interface from 0.75 V to 1.975 V, the device supports low-voltage DSPs and processors, core power supplies, and memory modules in smart phones, PDAs, and handheld computers.

The FAN5355 operates at 3 MHz (nominal) fixed switching frequency using either its internal oscillator or an external SYNC frequency.

During light-load conditions, the regulator includes a PFM mode to enhance light-load efficiency. The regulator transitions smoothly between PWM and PFM modes with no glitches on V_{OUT}. In hardware shutdown, the current consumption is reduced to less than 200 nA.

The serial interface is compatible with Fast/Standard and High-Speed mode I^2C specifications, allowing transfers up to 3.4 Mbps. This interface is used for dynamic voltage scaling with 12.5 mV voltage steps for reprogramming the mode of operation (PFM or Forced PWM), or to disable/enable the output voltage.

The chip's advanced protection features include short-circuit protection and current and temperature limits. During a sustained over-current event, the IC shuts down and restarts after a delay to reduce average power dissipation into a fault.

During startup, the IC controls the output slew rate to minimize input current and output overshoot at the end of soft start. The IC maintains a consistent soft-start ramp, regardless of output load during startup.

The FAN5355 is available in 10-lead MLP (3x3 mm) and 12-bump WLCSP packages.

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Ordering Information

Order Number[1]	Option	Slave Address LSB		Output Current	V_{OUT} Programming		Power-up Defaults		Package
		A1	A0	mA	Min.	Max.	VSEL0	VSEL1	
FAN5355UC00X	00	0	0	800	0.7500	1.5375	1.05	1.35	WLCSP-12, 2.23 x 1.46 mm
FAN5355MP00X	00	0	0	800	0.7500	1.5375	1.05	1.35	MLP-10, 3 x 3 mm
FAN5355UC02X	02	1	0	800	0.7500	1.4375[2]	1.05	1.20	WLCSP-12, 2.23 x 1.46 mm
FAN5355UC03X	03	0	0	1000	0.7500	1.5375	1.00	1.20	WLCSP-12, 2.23 x 1.46 mm
FAN5355UC06X	06	0	0	1000	1.1875	1.9750	1.80	1.80	WLCSP-12, 2.23 x 1.46 mm
FAN5355UC08X	08	1	0	1100	0.7500	1.4375[2]	1.05	1.20	WLCSP-12, 2.23 x 1.46 mm

Notes:
1. The "X" designator specifies tape and reel packaging.
2. V_{OUT} is limited to the maximum voltage for all VSEL codes greater than the maximum V_{OUT} listed.

Typical Application

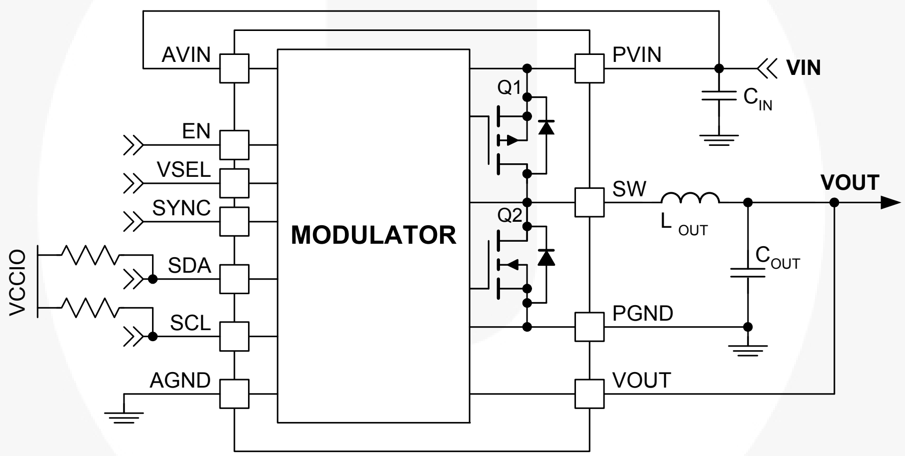

Figure 1. Typical Application

Table 1. Recommended External Components

Component	Description	Vendor	Parameter	Min.	Typ.	Max.	Units
L1 (L_{OUT})	1µH nominal	Murata LQM31P or FDK MIPSA2520	L[3]	0.7	1.0	1.2	µH
			DCR (series R)		100		mΩ
C_{OUT}	0603 (1.6x0.8x0.8) 10 µF X5R or better	Murata or equivalent GRM188R60G106ME47D	C[4]	5.6	10.0	12.0	µF
C_{IN}	0603 (1.6 x 0.8 x 0.8) 4.7 µF X5R or better	Murata or equivalent GRM188R60J475KE19D	C[4]	3.0	4.7	5.6	µF

Notes:
3. Minimum L incorporates tolerance, temperature, and partial saturation effects (L decreases with increasing current).
4. Minimum C is a function of initial tolerance, maximum temperature, and the effective capacitance being reduced due to frequency, dielectric, and voltage bias effects.

Pin Configuration

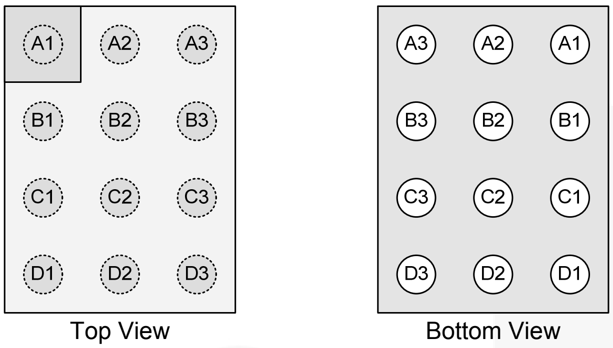

Figure 2. WLCSP-12, 2.23 x 1.46 mm

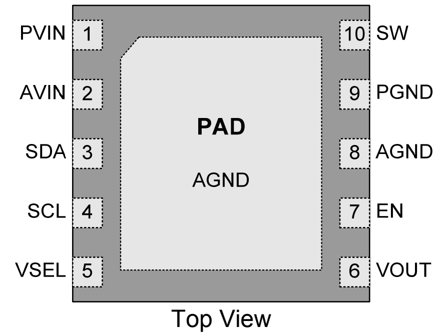

Figure 3. MLP10, 3 x 3 mm

Pin Definitions

Pin #		Name[5]	Description
WLCSP	**MLP**		
A1, B1	9	PGND	**Power GND**. Power return for gate drive and power transistors. Connect to AGND on PCB. The connection from this pin to the bottom of C_{IN} should be as short as possible.
A2	10	SW	**Switching Node**. Connect to output inductor.
A3	1	PVIN	**Power Input Voltage**. Connect to input power source. The connection from this pin to C_{IN} should be as short as possible.
B2	N/A	SYNC	**Sync**. When toggling and SYNC_EN bit is HIGH, the regulator synchronizes to the frequency on this pin. In PWM mode, when this pin is statically LOW or statically HIGH, or when its frequency is outside of the specified capture range, the regulator's frequency is controlled by its internal 3 MHz clock.
B3	2	AVIN	**Analog Input Voltage**. Connect to input power source as close as possible to the input bypass capacitor.
C1	8, PAD	AGND	**Analog GND**. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
C2	7	EN	**Enable**. When this pin is HIGH, the circuit is enabled. When LOW, quiescent current is minimized. This pin should not be left floating.
C3	3	SDA	**SDA**. I^2C interface serial data.
D1	6	VOUT	**Output Voltage Monitor**. Tie this pin to the output voltage. This is a signal input pin to the control circuit and does not carry DC current.
D2	5	VSEL	**Voltage Select**. When HIGH, V_{OUT} is set by VSEL1. When LOW, V_{OUT} is set by VSEL0. This behavior can be overridden through I^2C register settings. This pin should not be left floating.
D3	4	SCL	**SCL**. I^2C interface serial clock.

Note:

5. All logic inputs (SDA, SCL, SYNC, EN, and VSEL) are high impedance and should not be left floating. For minimum quiescent power consumption, tie unused logic inputs to AVIN or AGND. If I^2C control is unused, tie SDA and SCL to AVIN.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	AVIN, SW, PVIN Pins		-0.3	6.5	V
	Other Pins		-0.3	AVIN + 0.3[6]	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	3.5		KV
		Charged Device Model per JESD22-C101	1.5		KV
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

6. Lesser of 6.5V or AVIN+0.3V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	2.7	5.5	V
f	Frequency Range	2.7	3.3	MHz
V_{CCIO}	SDA and SCL Voltage Swing[7]		2.5	V
T_A	Ambient Temperature	–40	+85	°C
T_J	Junction Temperature	–40	+125	°C

Note:

7. The I^2C interface operates with $t_{HD;DAT}$ = 0 as long as the pull-up voltage for SDA and SCL is less than 2.5 V. If voltage swings greater than 2.5 V are required (for example if the I^2C bus is pulled up to V_{IN}), the minimum $t_{HD;DAT}$ must be increased to 80 ns. Most I^2C masters change SDA near the midpoint between the falling and rising edges of SCL, which provides ample $t_{HD;DAT}$.

Dissipation Ratings[8]

Package	θ_{JA}[9]	Power Rating at $T_A \leq 25°C$	Derating Factor > T_A = 25ºC
Molded Leadless Package (MLP)	49ºC/W	2050 mW	21 mW/ºC
Wafer-Level Chip-Scale Package (WLCSP)	110ºC/W	900 mW	9 mW/ºC

Notes:

8. Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = [T_{J(max)} - T_A] / \theta_{JA}$.
9. This thermal data is measured with high-K board (four-layer board according to JESD51-7 JEDEC standard).

Electrical Specifications

V_{IN} = 3.6 V, EN = V_{IN}, VSEL = V_{IN}, SYNC = GND, VSEL0(6) bit = 1, CONTROL2[4:3] = 00. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Circuit and components according to Figure 1.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies						
V_{IN}	Input Voltage Range		2.7		5.5	V
I_Q	Quiescent Current	I_O = 0 mA, PFM Mode		37	50	µA
		I_O = 0 mA, 3 MHz PWM Mode		4.8		mA
I_{SD}	Shutdown Supply Current	EN = GND		0.1	2.0	µA
		EN = V_{IN}, EN_DCDC bit = 0, SDA = SCL = V_{IN}		0.1	2.0	
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.40	2.60	V
		V_{IN} Falling	2.00	2.15	2.30	V
V_{UVHYST}	Under-Voltage Lockout Hysteresis		200	250	300	mV
ENABLE, VSEL, SDA, SCL, SYNC						
V_{IH}	HIGH-Level Input Voltage		1.2			V
V_{IL}	LOW-Level Input Voltage				0.4	V
I_{IN}	Input Bias Current	Input tied to GND or V_{IN}		0.01	1.00	µA
Power Switch and Protection						
$R_{DS(ON)P}$	P-Channel MOSFET On Resistance	V_{IN} = 3.6 V, CSP Package		145		mΩ
		V_{IN} = 3.6 V, MLP Package		165		
		V_{IN} = 2.7 V, MLP Package		200		
I_{LKGP}	P-Channel Leakage Current	V_{DS} = 6 V			1	µA
$R_{DS(ON)N}$	N-Channel MOSFET On Resistance	V_{IN} = 3.6 V, CSP Package		75		mΩ
		V_{IN} = 3.6 V, MLP Package		95		
		V_{IN} = 2.7 V, MLP Package		101		
I_{LKGN}	N-Channel Leakage Current	V_{DS} = 6 V			1	µA
R_{DIS}	Discharge Resistor for Power-Down Sequence	Options 03 and 06		60	120	Ω
I_{LIMPK}	P-MOS Current Limit	2.7 V ≤ V_{IN} ≤ 4.2 V, Options 00 and 02	1150	1350	1600	mA
		2.7 V ≤ V_{IN} ≤ 5.5 V, Options 00 and 02	1050	1350	1600	
		2.7 V ≤ V_{IN} ≤ 4.2 V, Options 03 and 06	1350	1550	1800	
		2.7 V ≤ V_{IN} ≤ 5.5 V, Options 03 and 06	1250	1550	1800	
		2.7 V ≤ V_{IN} ≤ 4.5 V, Option 08	1400	1650		
T_{LIMIT}	Thermal Shutdown			150		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
Frequency Control						
f_{SW}	Oscillator Frequency		2.65	3.00	3.35	MHz
f_{SYNC}	Synchronization Range		2.7	3.0	3.3	MHz
D_{SYNC}	Synchronization Duty Cycle		20		80	%

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Electrical Specifications (Continued)

V_{IN} = 3.6 V, EN = V_{IN}, VSEL = V_{IN}, SYNC = GND, VSEL0(6) bit = 1, CONTROL2[4:3] = 00. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Circuit and components according to Figure 1.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
Output Regulation							
V_{OUT}	V_{OUT} Accuracy	Option 00	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = 1.35 V	–1.5		1.5	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.5375, $I_{OUT(DC)}$ = 0 to 800 mA, Forced PWM	–2		2	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.5375, $I_{OUT(DC)}$ = 0 to 800 mA, PFM Mode	–1.5		3.5	%
		Option 02	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = 1.20 V	–1.5		1.5	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.4375, $I_{OUT(DC)}$ = 0 to 800 mA, Forced PWM	–2		2	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.4375, $I_{OUT(DC)}$ = 0 to 800 mA, PFM Mode	–1.5		3.5	%
		Option 03	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = 1.20 V	–1.5		1.5	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.5375, $I_{OUT(DC)}$ = 0 to 1 A, Forced PWM	–2		2	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.5375, $I_{OUT(DC)}$ = 0 to 1 A, PFM Mode	–1.5		3.5	%
		Option 06	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = 1.800 V	–1.5		1.5	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 1.185 to 1.975, $I_{OUT(DC)}$ = 0 to 1 A, Forced PWM	–2		2	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 1.185 to 1.975, $I_{OUT(DC)}$ = 0 to 1 A, PFM Mode	–1.5		3.5	%
		Option 08	$I_{OUT(DC)}$ = 0, Forced PWM, V_{OUT} = 1.20 V	–1.5		1.5	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.4375, $I_{OUT(DC)}$ = 0 to 1100 mA, Forced PWM	–2		2	%
			2.7 V ≤ V_{IN} ≤ 5.5 V, V_{OUT} from 0.75 to 1.4375, $I_{OUT(DC)}$ = 0 to 1100 mA, PFM Mode	–1.5		3.5	%
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation		$I_{OUT(DC)}$ = 0 to 800 mA, Forced PWM		–0.5		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation		2.7 V ≤ V_{IN} ≤ 5.5 V, $I_{OUT(DC)}$ = 300 mA		0		%/V
V_{RIPPLE}	Output Ripple Voltage		PWM Mode, V_{OUT} = 1.35 V		2.2		mV_{PP}
			PFM Mode, $I_{OUT(DC)}$ = 10 mA		20		mV_{PP}

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Electrical Specifications (Continued)

V_{IN} = 3.6 V, EN = V_{IN}, VSEL = V_{IN}, SYNC = GND, VSEL0(6) bit = 1, CONTROL2[4:3] = 00. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C. Circuit and components according to Figure 1.

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Units
6-Bit DAC							
	Differential Nonlinearity		Monotonicity Assured by Design			0.8	LSB
Timing							
I^2C_{EN}	EN HIGH to I^2C Start			250			µs
$t_{V(L-H)}$	V_{OUT} LOW to HIGH Settling		R_{LOAD} = 75 Ω, Transition from 1.0 to 1.5375 V, V_{OUT} Settled to within 2% of Set Point		7		µs
Soft Start							
t_{SS}	Regulator Enable to Regulated V_{OUT}	Option 06	R_{LOAD} ≥ 5 Ω, to V_{OUT} = 1.8000 V		170	210	µs
		All Other Options	R_{LOAD} ≥ 5 Ω, to V_{OUT} = Power-up Default		140	180	µs
V_{SLEW}	Soft-start V_{OUT} Slew Rate[10]				18.75		V/ms

Note:

10. Option 03 and 06 slew rates are 35.5 V/ms during the first 16 µs of soft start.

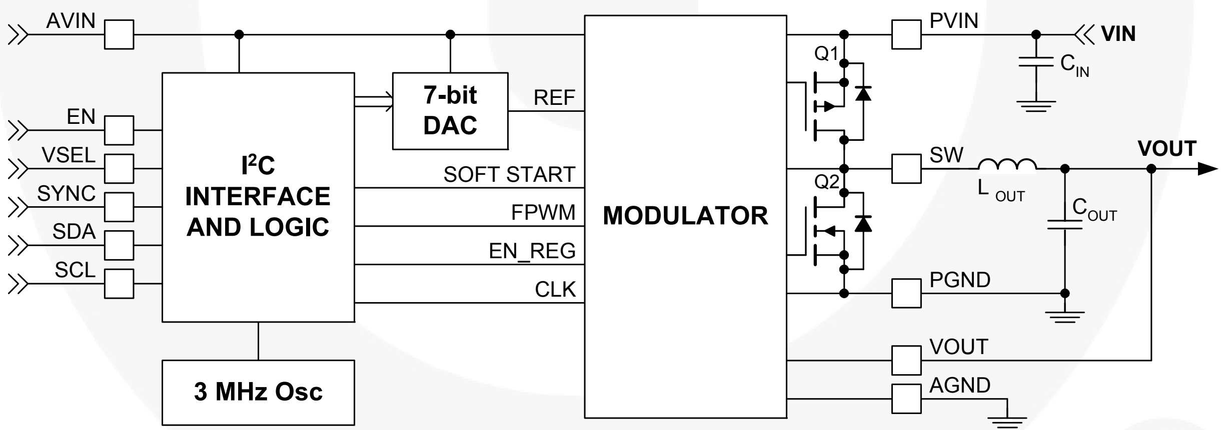


Figure 4. Block Diagram

I²C Timing Specifications

Guaranteed by design.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL Clock Frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
		High-Speed Mode, $C_B \le 100$ pF			3400	kHz
		High-Speed Mode, $C_B \le 400$ pF			1700	kHz
t_{BUF}	Bus-Free Time between STOP and START Conditions	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
$t_{HD;STA}$	START or Repeated-START Hold Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
t_{LOW}	SCL LOW Period	Standard Mode		4.7		µs
		Fast Mode		1.3		µs
		High-Speed Mode, $C_B \le 100$ pF		160		ns
		High-Speed Mode, $C_B \le 400$ pF		320		ns
t_{HIGH}	SCL HIGH Period	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode, $C_B \le 100$ pF		60		ns
		High-Speed Mode, $C_B \le 400$ pF		120		ns
$t_{SU;STA}$	Repeated-START Setup Time	Standard Mode		4.7		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
$t_{SU;DAT}$	Data Setup Time	Standard Mode		250		ns
		Fast Mode		100		ns
		High-Speed Mode		10		ns
$t_{HD;DAT}$	Data Hold Time[7]	Standard Mode	0		3.45	µs
		Fast Mode	0		900	ns
		High-Speed Mode, $C_B \le 100$ pF	0		70	ns
		High-Speed Mode, $C_B \le 400$ pF	0		150	ns
t_{RCL}	SCL Rise Time	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100$ pF		10	80	ns
		High-Speed Mode, $C_B \le 400$ pF		20	160	ns
t_{FCL}	SCL Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100$ pF		10	40	ns
		High-Speed Mode, $C_B \le 400$ pF		20	80	ns
t_{RDA} t_{RCL1}	SDA Rise Time Rise Time of SCL After a Repeated START Condition and After ACK Bit	Standard Mode	$20+0.1C_B$		1000	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100$ pF		10	80	ns
		High-Speed Mode, $C_B \le 400$ pF		20	160	ns
t_{FDA}	SDA Fall Time	Standard Mode	$20+0.1C_B$		300	ns
		Fast Mode	$20+0.1C_B$		300	ns
		High-Speed Mode, $C_B \le 100$ pF		10	80	ns
		High-Speed Mode, $C_B \le 400$ pF		20	160	ns
$t_{SU;STO}$	Stop Condition Setup Time	Standard Mode		4		µs
		Fast Mode		600		ns
		High-Speed Mode		160		ns
C_B	Capacitive Load for SDA and SCL				400	pF

Timing Diagrams

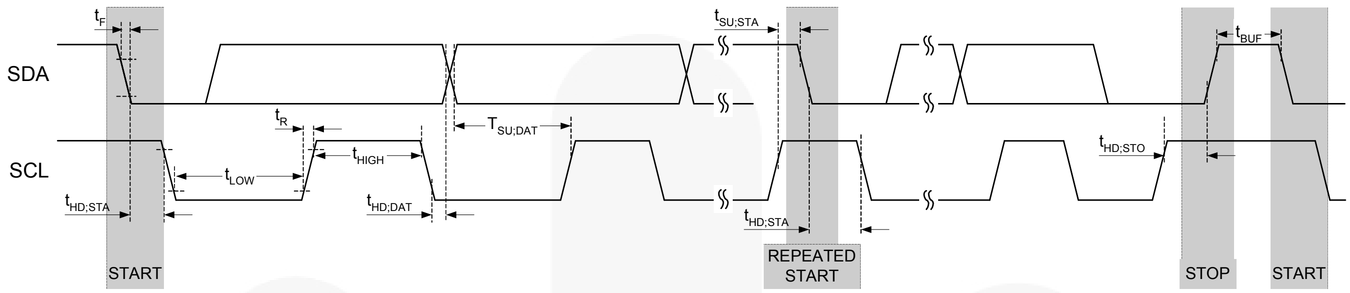
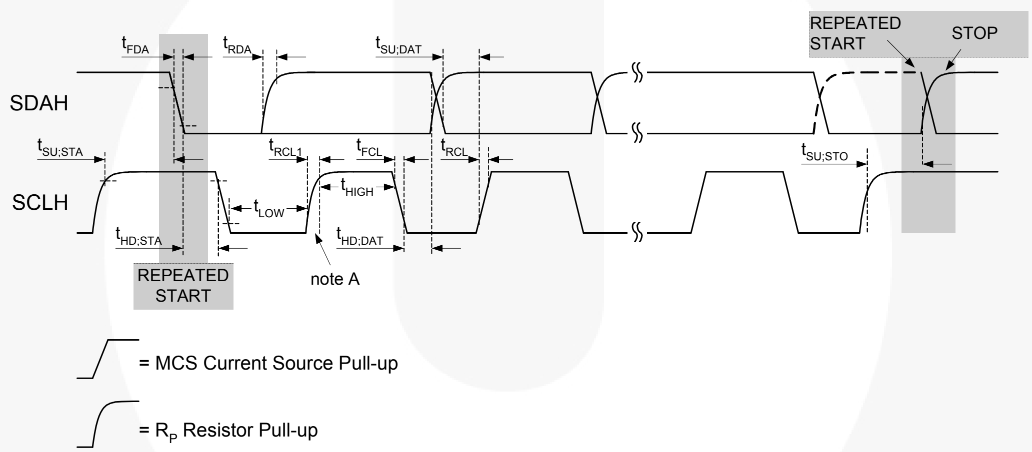


Figure 5. I²C Interface Timing for Fast and Slow Modes



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 6. I²C Interface Timing for High-Speed Mode

Typical Performance Characteristics

Unless otherwise specified, Auto-PWM/PFM, V_{IN} = 3.6 V, T_A = 25°C, and recommended components as specified in Table 1.

Efficiency

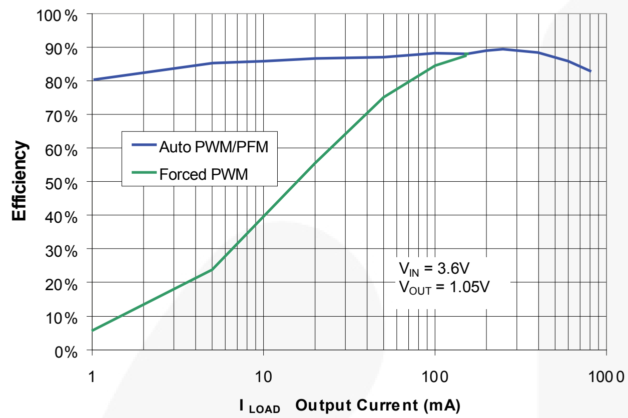


Figure 7. Efficiency vs. Load at V_{OUT} = 1.05 V

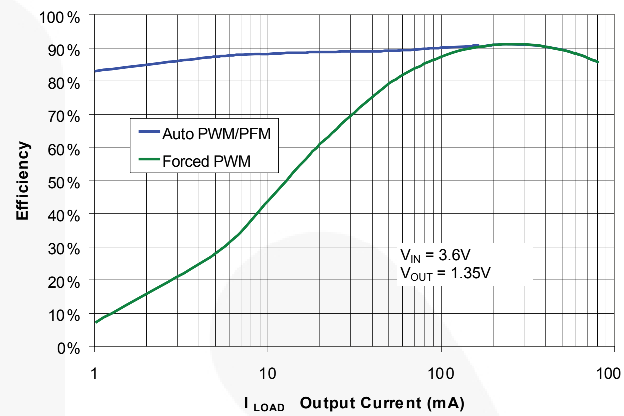


Figure 8. Efficiency vs. Load at V_{OUT} = 1.35 V

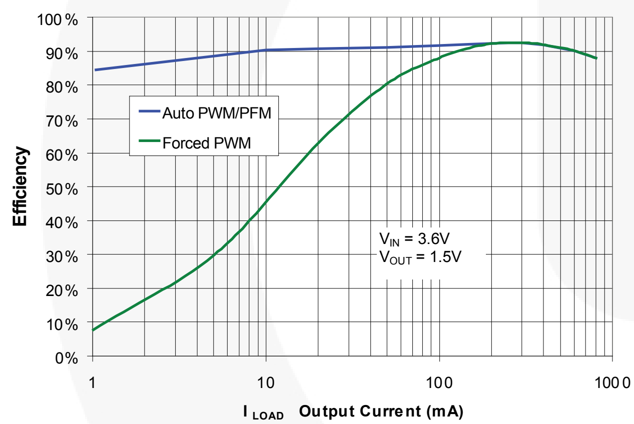


Figure 9. Efficiency vs. Load at V_{OUT} = 1.50 V

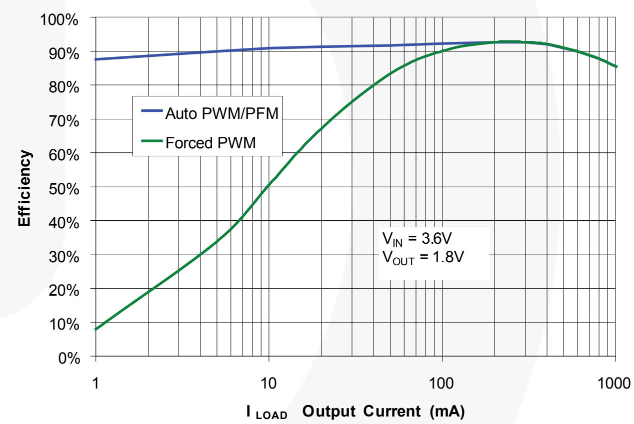


Figure 10. Efficiency vs. Load at V_{OUT} = 1.80 V

Typical Performance Characteristics

Unless otherwise specified, Auto-PWM/PFM, V_{IN} = 3.6 V, T_A = 25°C, and recommended components as specified in Table 1.

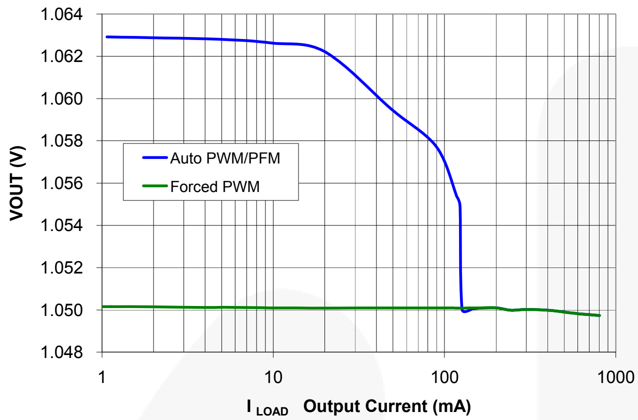


Figure 11. Load Regulation at V_{OUT} = 1.05 V

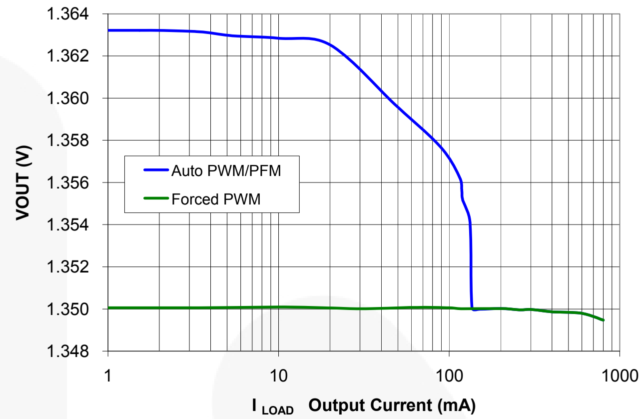


Figure 12. Load Regulation at V_{OUT} = 1.35 V

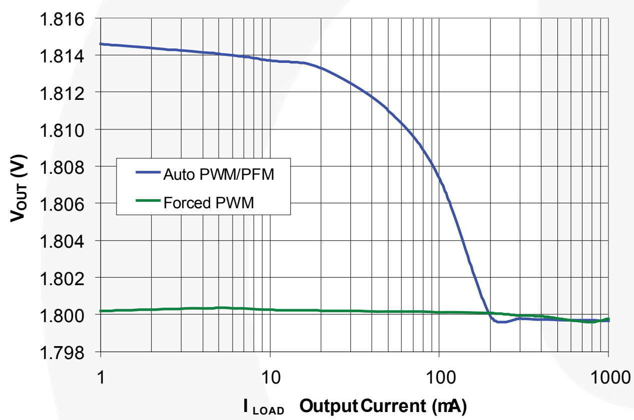


Figure 13. Load Regulation at V_{OUT} = 1.80 V

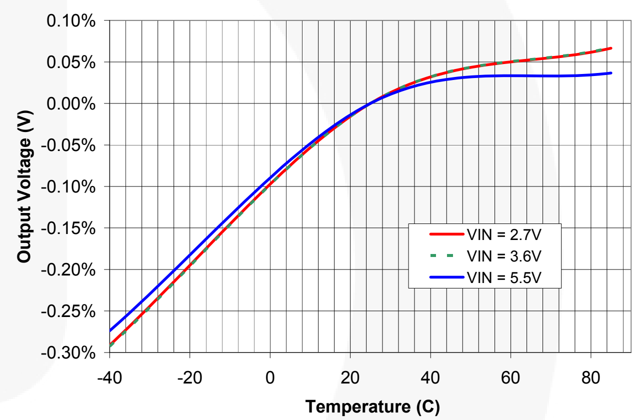


Figure 14. % V_{OUT} Shift vs. Temperature (Normalized)

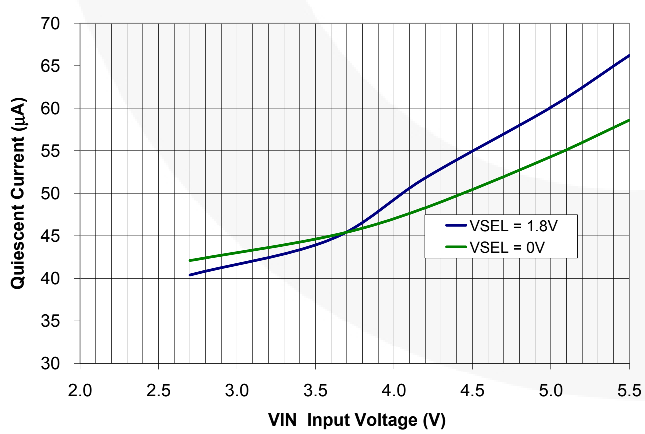


Figure 15. Quiescent Current, I_{LOAD} = 0, EN = 1.8 V

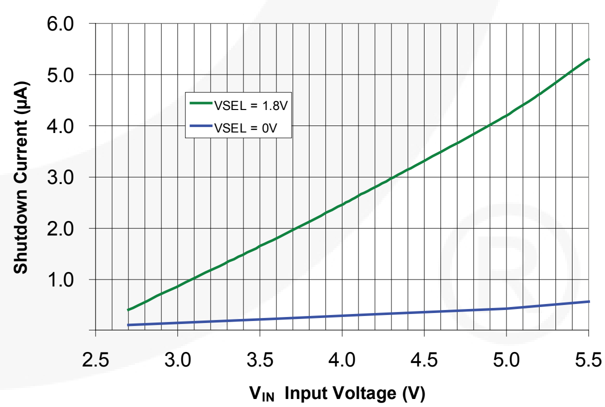


Figure 16. Shutdown Current, I_{LOAD} = 0, EN = 0

Typical Performance Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V, V_{OUT} = 1.35 V, and load step t_R = t_F < 100 ns.

Load Transient Response

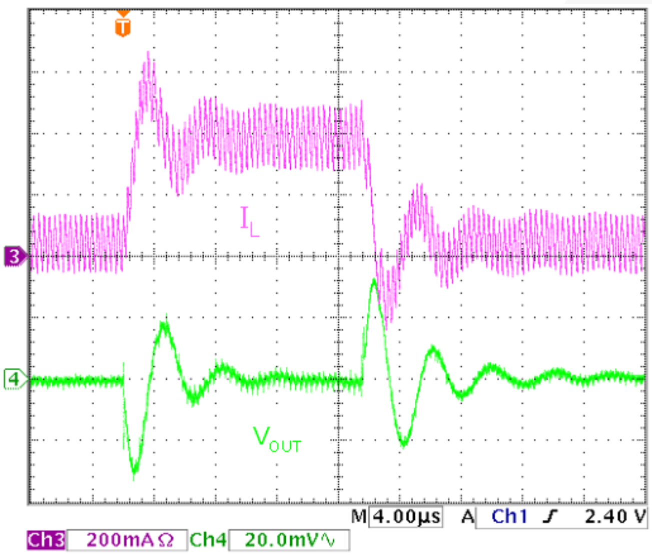


Figure 17. 50 mA to 400 mA to 50 mA, Forced PWM

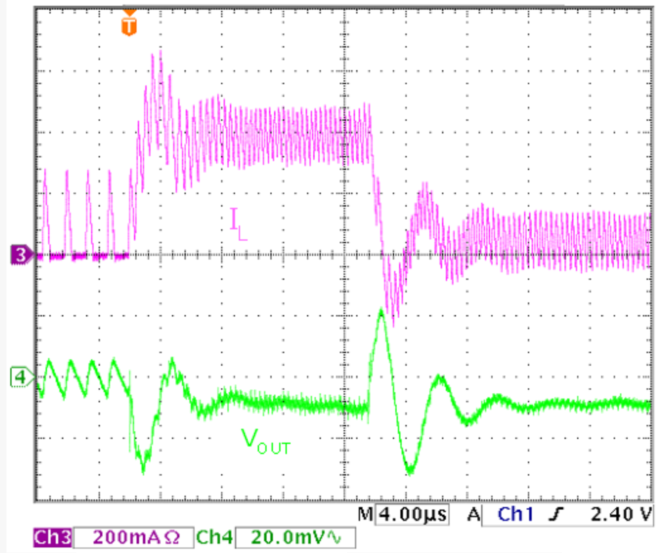


Figure 18. 50 mA to 400 mA to 50 mA, Auto PWM/PFM

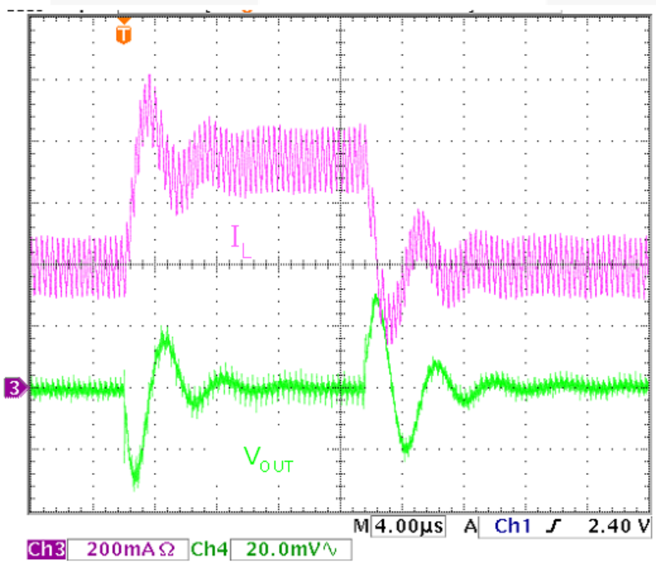


Figure 19. 400 mA to 750 mA to 400 mA, Auto PWM/PFM

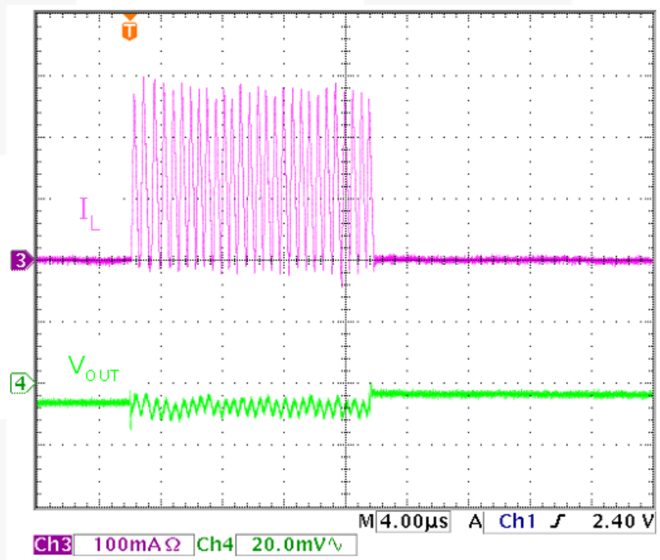


Figure 20. 0 mA to 125 mA to 0 mA, Auto PWM/PFM

Typical Performance Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V.

VSEL Transitions

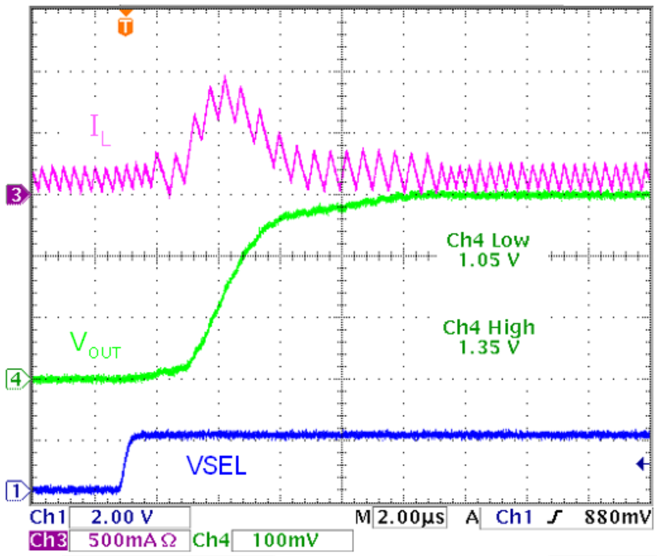


Figure 21. Single-Step, R_{LOAD} = 6.2 Ω

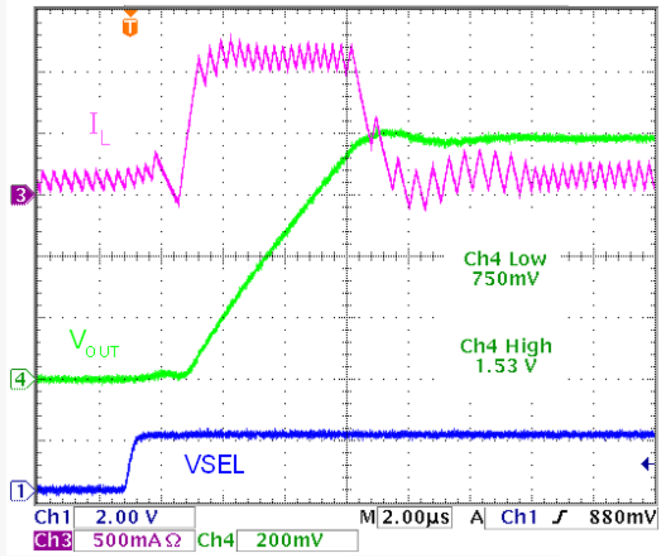


Figure 22. Single-Step, R_{LOAD} = 6.2 Ω

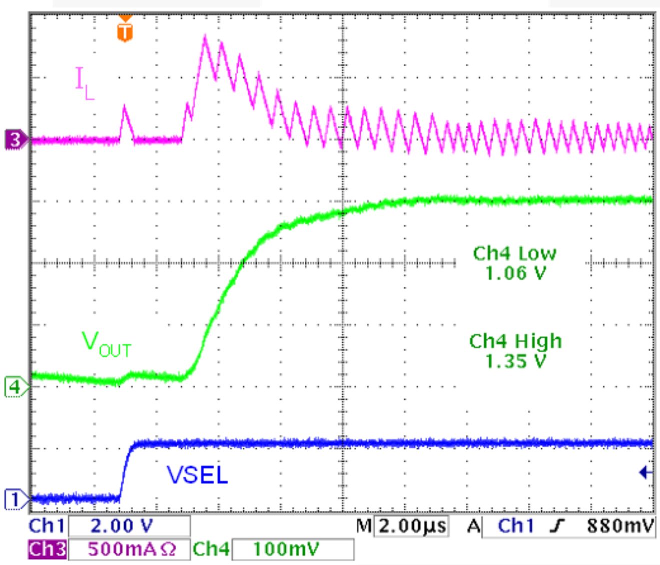


Figure 23. Single-Step, R_{LOAD} = 50 Ω

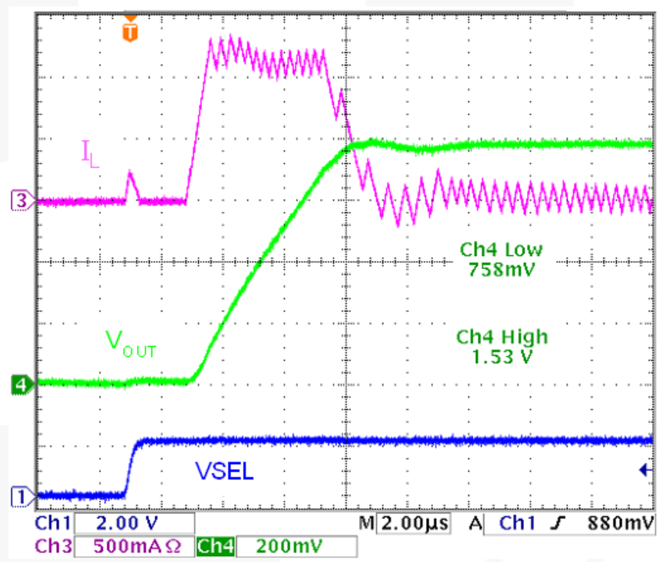


Figure 24. Single-Step, R_{LOAD} = 50 Ω

Typical Performance Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V.

VSEL Transitions

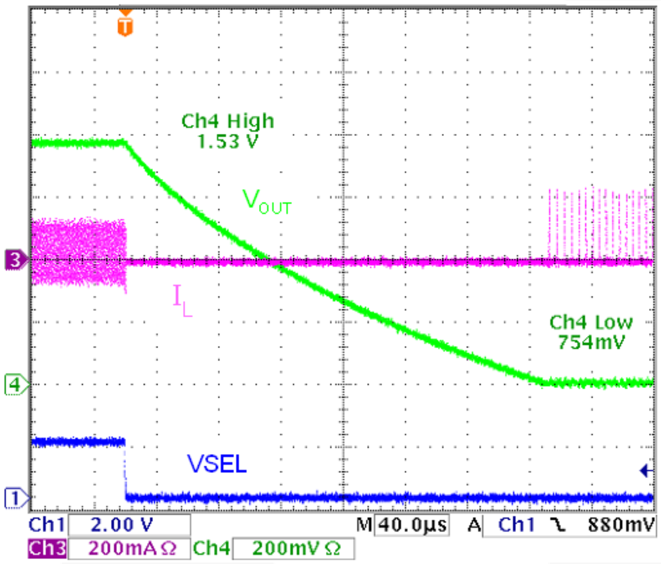


Figure 25. Single-Step from Forced PWM (MODE1=0), R_{LOAD} = 50 Ω

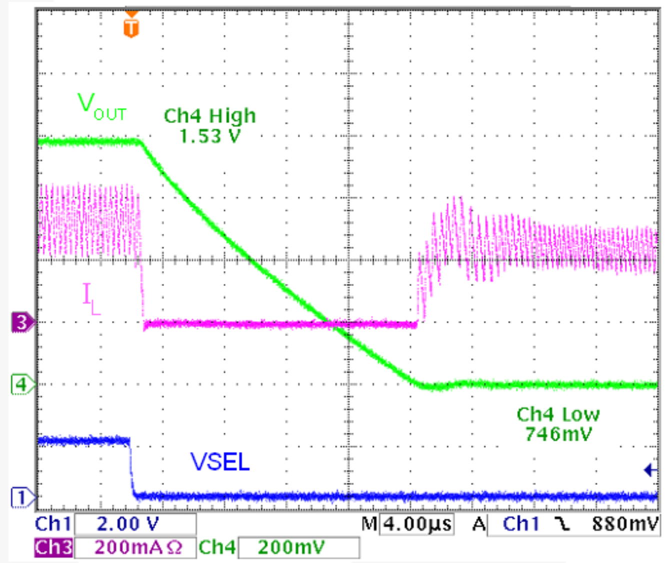


Figure 26. Single-Step, R_{LOAD} = 6.2 Ω

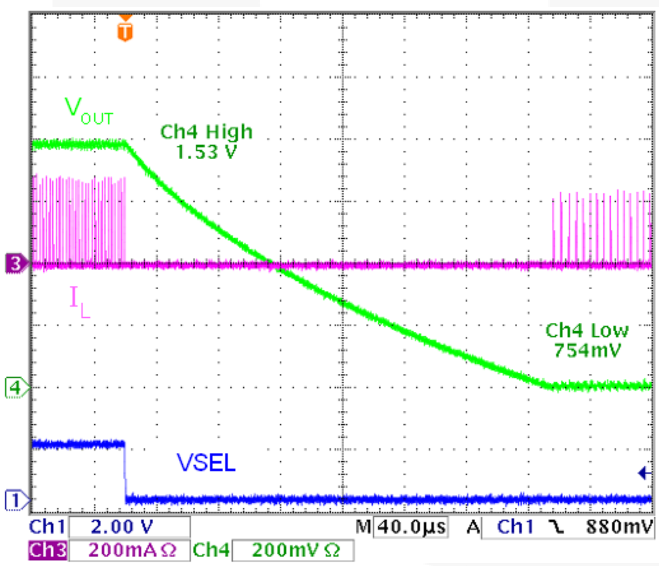


Figure 27. Single–Step from Auto PWM/PFM (MODE1=1), R_{LOAD} = 50 Ω

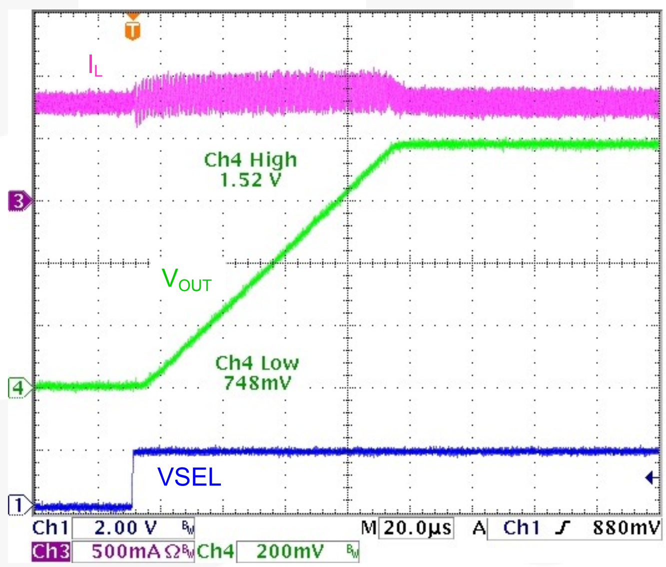


Figure 28. Multi-Step, Controlled DAC Step (9.6 mV/µs) DEF_Slew 6 (110), 800 mA Load

Typical Performance Characteristics (Continued)

R_{LOAD} is switched with N-channel MOSFET from VOUT to GND. V_{IN} = 3.6 V, initial V_{OUT} = 1.35 V, initial I_{LOAD} = 0 mA.

Short Circuit and Over-Current Fault Response

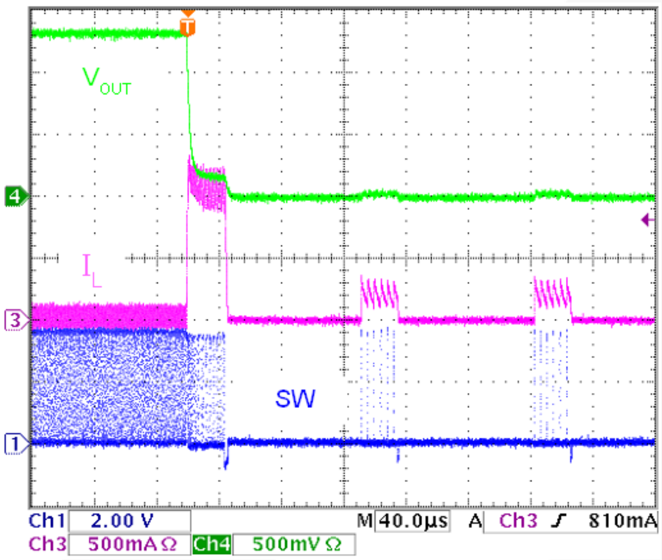


Figure 29. Metallic Short Applied at VOUT

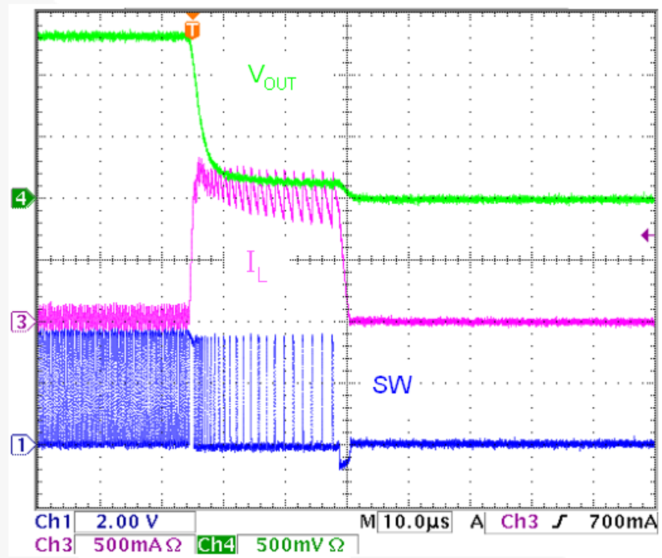


Figure 30. Metallic Short Applied at VOUT

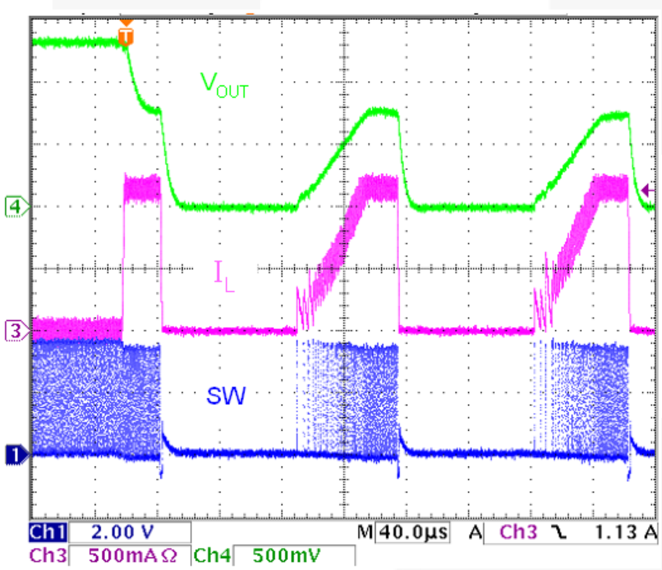


Figure 31. R_{LOAD} = 660 mΩ

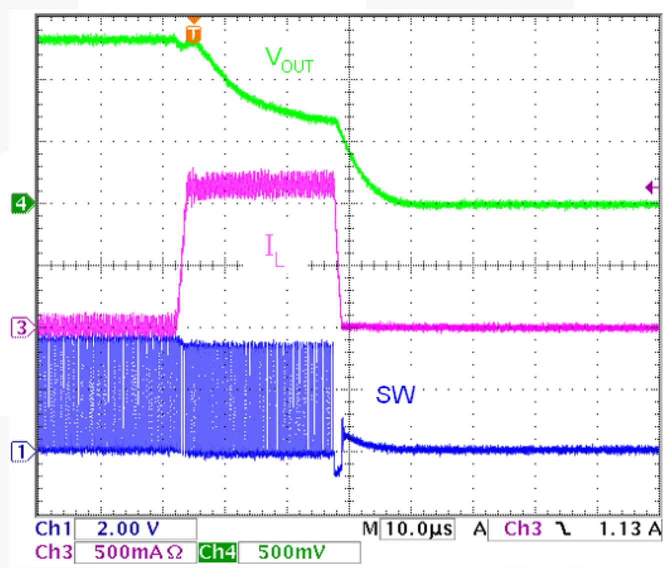


Figure 32. R_{LOAD} = 660 mΩ

Typical Performance Characteristics (Continued)

Unless otherwise specified, V_{IN} = 3.6 V.

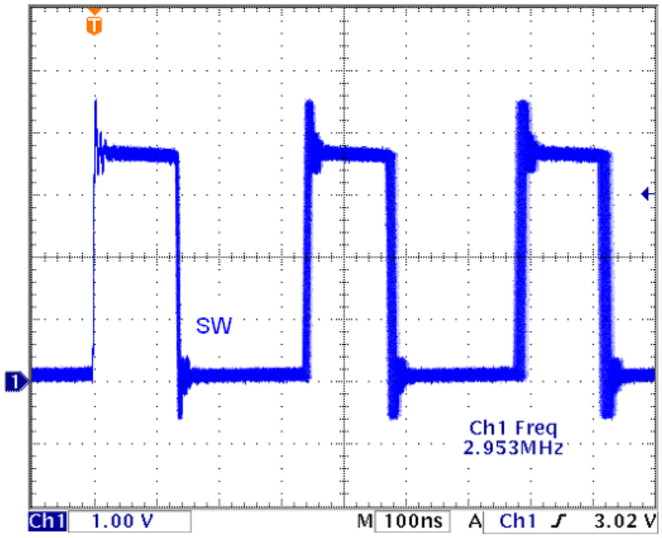


Figure 33. SW-Node Jitter (Infinite Persistence), I_{LOAD} = 200 mA

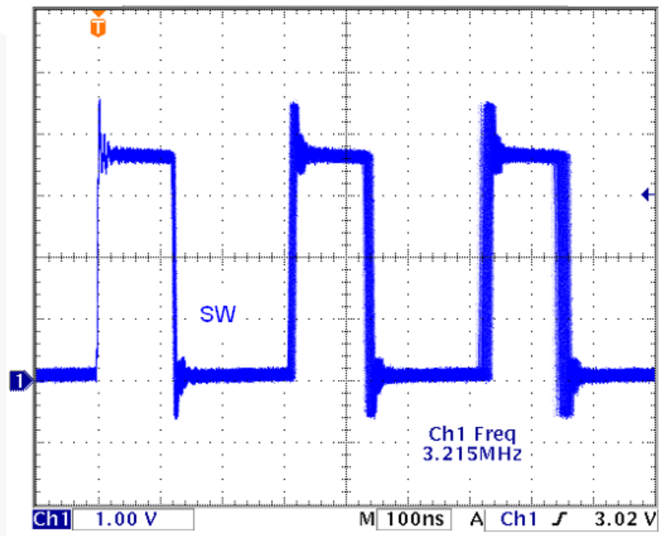


Figure 34. SW-Node Jitter, External Synchronization (Infinite Persistence), I_{LOAD} = 200 mA

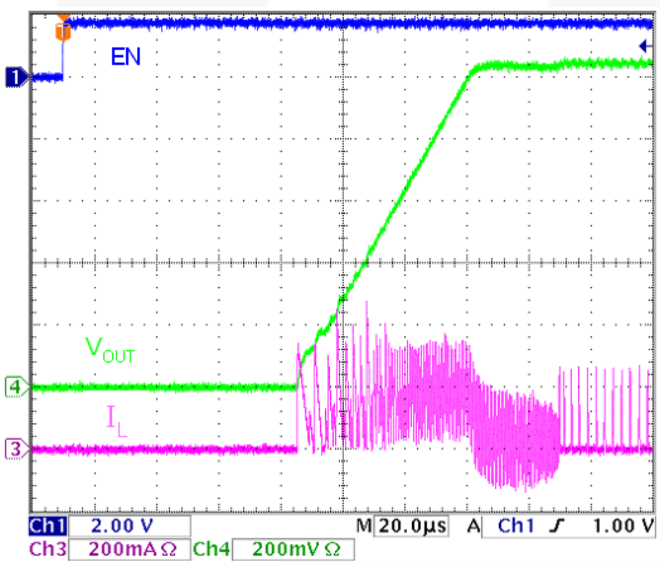


Figure 35. Soft Start, R_{LOAD} = 50 Ω

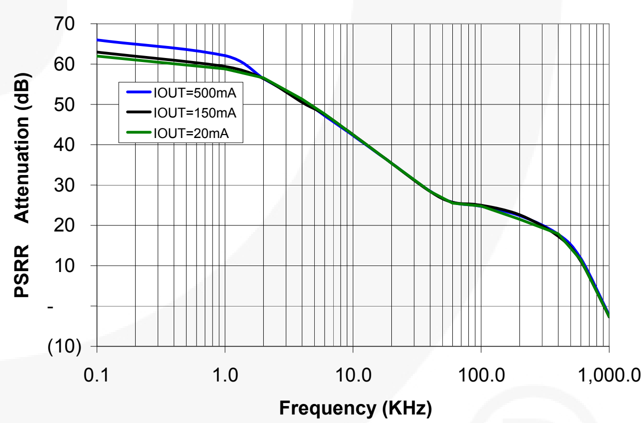


Figure 36. V_{IN} Ripple Rejection (PSRR)

Circuit Description

Overview

The FAN5355 is a synchronous buck regulator that typically operates at 3 MHz with moderate to heavy load currents. At light load currents, the converter operates in power-saving PFM mode. The regulator automatically transitions between fixed-frequency PWM and variable-frequency PFM mode to maintain the highest possible efficiency over the full range of load current.

The FAN5355 uses a very fast non-linear control architecture to achieve excellent transient response with minimum-sized external components.

The FAN5355 integrates an I^2C-compatible interface, allowing transfers up to 3.4 Mbps. This communication interface can be used to:

1. Dynamically re-program the output voltage in 12.5 mV increments.
2. Reprogram the mode of operation to enable or disable PFM mode.
3. Control voltage transition slew rate.
4. Control the frequency of operation by synchronizing to an external clock.
5. Enable / disable the regulator.

For more details, refer to the I^2C Interface and Register Description sections.

Output Voltage Programming

Option[11]	V_{OUT} Equation	
00, 02, 03, 08	$V_{OUT} = 0.75 + N_{VSEL} \bullet 12.5mV$	(1)
06	$V_{OUT} = 1.1875 + N_{VSEL} \bullet 12.5mV$	(2)

where N_{VSEL} is the decimal value of the setting of the VSEL register that controls V_{OUT}.

Note:

11. Option 02 and 08 maximum voltage is 1.4375 V *(see Table 3)*.

Power-Up, EN, and Soft-Start

All internal circuits remain de-biased and the IC is in a very low quiescent-current state until the following are true:

1. V_{IN} is above its rising UVLO threshold, and
2. EN is HIGH.

At that point, the IC begins a soft-start cycle, its I^2C interface is enabled, and its registers are loaded with their default values.

During the initial soft start, V_{OUT} ramps linearly to the set point programmed in the VSEL register selected by the VSEL pin. The soft start features a fixed output-voltage slew rate of 18.75V/ms and achieves regulation approximately 90µs after EN rises. PFM mode is enabled during soft start until the output is in regulation, regardless of the MODE bit settings. This allows the regulator to start into a partially charged output without discharging it; in other words, the regulator does not allow current to flow from the load back to the battery.

As soon as the output has reached its set point, the control forces PWM mode for about 85µs to allow all internal control circuits to calibrate.

Table 2. Soft-Start Timing *(see Figure 37)*

Symbol	Description		Value (µs)
t_{SSDLY}	Time from EN to start of soft-start ramp		75
t_{REG}	V_{OUT} ramp start to regulation	Opt 03, 06	16 +(VSEL–0.7) X 53
		Opt 00, 02, 08	(VSEL–0.1) X 53
t_{POK}	PWROK (CONTROL2[5]) rising from end of t_{REG} and regulator stays in PWM mode during this time		10

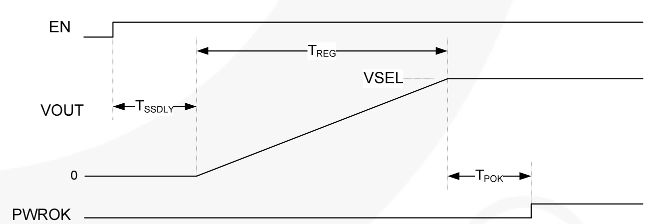


Figure 37. Soft-Start Timing

Table 3. VSEL vs. VOUT

VSEL Value			VOUT		
Dec	Binary	Hex	00, 03	02, 08	06
0	000000	00	0.7500	0.7500	1.1875
1	000001	01	0.7625	0.7625	1.2000
2	000010	02	0.7750	0.7750	1.2125
3	000011	03	0.7875	0.7875	1.2250
4	000100	04	0.8000	0.8000	1.2375
5	000101	05	0.8125	0.8125	1.2500
6	000110	06	0.8250	0.8250	1.2625
7	000111	07	0.8375	0.8375	1.2750
8	001000	08	0.8500	0.8500	1.2875
9	001001	09	0.8625	0.8625	1.3000
10	001010	0A	0.8750	0.8750	1.3125
11	001011	0B	0.8875	0.8875	1.3250
12	001100	0C	0.9000	0.9000	1.3375
13	001101	0D	0.9125	0.9125	1.3500
14	001110	0E	0.9250	0.9250	1.3625
15	001111	0F	0.9375	0.9375	1.3750
16	010000	10	0.9500	0.9500	1.3875
17	010001	11	0.9625	0.9625	1.4000
18	010010	12	0.9750	0.9750	1.4125
19	010011	13	0.9875	0.9875	1.4250
20	010100	14	1.0000	1.0000	1.4375
21	010101	15	1.0125	1.0125	1.4500
22	010110	16	1.0250	1.0250	1.4625
23	010111	17	1.0375	1.0375	1.4750
24	011000	18	1.0500	1.0500	1.4875
25	011001	19	1.0625	1.0625	1.5000
26	011010	1A	1.0750	1.0750	1.5125
27	011011	1B	1.0875	1.0875	1.5250
28	011100	1C	1.1000	1.1000	1.5375
29	011101	1D	1.1125	1.1125	1.5500
30	011110	1E	1.1250	1.1250	1.5625
31	011111	1F	1.1375	1.1375	1.5750
32	100000	20	1.1500	1.1500	1.5875
33	100001	21	1.1625	1.1625	1.6000
34	100010	22	1.1750	1.1750	1.6125
35	100011	23	1.1875	1.1875	1.6250
36	100100	24	1.2000	1.2000	1.6375
37	100101	25	1.2125	1.2125	1.6500
38	100110	26	1.2250	1.2250	1.6625
39	100111	27	1.2375	1.2375	1.6750
40	101000	28	1.2500	1.2500	1.6875
41	101001	29	1.2625	1.2625	1.7000
42	101010	2A	1.2750	1.2750	1.7125
43	101011	2B	1.2875	1.2875	1.7250
44	101100	2C	1.3000	1.3000	1.7375
45	101101	2D	1.3125	1.3125	1.7500
46	101110	2E	1.3250	1.3250	1.7625
47	101111	2F	1.3375	1.3375	1.7750
48	110000	30	1.3500	1.3500	1.7875
49	110001	31	1.3625	1.3625	1.8000
50	110010	32	1.3750	1.3750	1.8125
51	110011	33	1.3875	1.3875	1.8250
52	110100	34	1.4000	1.4000	1.8375
53	110101	35	1.4125	1.4125	1.8500
54	110110	36	1.4250	1.4250	1.8625
55	110111	37	1.4375	1.4375	1.8750
56	111000	38	1.4500	1.4375	1.8875
57	111001	39	1.4625	1.4375	1.9000
58	111010	3A	1.4750	1.4375	1.9125
59	111011	3B	1.4875	1.4375	1.9250
60	111100	3C	1.5000	1.4375	1.9375
61	111101	3D	1.5125	1.4375	1.9500
62	111110	3E	1.5250	1.4375	1.9625
63	111111	3F	1.5375	1.4375	1.9750

Software Enable

The EN_DCDC bit, VSELx[7] can enable the regulator in conjunction with the EN pin. Setting EN_DCDC with EN HIGH begins the soft-start sequence described above.

Table 4. EN_DCDC Behavior

EN_DCDC Bit	EN Pin	I^2C	REGULATOR
0	0	OFF	OFF
1	1	ON	ON
1	0	OFF	OFF
0	1	ON	OFF

Light-Load (PFM) Operation

The FAN5355 offers a low-ripple, single-pulse PFM mode to save power and improve efficiency when the load current is very low. PFM operation features:

- Smooth transitions between PFM and PWM modes
- Single-pulse operation for low ripple
- Predictable PFM entry and exit currents.

PFM begins after the inductor current has become discontinuous, crossing zero during the PWM cycle in 32 consecutive cycles. PFM exit occurs when discontinuous current mode (DCM) operation cannot supply sufficient current to maintain regulation. During PFM mode, the inductor current ripple is about 40% higher than in PWM mode. The load current required to exit PFM mode is thereby about 20% higher than the load current required to enter PFM mode, providing sufficient hysteresis to prevent “mode chatter.”

While PWM ripple voltage is typically less than $4mV_{PP}$, PFM ripple voltage can be up to 30 mV_{PP} during very light load. To prevent significant undershoot when a load transient occurs, the initial DC set point for the regulator in PFM mode is set 10 mV higher than in PWM mode. This offset decays to about 5 mV after the regulator has been in PFM mode for ~100 µs. The maximum instantaneous voltage in PFM is 30 mV above the set point.

PFM mode can be disabled by writing to the mode control bits: CONTROL1[3:0] (*see Table 1 for details*).

Some vendors provide both “Light PFM” (LPFM) and “Fast PFM” (FPFM) modes, while the FAN5355 provides only one PFM mode. The FAN5355’s single PFM mode features the fast transient recovery of FPFM, but does this with the low quiescent current consumption similar to LPFM mode.

Switching-Frequency Control and Synchronization

The nominal internal oscillator frequency is 3 MHz. The regulator runs at its internal clock frequency until these conditions are met:

1. EN_SYNC bit, CONTROL1[5], is set; and
2. A valid frequency appears on the SYNC pin.

Table 5. SYNC Frequency Validation for fOSC(INTERNAL)=3.0 MHz

CONTROL2		f_{SYNC} Valid		
PLL_MULT	f_{SYNC} Divider	Min.	Typ.	Max.
00	1	1.80	3.00	4.00
01	2	0.90	1.50	2.00
10	3	0.60	1.00	1.33
11	4	0.45	0.75	1.00

If the EN_SYNC is set and SYNC fails validation, the regulator continues to run at its internal oscillator frequency. The regulator is functional if f_{SYNC} is valid, as defined in Table 5, but its performance is compromised if f_{SYNC} is outside the f_{SYNC} window in the Electrical Specifications.

When CONTROL1[3:2] = 00 and the VSEL line is LOW, the converter operates according to the MODE0 bit, CONTROL1[0], with synchronization disabled regardless of the state of the EN_SYNC and HW_nSW bits.

Output Voltage Transitions

The IC regulates V_{OUT} to one of two set point voltages, as determined by the VSEL pin and the HW_nSW bit.

Table 6. V_{OUT} Set Point and Mode Control MODE_CTRL, CONTROL1[3:2] = 00

VSEL Pin	HW_nSW Bit	V_{OUT} Set Point	PFM
0	1	VSEL0	Allowed
1	1	VSEL1	Per MODE1
x	0	VSEL1	Per MODE1

If HW_nSW = 0, V_{OUT} transitions are initiated through the following sequence:

1. Write the new setpoint in VSEL1.
2. Write desired transition rate in DEFSLEW, CONTROL2[2:0], and set the GO bit in CONTROL2[7].

If HW_nSW = 1, V_{OUT} transitions are initiated either by changing the state of the VSEL pin or by writing to the VSEL register selected by the VSEL pin.

Positive Transitions

When transitioning to a higher V_{OUT}, the regulator can perform the transition using multi-step or single-step mode.

Multi-Step Mode:

Applies to Options 03 and 06 only.

The internal DAC is stepped at a rate defined by DEFSLEW, CONTROL2[2:0], ranging from 000 to 110. This mode minimizes the current required to charge C_{OUT} and thereby minimizes the current drain from the battery when transitioning. The PWROK bit, CONTROL2[5], remains LOW until about 1.5 µs after the DAC completes its ramp.

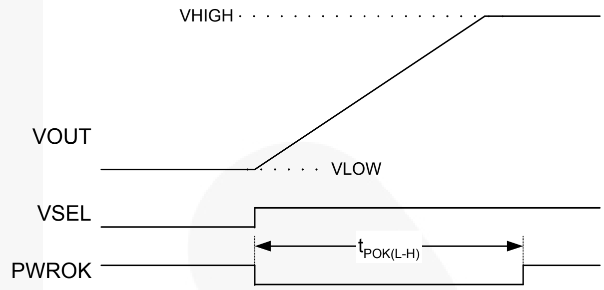


Figure 38. Multi-Step V_{OUT} Transition

Single-Step Mode:

Used if DEFSLEW, CONTROL2[2:0] = 111. The internal DAC is immediately set to the higher voltage and the regulator performs the transition as quickly as its current-limit circuit allows, while avoiding excessive overshoot.

Figure 39 shows single-step transition timing. $t_{V(L-H)}$ is the time it takes the regulator to settle to within 2% of the new set point and is typically 7 µs for a full-range transition (from 000000 to 111111). The PWROK bit, CONTROL2[5], goes LOW until the transition is complete and V_{OUT} settled. This typically occurs ~2 µs after $t_{V(L-H)}$.

It is good practice to reduce the load current before making positive VSEL transitions. This reduces the time required to make positive load transitions and avoids current-limit-induced overshoot.

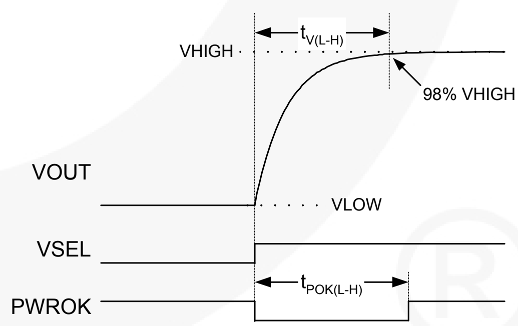


Figure 39. Single-Step V_{OUT} Transition

All positive V_{OUT} transitions inhibit PFM until the transition is complete, which occurs at the end of $t_{POK(L-H)}$.

Negative Transitions

When moving from VSEL=1 to VSEL=0, the regulator enters PFM mode, regardless of the condition of the SYNC pin or MODE bits, and remains in PFM until the transition is completed. Reverse current through the inductor is blocked, and the PFM minimum frequency control inhibited, until the new set point is reached, at which time the regulator resumes control using the mode established by MODE_CTRL. The transition time from V_{HIGH} to V_{LOW} is controlled by the load current and output capacitance as:

$$t_{V(H-L)} = C_{OUT} \bullet \frac{V_{HIGH} - V_{LOW}}{I_{LOAD}} \quad (3)$$

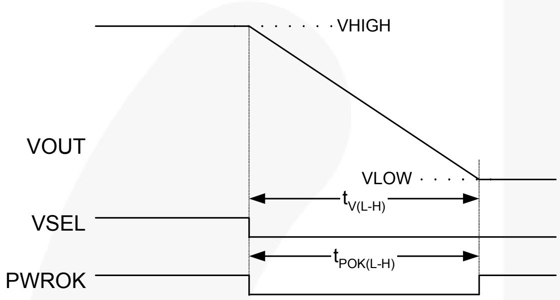


Figure 40. Negative V_{OUT} Transition

Protection Features

Current Limit / Auto-Restart

The regulator includes cycle-by-cycle current limiting, which prevents the instantaneous inductor current from exceeding the current-limit threshold.

The IC enters "fault" mode after sustained over-current. If current limit is asserted for more than 32 consecutive cycles (about 20 µs), the IC returns to shut-down state and remains in that condition for ~80 µs. After that time, the regulator attempts to restart with a normal soft-start cycle. If the fault has not cleared, it shuts down ~10 µs later.

If the fault is a short circuit, the initial current limit is ~30% of the normal current limit, which produces a very small drain on the system power source.

Thermal Protection

When the junction temperature of the IC exceeds 150°C, the device turns off all output MOSFETs and remains in a low quiescent-current state until the die cools to 130°C before commencing a normal soft-start cycle.

Under-Voltage Lockout (UVLO)

The IC turns off all MOSFETs and remains in a very low quiescent-current state until V_{IN} rises above the UVLO threshold.

I²C Interface

The FAN5355's serial interface is compatible with standard, fast, and HS mode I²C bus specifications. The FAN5355's SCL line is an input and its SDA line is a bi-directional open-drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

SDA and SCL are normally pulled up to a system I/O power supply (VCCIO), as shown in Figure 1. If the I²C interface is not used, SDA and SCL should be tied to AVIN to minimize quiescent current consumption.

Addressing

FAN5355 has four user-accessible registers:

Table 7. I²C Register Addresses

	Address							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VSEL0	0	0	0	0	0	0	0	0
VSEL1	0	0	0	0	0	0	0	1
CONTROL1	0	0	0	0	0	0	1	0
CONTROL2	0	0	0	0	0	0	1	1

Slave Address

In Table 8, A1 and A0 are according to the Ordering Information table on page 2.

Table 8. I²C Slave Address

7	6	5	4	3	2	1	0
1	0	0	1	0	A1	A0	R/$\overline{W}$

Bus Timing

As shown in Figure 41, data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow ample time for the data to set up before the next SCL rising edge.

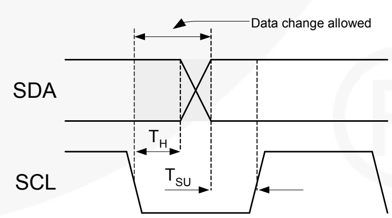


Figure 41. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a "START" condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 42.

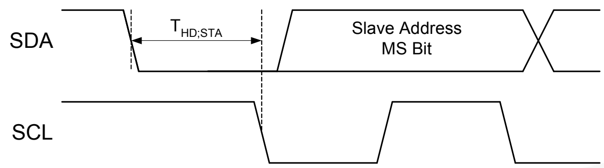


Figure 42. Start Bit

A transaction ends with a “STOP” condition, which is defined as SDA transitioning from 0 to 1 with SCL HIGH, as shown in Figure 43.

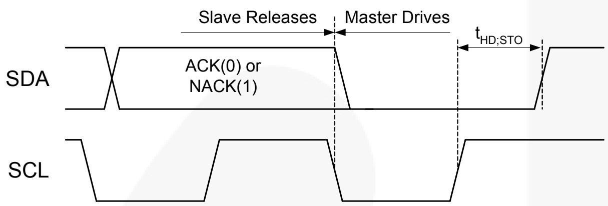


Figure 43. Stop Bit

During a read from the FAN5355 (Figure 46), the master issues a “Repeated Start” after sending the register address and before resending the slave address. The “Repeated Start” is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 44.

High-Speed (HS) Mode

The protocols for High-Speed (HS), Low-Speed (LS), and Fast-Speed (FS) modes are identical, except the bus speed for HS mode is 3.4 MHz. HS mode is entered when the bus master sends the HS master code 00001XXX after a start condition. The master code is sent in FS mode (less than 400 KHz clock) and slaves do not ACK this transmission.

The master then generates a repeated-start condition (Figure 44) that causes all slaves on the bus to switch to HS mode. The master then sends I²C packets, as described above, using the HS-mode clock rate and timing.

The bus remains in HS mode until a stop bit (Figure 43) is sent by the master. While in HS mode, packets are separated by repeated-start conditions (Figure 44).

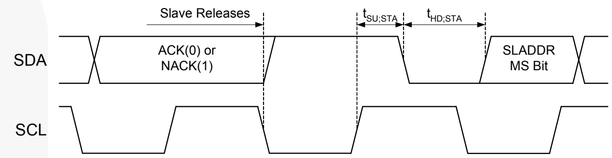


Figure 44. Repeated-Start Timing

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Drives Bus.

All addresses and data are MSB first.

Table 9. I²C Bit Definitions for Figure 45 - Figure 46

Symbol	Definition
S	START, *see Figure 42*.
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.
R	Repeated START, *see Figure 44*.
P	STOP, *see Figure 43*.

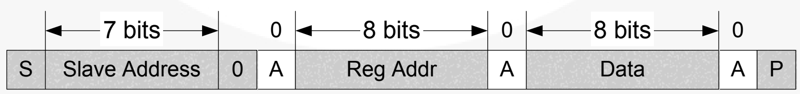


Figure 45. Write Transaction

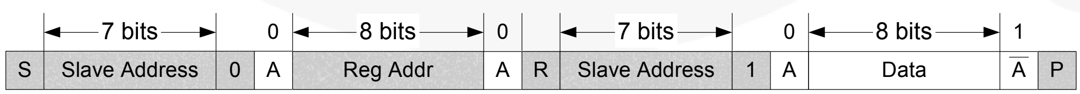


Figure 46. Read Transaction

Register Descriptions

Default Values

Each option of the FAN5355 *(see Ordering Information on page 2)* has different default values for the some of the register bits. Table 10 defines both the default values and the bit's type (as defined in Table 11) for each available option.

Table 10. Default Values and Bit Types for VSEL and CONTROL Registers

VSEL0

Option	7	6	5	4	3	2	1	0	V_{OUT}
00	1	1	0	1	1	0	0	0	1.05
02	1	1	0	1	1	0	0	0	1.05
03	1	1	0	1	0	1	0	0	1.00
06	1	1	1	1	0	0	0	1	1.80
08	1	1	0	1	1	0	0	0	1.05

VSEL1

Option	7	6	5	4	3	2	1	0	V_{OUT}
00	1	1	1	1	0	0	0	0	1.35
02	1	1	1	0	0	1	0	0	1.20
03	1	1	1	0	0	1	0	0	1.20
06	1	1	1	1	0	0	0	1	1.80
08	1	1	1	0	0	1	0	0	1.20

CONTROL1

Option	7	6	5	4	3	2	1	0
00, 02, 08	1	0	0	1	0	0	0	0
03, 06	1	0	0	1	0	0	0	0

CONTROL2

Option	7	6	5	4	3	2	1	0
00, 02, 08	0	0	1	0	0	1	1	1
03, 06	0	0	1	0	0	1	1	1

Table 11. Bit-Type Definitions for Table 10

#	**Active bit.**	Changing this bit changes the behavior of the converter, as described below.
#	**Disabled.**	Converter logic ignores changes made to this bit. Bit can be written to and read-back.
#	**Read-only**.	Writing to this bit through I^2C does not change the read-back value, nor does it change converter behavior.

Bit Definitions

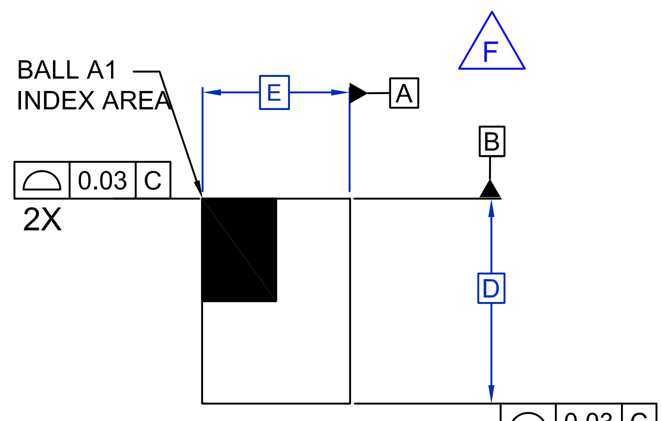
The following table defines the operation of each register bit. Superscript characters define the default state for each option. Superscripts [0,2,3,6,8] signify the default values for options 00, 02, 03, 06, and 08 respectively. [A] signifies the default for all options.

Bit	Name	Value	Description
VSEL0			**Register Address: 00**
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL1. A write to bit 7 in either register establishes the EN_DCDC value.
		1[A]	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved	1	
5:0	DAC[5:0]	*Table 10*	6-bit DAC value to set V_{OUT}.
VSEL1			**Register Address: 01**
7	EN_DCDC	0	Device in shutdown regardless of the state of the EN pin. This bit is mirrored in VSEL0. A write to bit 7 in either register establishes the EN_DCDC value.
		1[A]	Device enabled when EN pin is HIGH, disabled when EN is LOW.
6	Reserved	1	
5:0	DAC[5:0]	*Table 10*	6-bit DAC value to set V_{OUT}.
CONTROL1			**Register Address: 02**
7:6	Reserved	10 [A]	Vendor ID bits. Writing to these bits has no effect on regulator operation. These bits can be used to distinguish between vendors via I^2C.
5	EN_SYNC	0[A]	Disables external signal on SYNC from affecting the regulator.
		1	When a valid frequency is detected on SYNC, the regulator synchronizes to it and PFM is disabled, except when MODE = 00, VSEL pin = LOW, and HW_nSW = 1.
4	HW_nSW	0	V_{OUT} is controlled by VSEL1. Voltage transitions occur by writing to the VSEL1, then setting the GO bit.
		1[A]	V_{OUT} is programmed by the VSEL pin. V_{OUT} = VSEL1 when VSEL is HIGH, and VSEL0 when VSEL is LOW.
3:2	MODE_CTRL	00[A]	Operation follows MODE0, MODE1.
		01	PFM with automatic transitions to PWM, regardless of VSEL.
		10	PFM disabled (forced PWM), regardless of VSEL.
		11	Unused.
1	MODE1	0[A]	PFM disabled (forced PWM) when regulator output is controlled by VSEL1.
		1	PFM with automatic transitions to PWM when regulator output is controlled by VSEL1.
0	MODE0	0[A]	PFM with automatic transitions to PWM when VSEL is LOW. Changing this bit has no effect on the operation of the regulator.
		1	
CONTROL2			**Register Address: 03**
7	GO	0[A]	This bit has no effect when HW_nSW = 1.
		1	Starts a V_{OUT} transition if HW_nSW = 0. This bit must be written by the external master to 1 for the next V_{OUT} transition to start, even if its value might have already been 1 from the last V_{OUT} transition.
6	OUTPUT_ DISCHARGE	0[A]	When the regulator is disabled, V_{OUT} is not discharged.
		1	When the regulator is disabled, V_{OUT} discharges through an internal pull down.
5	PWROK (read only)	0	V_{OUT} is not in regulation or is in current limit.
		1	V_{OUT} is in regulation.
4:3	PLL_MULT	00[A]	$f_{SW} = f_{SYNC}$ when synchronization is enabled.
		01	f_{SW} = 2 X f_{SYNC} when synchronization is enabled.
		10	f_{SW} = 3 X f_{SYNC} when synchronization is enabled.
		11	f_{SW} = 4 X f_{SYNC} when synchronization is enabled.
2:0	DEFSLEW	000	V_{OUT} slews at 0.15 mV/µs during positive V_{OUT} transitions.
		001	V_{OUT} slews at 0.30 mV/µs during positive V_{OUT} transitions.
		010	V_{OUT} slews at 0.60 mV/µs during positive V_{OUT} transitions.
		011	V_{OUT} slews at 1.20 mV/µs during positive V_{OUT} transitions.
		100	V_{OUT} slews at 2.40 mV/µs during positive V_{OUT} transitions.
		101	V_{OUT} slews at 4.80 mV/µs during positive V_{OUT} transitions.
		110	V_{OUT} slews at 9.60 mV/µs during positive V_{OUT} transitions.
		111[A]	Positive V_{OUT} transitions use single-step mode *(see Figure 39)*.

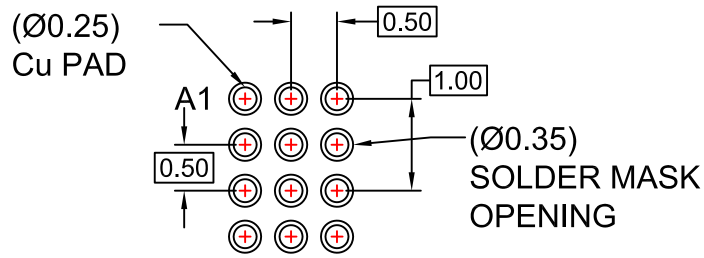
The table below pertains to the Marketing outline drawing on the following page.

Product-Specific Dimensions

Product	D	E	X	Y
FAN5355UC	2.200 ±0.030	1.430 ±0.030	0.220	0.355

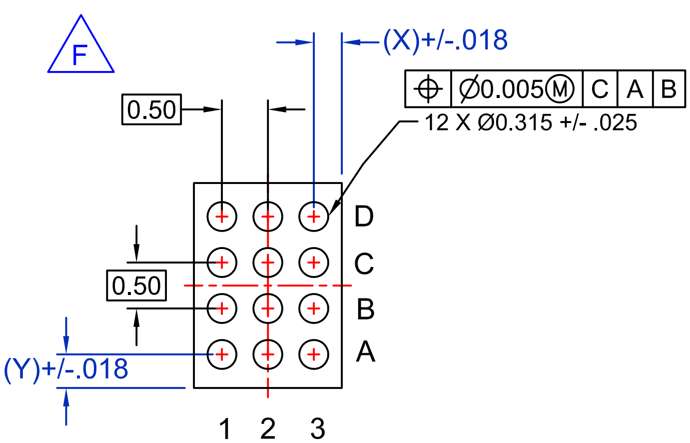


TOP VIEW



RECOMMENDED LAND PATTERN (NSMD)

SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE TYPICAL HEIGHT IS 582 MICRONS ± 38 MICRONS (539-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012AArev2

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