FEBFAN6248HA_CP21U240

FAN6248 Evaluation Board User's Manuals

240 W Power supply with Synchronous Rectification for LLC Resonant Converter

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EVAL BOARD USER'S MANUAL

Overview

The presented design demonstrates high power density DC-DC power supply with high efficiency through load variation. The design utilizes NCP1399AA for the primary side controller, and FAN6248 for the secondary side synchronous rectification (SR) controller.

The NCP1399 is a current mode controller for half bridge resonant converter featuring 600 V gate drivers, high-frequency operation from 20kHz up to 750kHz, automatic dead−time with maximum dead−time clamp, and skip mode operation for improved light load efficiency. The secondary side controller FAN6248 is an advanced synchronous rectifier controller that is optimized for LLC resonant converter topology with minimum external components. It has two driver stages for driving the SR MOSFETs which are rectifying the output current of the secondary transformer. These two gate driver stages have dedicated sense inputs and operate independently each other. The adaptive dead time control function compensates parasitic inductance offset voltage and minimizes the body diode conduction and maximize the efficiency. The advanced control algorithm allows stable SR operation over entire load range.

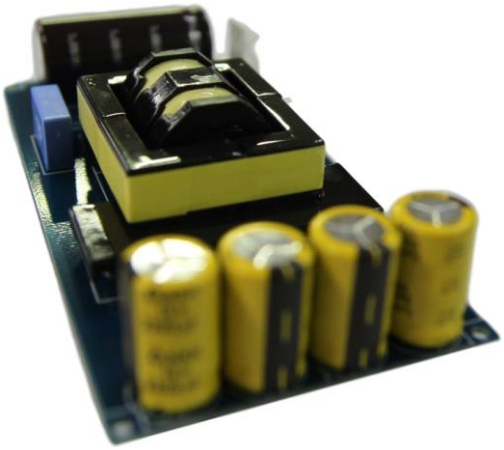

Figure 1. Evaluation Board Photo

Features

- Highly integrated self-contained control of synchronous rectifier with a minimum external component count
- Optimized for LLC resonant converter
- Anti shoot-through control for reliable SR operation
- Separate 100V rated sense inputs for sensing the drain and source voltage of each SR MOSFET
- Adaptive parasitic inductance compensation to minimize the body diode conduction
- SR current inversion detection under light load condition
- Light load detection for preventing inversion current
- Adaptive minimum on time for noise immunity
- Operating voltage range up to 30 V
- Low start-up and stand-by current consumption
- Operating frequency range from 25kHz up to 700 kHz
- SOIC−8 Package
- High driver output voltage of 10.5 V to drive all MOSFET brands to the lowest R_{DS_ON}
- Low operating current in green mode (typ. 350μA)

Circuit Description

Table I shows general information of the evaluation board (EVB). In the primary side, LLC topology provides a high efficiency and high power density by zero voltage switching (ZVS) of half-bridge MOSFETs. The power stage operates in below resonance area at around the resonant frequency between a resonant capacitor Cr and a resonance inductor Lr. Thereofore, it can provide high efficiency with less frequency variation for light load condition. In addition, zero current switching (ZCS) of secondary rectifiers removes its reverse recovery problem and reduces drain voltage spike of the SR MOSFET.

As shown in Figure 2, the EVB is implemented with LLC stage only and PFC stage is excluded. This evaluation board can be divided into a square wave generator, a resonant tank, and output rectifier. The square wave generator produces square wave voltage which has V_{in} of amplitude by driving half-bridge MOSFETs M1 and M2 (FCB20N60) with 50% duty cycle for each switch. The resonant tank consists of a Cr, Lr, and magnetizing inductance Lp of the transformer which is designed by SRX35ER from TDK. The resonant tank filters the higher order harmonic current so that only sinusoidal currents is allowed to flow through the resonant tank. The sinusoidal current Ip lags the voltage applied to the resonant tank, which allows the half-bridge MOSFETs to be turned on with zero voltage. The output rectifier generates DC voltage by rectifying the AC current with SR MOSFETs (FDB9406_F085) controlled by FAN6248. The detailed LLC resonant converter design with NCP1399 is decribed in the NCP1399AIOEVB test report EVBUM2342-D.

In Figure 2, FAN6248 only requires two drain voltage sensing resistor (Roffset1, Roffset2). Then it controls SR MOSFETs M3, M4 based on the instantaneous drain-to-source voltage sensed across DRAIN and SOURCE pins of M3 and M4. If severe noise is induced to drain sensing pin, a filter capacitor can be used.

Table I. GENERAL INFORMATIONS

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	390	VDC
Output Voltage	V_O	12	V
Maximum Output Current	I_{OUTMAX}	20	A
Output Power	P_O	240	W
Operating frequency @ full load condition	f_s	110	kHz
Maximum Efficiency	η	96.9	%
4 points Average Efficiency (100%, 75%, 50%, 25%)	η	95	%
Output voltage ripple I_{OUT} = 20A	V_{OUT_PK-PK}	384	mV
Board Dimension		124 x 58	mm

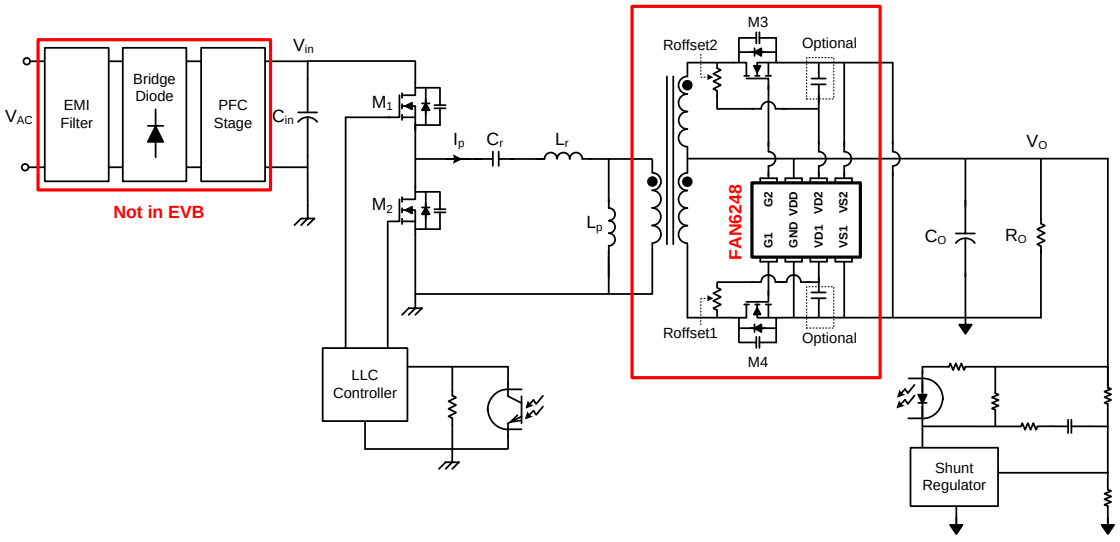

Figure 2. Simplified Application Circuit

Evaluation Board Schematic

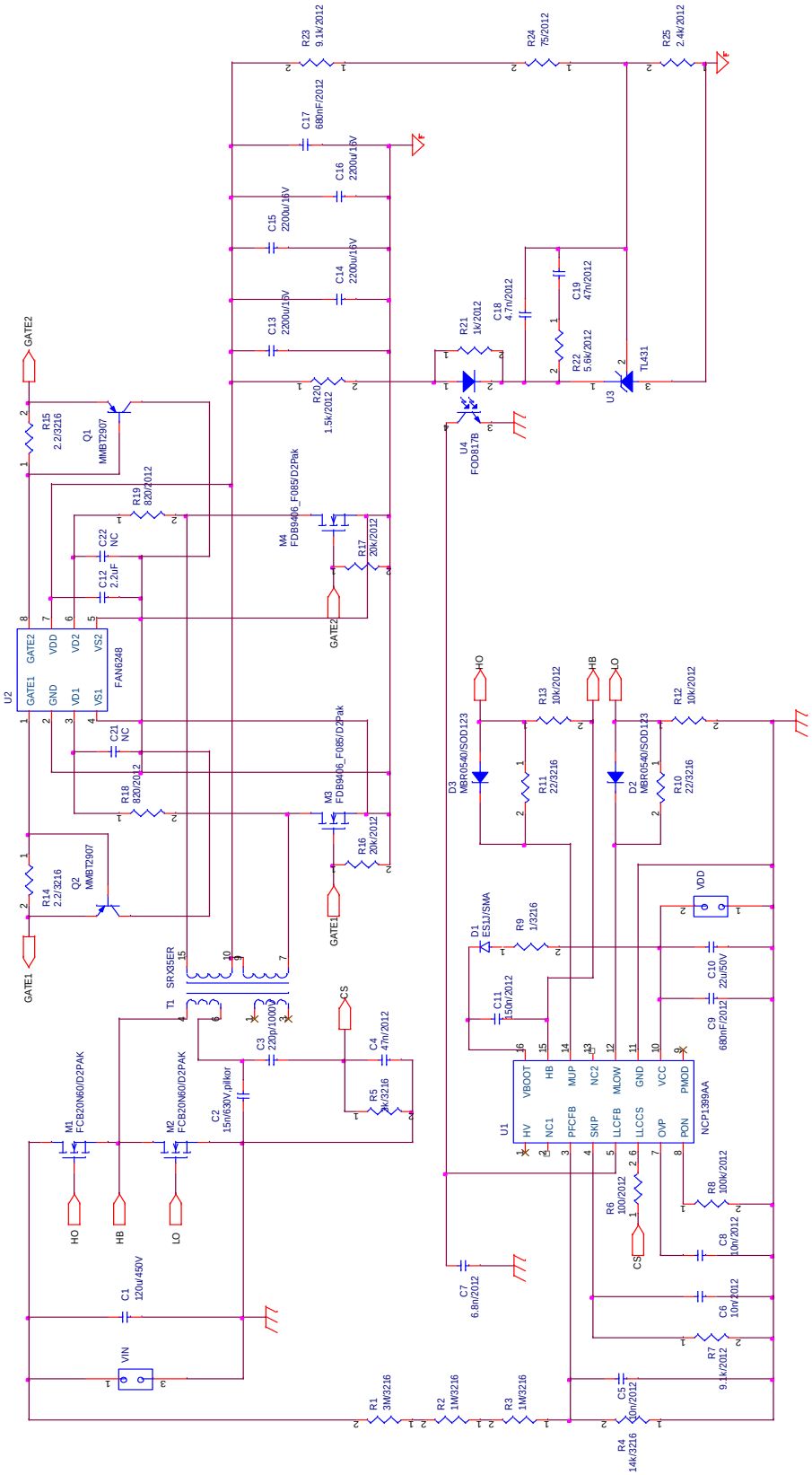

Figure 3. Evaluation Board Schematic

PCB Layout

Board Demension : 124mm x 58 mm

PCB material : FR4

Copper : 2 oz

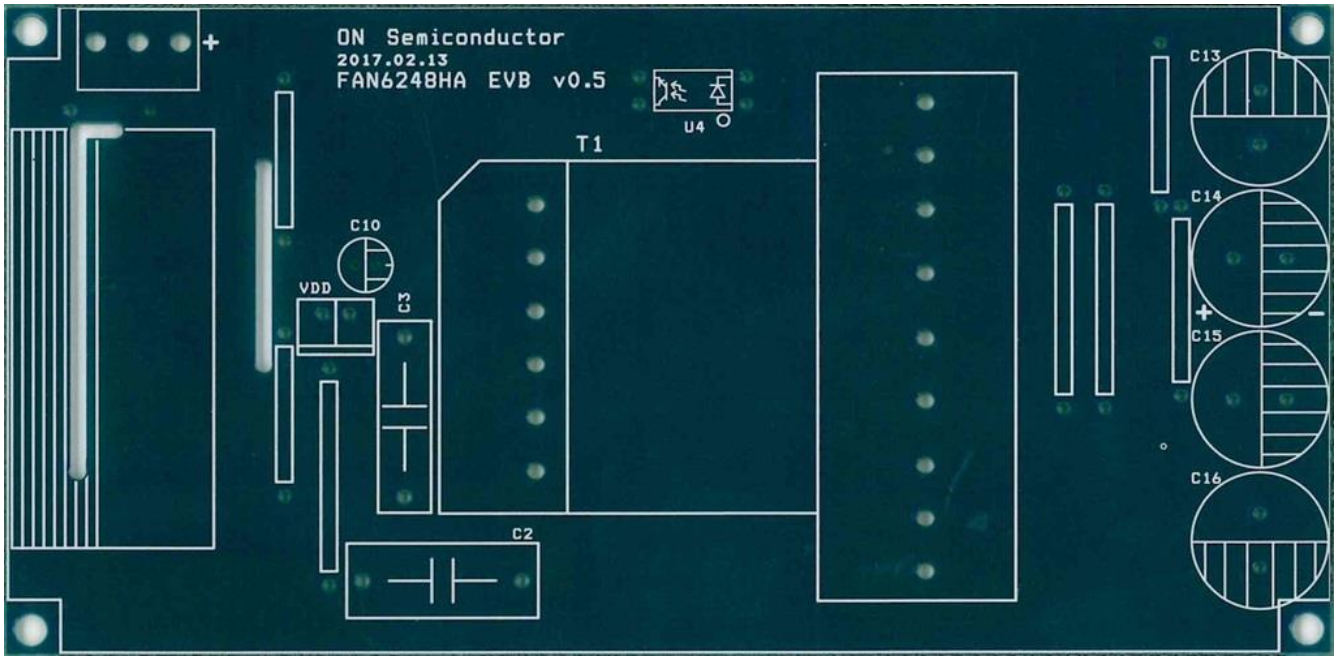

Figure 4. Top side of evaluation board

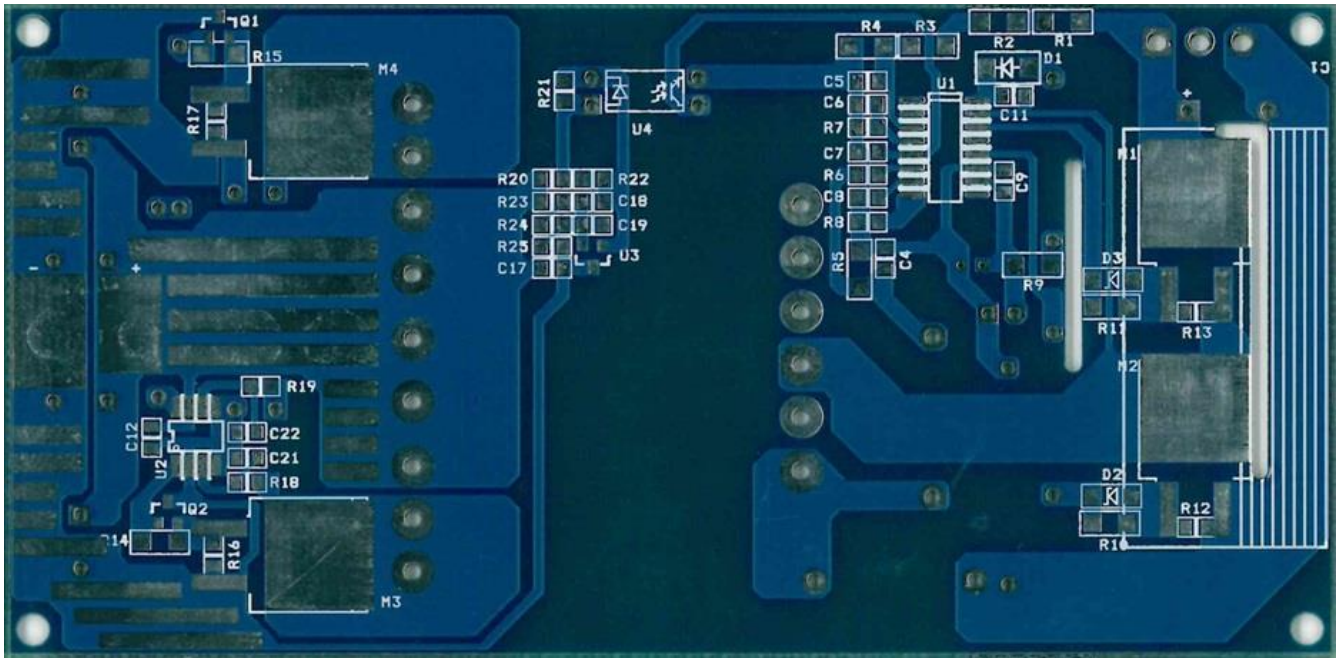

Figure 5. Bottome side of evaluation board

Bill of Materials

Table 2. Bill of materials

Type	Location	Value	Footprint	Manufacturer	P/N
Capacitor	C1	120μF/450V	Through Hole	Samyoung	NFL series
	C10	22μF/50V	Through Hole	Samyoung	KMG series
	C11	150nF	0805	Variable	
	C12	2.2uF	0805	Variable	
	C13,C14,C15,C16	2200μF/16V	Through Hole	Samyoung	NXH series
	C18	4.7nF	0805	Variable	
	C2	15nF/1000V	Through Hole	Pilkor	MMKP series
	C3	220pF/1000V	Through Hole	Pilkor	MMKP series
	C4,C19	47nF	0805	Variable	
	C5,C6,C8	10nF	0805	Variable	
	C7	6.8nF	0805	Variable	
	C9,C17	680nF	0805	Variable	
Resistor	R1	3MΩ	1206	Variable	
	R10,R11	22Ω	1206	Variable	
	R12,R13	10kΩ	0805	Variable	
	R14,R15	2.2Ω	1206	Variable	
	R16,R17	20kΩ	0805	Variable	
	R18,R19	820Ω	0805	Variable	
	R2,R3	1MΩ	1206	Variable	
	R20	1.5kΩ	0805	Variable	
	R21	1kΩ	0805	Variable	
	R22	5.6kΩ	0805	Variable	
	R23	9.1kΩ	0805	Variable	
	R24	75Ω	0805	Variable	
	R25	2.4kΩ	0805	Variable	
	R4	14kΩ	1206	Variable	
	R5	3kΩ	1206	Variable	
	R6	100Ω	0805	Variable	
	R7	9.1kΩ	0805	Variable	
	R8	100kΩ	0805	Variable	
	R9	1Ω	1206	Variable	
Transformer	T1	SRX35ER	EER3037	TDK	SRX35ER-600 TDK K 6Y0112
IC/ Photo coupler	U1	NCP1399	SOIC-16NB	On Semiconductor	NCP1399AA
	U2	FAN6248	SOIC-8NB	On Semiconductor	FAN6248HA
	U3	LM431	SOT-23	On Semiconductor	LM431SCCM3X
	U4	FOD817B	DIP-4	On Semiconductor	FOD817B
Connector	CON1	3PIN			Yeonho
	CON2	2PIN			Yeonho
Diode	D1	ES1J	SMA	On Semiconductor	ES1J
	D2,D3,D4,D5	MBR0540	SOD-123	On Semiconductor	MBR0540
MOSFET	M1,M2	FCB20N60	D2PAK	On Semiconductor	FCB20N60
	M3,M4	FDB9406_F085	D2PAK	On Semiconductor	FDB9406_F085
Trnasistor	Q1	MMBT2907	SOT-23	On Semiconductor	MMBT2907
	Q2	MMBT2907	SOT-23	On Semiconductor	MMBT2907

Transformer specification

SRX35ER Core which has 97mm^2 of effective area is utilized for LLC transformer. For the optimal design of the resonant trank, 600 μH of L_p and 100 μH of resonant inductance L_r are designed, respectively. For reference design, TDK SRX35ER-600 TDK K 6Y0112 is utilized.

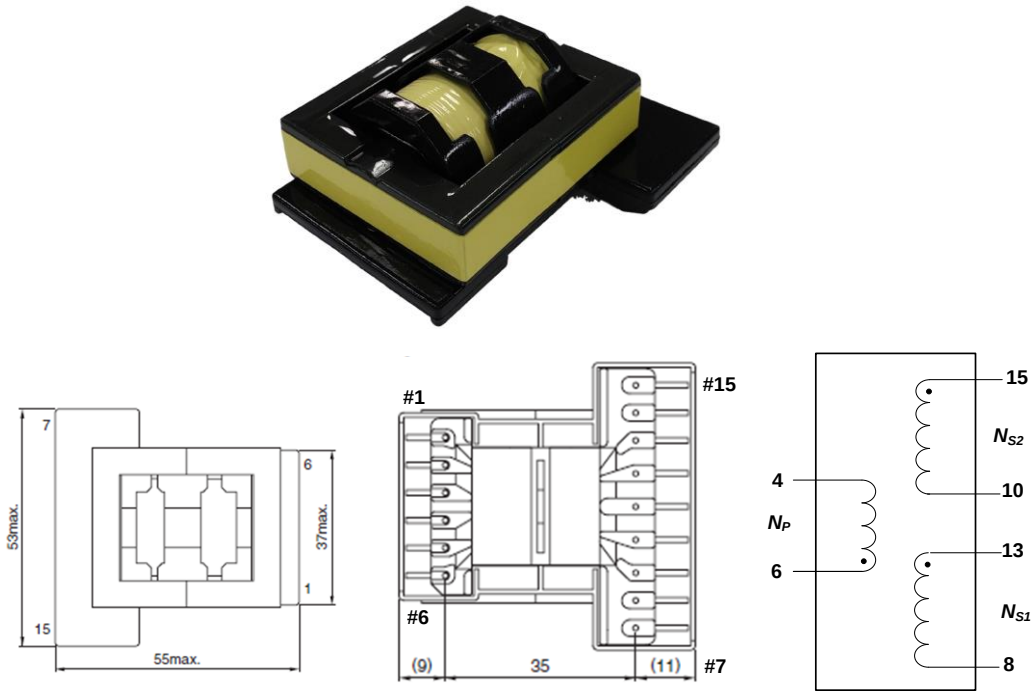

Figure 6. Transformer dimension and shapes

Table 3. Transformer widing method

	Pin (Start → Finish)	Wire	Turns	Winding Method
N_p	6 → 4	0.1φ×50 USTC	37	Solenoid winding
Insulation : Polyester Tape t = 0.025mm, 2Layers				
N_s	15→10 13→8	0.10φ×75 USTC	2	Bifilar
Insulation : Polyester Tape t = 0.025mm, 2Layers				
N_s	14→9 12→7	0.10φ×75 USTC	2	Bifilar
Insulation : Polyester Tape t = 0.025mm, 2Layers				
N_s	15→10 13→8	0.10φ×75 USTC	2	Bifilar
Insulation : Polyester Tape t = 0.025mm, 2Layers				
N_s	14→9 12→7	0.10φ×75 USTC	2	Bifilar
Insulation : Polyester Tape t = 0.025mm, 2Layers				

Design parameters : L_p=600 μH, L_r=100μH at f=100kHz

Efficiency

The efficiency of FAN6248 is compared with ‘A’ LLC SR product.

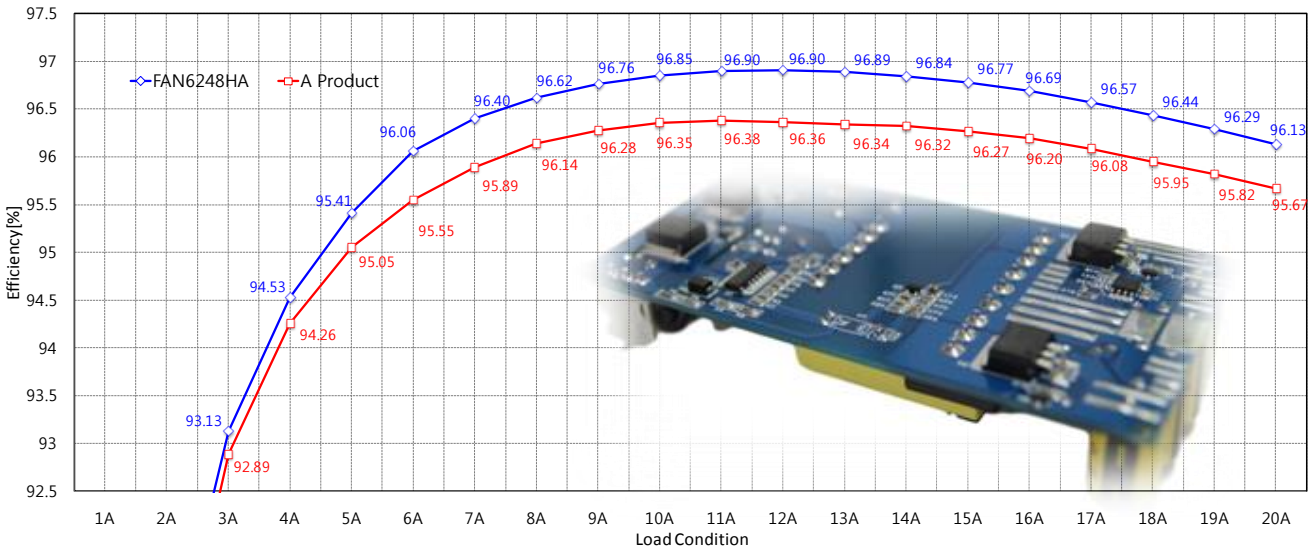

Figure 7. Efficiency for load variation

Load Regulation

Load regulation is measured to 38mV at load variation from 0A to 20A.

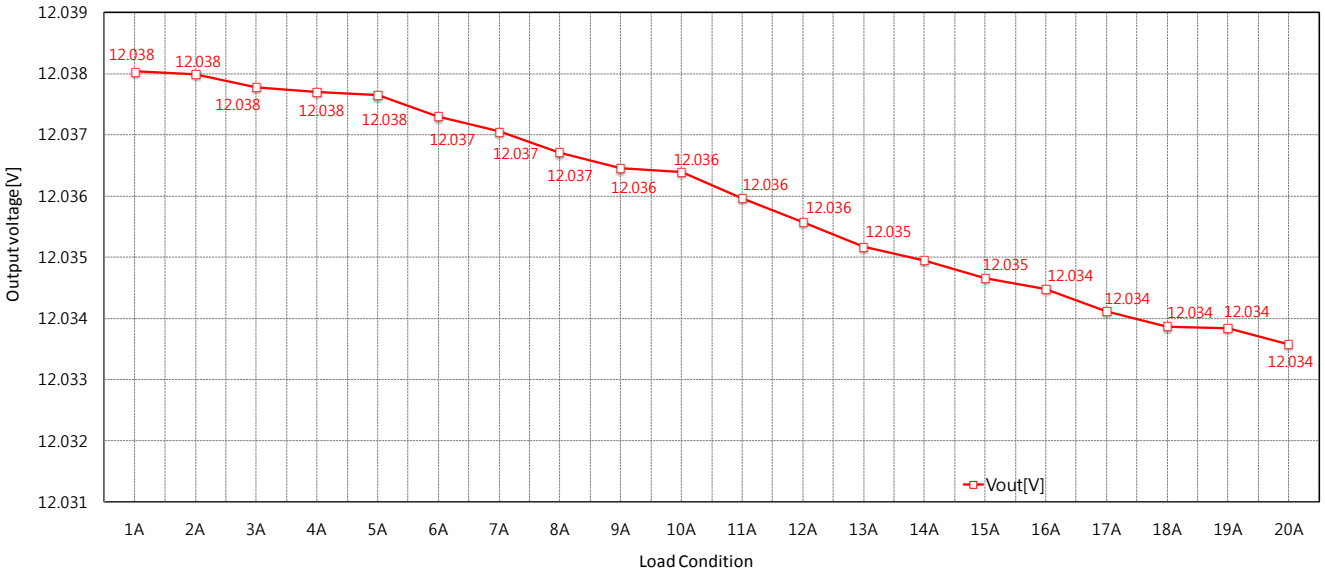

Figure 8. Load Regulation is 1.9mV/A

Syschronous rectification control and normal operation

FAN6248 controls the SR MOSFET based on the instantaneous drain-to-source voltage sensed across DRAIN and SOURCE pins. Before SR gate is turned on, SR body diode conducts as the conventional diode rectifier. Once the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold voltage V_{TH_ON} which triggers the turn-on of the SR gate. Then the drain-to-source voltage is determined by the product of turn-on resistance R_{ds_on} of SR MOSFET and instantaneous SR current. When the drain-to-source voltage reaches the turn-off threshold voltage V_{TH_OFF} as SR MOSFET current decreases to near zero, FAN6248 turns off the gate. If a SR dead time is larger or smaller than the dead time regulation target t_{DEAD}, FAN6248 adaptively changes internal offset voltage to compensate the dead time. In addition, to prevent cross conduction SR operation, FAN6248 has 200ns of turn-on blaking time just after alternating SR gate is turned off.

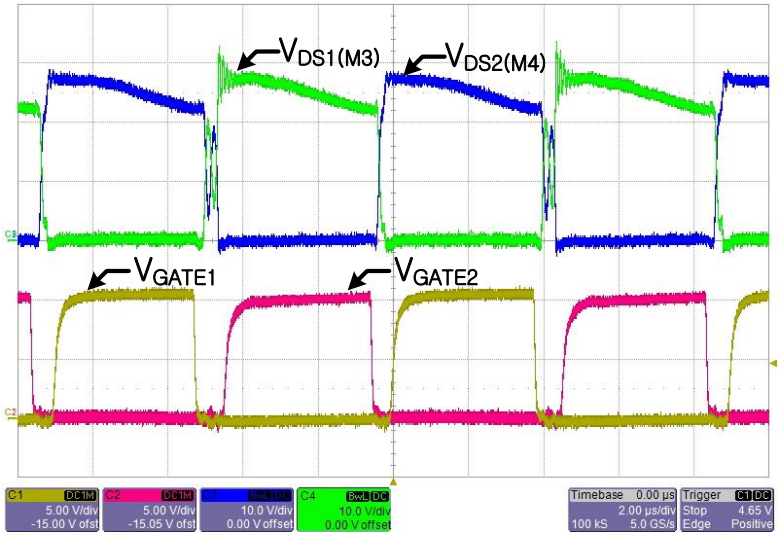

Figure 9. V_{IN}=390V_{DC}, I_{OUT} = 20A Full load, Waveform of SR Gate and Drain voltage

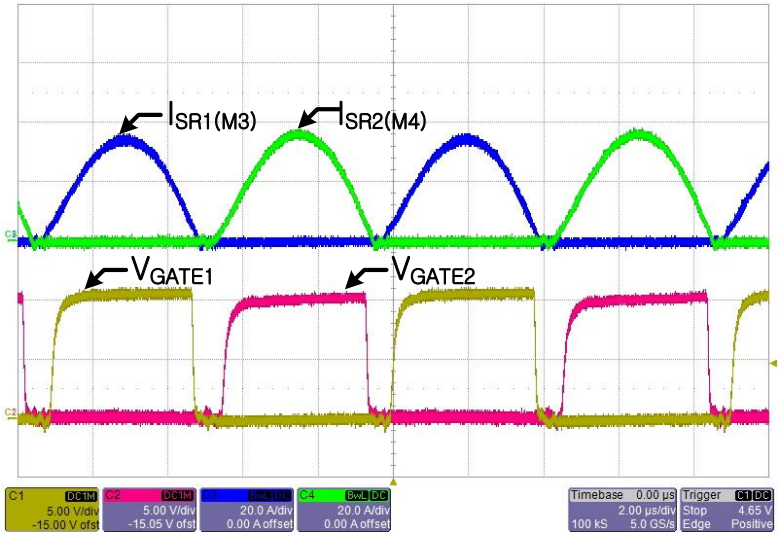

Figure 10. V_{IN}=390V_{DC}, I_{OUT} = 20A Full load, Waveform of SR Gate voltage and Drain current

Output Voltage Ripple

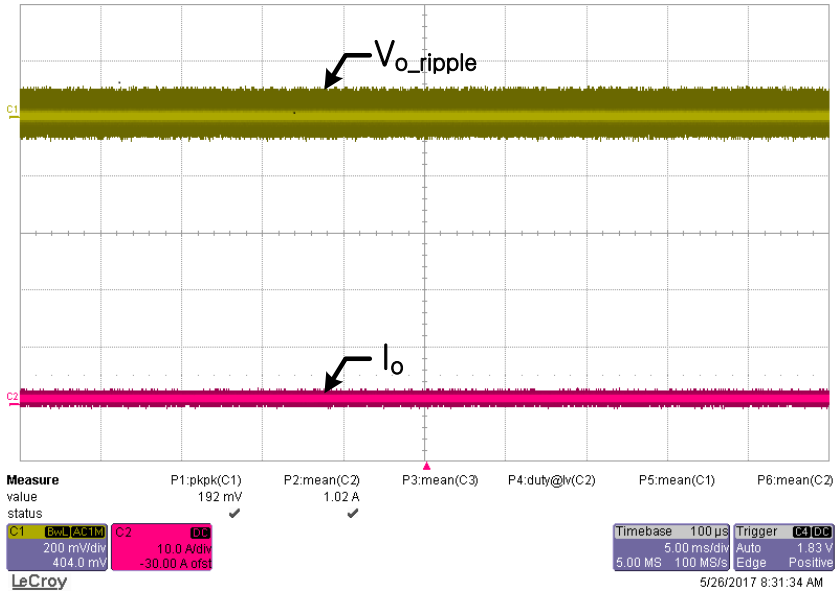

Figure 11. V_{IN}=390V_{DC}, I_{OUT} = 1A, $\Delta V_{OUTPK-PK}$ = 192 mV

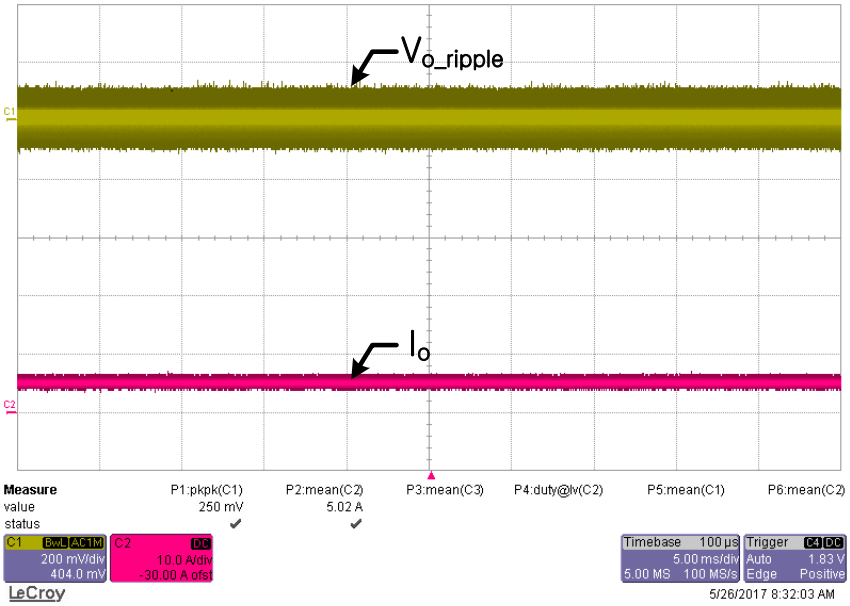

Figure 12. V_{IN}=390V_{DC}, I_{OUT} = 5A, $\Delta V_{OUTPK-PK}$ = 250 mV

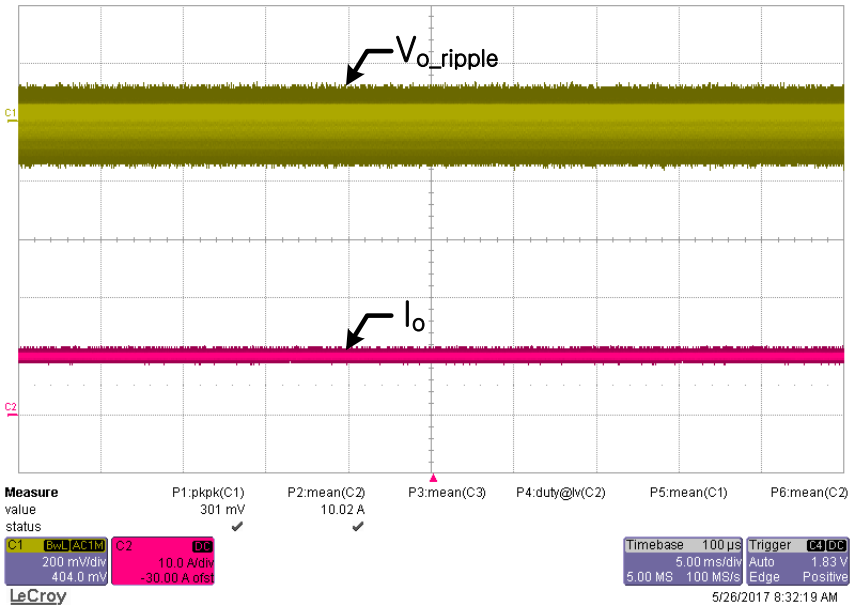

Figure 13. V_{IN}=390V_{DC}, I_{OUT} = 10A, $\Delta V_{OUTPK-PK}$ = 301 mV

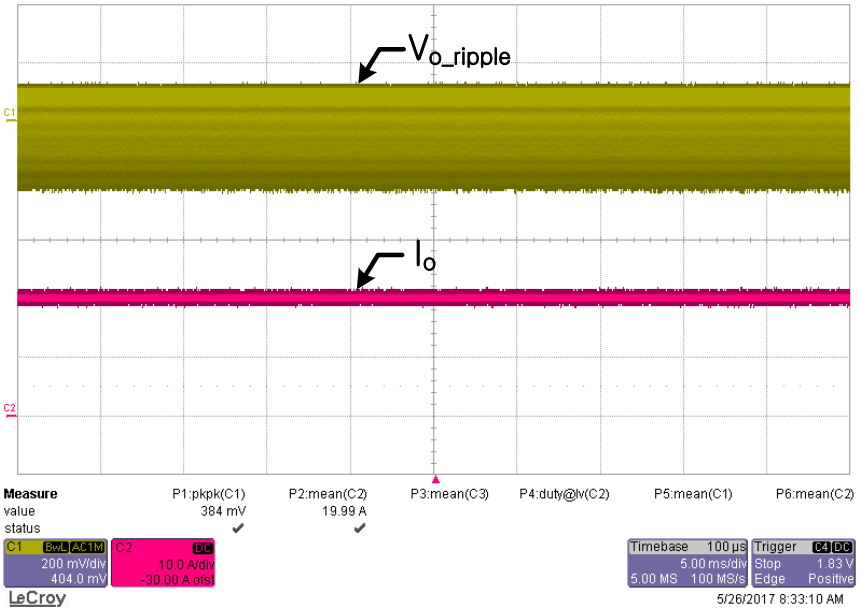

Figure 14. V_{IN}=390V_{DC}, I_{OUT} = 20A Full load, $\Delta V_{OUTPK-PK}$ = 384 mV

Start up

When V_{DD} is higher than V_{DD_ON}, FAN6248 outputs gate signals. If the sensed drain voltage cannot meet turn-on condition, SR operation may be delayed after V_{DD_ON}.

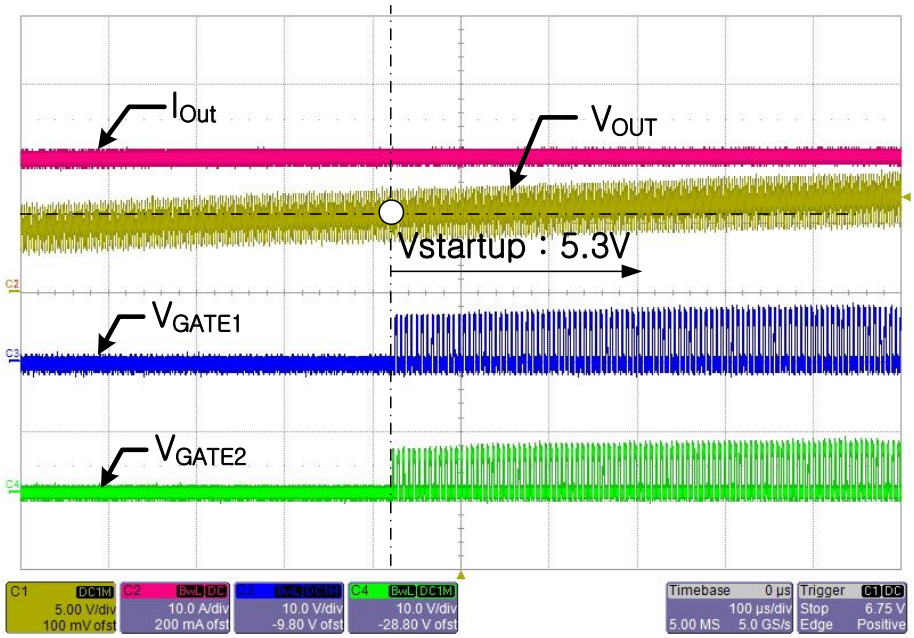

Figure 15. V_{IN}=390V_{DC}, I_{OUT} = 20A Full load

Power off

When input power source is disconnected, FAN6248 can be disabled by no-signal of drain sensing voltage.

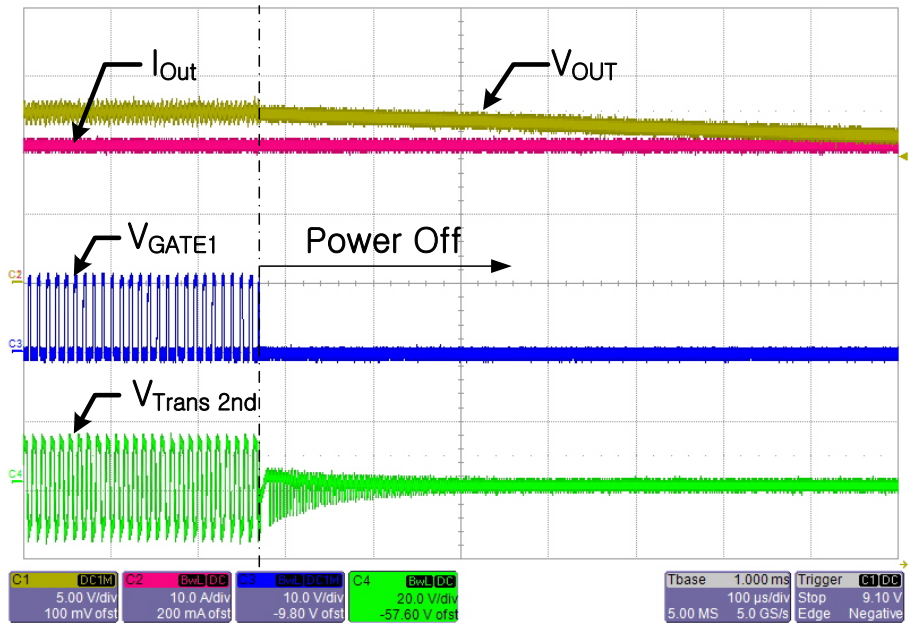

Figure 16. V_{IN}=390V_{DC}, I_{OUT} = 20A Full load

Output current transients response

Current slew rate is 5mA/1μs

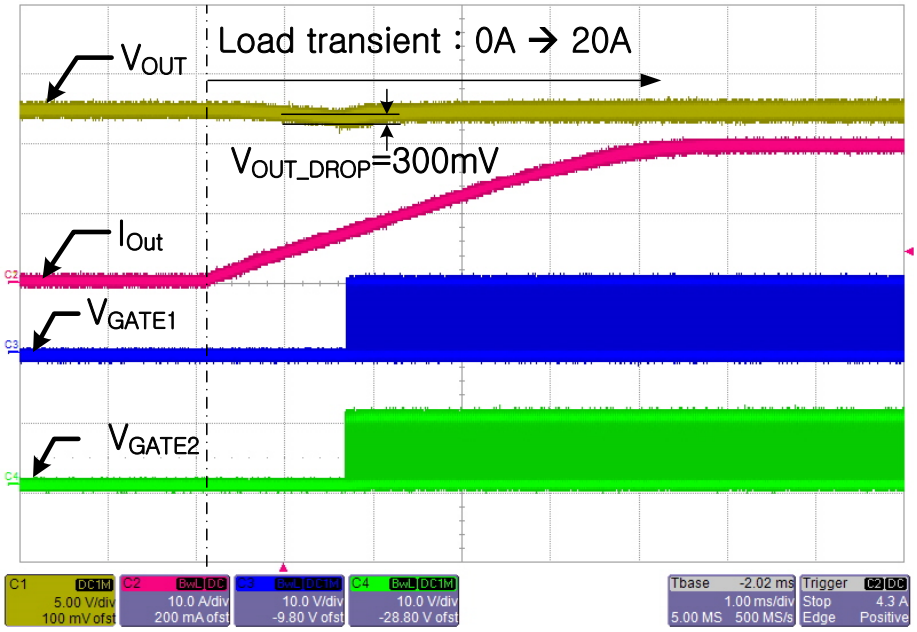

Figure 17. V_{IN}=390V_{DC}, I_{OUT} = 0-20A, V_{OUT_DROP}=300 mV

Current slew rate is 20mA/1μs

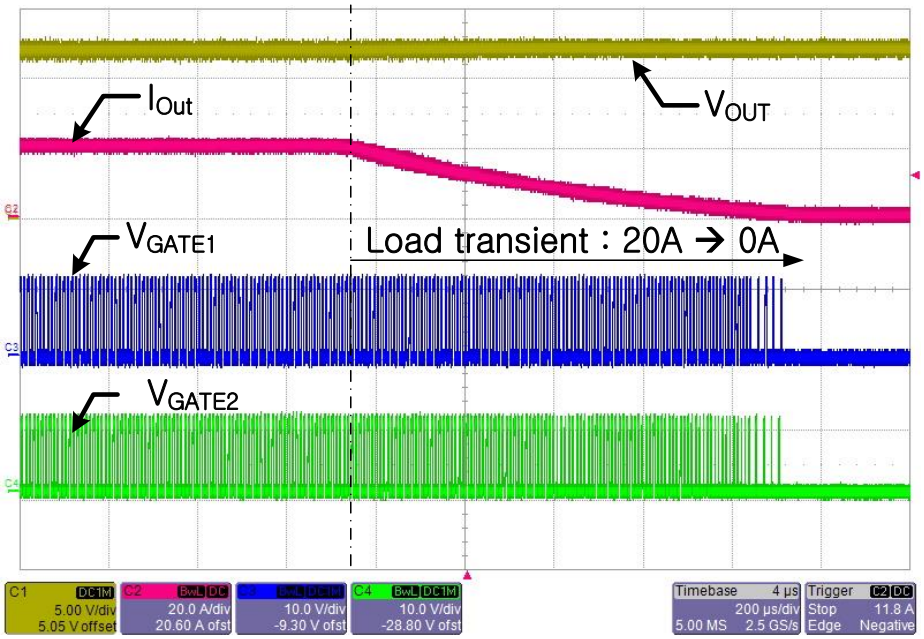

Figure 18. V_{IN}=390V_{DC}, I_{OUT} = 20-0A, No drop the output voltage

Load on/off test

Load on/off frequency: 1kHz

Load A/B : 20A/0A

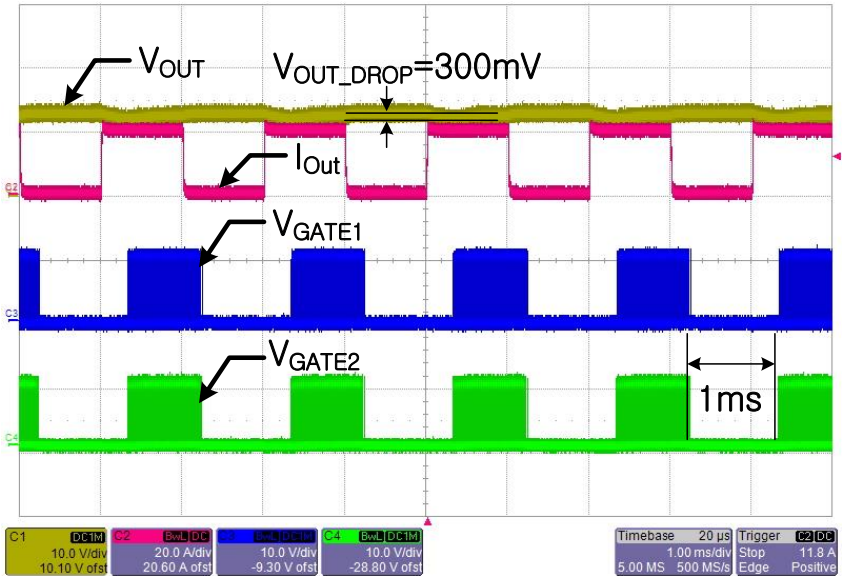

Figure 19. V_{IN}=390V_{DC}, I_{OUT} = 0-20A repetitive current, V_{OUT_DROP}=300mV

Output short test

When V_{DD} is decreased to V_{DD_OFF} by output short, FAN6248 immediately stops SR operation. In this case, LLC resonant converter can operate until over-load protection tirigger

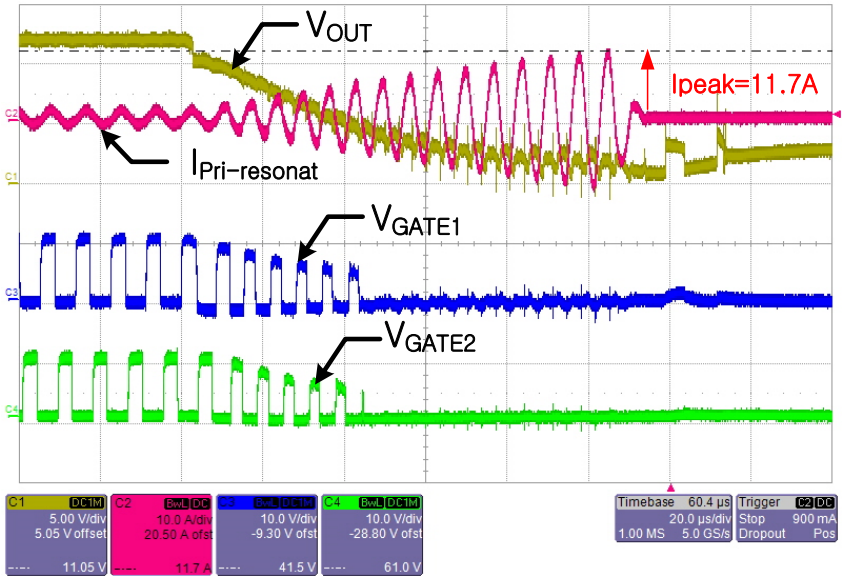

Figure 20. V_{IN}=390V_{DC}, I_{OUT} = 10A , normal load

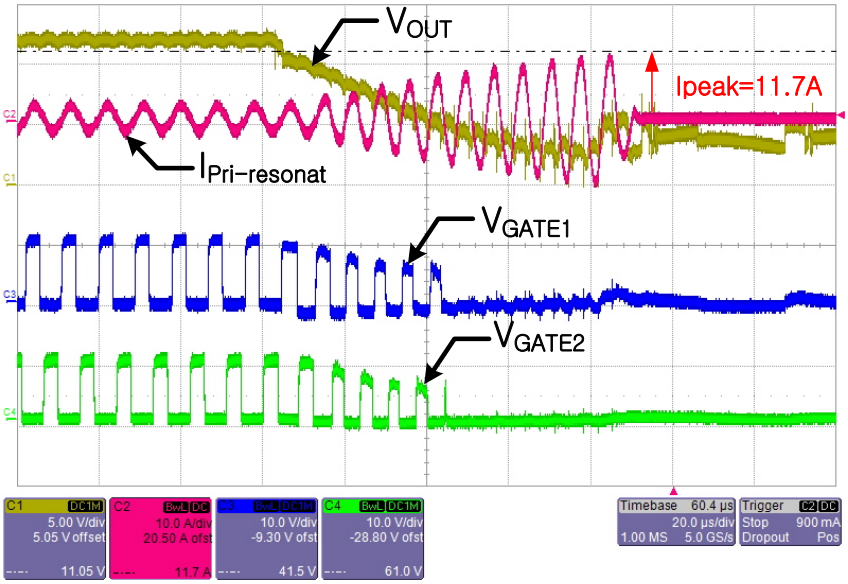

Figure 21. V_{IN}=390V_{DC}, I_{OUT} = 20A , Full load

Thermal Test

Test condition : full load condition after 1 hour aging with open frame

Number	Description	Location	Measurment
①	Primary FET : FCB20N60	M2	45.5℃
②	Primary controller : NCP1399AA	U1	60.7℃
③	Secondary FET : FDB9406_F085	M3	85.5℃
④	S.R controller : FAN6248	U2	91.4℃
⑤	Secondary FET : FDB9406_F085	M4	80.5℃
⑥	Input capacitor	C1	38.5℃
⑦	Primary resonant capacitor	C2	43.4℃
⑧	Transformer	T1	98℃
⑨	Output capacitor	C15	63.4℃

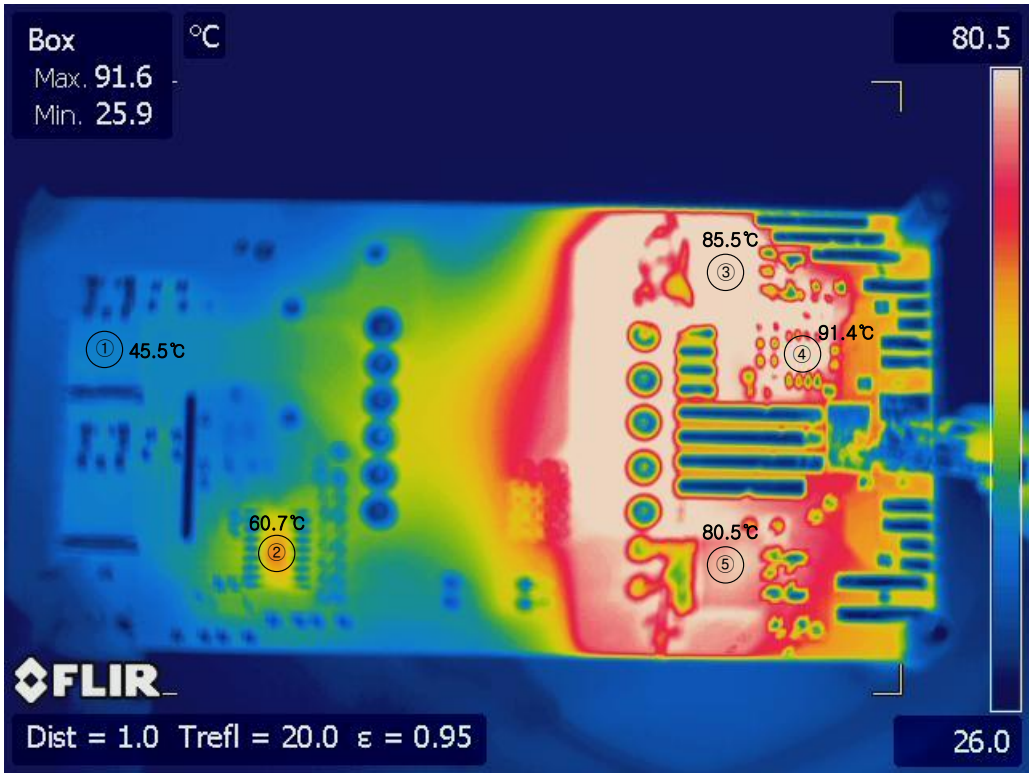

Figure 22. V_{IN}=390V_{DC}, I_{OUT} = 20A, Bottom side picture

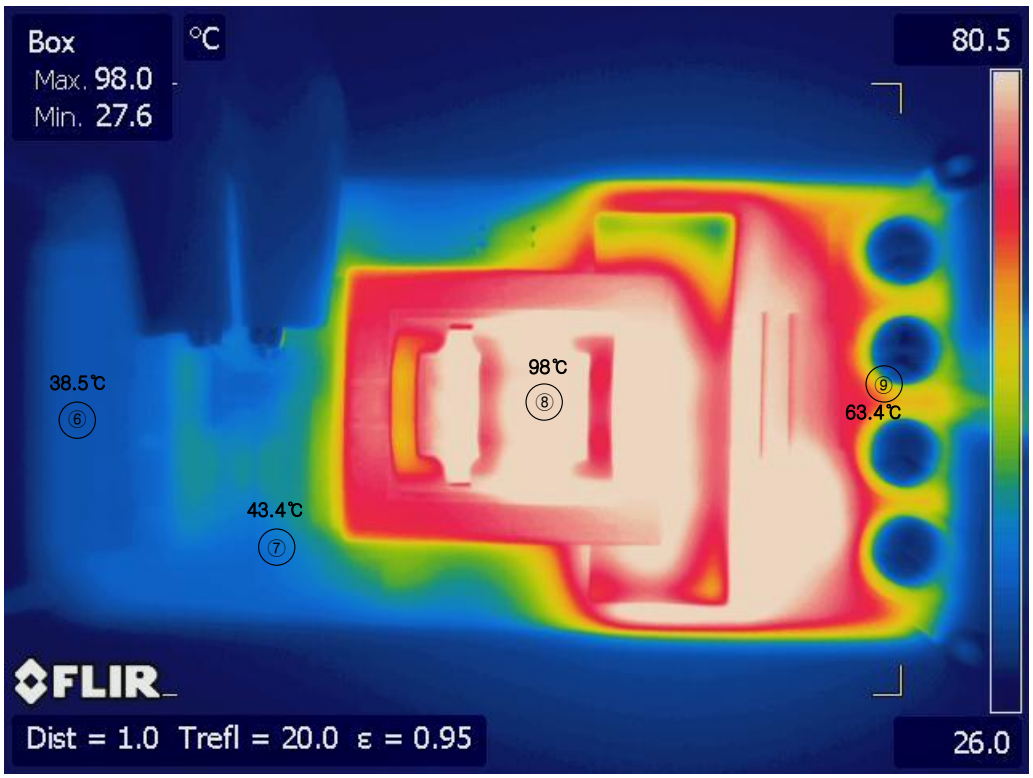

Figure 23. V_{IN}=390V_{DC}, I_{OUT} = 20A, Top side picture

Driver Circuit Guide

To fast turn-off and stable operation, following circuit is recommended.
- Q1, Q2 : PNP transistor for fast turn-off
- GND, VS1, VS2 pin : need to be connected together on PCB pattern

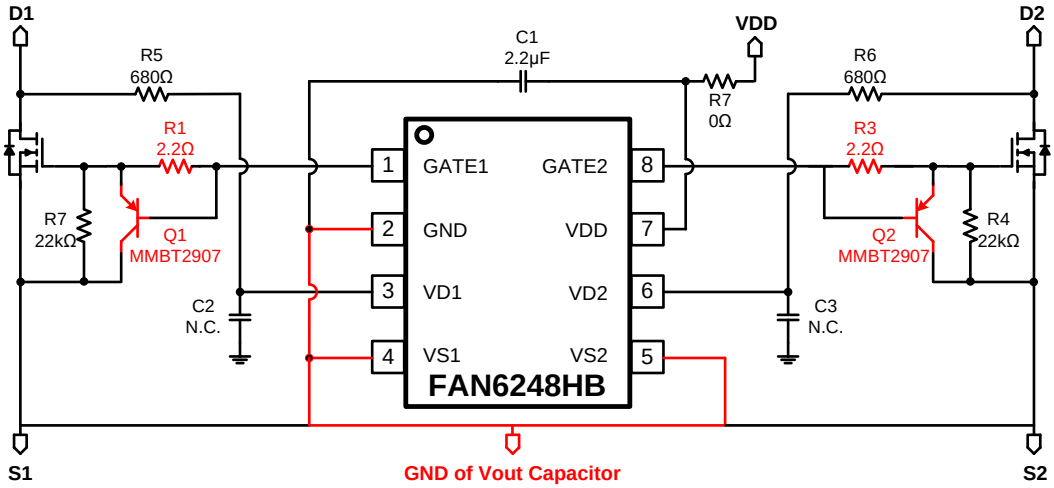

Figure 24. FAN6248 recommended circuit

Recommended PCB Layout

To reduce sensing noise, drain voltage need to be sensed at quite place as below

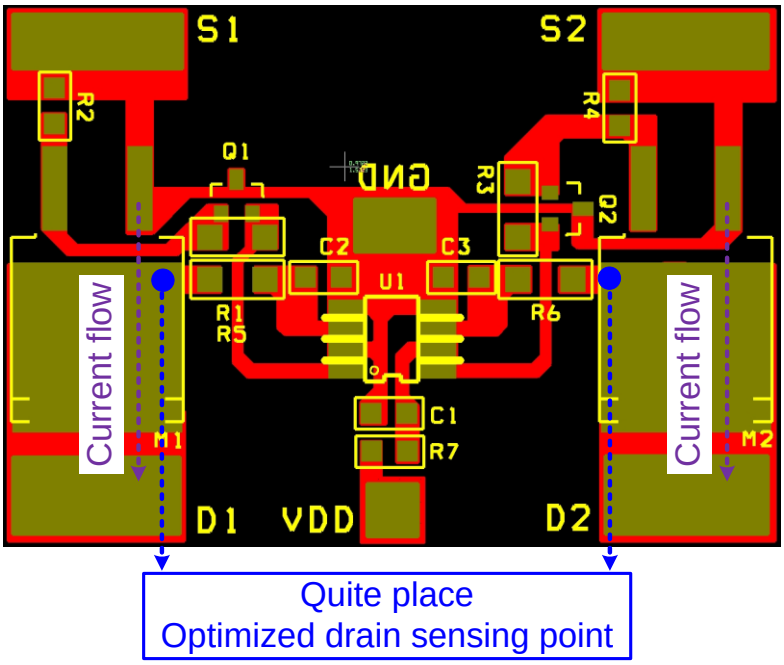

Figure 25. Recommended PCB layout