January 2015

FSA644 — 2:1 MIPI D-PHY (1.5Gbps) 4-Data Lane Switch

Features

Switch Type	SPDT (10x)
Signal Types	**MIPI, D-PHY**
V_{CC}	1.65 to 4.5 V
Input Signals	0 to V_{CC}
R_{ON}	6 Ω Typical HS MIPI 8 Ω Typical LP MIPI
ΔR_{ON}	0.6 Ω Typical HS & LP MIPI
R_{ON_FLAT}	0.3 Ω Typical
I_{CCZ}	0.5 µA Maximum
I_{CC}	32 µA Maximum
O_{IRR}	-40 dB Typical
X_{TALK}	-25 dB Typical
Bandwidth	1100 MHz Minimum
Channel-to-Channel Skew	6 ps Typical
C_{ON}	5.2 pF
Operating Temperature	-40 to +85°C
Package	36-Ball WLCSP
FSA644UCX Top Mark	M7
Ordering Information	FSA644UCX
FSA644BUCX Top Mark	KM
Ordering Information	FSA644BUCX

Description

The FSA644 is a four-data-lane, MIPI, D-PHY switch. This single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed or low-power MIPI sources. The FSA644 is designed for the MIPI specification and allows connection to a CSI or DSI module.

Applications

- Cellular Phones, Smart Phones
- Displays

Related Resources

- FSA644 Demonstration Board

Typical Application

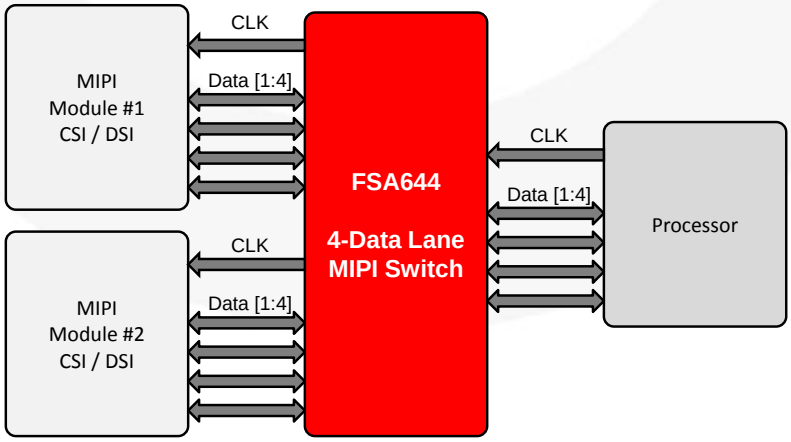


Figure 1. Mobile Phone Example

Pin Descriptions

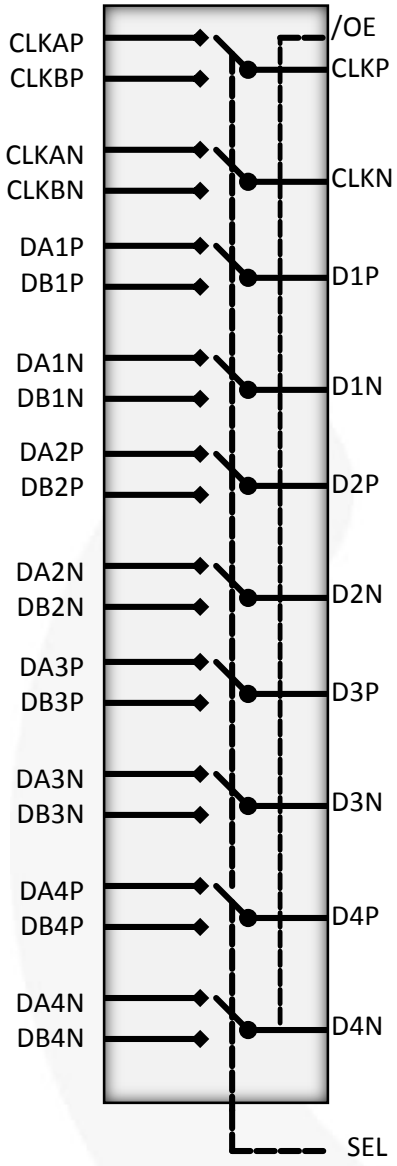


Figure 2. Analog Symbol

Pin Name	Description		
$CLK_{P/N}$	Common Clock Path		
$D1_{P/N}$	Common Data Path 1		
$D2_{P/N}$	Common Data Path 2		
$D3_{P/N}$	Common Data Path 3		
$D4_{P/N}$	Common Data Path 4		
$CLKA_{P/N}$	A-Side Clock Path		
$DA1_{P/N}$	A-Side Data Path 1		
$DA2_{P/N}$	A-Side Data Path 2		
$DA3_{P/N}$	A-Side Data Path 3		
$DA4_{P/N}$	A-Side Data Path 4		
$CLKB_{P/N}$	B-Side Clock Path		
$DB1_{P/N}$	B-Side Data Path 1		
$DB2_{P/N}$	B-Side Data Path 2		
$DB3_{P/N}$	B-Side Data Path 3		
$DB4_{P/N}$	B-Side Data Path 4		
SEL	Control Pin	SEL=0	CLKP=CLKAP, CLKN=CLKAN, Dn(P/N)=DAn(P/N)
		SEL=1	CLKP=CLKBP, CLKN=CLKBN, Dn(P/N)=DBn(P/N)
/OE	Output Enable		
V_{CC}	Power		
GND	Ground		
NC	No Connect		

Pin Definitions

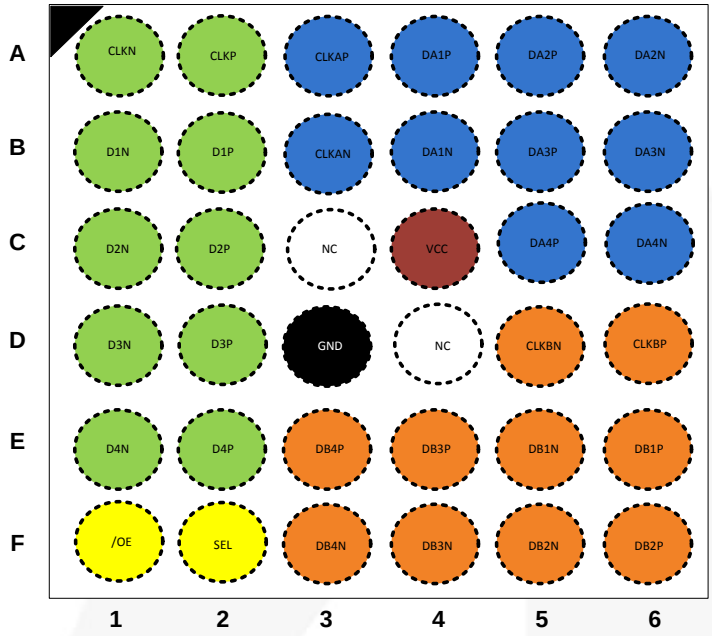


Figure 3. Top Through View

Table 1. Ball-to-Pin Mappings

Ball	Pin Name
A1	CLK_N
A2	CLK_P
A3	$CLKA_P$
A4	$DA1_P$
A5	$DA2_P$
A6	$DA2_N$
B1	$D1_N$
B2	$D1_P$
B3	$CLKA_N$
B4	$DA1_N$
B5	$DA3_P$
B6	$DA3_N$
C1	$D2_N$
C2	$D2_P$
C3	NC
C4	V_{CC}
C5	$DA4_P$
C6	$DA4_N$
D1	$D3_N$
D2	$D3_P$
D3	GND
D4	NC
D5	$CLKB_N$
D6	$CLKB_P$
E1	$D4_N$
E2	$D4_P$
E3	$DB4_P$
E4	$DB3_P$
E5	$DB1_N$
E6	$DB1_P$
F1	/OE
F2	SEL
F3	$DB4_N$
F4	$DB3_N$
F5	$DB2_N$
F6	$DB2_P$

Truth Table

SEL	/OE	Function
LOW	LOW	CLK_P=$CLKA_P$, CLK_N=$CLKA_N$, Dn(P/N)=DAn(P/N)
HIGH	LOW	CLK_P=$CLKB_P$, CLK_N=$CLKB_N$, Dn(P/N)=DBn(P/N)
X	HIGH	DAn(P/N), DBn(P/N) Data Ports High Impedance

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.50	+5.25	V
V_{CNTRL}	DC Input Voltage (/OE)[1]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			50	mA
T_{STG}	Storage Temperature		-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		3.5	kV
		I/O to GND		3.5	
		Power to GND		8.0	
	Charged Device Model, JEDEC: JESD22-C101			1.5	
	IEC 61000-4-2 System	Contact		8.0	
		Air Gap		15.0	

Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		1.65	4.50	V
V_{CNTRL}	Control Input Voltage (S, /OE)[2]		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (CLKn, CLKAn, CLKBn, Dn, DAn, DBn)	HS Mode	0.1	0.3	V
		LP Mode	0	1.2	
T_A	Operating Temperature		-40	+85	°C

Note:

2. The control input must be held HIGH or LOW; it must not float.

DC Electrical Characteristics

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
V_{IK}	Clamp Diode Voltage	I_{IN}=-18 mA	2.8			-1.2	V
V_{IH}	Input Voltage High		1.65 to 4.50	1.0			V
V_{IL}	Input Voltage Low		1.65 to 4.50			0.4	V
I_{IN}	Control Input Leakage (SEL,/OE)	V_{SW}=0 to V_{CC}	1.65 to 4.50	-100		100	nA
$I_{NO(OFF)}$, $I_{NC(OFF)}$	Off Leakage Current of Port CLKAn, DAn, CLKBn, DBn	CLKn, Dn=0.3 V; V_{CC}-0.3 V; CLKAn, DAn, or CLKBn; DBn= V_{CC}-0.3 V, 0.3 V, or Floating; /OE=0 V	1.65 to 4.50	-100		100	nA
$I_{A(ON)}$	On Leakage Current of Common Ports (CLKn, Dn)	CLKn, Dn = 0.3 V; V_{CC}-0.3 V; CLKAn, DAn, or CLKBn; DBn=V_{CC}-0.3 V, 0.3 V, or Floating; /OE=0 V	1.65 to 4.50	-100		100	nA
I_{OFF}	Power-Off Leakage Current	CLKn, Dn, or CLKAn; DAn or CLKBn, DBn; V_{IN}=0 V to 4.5 V; V_{CC}=0 V	0	-100		100	nA
I_{OZ}	Off-State Leakage	0 ≤ CLKn, Dn, CLKAn, CLKBn, DAn, DBn ≤ 3.6 V, /OE=High	4.5	-100		100	nA
$R_{ON\_MIPI\_HS}$	Switch On Resistance for HS MIPI Applications(3)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8		7	12	Ω
			2.5		6	9	
			3.6		6	9	
			4.5		6	9	
$R_{ON\_MIPI\_LP}$	Switch On Resistance for LP MIPI Applications(3)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0V, $CLK_{A, B}$, DBn or DAn=0, 0.6, 1.2 V	1.8		6.7	12.0	Ω
			2.5		6.4	9.0	
			3.6		6.2	9.0	
			4.5		6.0	9.0	
$\Delta R_{ON\_MIPI\_HS}$	On Resistance Matching Between HS MIPI Channels(4)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0 V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8		0.8		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$\Delta R_{ON\_MIPI\_LP}$	On Resistance Matching Between LP MIPI Channels(4)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0 V, $CLK_{A,B}$, DBn or DAn= 0.0, 0.6, 1.2 V	1.8		0.8		Ω
			2.5		0.6		
			3.6		0.5		
			4.5		0.5		
$R_{ON\_FLAT\_MIPI\_HS}$	On Resistance Flatness for HS MIPI Signals(4)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0 V, $CLK_{A, B}$, DBn or DAn=0.1, 0.2, 0.3	1.8		1.5		Ω
			2.5		0.5		
			3.6		0.3		
			4.5		0.2		
$R_{ON\_FLAT\_MIPI\_LP}$	On Resistance Flatness for LP MIPI Signals(4)	I_{ON}=-10 mA, /OE=0 V, SEL=V_{CC} or 0 V, $CLK_{A, B}$, DB_n or DAn=0.0, 0.6, 1.2 V	1.8		35		Ω
			2.5		2		
			3.6		1		
			4.5		0.5		

Continued on the following page…

DC Electrical Characteristics

All typical values are at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
I_{CCZ}	Quiescent Hi-Z Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	4.5			0.5	µA
I_{CC}	Quiescent Supply Current	V_{IN}=0 or V_{CC}, I_{OUT}=0	2.5 to 4.5			32	µA
			1.8			22	
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	$V_{SEL,/OE}$=1.65 V	4.5			4	µA
			2.5			0.1	

Notes:

3. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltage on the two (A or B ports).
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical values are for V_{CC}=3.3V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
t_{INIT}	Initalization Time V_{CC} to Output (5)	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V	2.5 to 4.5			100	µs
			1.8			150	
t_{EN}	Enable Turn-On Time, /OE to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V	2.5 to 4.5		120	200	ns
			1.8		250	500	
t_{DIS}	Disable Turn-Off Time, /OE to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V	2.5 to 4.5		25	50	ns
			1.8		50	90	
t_{ON}	Turn-On Time, SEL to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V	2.5 to 4.5		50	100	ns
			1.8		75	125	
t_{OFF}	Turn-Off Time SEL to Output	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V	2.5 to 4.5		50	200	ns
			1.8		200	325	
t_{BBM}	Break-Before-Make Time	R_L=50 Ω, C_L=5 pF, V_{SW}=1.2 V		10	50		ns
O_{IRR}	Off Isolation for MIPI(5)	R_L=50 Ω, f=750 MHz, /OE=V_{CC} V_{SW}=-1 dBm (200 mV_{PP})	1.65 to 4.5		-18		dB
X_{TALK}	Crosstalk for MIPI(5)	R_L=50 Ω, f=750 MHz, V_{SW}=-1 dBm (200 mV_{PP})	1.65 to 4.5		-25		dB
BW	-3db Bandwidth(5)	R_L=50 Ω, C_L=0 pF	3.0	1100	1600		MHz
S_{DD21}	Differential Data Rate	Inter-operability Data Rate	3.0		1.5		Gbps

Note:

5. Guaranteed by characterization.

High-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40ºC to +85ºC			Unit
				Min.	Typ.	Max.	
$t_{SK(O)}$	Channel-to-Channel Single-Ended Skew[6]	TDR-Based Method (V_{SW}=0.2 V_{PP}, C_L=C_{ON})	3.3		6	20	ps
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output[6]	TDR-Based Method (V_{SW}=0.2 V_{PP}, C_L=C_{ON})	3.3		6	20	ps

Note:

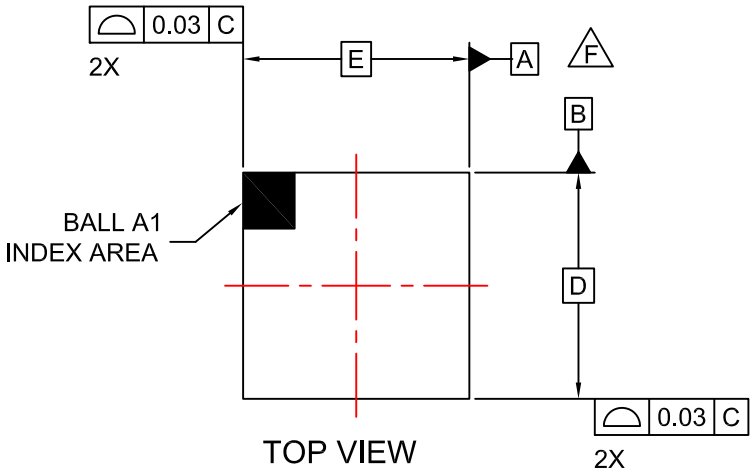
6. Guaranteed by characterization.

Capacitance

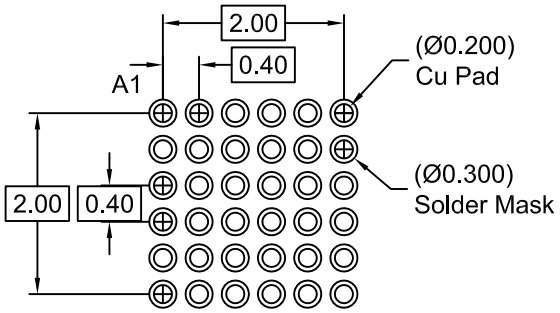
Symbol	Parameter	Conditions	T_A=- 40ºC to +85ºC			Unit
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0 V, f=1 MHz		2.1		pF
C_{ON}	Out On Capacitance	V_{CC}=3.3 V, /OE=0 V, f=1 MHz		5.2		
C_{OFF}	Out Off Capacitance	V_{CC} and /OE=3.3 V, f=1 MHz		2.0		

Ordering Information

Part Number	Top Mark	Package	D	E	X	Y
FSA644UCX	M7	36-Ball WLCSP, Non-JEDEC 2.36 mm x 2.36 mm, 0.4 mm Pitch	2.36 mm	2.36 mm	0.18 mm	0.18 mm
FSA644BUCX	KM	36-Ball WLCSP, Non-JEDEC 2.415 mm x 2.415 mm, 0.4 mm Pitch	2.415 mm	2.415 mm	0.208 mm	0.208 mm



TOP VIEW



RECOMMENDED LAND PATTERN
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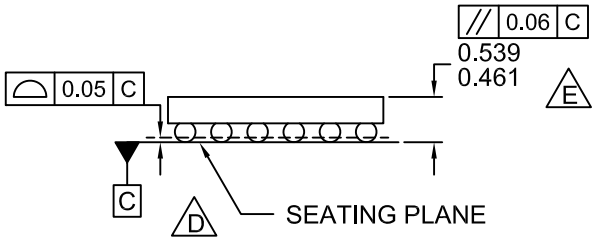
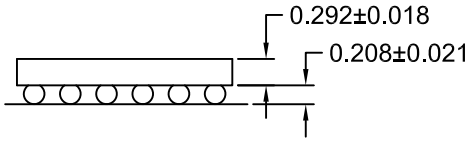
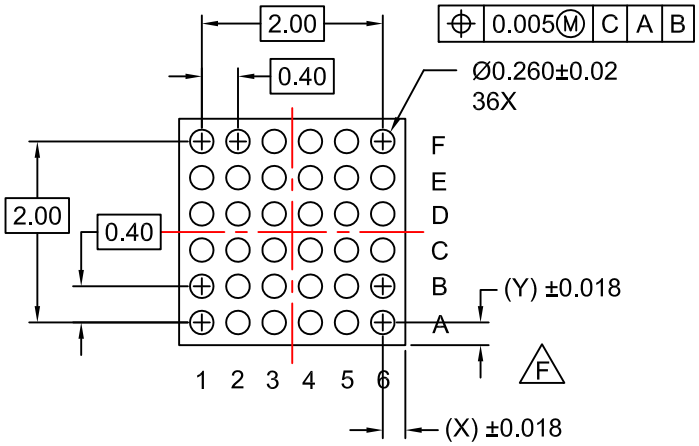




SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

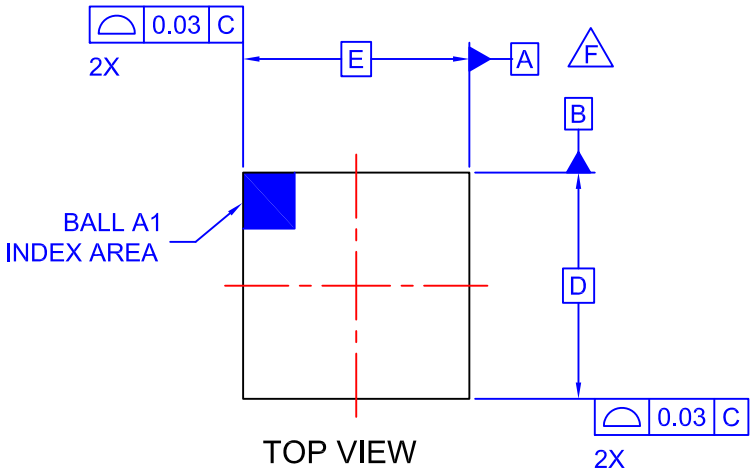
C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

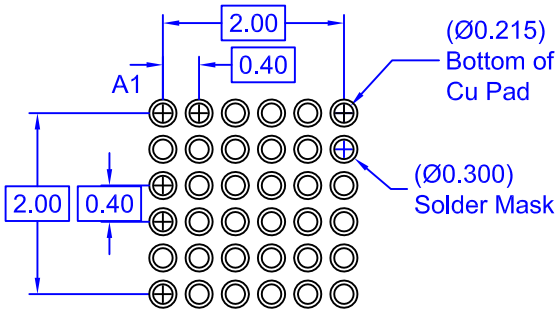
E. PACKAGE NOMINAL HEIGHT IS 500 ± 39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC036AArev1.



TOP VIEW



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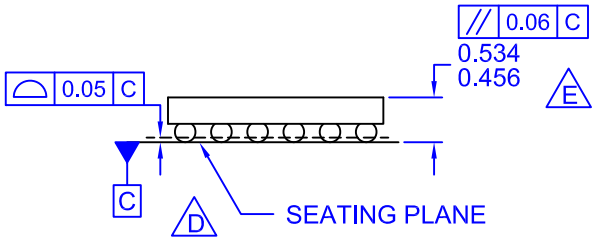

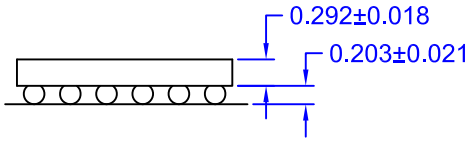

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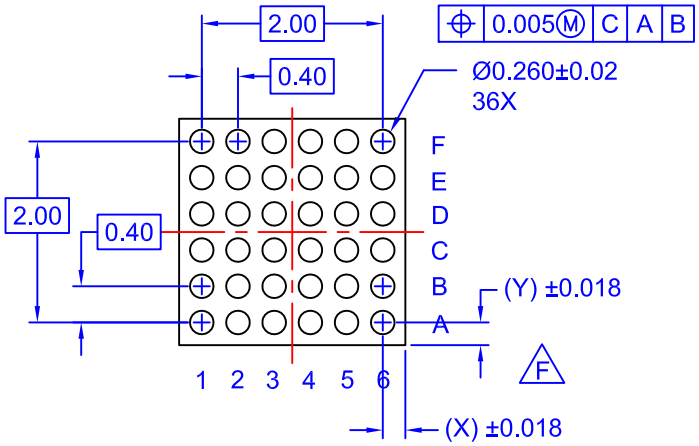

BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASMEY14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 495 ± 39 MICRONS (456-534 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC036AB REV1.

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SuperSOT™-6
SuperSOT™-8
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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