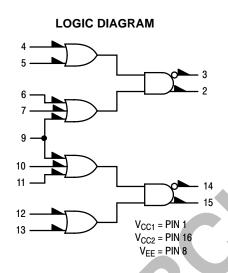
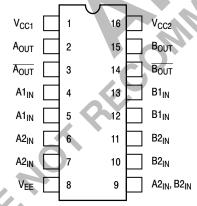
Dual 2-Wide 2-3-Input OR-AND/OR-AND Gate

The MC10117 is a dual 2-wide 2-3-input OR-AND/OR-AND-Invert gate. This general purpose logic element is designed for use in data control, such as digital multiplexing or data distribution. Pin 9 is common to both gates.

- $P_D = 100 \text{ mW typ/pkg (No Load)}$
- $t_{pd} = 2.3 \text{ ns typ}$
- t_r , $t_f = 2.2$ ns typ (20%–80%)



DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 18 of the ON Semiconductor MECL Data Book (DL122/D).



ON Semiconductor

http://onsemi.com

MARKING DIAGRAMS



CDIP-16 L SUFFIX CASE 620





PDIP-16 P SUFFIX CASE 648





PLCC-20 FN SUFFIX CASE 775



A = Assembly Location

WL = Wafer Lot YY = Year WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping		
MC10117L	CDIP-16	25 Units / Rail		
MC10117P	PDIP-16	25 Units / Rail		
MC10117FN	PLCC-20	46 Units / Rail		

ELECTRICAL CHARACTERISTICS

Characteristic Symbolic Power Supply Drain Current I _E Input Current I _{inH} Output Current I _{inH} Output Voltage Logic 1 V _{OH} Output Voltage Logic 0 V _{OL} Threshold Voltage Logic 0 V _{OL} Switching Times (50Ω Load) V _{OL} Propagation Delay t ₄₊₂ -t ₄₋₂ -t ₄₊₃ -t ₄₋₃ -t ₄₋₃ -t ₄₋₃ t ₂₋ t ₃₋ Rise Time (20 to 80%) t ₂ -t ₃ -t ₃ Inputs 4, 5, 12 and 13 have same I _{inH} I _{inH} Inputs 6, 7, 10 and 11 have same I _{inH}	bol ** L H L HA A 22+ 22- 33- 34+	Pin Jnder Test 8 6 9 4 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 3 2 3 3 3 2 3 3 3 2 3 3 3 2 3 3 3 3 2 3 3 3 3 2 3 3 3 3 2 3 3 3 3 2 3 3 3 3 2 3 3 3 3 3 3 4 3 4	0.5 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080 -1.080	PC Max 29 425 560 390 -0.890 -0.780 -1.675 -1.675 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1 4.1	0.5 -0.960 -0.960 -1.850 -0.980 -0.980 -0.980 -1.4 1.4 1.4 1.1 1.1 1.1 1.1	+25°C Typ 20 2.3 2.3 2.3 2.3 2.2 2.2 2.2	-0.810 -0.700 -1.650 -1.630 -1.630 -1.630 -1.630	-85 Min 0.3 -0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.1 1.1 1.1	-0.700 -0.590 -1.615 -1.595 -1.595 -1.595 -1.615	Unit mAd μAdd Vdc Vdc Vdc ns
Power Supply Drain Current IE	H	8 6 9 4 4 2 3 2 3 2 3 2 3 2 3 2 3 3 2 3 3 2 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	0.5 -1.060 -1.890 -1.890 -1.080 -1.080 1.4 1.4 1.4 1.4 1.4 0.9 0.9 0.9	29 425 560 390 -0.890 -0.780 -1.675 -1.675 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	0.5 -0.960 -0.960 -1.850 -0.980 -0.980 -0.980 1.4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.3 2.3 2.2 2.2	26 265 350 245 -0.810 -0.700 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 3.4 4.0 4.0 4.0	0.3 -0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	29 265 350 245 -0.700 -0.590 -1.615 -1.615 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	mAc μAd Vdc Vdc
Input Current Inh' In	1* L H H A -A	6 9 4 4 2 3 2 3 2 3 2 3 2 3 2 3 2 3 3 2 2 3 3 2 3 3 2 3 3 2 3 3 3 2 3 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	425 560 390 -0.890 -0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.3 2.2 2.2	265 350 245 -0.810 -0.700 -1.650 -1.650 -1.630 3.4 3.4 3.4 3.4 4.0 4.0	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	265 350 245 -0.700 -0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	μAc Vd Vd
InL Output Voltage Logic 1 VOH Output Voltage Logic 0 VOL Threshold Voltage Logic 1 VOH Threshold Voltage Logic 0 VOL Switching Times (50Ω Load) Propagation Delay t4+2-t4-2-t4+3-t4-3-t4-3-t1-3-t1-3-t1-3-t1-3-t1-3-t1-	L H H L HA LA	9 4 2 3 2 3 2 3 2 3 2 3 2 3 3 2 3 3 2 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	-0.890 -0.780 -1.675 -1.675 -1.655 -1.655 -3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	350 245 -0.810 -0.700 -1.650 -1.650 -1.630 3.4 3.4 3.4 3.4 3.4 4.0 4.0	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	350 245 -0.700 -0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	μAc Vd Vd Vd
Output Voltage Logic 1 VOH Output Voltage Logic 0 VOL Threshold Voltage Logic 1 VOH Threshold Voltage Logic 0 VOL Switching Times (50Ω Load) Forpagation Delay t4+2-14-2-14-3-14-3-14-3-14-3-14-3-14-3-14-	H	4 4 2 3 2 3 2 3 2 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	390 -0.890 -0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-0.810 -0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 4.0 4.0	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-0.700 -0.590 -1.615 -1.615 -1.595 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	Vd Vd Vd
Output Voltage Logic 1 VOH Output Voltage Logic 0 VOL Threshold Voltage Logic 1 VOH Threshold Voltage Logic 0 VOL Switching Times (50Ω Load) Forpagation Delay t4+2-14-2-14-3-14-3-14-3-14-3-14-3-14-3-14-	H	4 2 3 2 3 2 3 2 3 2 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	-0.890 -0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-0.810 -0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 4.0 4.0	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-0.700 -0.590 -1.615 -1.615 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	Vd Vd Vd
Output Voltage Logic 1 VOH Output Voltage Logic 0 VOL Threshold Voltage Logic 1 VOH Threshold Voltage Logic 0 VOL Switching Times (50Ω Load) Propagation Delay t ₄₊₂ -t ₄₋₂ -t ₄₊₃ -t ₄₋₃ -t ₄₋₃ Rise Time (20 to 80%) t ₂ +t ₃ -t ₃ Fall Time (20 to 80%) t ₂ -t ₃ -t ₃ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	H	2 3 2 3 2 3 3 2 2 3 3 2 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.060 -1.890 -1.890 -1.080 -1.080 -1.080	-0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -0.960 -1.850 -1.850 -0.980 -0.980 -1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 4.0 4.0 4.0	-0.890 -0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-0.590 -1.615 -1.615 -1.595 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	Vd Vd Vd
Output Voltage Logic 0 V _{OL} Threshold Voltage Logic 1 V _{OH} , Threshold Voltage Logic 0 V _{OL} Switching Times (50Ω Load) Propagation Delay t ₄₊₂ t ₄₋₂ t ₄₊₃ t ₄₋₃ Rise Time (20 to 80%) t ₂₊ t ₃₊ Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	2+ 2- 3- 3+ +	3 2 3 2 3 2 2 3 3 2 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 2 3 3 3 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	-1.060 -1.890 -1.890 -1.080 -1.080 -1.080 1.4 1.4 1.4 1.4 1.4 0.9 0.9 0.9	-0.780 -1.675 -1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.960 -1.850 -1.850 -0.980 -0.980 -0.980 -1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-0.700 -1.650 -1.650 -1.630 -1.630 3.4 3.4 3.4 3.4 4.0 4.0 4.0	-0.890 -1.825 -1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-0.590 -1.615 -1.615 -1.595 -1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6 4.6	Vd. Vd.
Threshold Voltage Logic 1 V_{OH} . Threshold Voltage Logic 0 V_{OL} . Switching Times (50 Ω Load) Propagation Delay $t_{4+2-t_{4-2-t_{4+3-t_{4-3}}}$. Rise Time (20 to 80%) $t_{2-t_{3-1}}$. Fall Time (20 to 80%) $t_{2-t_{3-1}}$. Inputs 4, 5, 12 and 13 have same t_{inH} . Inputs 6, 7, 10 and 11 have same t_{inH} .	2+ 2- 3- 3+ +	3 2 3 2 3 2 2 2 3 3 2 3 2 3 3 2 3 3	-1.890 -1.080 -1.080 1.4 1.4 1.4 1.4 0.9 0.9 0.9 0.9	-1.675 -1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-1.850 -0.980 -0.980 1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-1.650 -1.630 -1.630 3.4 3.4 3.4 4.0 4.0 4.0	-1.825 -0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-1.615 -1.595 -1.595 3.8 3.8 3.8 4.6 4.6 4.6	Vd
Threshold Voltage Logic 0 V_{OL} Switching Times (50 Ω Load) Propagation Delay t_{4+2-1} t_{4-2-1} t_{4+3-1} t_{4-3} Rise Time (20 to 80%) t_{2+1} t_{3+1} Fall Time (20 to 80%) t_{2-1} t_{3-1} Inputs 4, 5, 12 and 13 have same t_{1} Inputs 6, 7, 10 and 11 have same t_{1}	2+ 2- 3- 3+ +	2 3 2 3 2 2 2 3 3 2 3 2 3	-1.080 -1.080 1.4 1.4 1.4 1.4 0.9 0.9 0.9 0.9	-1.655 -1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.980 -0.980 1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	-1.630 -1.630 3.4 3.4 3.4 3.4 4.0 4.0	-0.910 -0.910 1.4 1.4 1.4 1.4 1.1 1.1	-1.595 -1.595 3.8 3.8 3.8 3.8 4.6 4.6	Vd
Threshold Voltage Logic 0 V_{OL} Switching Times (50 Ω Load) Propagation Delay t_{4+2-1} t_{4-2-1} t_{4+3-1} t_{4-3} Rise Time (20 to 80%) t_{2+1} t_{3+1} Fall Time (20 to 80%) t_{2-1} t_{3-1} Inputs 4, 5, 12 and 13 have same t_{1} Inputs 6, 7, 10 and 11 have same t_{1}	2+ 2- 3- 3+ +	3 2 3 2 2 2 3 3 2 3 2 3	1.4 1.4 1.4 1.4 0.9 0.9 0.9	-1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	-0.980 1.4 1.4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.4 1.1 1.1	-1.595 3.8 3.8 3.8 3.8 4.6 4.6	Vd
Switching Times (50Ω Load) Propagation Delay t ₄₊₂ - t ₄₋₂ - t ₄₊₃ - t ₄₋₃ - Rise Time (20 to 80%) t ₂ + t ₃ + Fall Time (20 to 80%) t ₂ - t ₃ - Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	2+ 2- 3- 3+ +	2 3 2 2 3 3 2 3 2 3	1.4 1.4 1.4 1.4 0.9 0.9 0.9	-1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	1.4 1.4 1.4 1.4 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.4 1.1 1.1	-1.595 3.8 3.8 3.8 3.8 4.6 4.6	
Switching Times (50Ω Load) Propagation Delay t ₄₊₂ - t ₄₋₂ - t ₄₊₃ - t ₄₋₃ - Rise Time (20 to 80%) t ₂ + t ₃ + Fall Time (20 to 80%) t ₂ - t ₃ - Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	2+ 2- 3- 3+ +	3 2 2 3 3 2 3 2 3	1.4 1.4 1.4 0.9 0.9 0.9	-1.655 3.9 3.9 3.9 3.9 4.1 4.1 4.1	1,4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.1 1.1	-1.595 3.8 3.8 3.8 3.8 4.6 4.6	
Propagation Delay t ₄₊₂ . t ₄₋₂ . t ₄₊₃ . t ₄₋₃ . Rise Time (20 to 80%) t ₂₊ t ₃₊ Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	2_ 3_ 3+ + - -	2 2 3 3 2 3	1.4 1.4 1.4 0.9 0.9 0.9	3.9 3.9 3.9 3.9 4.1 4.1 4.1	1,4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.1 1.1	3.8 3.8 3.8 3.8 4.6 4.6	ns
Propagation Delay t ₄₊₂ . t ₄₋₂ . t ₄₊₃ . t ₄₋₃ . Rise Time (20 to 80%) t ₂₊ t ₃₊ Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	2_ 3_ 3+ + - -	2 3 3 2 3 2 3	1.4 1.4 1.4 0.9 0.9 0.9	3.9 3.9 3.9 4.1 4.1 4.1	1,4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.1 1.1	3.8 3.8 3.8 4.6 4.6 4.6	
Table 1. The same linh linh linh linh linh linh linh linh	2_ 3_ 3+ + - -	2 3 3 2 3 2 3	1.4 1.4 1.4 0.9 0.9 0.9	3.9 3.9 3.9 4.1 4.1 4.1	1,4 1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.3 2.2 2.2	3.4 3.4 3.4 4.0 4.0	1.4 1.4 1.4 1.1 1.1	3.8 3.8 3.8 4.6 4.6 4.6	
Rise Time (20 to 80%) t ₂₊ t ₃₊ Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	3 3+ + - -	3 2 3 2 3	1.4 1.4 0.9 0.9 0.9	3.9 3.9 4.1 4.1 4.1	1.4 1.4 1.1 1.1 1.1	2.3 2.3 2.2 2.2	3.4 3.4 4.0 4.0 4.0	1.4 1.1 1.1	3.8 3.8 4.6 4.6 4.6	
Rise Time (20 to 80%) t ₂₊ t ₃₊ Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same I _{inH} Inputs 6, 7, 10 and 11 have same I _{inH}	+ + -	2 3 2 3	0.9 0.9 0.9 0.9	4.1 4.1 4.1 4.1	1.1 1.1 1.1 1.1	2.2 2.2 2.2	4.0 4.0 4.0	1.1 1.1 1.1	4.6 4.6 4.6	
Fall Time (20 to 80%) t ₂₋ t ₃₋ Inputs 4, 5, 12 and 13 have same l _{inH} Inputs 6, 7, 10 and 11 have same l _{inH}	+ - -	3 2 3	0.9 0.9 0.9	4.1 4.1 4.1	1.1 1.1 1.1	2.2	4.0 4.0	1.1 1.1	4.6 4.6	
Fall Time (20 to 80%) t_{2-} t_{3-} Inputs 4, 5, 12 and 13 have same l_{inH} Inputs 6, 7, 10 and 11 have same l_{inH}	-	2 3	0.9 0.9	4.1 4.1	1.1 1.1	2.2	4.0	1.1	4.6	
Inputs 4, 5, 12 and 13 have same l_{inH} Inputs 6, 7, 10 and 11 have same l_{inH}	-	3	0.9	4.1	1.1					
Inputs 4, 5, 12 and 13 have same I _{inH} Inputs 6, 7, 10 and 11 have same I _{inH}						,				i
OENICERIO	RE									

ELECTRICAL CHARACTERISTICS (continued)

				TEST VOLTAGE VALUES (Volts)					
		@ Test Te	mperature	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	
			–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	
			+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	
			+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	
			Pin	TEST V					
Characteristic		Symbol	Under Test	V _{IHmax}	V _{ILmin}	V _{IHAmin}	V _{ILAmax}	V _{EE}	(V _{CC}) Gnd
Power Supply Drain C	Current	ΙΕ	8					8	1, 16
Input Current		I _{inH} *	6	4				8	1, 16
			9 4	9	4			8 8	1, 16 1, 16
		-			•			_	
		I _{inL}	4		9			8	1, 16
Output Voltage	Logic 1	V _{OH}	2 3	4, 9				8 8	1, 16 1, 16
Output Voltage	Logic 0	V _{OL}	2 3	4, 9			•	8 8	1, 16 1, 16
Threshold Voltage	Logic 1	V _{OHA}	2 3	9		4	4	8 8	1, 16 1, 16
Threshold Voltage	Logic 0	V _{OLA}	2 3	9		4	4	8 8	1, 16 1, 16
Switching Times	(50Ω Load)			+1.11V		Pulse In	Pulse Out	-3.2 V	+2.0 V
Propagation Delay		t ₄₊₂₊ t ₄₋₂₋ t ₄₊₃₋ t ₄₋₃₊	2 2 3 3	9 9 9 9		4 4 4 4	2 2 3 3	8 8 8	1, 16 1, 16 1, 16 1, 16
Rise Time	(20 to 80%)	t ₂₊ t ₃₊	2 3	9 9		4 4	2 3	8 8	1, 16 1, 16
Fall Time	(20 to 80%)	t ₂₋ t ₃₋	2 3	9 9		4 4	2 3	8 8	1, 16 1, 16

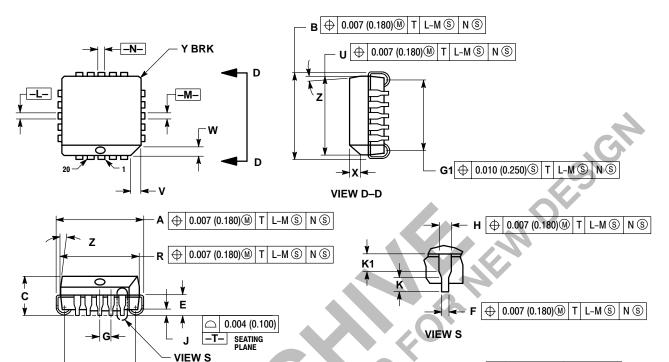
^{*} Inputs 4, 5, 12 and 13 have same I_{inH} limit. Inputs 6, 7, 10 and 11 have same I_{inH} limit.

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibitum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to –2.0 volts. Test procedures are shown for only one gate. The other gates are tested in the same manner.

PACKAGE DIMENSIONS

PLCC-20 **FN SUFFIX**

PLASTIC PLCC PACKAGE CASE 775-02 ISSUE C



NOTES:

- OTES:

 1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.

 2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.

 3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.

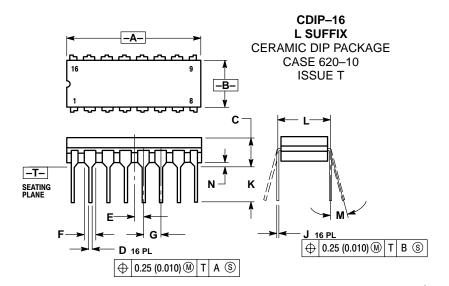
 4. DIMENSIONING AND TOLERANCING PER ANSI Y14 5M 1982
- Y14.5M, 1982. CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT
- INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.385	0.395	9.78	10.03	
В	0.385	0.395	9.78	10.03	
С	0.165	0.180	4.20	4.57	
Ε	0.090	0.110	2.29	2.79	
F	0.013	0.019	0.33	0.48	
G	0.050	BSC	1.27	BSC	
Н	0.026	0.032	0.66	0.81	
J	0.020		0.51		
K	0.025		0.64		
R	0.350	0.356	8.89	9.04	
U	0.350	0.356	8.89	9.04	
٧	0.042	0.048	1.07	1.21	
W	0.042	0.048	1.07	1.21	
X	0.042	0.056	1.07	1.42	
Υ		0.020		0.50	
Z	2°	10°	2°	10 °	
G1	0.310	0.330	7.88	8.38	
K1	0.040		1.02		

G1 ⊕ 0.010 (0.250)③ T L-M ⑤ N ⑤

OENICE NOT RECO

PACKAGE DIMENSIONS



NOTES:

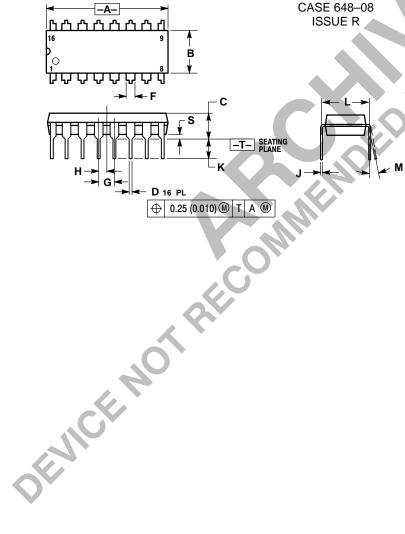
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: INCH.
 DIMENSION LTO CENTER OF LEAD WHEN CONTROLLING DIMENSION LTO CENTER OF LEAD WHEN

- FORMED PARALLEL

 DIMENSION F MAY NARROW TO 0.76 (0.030)
 WHERE THE LEAD ENTERS THE CERAMIC
 BODY.

	INC	HES	MILLIMETERS				
DIM	MIN	MAX	MIN	MAX			
Α	0.750	0.785	19.05	19.93			
В	0.240	0.295	6.10	7.49			
С		0.200		5.08			
D	0.015	0.020	0.39	0.50			
E	0.050	BSC	1.27 BSC				
F	0.055	0.065	1.40	1.65			
G	0.100	BSC	2.54 BSC				
Н	0.008	0.015	0.21	0.38			
K	0.125	0.170	3.18	4.31			
L	0.300	BSC	7.62 BSC				
М	0 °	15°	0 0	15°			
N	0.020	0.040	0.51	1.01			





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS		
DIM	MIN MAX		MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10°	0°	10 °	
S	0.020	0.040	0.51	1.01	

Notes



Notes





ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada **Fax**: 303–675–2176 or 800–344–3867 Toll Free USA/Canada

Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center 4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031

Phone: 81–3–5740–2700 **Email**: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local

Sales Representative.

MC10117/D