MC14029B

Binary/Decade Up/Down Counter

The MC14029B Binary/Decade up/down counter is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. The counter consists of type D flip−flop stages with a gating structure to provide toggle flip−flop capability. The counter can be used in either Binary or BCD operation. This complementary MOS counter finds primary use in up/down and difference counting and frequency synthesizer applications where low power dissipation and/or high noise immunity is desired. It is also useful in A/D and D/A conversion and for magnitude and sign generation.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Speed
- Logic Edge−Clocked Design – Count Occurs on Positive Going Edge of Clock
- Asynchronous Preset Enable Operation
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Pin for Pin Replacement for CD4029B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

ON Semiconductor®

SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAM

16

14029BG
o AWLYWW

1

A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Indicator

ORDERING INFORMATION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq$ (V_{in} or V_{out}) $\leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
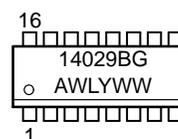
March, 2015 − Rev. 10

MC14029B

PIN ASSIGNMENT

```
        PE [ 1 ●      16 ] V_DD
        Q3 [ 2        15 ] CLK
        P3 [ 3        14 ] Q2
        P0 [ 4        13 ] P2
       C̄in [ 5        12 ] P1
        Q0 [ 6        11 ] Q1
      C̄out [ 7        10 ] U/D
       V_SS [ 8        9 ] B/D
```
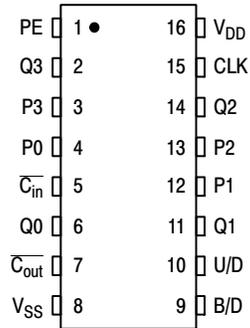
TRUTH TABLE

$\overline{\text{Carry In}}$	Up/Down	Preset Enable	Action
1	X	0	No Count
0	1	0	Count Up
0	0	0	Count Down
X	X	1	Preset

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping†
MC14029BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14029BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC14029B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level ($V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current Source ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
Sink ($V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance, ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0 10 15			$I_T = (0.58 \ \mu A/kHz) \ f + I_{DD}$ $I_T = (1.20 \ \mu A/kHz) \ f + I_{DD}$ $I_T = (1.70 \ \mu A/kHz) \ f + I_{DD}$					µAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in µA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.001$.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ (Note 6)	Max	
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns

Propagation Delay Time
Clk to Q
   t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns
   t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns
   t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
			–
			–
			–
				200
				100
				90
					400
					200
					180
						ns

Clk to $\overline{C_{out}}$
   t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns
   t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns
   t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
			–
			–
			–
				250
				130
				85
					500
					260
					190
						ns

$\overline{C_{in}}$ to $\overline{C_{out}}$
   t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 95 ns
   t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 47 ns
   t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
			–
			–
			–
				175
				50
				50
					360
					120
					100
						ns

PE to Q
   t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 230 ns
   t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns
   t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
			–
			–
			–
				235
				100
				80
					470
					200
					160
						ns

PE to $\overline{C_{out}}$
   t_{PLH}, t_{PHL} = (1. 7 ns/pF) C_L + 465 ns
   t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 192 ns
   t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 125 ns
	t_{PLH},
	t_{PHL}
		5.0
		10
		15
			–
			–
			–
				320
				145
				105
					640
					290
					210
						ns

Clock Pulse Width	$t_{W(cl)}$	5.0 10 15	180 80 60	90 40 30	– – –	ns
Clock Pulse Frequency	f_{cl}	5.0 10 15	– – –	4.0 8.0 10	2.0 4.0 5.0	MHz
Preset Removal Time The Preset Signal must be low prior to a positive–going transition of the clock.	t_{rem}	5.0 10 15	160 80 60	80 40 30	– – –	ns
Clock Rise and Fall Time	$t_{r(cl)}$ $t_{f(cl)}$	5.0 10 1 5	– – –	– – –	15 5 4	μs
$\overline{Carry}$ In Setup Time	t_{su}	5.0 10 15	150 60 40	75 30 20	– – –	ns
Up/Down Setup Time		5.0 10 15	340 140 100	170 70 50	– – –	ns
Binary/Decade Setup Time		5.0 10 15	320 140 100	160 70 50	– – –	ns
Preset Enable Pulse Width	t_W	5.0 10 15	130 70 50	65 35 25	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
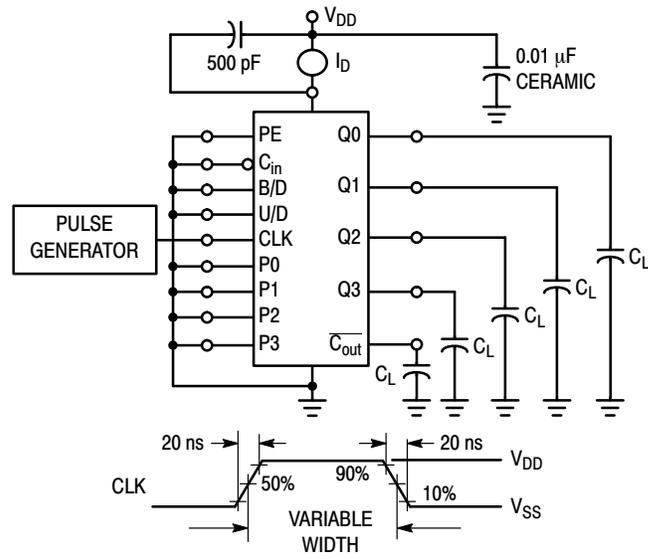
MC14029B
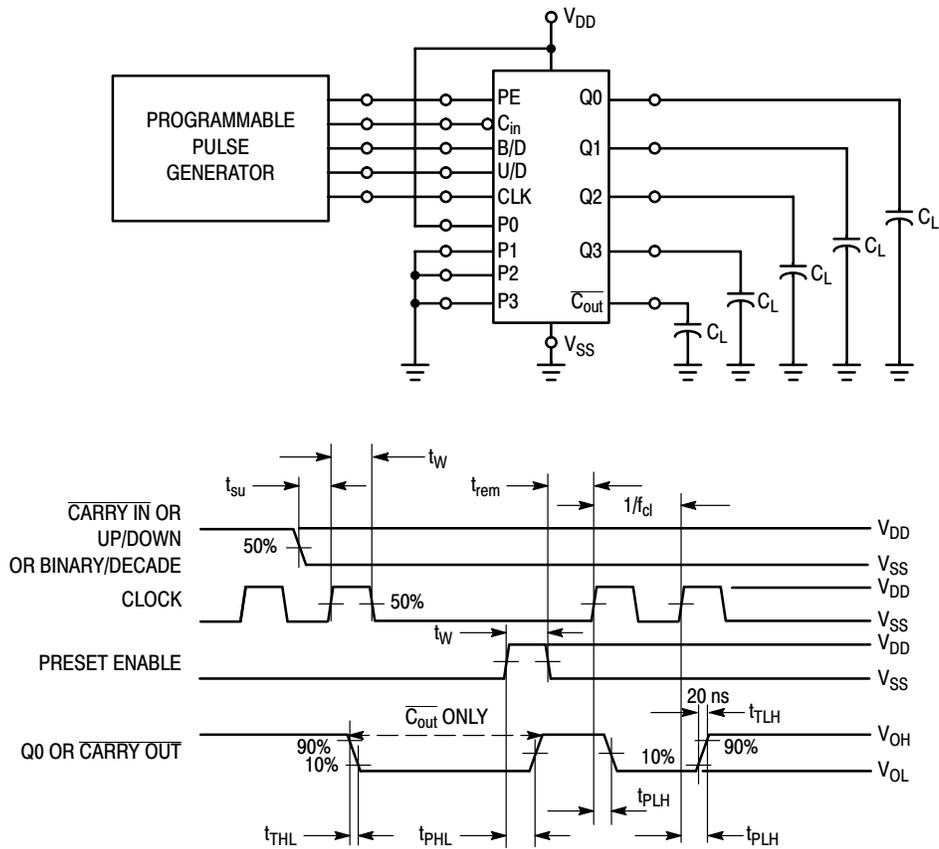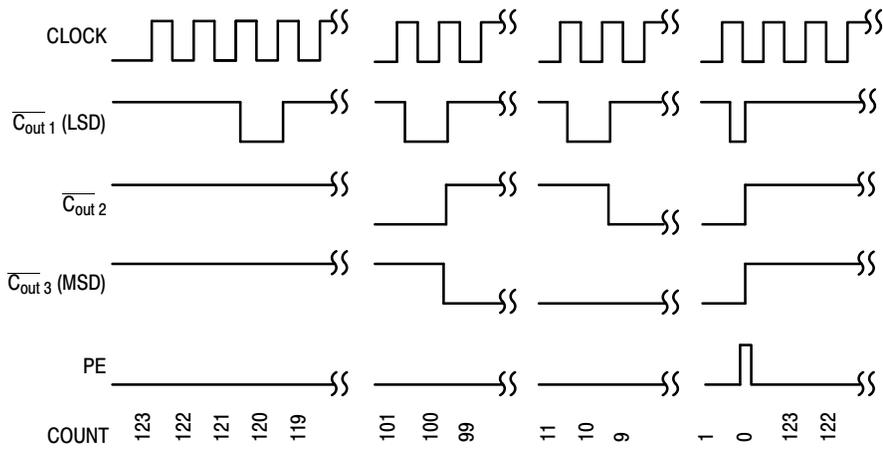

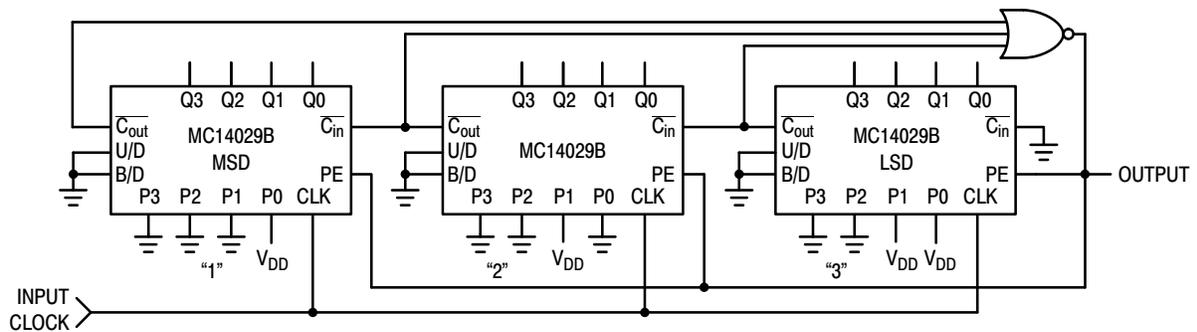**Figure 1. Power Dissipation Test Circuit and Waveform**

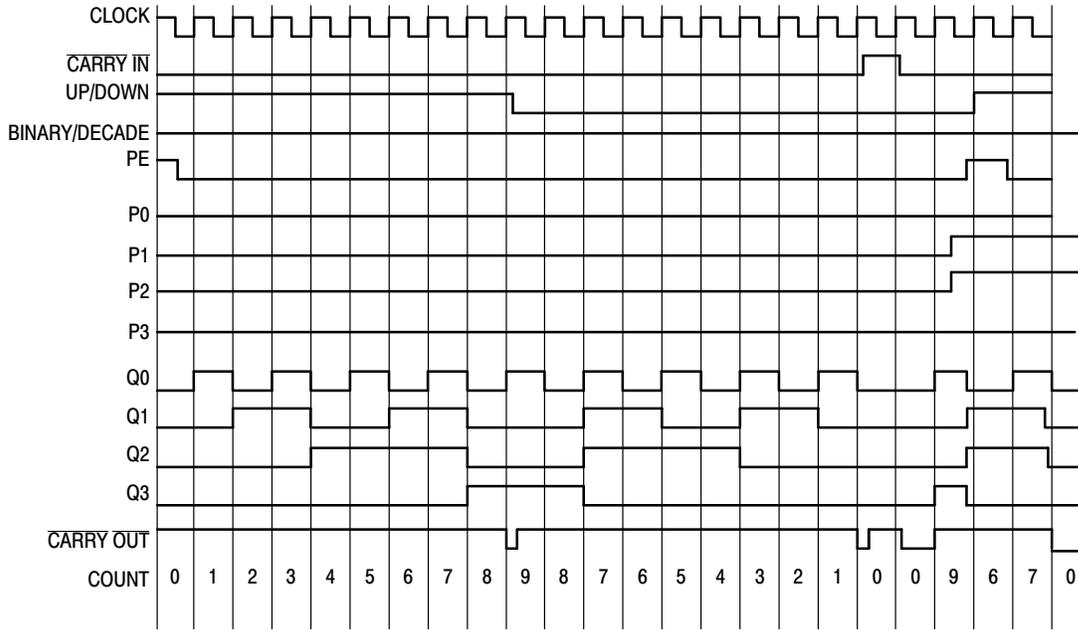**Figure 2. Switching Time Test Circuit and Waveforms**
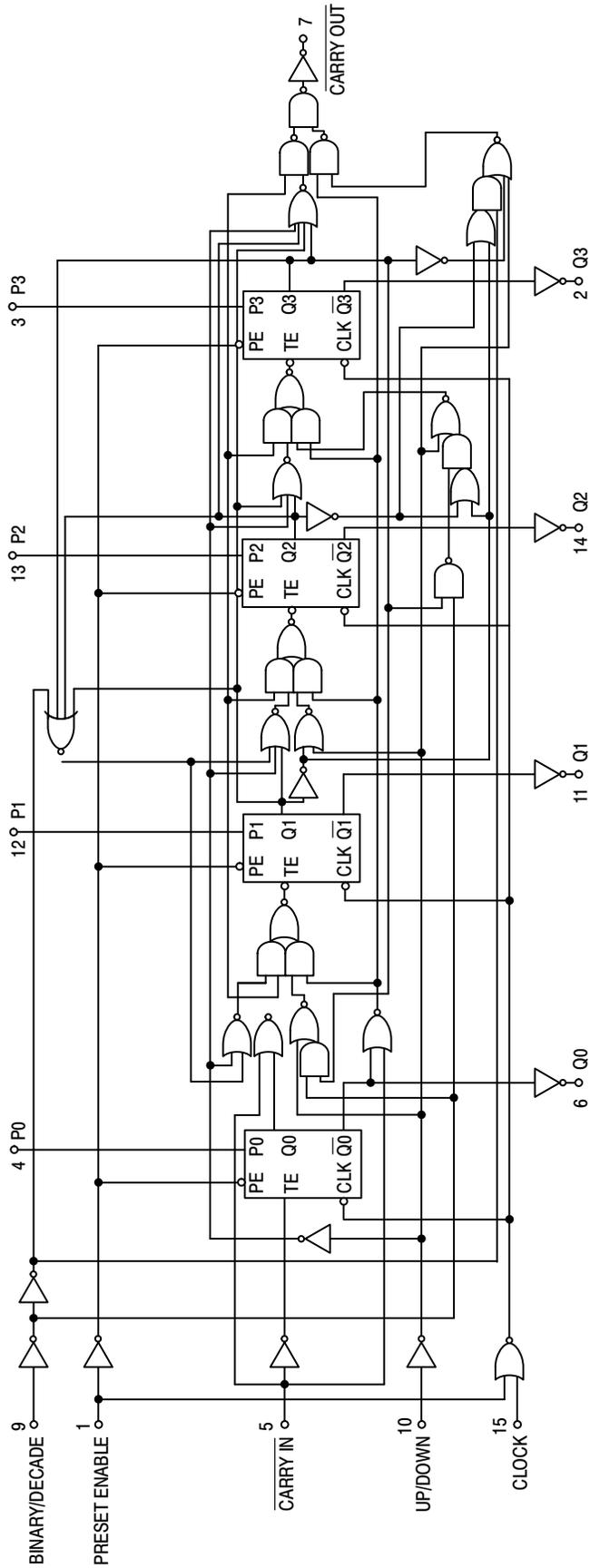
MC14029B

TIMING DIAGRAM

*$t_W \cong 900$ ns @ $V_{DD} = 5$ V

Figure 3. Divide by N BCD Down Counter and Timing Diagram
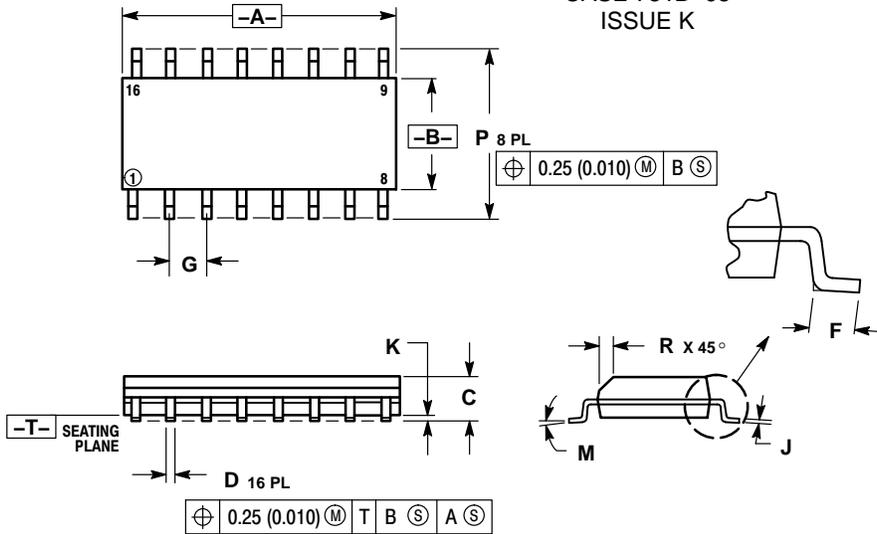**(Shown for N = 123)**

LOGIC DIAGRAM

MC14029B

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B−05
ISSUE K

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS
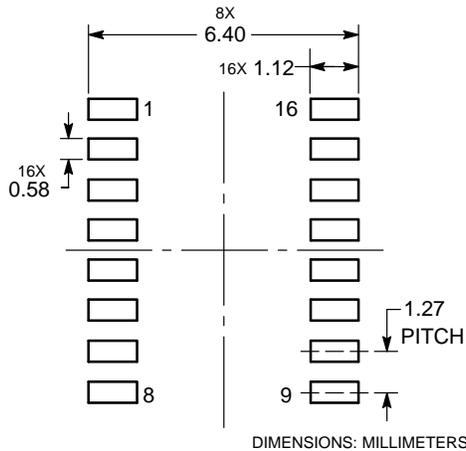
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14029B/D