

# MC14046B

## Phase Locked Loop

The MC14046B phase locked loop contains two phase comparators, a voltage-controlled oscillator (VCO), source follower, and zener diode. The comparators have two common signal inputs, PCA<sub>in</sub> and PCB<sub>in</sub>. Input PCA<sub>in</sub> can be used directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. The self-bias circuit adjusts small voltage signals in the linear region of the amplifier. Phase comparator 1 (an exclusive OR gate) provides a digital error signal PC1<sub>out</sub>, and maintains 90° phase shift at the center frequency between PCA<sub>in</sub> and PCB<sub>in</sub> signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals, PC2<sub>out</sub> and LD, and maintains a 0° phase shift between PCA<sub>in</sub> and PCB<sub>in</sub> signals (duty cycle is immaterial). The linear VCO produces an output signal VCO<sub>out</sub> whose frequency is determined by the voltage of input VCO<sub>in</sub> and the capacitor and resistors connected to pins C1<sub>A</sub>, C1<sub>B</sub>, R1, and R2. The source-follower output SF<sub>out</sub> with an external resistor is used where the VCO<sub>in</sub> signal is needed but no loading can be tolerated. The inhibit input Inh, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode can be used to assist in power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis and multiplication, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle Limited

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>) (Note 2.)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub>	Input Voltage Range (All Inputs)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 3.)	500	mW
T <sub>A</sub>	Operating Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C



ON Semiconductor

<http://onsemi.com>

**MARKING DIAGRAMS**

**PDIP-16**  
**P SUFFIX**  
**CASE 648**

**SOIC-16**  
**DW SUFFIX**  
**CASE 751G**

**SOEIAJ-16**  
**F SUFFIX**  
**CASE 966**

A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week

### ORDERING INFORMATION

Device	Package	Shipping
MC14046BCP	PDIP-16	2000/Box
MC14046BDW	SOIC-16	2350/Box
MC14046BDWR2	SOIC-16	1000/Tape & Reel
MC14046BF	SOEIAJ-16	See Note 1.
MC14046BFEL	SOEIAJ-16	See Note 1.

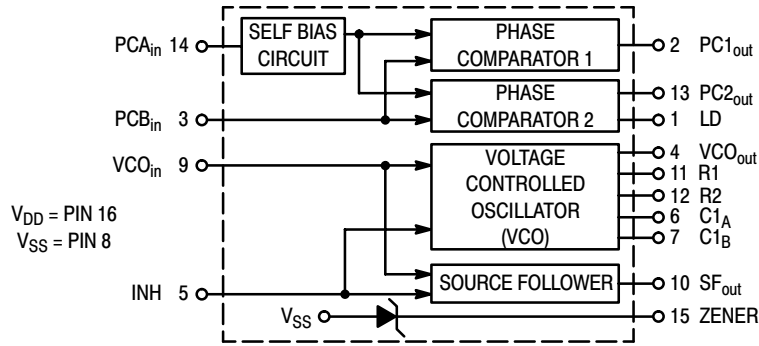
1. For ordering information on the EIAJ version of the SOIC packages, please contact your local ON Semiconductor representative.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

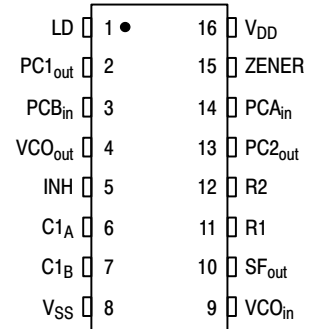
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.

# MC14046B

## BLOCK DIAGRAM



## PIN ASSIGNMENT



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	-55°C		25°C			125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
		10	—	0.05	—	0	0.05	—	0.05	
V <sub>in</sub> = 0 or V <sub>DD</sub>	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
		10	9.95	—	9.95	10	—	9.95	—	
Input Voltage (4.) (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)	"0" Level V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc
		10	—	3.0	—	4.50	3.0	—	3.0	
(V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	"1" Level V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—	Vdc
		10	7.0	—	7.0	5.50	—	7.0	—	
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)	Source I <sub>OH</sub>	5.0	-1.2	—	-1.0	-1.7	—	-0.7	—	mAdc
		10	-0.25	—	-0.2	-0.36	—	-0.14	—	
(V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
Input Current	I <sub>in</sub>	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) Inh = PCA <sub>in</sub> = V <sub>DD</sub> , Zener = VCO <sub>in</sub> = 0 V, PCB <sub>in</sub> = V <sub>DD</sub> or 0 V, I <sub>out</sub> = 0 μA	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
Total Supply Current (5.) (Inh = "0", f <sub>o</sub> = 10 kHz, C <sub>L</sub> = 50 pF, R1 = 1.0 MΩ, R2 = ∞, R <sub>SF</sub> = ∞, and 50% Duty Cycle)	I <sub>T</sub>	5.0	I <sub>T</sub> = (1.46 μA/kHz) f + I <sub>DD</sub>							mAdc
		10	I <sub>T</sub> = (2.91 μA/kHz) f + I <sub>DD</sub>							
		15	I <sub>T</sub> = (4.37 μA/kHz) f + I <sub>DD</sub>							

4. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V<sub>DD</sub> = 5.0 Vdc  
 2.0 Vdc min @ V<sub>DD</sub> = 10 Vdc  
 2.5 Vdc min @ V<sub>DD</sub> = 15 Vdc

5. To Calculate Total Current in General:

$$I_T \approx 2.2 \times V_{DD} \left( \frac{V_{CO_{in}} - 1.65}{R1} + \frac{V_{DD} - 1.35}{R2} \right)^{3/4} + 1.6 \times \left( \frac{V_{CO_{in}} - 1.65}{R_{SF}} \right)^{3/4} + 1 \times 10^{-3} (C_L + 9) V_{DD} f +$$

$$1 \times 10^{-1} V_{DD}^2 \left( \frac{100\% \text{ Duty Cycle of PCA}_{in}}{100} \right) + I_Q \quad \text{where: } I_T \text{ in } \mu\text{A}, C_L \text{ in pF, } V_{CO_{in}}, V_{DD} \text{ in Vdc, } f \text{ in kHz, and } R1, R2, R_{SF} \text{ in M}\Omega, C_L \text{ on VCO}_{out}$$

# MC14046B

## ELECTRICAL CHARACTERISTICS <sup>(6.)</sup> ( $C_L = 50 \text{ pF}$ , $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Minimum	Typical	Maximum	Units
			Device		Device	
Output Rise Time $t_{TLH} = (3.0 \text{ ns/pF}) C_L + 30 \text{ ns}$ $t_{TLH} = (1.5 \text{ ns/pF}) C_L + 15 \text{ ns}$ $t_{TLH} = (1.1 \text{ ns/pF}) C_L + 10 \text{ ns}$	$t_{TLH}$	5.0 10 15	— — —	180 90 65	350 150 110	ns
Output Fall Time $t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{THL}$	5.0 10 15	— — —	100 50 37	175 75 55	ns

### PHASE COMPARATORS 1 and 2

Input Resistance — $PCA_{in}$	$R_{in}$	5.0 10 15	1.0 0.2 0.1	2.0 0.4 0.2	— — —	$M\Omega$
— $PCB_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$
Minimum Input Sensitivity AC Coupled — $PCA_{in}$ C series = 1000 pF, f = 50 kHz	$V_{in}$	5.0 10 15	— — —	200 400 700	300 600 1050	mV p-p
DC Coupled — $PCA_{in}$ , $PCB_{in}$	—	5 to 15	See Noise Immunity			

### VOLTAGE CONTROLLED OSCILLATOR (VCO)

Maximum Frequency ( $VCO_{in} = V_{DD}$ , $C1 = 50 \text{ pF}$ $R1 = 5.0 \text{ k}\Omega$ , and $R2 = \infty$ )	$f_{max}$	5.0 10 15	0.5 1.0 1.4	0.7 1.4 1.9	— — —	MHz
Temperature — Frequency Stability ( $R2 = \infty$ )	—	5.0 10 15	— — —	0.12 0.04 0.015	— — —	%/°C
Linearity ( $R2 = \infty$ ) ( $VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $R1 > 10 \text{ k}\Omega$ ) ( $VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $R1 > 400 \text{ k}\Omega$ ) ( $VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $R1 \geq 1000 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.0 1.0 1.0	— — —	%
Output Duty Cycle	—	5 to 15	—	50	—	%
Input Resistance — $VCO_{in}$	$R_{in}$	15	150	1500	—	$M\Omega$

### SOURCE-FOLLOWER

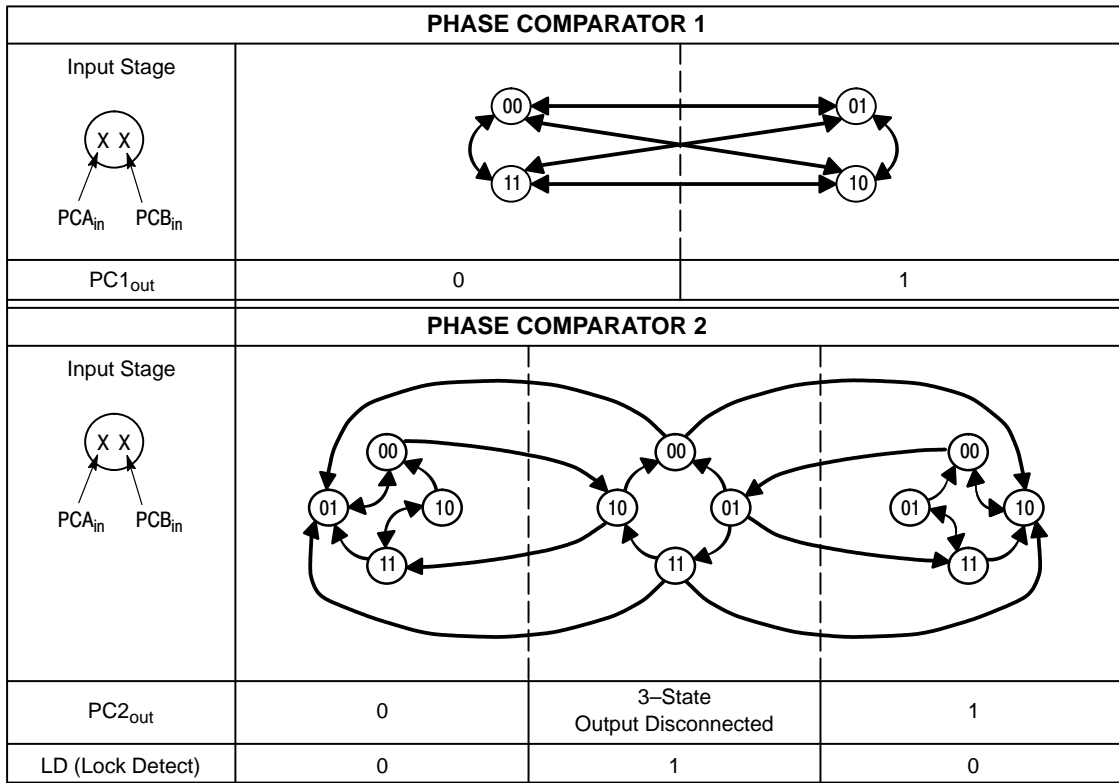
Offset Voltage ( $VCO_{in}$ minus $SF_{out}$ , $R_{SF} > 500 \text{ k}\Omega$ )	—	5.0 10 15	— — —	1.65 1.65 1.65	2.2 2.2 2.2	V
Linearity ( $VCO_{in} = 2.5 \text{ V} \pm 0.3 \text{ V}$ , $R_{SF} > 50 \text{ k}\Omega$ ) ( $VCO_{in} = 5.0 \text{ V} \pm 2.5 \text{ V}$ , $R_{SF} > 50 \text{ k}\Omega$ ) ( $VCO_{in} = 7.5 \text{ V} \pm 5.0 \text{ V}$ , $R_{SF} > 50 \text{ k}\Omega$ )	—	5.0 10 15	— — —	0.1 0.6 0.8	— — —	%

### ZENER DIODE

Zener Voltage ( $I_z = 50 \mu\text{A}$ )	$V_Z$	—	6.7	7.0	7.3	V
Dynamic Resistance ( $I_z = 1.0 \text{ mA}$ )	$R_Z$	—	—	100	—	$\Omega$

6. The formula given is for the typical characteristics only.

# MC14046B



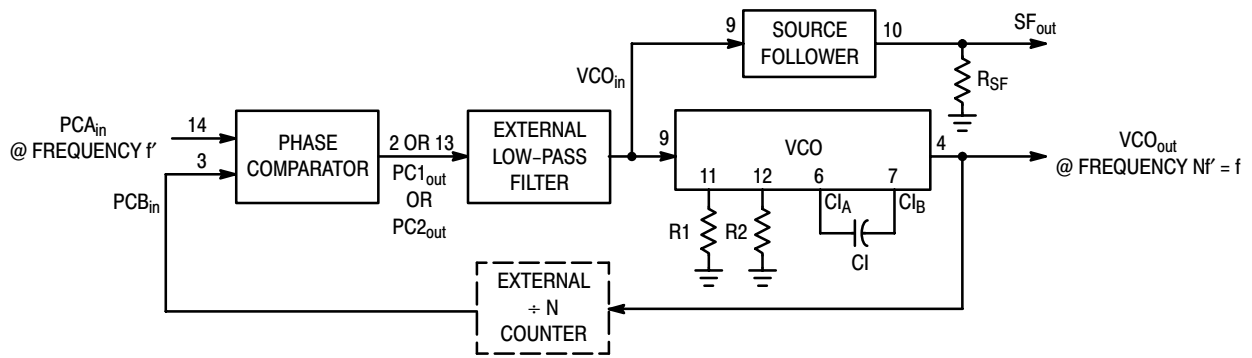
Refer to Waveforms in Figure 3.

**Figure 1. Phase Comparators State Diagrams**

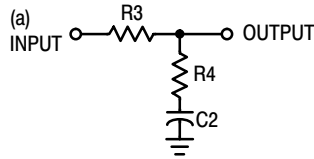
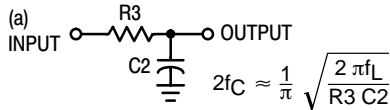
Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input PCA <sub>in</sub> .	VCO in PLL system adjusts to center frequency (f <sub>0</sub> ).	VCO in PLL system adjusts to minimum frequency (f <sub>min</sub> ).
Phase angle between PCA <sub>in</sub> and PCB <sub>in</sub> .	90° at center frequency (f <sub>0</sub> ), approaching 0° and 180° at ends of lock range (2f <sub>L</sub> )	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	High	Low
Lock frequency range (2f <sub>L</sub> ).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2f <sub>L</sub> = full VCO frequency range = f <sub>max</sub> - f <sub>min</sub> .	
Capture frequency range (2f <sub>C</sub> ).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (see Figure 3). f <sub>C</sub> ≤ f <sub>L</sub>	f <sub>C</sub> = f <sub>L</sub>
Center frequency (f <sub>0</sub> ).	The frequency of VCO <sub>out</sub> , when VCO <sub>in</sub> = 1/2 V <sub>DD</sub>	
VCO output frequency (f).	$f_{min} = \frac{1}{R_2(C_1 + 32 \text{ pF})} \quad (V_{CO} \text{ input} = V_{SS})$ $f_{max} = \frac{1}{R_1(C_1 + 32 \text{ pF})} + f_{min} \quad (V_{CO} \text{ input} = V_{DD})$	
Note: These equations are intended to be a design guide. Since calculated component values may be in error by as much as a factor of 4, laboratory experimentation may be required for fixed designs. Part to part frequency variation with identical passive components is typically less than ± 20%.	Where: 10K ≤ R <sub>1</sub> ≤ 1 M 10K ≤ R <sub>2</sub> ≤ 1 M 100pF ≤ C <sub>1</sub> ≤ .01 μF	

**Figure 2. Design Information**

# MC14046B



## Typical Low-Pass Filters



Typically:

$$R_4 C_2 = \frac{6N}{f_{\max}} - \frac{N}{2\pi \Delta f}$$

$$(R_3 + 3,000\Omega) C_2 = \frac{100N\Delta f}{f_{\max}^2} - R_4 C_2$$

$$\Delta f = f_{\max} - f_{\min}$$

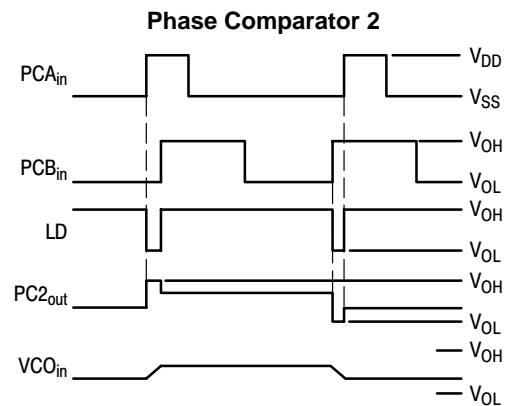
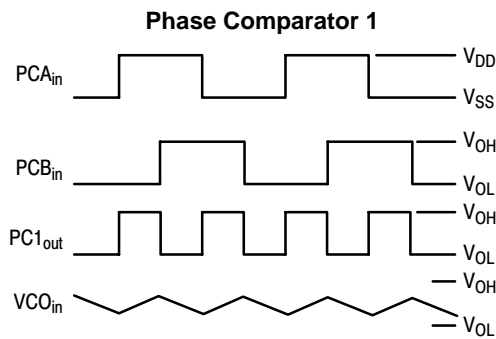
NOTE: Sometimes R3 is split into two series resistors each  $R_3 \div 2$ . A capacitor  $C_C$  is then placed from the midpoint to ground. The value for  $C_C$  should be such that the corner frequency of this network does not significantly affect  $\omega_n$ . In Figure B, the ratio of R3 to R4 sets the damping,  $R_4 \approx (0.1)(R_3)$  for optimum results.

## LOW-PASS FILTER

Definitions:  $N$  = Total division ratio in feedback loop  
 $K\phi = V_{DD}/\pi$  for Phase Comparator 1  
 $K\phi = V_{DD}/4\pi$  for Phase Comparator 2  
 $KVCO = \frac{2\pi \Delta f_{VCO}}{V_{DD} - 2V}$   
 for a typical design  $\omega_n \approx \frac{2\pi f_r}{10}$  (at phase detector input)  
 $\zeta \approx 0.707$

Filter A	Filter B
$\omega_n = \sqrt{\frac{K\phi KVCO}{NR_3 C_2}}$	$\omega_n = \sqrt{\frac{K\phi KVCO}{NC_2(R_3 + R_4)}}$
$\zeta = \frac{N\omega_n}{2K\phi KVCO}$	$\zeta = 0.5 \omega_n (R_3 C_2 + \frac{N}{K\phi KVCO})$
$F(s) = \frac{1}{R_3 C_2 S + 1}$	$F(s) = \frac{R_3 C_2 S + 1}{S(R_3 C_2 + R_4 C_2) + 1}$

## Waveforms



Note: for further information, see:

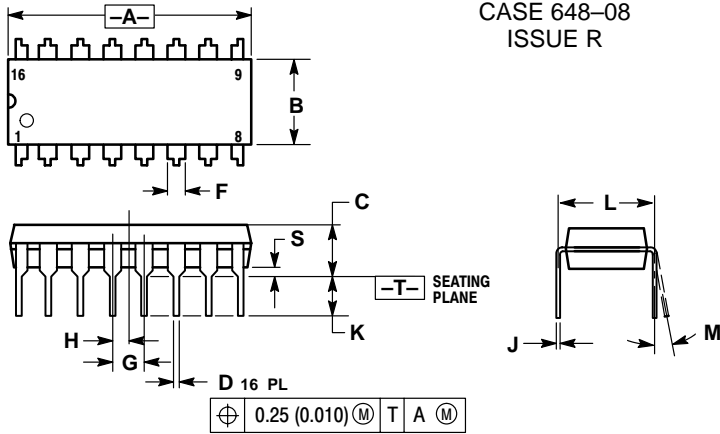
- (1) F. Gardner, "Phase-Lock Techniques", John Wiley and Son, New York, 1966.
- (2) G. S. Moschytz, "Miniature RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
- (3) Garth Nash, "Phase-Lock Loop Design Fundamentals", AN-535, Motorola Inc.
- (4) A. B. Przedpelski, "Phase-Locked Loop Design Articles", AR254, reprinted by Motorola Inc.

Figure 3. General Phase-Locked Loop Connections and Waveforms

# MC14046B

## PACKAGE DIMENSIONS

### PDIP-16 P SUFFIX PLASTIC DIP PACKAGE CASE 648-08 ISSUE R

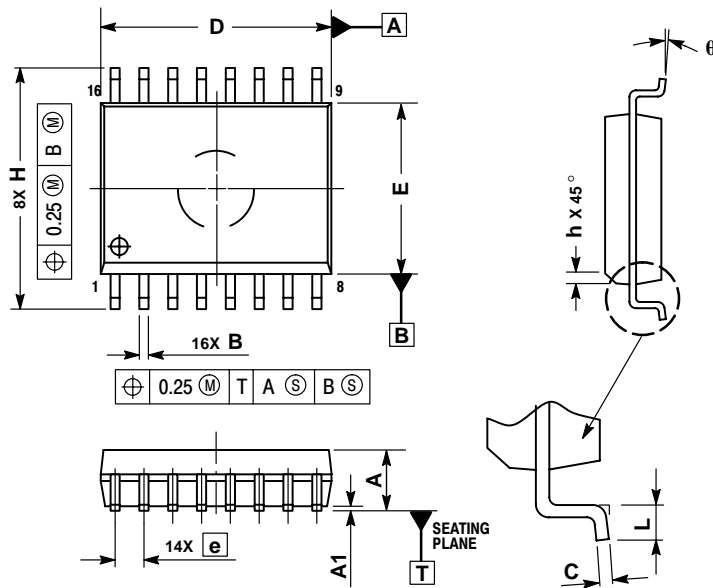


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

### SOIC-16 DW SUFFIX PLASTIC SOIC PACKAGE CASE 751G-03 ISSUE B



NOTES:

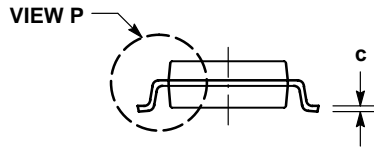
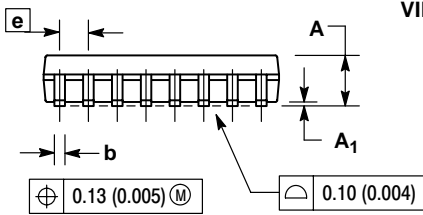
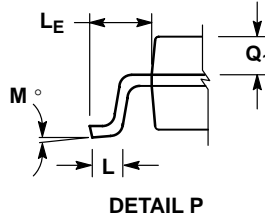
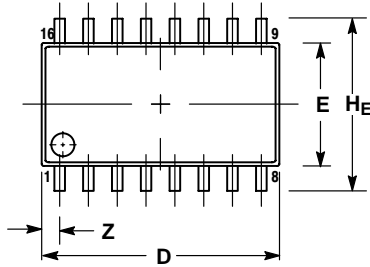
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

# MC14046B

## PACKAGE DIMENSIONS

SOEIAJ-16  
F SUFFIX  
PLASTIC EIAJ SOIC PACKAGE  
CASE 966-01  
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### **NORTH AMERICA Literature Fulfillment:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com  
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**EUROPE:** LDC for ON Semiconductor – European Support

**German Phone:** (+1) 303-308-7140 (Mon-Fri 2:30pm to 7:00pm CET)  
**Email:** ONlit-german@hibbertco.com  
**French Phone:** (+1) 303-308-7141 (Mon-Fri 2:00pm to 7:00pm CET)  
**Email:** ONlit-french@hibbertco.com  
**English Phone:** (+1) 303-308-7142 (Mon-Fri 12:00pm to 5:00pm GMT)  
**Email:** ONlit@hibbertco.com

**EUROPEAN TOLL-FREE ACCESS\*: 00-800-4422-3781**

\*Available from Germany, France, Italy, UK

### **CENTRAL/SOUTH AMERICA:**

**Spanish Phone:** 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)  
**Email:** ONlit-spanish@hibbertco.com

**ASIA/PACIFIC:** LDC for ON Semiconductor – Asia Support

**Phone:** 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)  
**Toll Free** from Hong Kong & Singapore:  
**001-800-4422-3781**  
**Email:** ONlit-asia@hibbertco.com

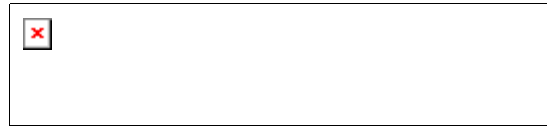
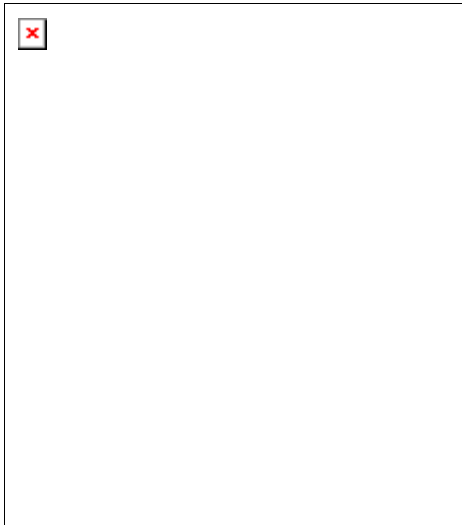
**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031

**Phone:** 81-3-5740-2745  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.

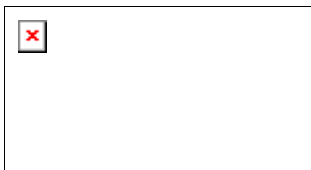




- Press Room**
- Sales & Distribution**
- About Us**
- Quality**
- Trade Shows**
- Investor Relations**
- Employment**
- Products**



- [Product Catalog](#)
- [New Products](#)
- [ON/Cherry Products](#)
- [Documentation](#)
- [Selector Guide](#)
- [On-line Ordering](#)
- [Models](#)
- [Reliability Data](#)
- [PCN](#)
- [Samples Search](#)
- [Order Status](#)
- [Tech Support](#)



Product Quick Links

**Associated Documents**

Item	Short Desc
<a href="#">Application Notes</a>	High Fidelity Switching Audio Amplifiers Using TMOS Power MOSFETs
<a href="#">Data Sheet</a>	Phase Locked Loop

**Device MC14046B**  
**Phase Locked Loop**

The MC14046B phase locked loop contains two phase comparators, a voltage-current source follower, and zener diode. The comparators have two common signal input  $PCA_{in}$  can be used directly coupled to large voltage signals, or indirectly coupled (via small voltage signals). The self-bias circuit adjusts small voltage signals in the line. Phase comparator 1 (an exclusive OR gate) provides a digital error signal  $PC1_{out}$ , which shifts at the center frequency between  $PCA_{in}$  and  $PCB_{in}$  signals (both at 50% duty cycle). Phase comparator 2 (with leading edge sensing logic) provides digital error signals,  $PC2_{out}$  and LD, and between  $PCA_{in}$  and  $PCB_{in}$  signals (duty cycle is immaterial). The linear VCO produces  $VCO_{out}$  whose frequency is determined by the voltage of input  $VCO_{in}$  and the capacitor connected to pins  $C1_A$ ,  $C1_B$ , R1, and R2. The source-follower output  $SF_{out}$  with an input where the  $VCO_{in}$  signal is needed but no loading can be tolerated. The inhibit input inhibits the VCO and source follower to minimize standby power consumption. The zener diode is used for power supply regulation.

Applications include FM and FSK modulation and demodulation, frequency synthesis, frequency discrimination, tone decoding, data synchronization and conditioning, voltage-to-frequency conversion and motor speed control.

**Features:**

- Buffered Outputs Compatible with MHTL and Low-Power TTL
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 to 18 V
- Pin-for-Pin Replacement for CD4046B
- Phase Comparator 1 is an Exclusive Or Gate and is Duty Cycle Limited
- Phase Comparator 2 switches on Rising Edges and is not Duty Cycle

**Orderable Parts**

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	Status
N/A	MC14046BCP	Phase Locked Loop	PDIP	16	<a href="#">648-08</a>	Active
N/A	MC14046BDW	Phase Locked Loop	SOIC	16	<a href="#">751G-03</a>	Active
N/A	MC14046BDWR2	Tape and Reel	SOIC	16	<a href="#">751G-03</a>	Active
N/A	MC14046BF	Phase Locked Loop	MFP	16	<a href="#">966-01</a>	Active
N/A	MC14046BFEL	Tape and Reel	MFP	16	<a href="#">966-01</a>	Active
N/A	MC14046BFL1	Tape and Reel	MFP	16	<a href="#">966-01</a>	LifeTime
N/A	MC14046BFL2	Tape and Reel	MFP	16	<a href="#">966-01</a>	LifeTime
N/A	MC14046BFR1	Tape and Reel	MFP	16	<a href="#">966-01</a>	LifeTime
N/A	MC14046BFR2	Tape and Reel	MFP	16	<a href="#">966-01</a>	LifeTime

[Register](#) | [Site Index](#) | [Contact Us](#) | [Home](#) | [China Site](#)

[Products](#) | [Press Room](#) | [Sales](#) | [About](#) | [Investor](#) | [Employment](#)

© Semiconductor Components Industries, L.L.C., 1999, 2000. All rights reserved. [Terms of use.](#)