KGF12N05

N-Channel 5.5V Power MOSFET

FN8787
Rev 1.00
December 18, 2015

The KGF12N05 is a 5.5V, 1.9mΩ, chip-scale, N-channel, multidirectional current flow MOSFET. The device uses technology that uniquely integrates low cost CMOS and WLCSP fabrication processes. The chip-scale WLCSP package offers small area, low vertical profile and is fully compatible with standard SMT assembly processes. The KGF12N05 device offers unprecedented low on-resistance and total gate charge, outperforming conventional trench MOSFETs and enabling high frequency, low voltage switching. The device offers extremely high power density, reducing the board size of DC/DC converters and other power management systems.

PRODUCT SUMMARY			
I_D	T_A = +25°C	12A	Maximum
$V_{(BR)DSS}$	I_D = 10mA	5.5V	Minimum
$r_{DS(ON)}$	V_{GS} = 4.5V	1.9mΩ	Typical
$r_{DS(ON)}$	V_{GS} = 3.5V	2.1mΩ	Typical
Q_g	I_D = 12A	5nC	Typical
Q_{gd}		1.2nC	Typical

Features

- Industry leading figures of merit: $r_{DS(ON)} \times Q_g$ and $r_{DS(ON)} \times Q_{gd}$
- Low profile/small footprint chip-scale WLCSP package
- High frequency switching
- Known Good FET (KGF) Quality Assurance Process

Applications

- Low thermal resistance
- Point-of-load DC/DC converters
- Portable electronics
- OR'ing diodes

Related Literature

- AN1968, "Unclamped Inductive Switching (UIS) Test and Rating Methodology"

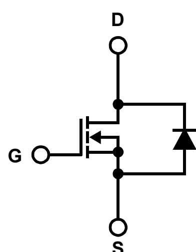


FIGURE 1. EQUIVALENT CIRCUIT

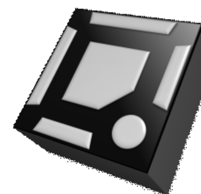


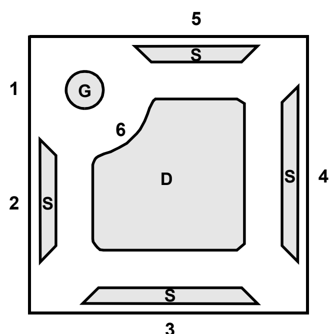
FIGURE 2. N-CHANNEL MOSFET WLCSP PACKAGE

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)
KGF12N05-400-SP	S	-55 to +150	6 Bump WLCSP

Pin Configuration

KGF12N05
(6 BUMP WLCSP)
LAND GRID ARRAY VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	G	Gate of MOSFET
2, 3, 4, 5	S	Source of MOSFET
6	D	Drain of MOSFET

Absolute Maximum Ratings (Note 1)

Drain-to-Source Voltage (V_{DS}) 5.5V
Gate-to-Source Voltage (V_{GS}) . . . . . ±5.5V
Drain Current
Continuous (I_D) 12A
Pulsed (I_{DM}) 40A
Single Pulse Avalanche Current (I_{AS})
L ≤ 50µH, R_G ≤ 25Ω 10A

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JP} (°C/W)
WLCSP Package	50	10

Maximum Power Dissipation (P_D) (Note 2)
T_A = +25°C 2.5W (10s)
T_A = +70°C 1.6W
Junction and Storage Temperature Range (T_J, T_{stg}) . . . . -55°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:
1. T_J = +25°C unless otherwise noted.
2. When mounted on 1 inch square 2oz copper clad FR-4.

Electrical Characteristics T_J = +25°C unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 3)	TYP (Note 4)	MAX (Note 3)	UNIT
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	V_{GS} = 0V, I_D = 10mA	5.5			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 3.5V, V_{GS} = 0V, T_J = +25°C			1	µA
		V_{DS} = 5.5V, V_{GS} = 0V, T_J = +25°C			25	µA
		V_{DS} = 5.5V, V_{GS} = 0V, T_J = +125°C			250	µA
I_{GSS}	Gate-Body Leakage	V_{GS} = 5.5V, V_{DS} = 0V			150	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	0.52	0.62	0.80	V
$r_{DS(ON)}$	Drain-to-Source On-State Resistance	V_{GS} = 3.5V, I_D = 12A		2.1	2.6	mΩ
		V_{GS} = 4.5V, I_D = 12A		1.9	2.4	mΩ
C_{iss}	Input Capacitance	V_{DS} = 5.5V, V_{GS} = 0V, f = 1MHz		750	940	pF
C_{oss}	Output Capacitance			940	1175	pF
C_{rss}	Reverse Transfer Capacitance			230	300	pF
C_{iss}	Input Capacitance	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz		790	990	pF
C_{oss}	Output Capacitance			1450	1800	pF
C_{rss}	Reverse Transfer Capacitance			270	400	pF
r_g	Gate Resistance	V_{DS} = 0V, f = 1MHz		1.0		Ω
Q_g	Total Gate Charge	V_{GS} = 3.5V, I_D = 12A, V_{DS} = 4.4V		5.0	6.0	nC
Q_{gs}	Gate-to-Source Charge			1.1	1.5	nC
Q_{gd}	Gate-to-Drain Charge			1.2	2.0	nC
Q_g	Total Gate Charge	V_{GS} = 4.5V, I_D = 12A, V_{DS} = 4.4V		6.2	7.0	nC
t_{rr}	Source-to-Drain Reverse Recovery Time	I_S = 3A, di/dt = 33A/µs		100		ns
V_{SD}	Diode Forward Voltage	I_S = 5A, V_{GS} = 0V		0.65	1.00	V

NOTES:
3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
4. Typical values are for T_A = +25°C.

Typical Performance Curves

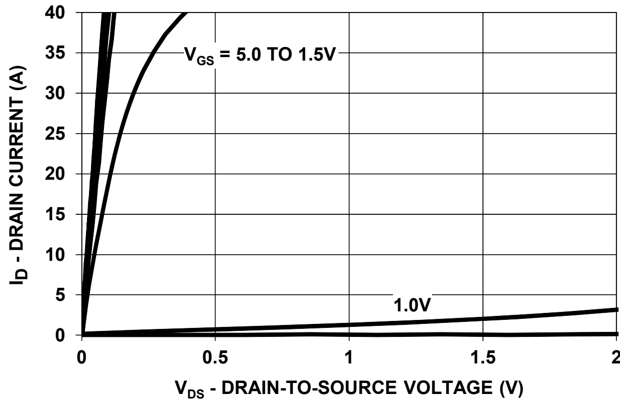


FIGURE 3. OUTPUT CHARACTERISTICS

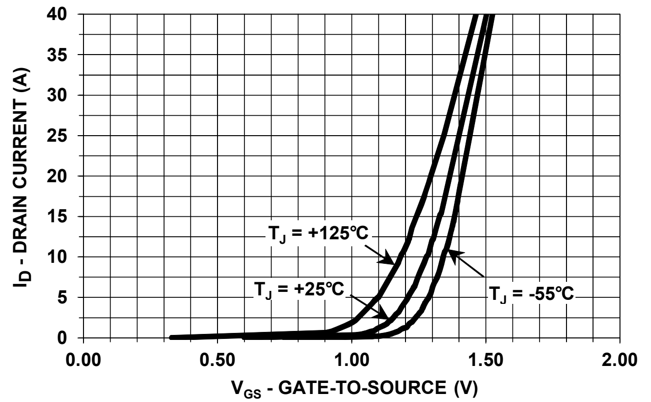


FIGURE 4. TRANSFER CHARACTERISTICS

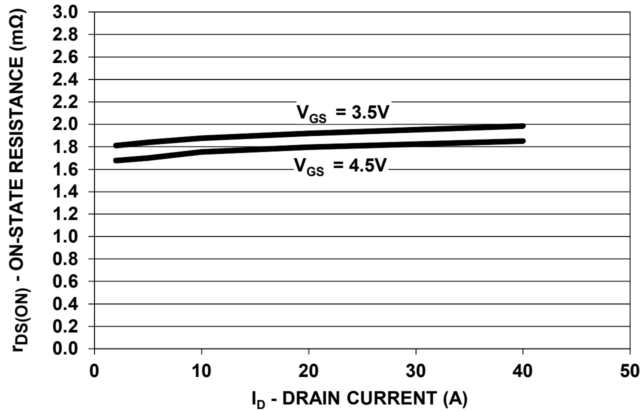


FIGURE 5. ON-RESISTANCE vs DRAIN CURRENT

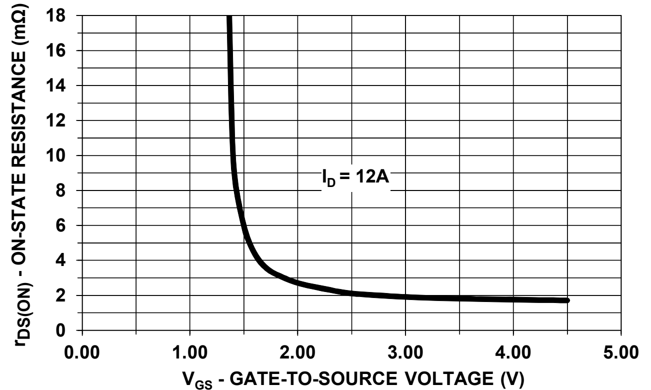


FIGURE 6. ON-RESISTANCE vs GATE-TO-SOURCE VOLTAGE

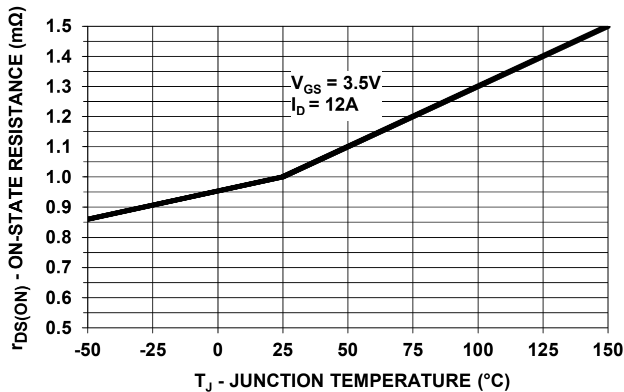


FIGURE 7. ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

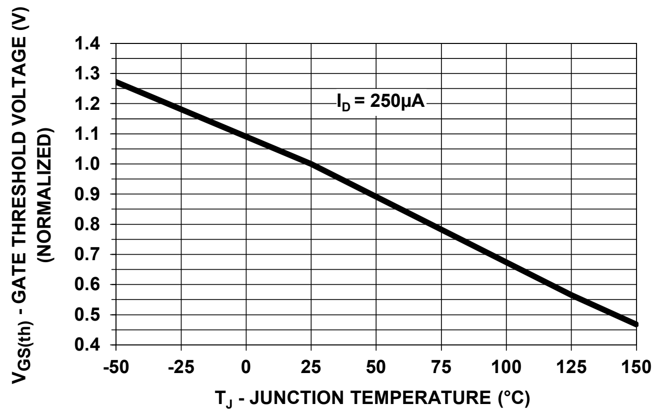


FIGURE 8. GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

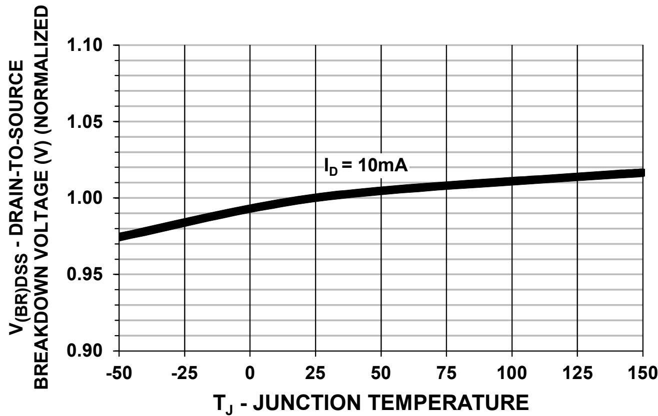


FIGURE 9. DRAIN-TO-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

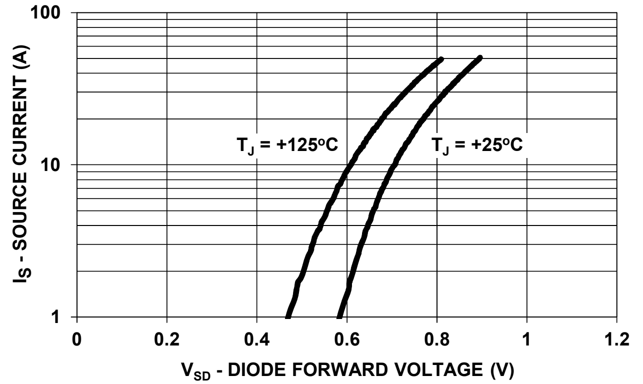


FIGURE 10. SOURCE-TO-DRAIN DIODE FORWARD VOLTAGE

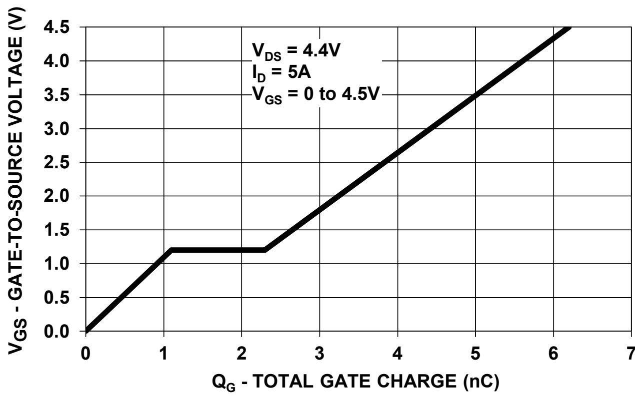


FIGURE 11. GATE CHARGE

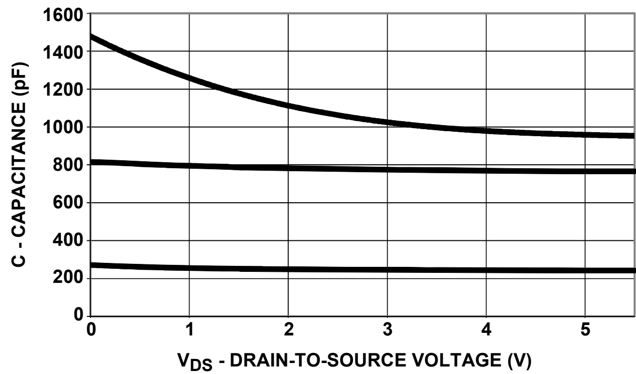


FIGURE 12. CAPACITANCE

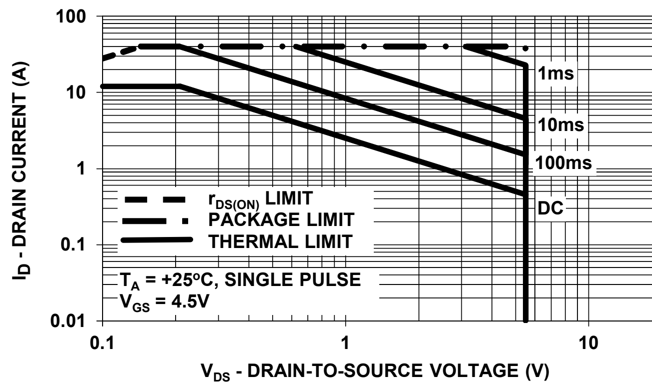


FIGURE 13. MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

Typical Performance Curves (Continued)

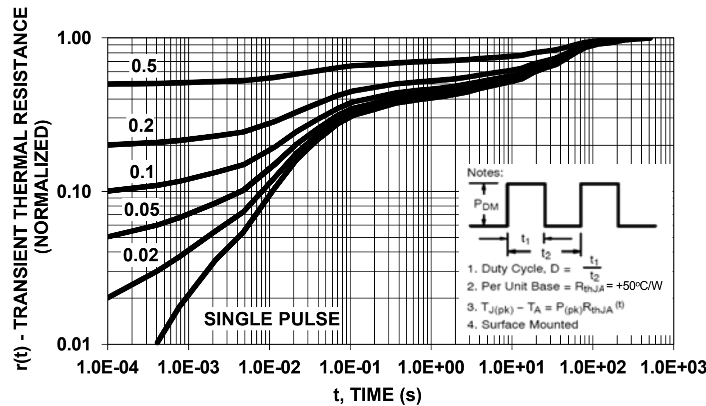


FIGURE 14. TRANSIENT THERMAL RESPONSE, JUNCTION-TO-AMBIENT

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
December 18, 2015	FN8787.1	Added "Note 1. T_J = +25°C unless otherwise noted." to Abs Max on page 3.
October 30, 2015	FN8787.0	Initial release

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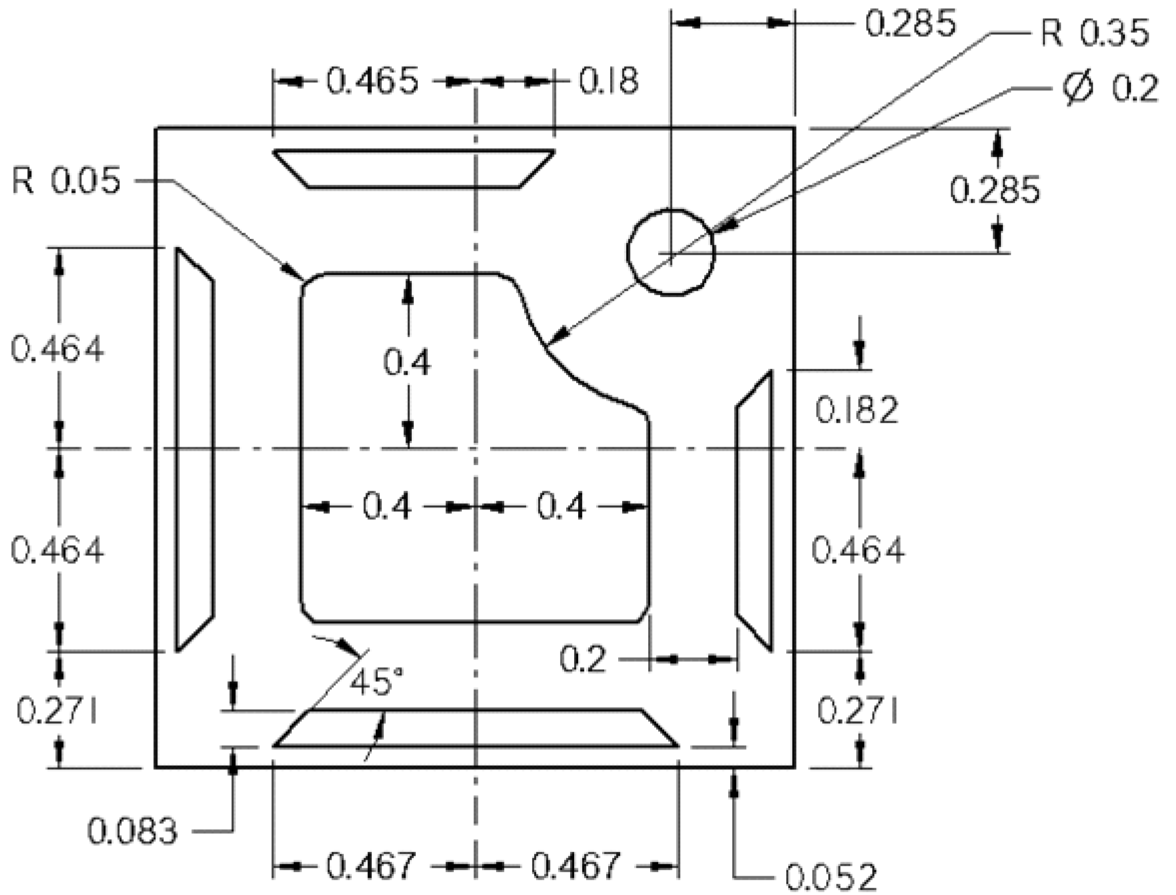
Dimensional Outline and Pad Layout



All dimensions in mm

Die Size = 1.47mm ± 0.005mm (square)

Pad Thickness = 3µm NiAu

Die Thickness = 400µm ± 15µm