300mA Variable / Fixed Output LDO Regulators

Pb Free ROHM Electronic Components   RoHS Directive Compliance

BDxxGA3WEFJ / BDxxGA3WNUX

●General Description

BDxxGA3WEFJ / BDxxGA3WNUX series devices are LDO regulators with output current capability of 0.3A. It has an output voltage accuracy of ±1%. Both fixed and variable output voltage devices are available. The variable output voltage can be varied from 1.5V to 13.0V using external resistors. Various fixed output voltage devices that do not use external resistors are also available. These LDO regulators are available in HTSOP-J8 / VSON008X2030 package and can be used in wide variety of digital appliances. It has built-in over current protection to protect the device when output is shorted, 0μA shutdown mode, and thermal shutdown circuit to protect the device during thermal over-load conditions. These LDO regulators are usable with ceramic capacitors that enable a smaller layout and longer life.

●Features

- High accuracy reference voltage circuit
- Built-in Over Current Protection (OCP)
- Built-in Thermal Shut Down circuit (TSD)
- Zero μA shutdown mode

●Key Specifications

- Input power supply voltage range: 4.5V to 14.0V
- Output voltage range(Variable type): 1.5V to 13.0V
- Output voltage(Fixed type): 1.5V/1.8V/2.5V/3.0V/3.3V 5.0V/6.0V/7.0V/8.0V/9.0V/10V/12V
- Output current: 0.3A (Max.)
- Shutdown current: 0μA(Typ.)
- Operating temperature range: -25℃ to +85℃

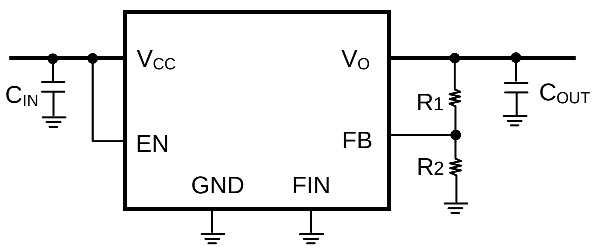
●Package

	(Typ.)	(Typ.)	(Max.)
HTSOP-J8 (EFJ)	4.90mm x	6.00mm x	1.00mm
VSON008X2030 (NUX)	2.00mm x	3.00mm x	0.60mm

HTSOP-J8 (EFJ)

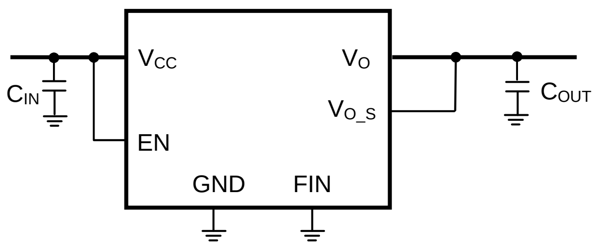
VSON008X2030 (NUX)

●Typical Application Circuit



C_{IN}, C_{OUT} : Ceramic Capacitor

Variable type output voltage



C_{IN}, C_{OUT} : Ceramic Capacitor

Fixed type output voltage

○Product structure : Silicon monolithic integrated circuit ○This product is not designed to have protection against radioactive rays.

●Ordering Information

B D x x G A 3 W y y y - z z

Part Number	Output voltage	Input Voltage	Output Current	Shutdown Mode	Package	Packaging and forming specification
	00:Variable 15:1.5V 18:1.8V 25:2.5V 30:3.0V 33:3.3V 50:5.0V 60:6.0V 70:7.0V 80:8.0V 90:9.0V J0:10.0V J2:12.0V	G:15V	A3:0.3A	"W":Included	EFJ :HTSOP-J8 NUX:VSON008X2030	E2:Emboss tape reel (HTSOP-J8) TR:Emboss tape reel (VSON008X2030)

●Line up

xx	Output Voltage(V)	Product Name	
00	variable	BD00GA3WEFJ-E2	BD00GA3WNUX-TR
15	1.5	BD15GA3WEFJ-E2	BD15GA3WNUX-TR*1
18	1.8	BD18GA3WEFJ-E2	BD18GA3WNUX-TR*1
25	2.5	BD25GA3WEFJ-E2	BD25GA3WNUX-TR*1
30	3.0	BD30GA3WEFJ-E2	BD30GA3WNUX-TR*1
33	3.3	BD33GA3WEFJ-E2	BD33GA3WNUX-TR*1
50	5.0	BD50GA3WEFJ-E2	BD50GA3WNUX-TR*1
60	6.0	BD60GA3WEFJ-E2	BD60GA3WNUX-TR*1
70	7.0	BD70GA3WEFJ-E2	BD70GA3WNUX-TR*1
80	8.0	BD80GA3WEFJ-E2	BD80GA3WNUX-TR*1
90	9.0	BD90GA3WEFJ-E2	BD90GA3WNUX-TR*1
J0	10.0	BDJ0GA3WEFJ-E2	BDJ0GA3WNUX-TR*1
J2	12.0	BDJ2GA3WEFJ-E2	BDJ2GA3WNUX-TR*1

*1 under development

●Block Diagram

BD00GA3WEFJ (Variable type output voltage)

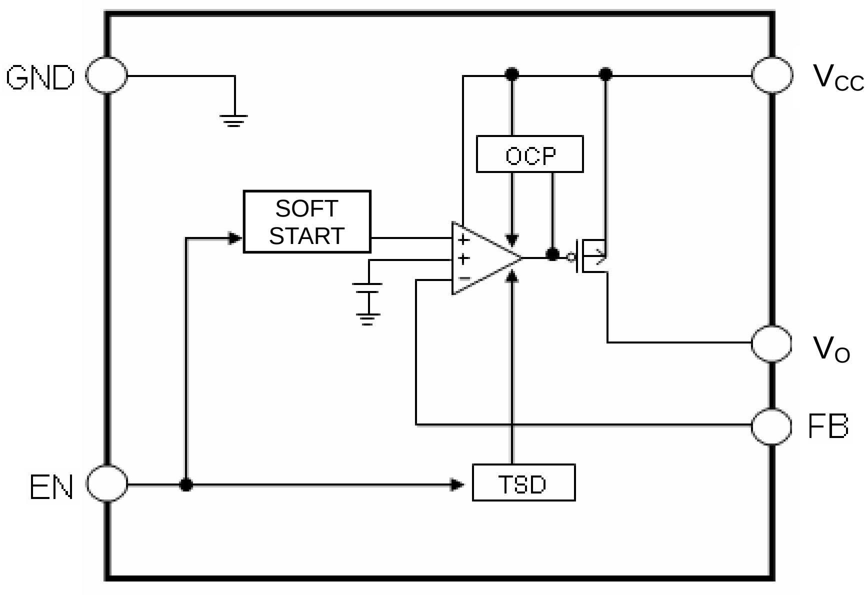
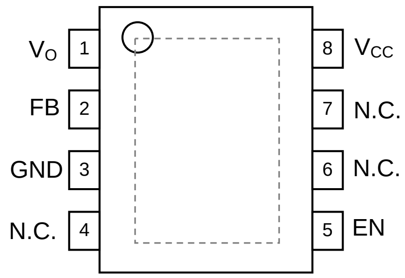
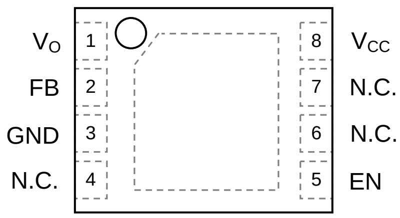


Figure 1. Block Diagram

●Pin Configuration (TOP VIEW)



(HTSOP-J8)



(VSON008X2030)

●Pin Description

Pin No.	Pin name	Pin Function
1	V_O	Output pin
2	FB	Feedback pin
3	GND	GND pin
4	N.C.	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C.	No Connection (Connect to GND or leave OPEN)
7	N.C.	No Connection (Connect to GND or leave OPEN)
8	V_{CC}	Input pin
Reverse	FIN	Substrate(Connect to GND)

●Block Diagram

BDxxGA3WEFJ (Fixed type output voltage)

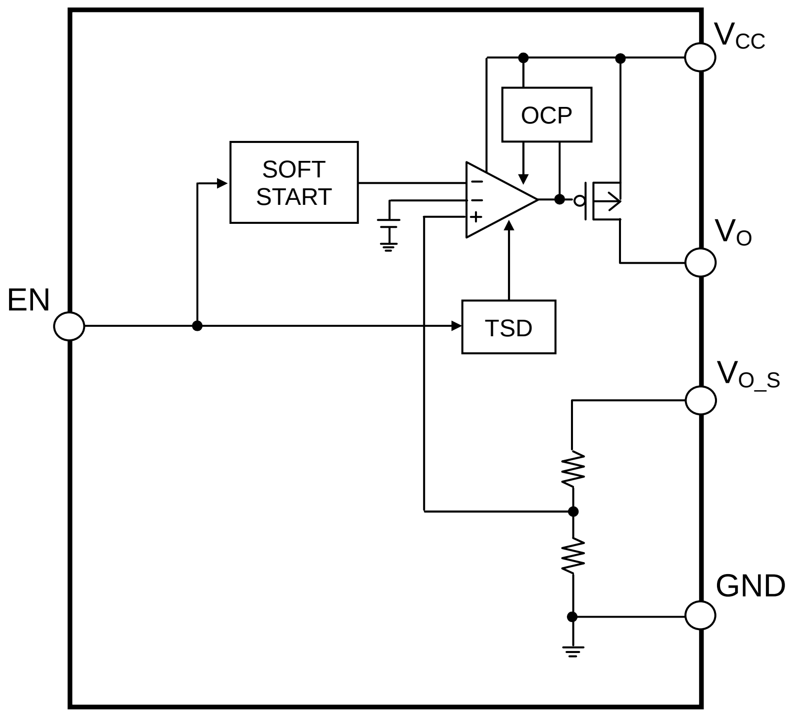
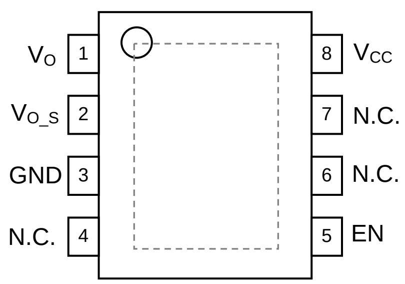
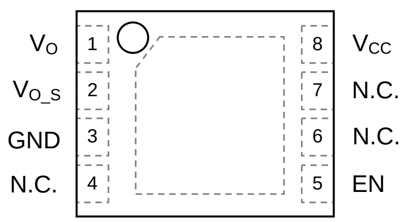


Figure 2. Block Diagram

●Pin Configuration (TOP VIEW)



(HTSOP-J8)



(VSON008X2030)

●Pin Description

Pin No.	Pin name	Pin Function
1	V_O	Output pin
2	V_{O_S}	Output voltage monitor pin
3	GND	GND pin
4	N.C.	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C.	No Connection (Connect to GND or leave OPEN)
7	N.C.	No Connection (Connect to GND or leave OPEN)
8	V_{CC}	Input pin
Reverse	FIN	Substrate(Connect to GND)

●Absolute Maximum Ratings (Ta=25℃)

Parameter		Symbol	Limits	Unit
Power supply voltage		V_{CC}	15.0 *2	V
EN voltage		V_{EN}	15.0	V
Power dissipation	HTSOP-J8	Pd*3	2110 *3	mW
	VSON008X2030	Pd*4	1700*4	
Operating Temperature Range		Topr	-25 to +85	℃
Storage Temperature Range		Tstg	-55 to +150	℃
Junction Temperature		Tjmax	+150	℃

*2 Not to exceed Pd
*3 Reduced by 16.9mW/℃ for temperature above 25℃. (When mounted on a two-layer glass epoxy board with 70mm×70mm×1.6mm dimension)
*4 Reduced by 13.6mW/℃ for temperature above 25℃. (When mounted on a four-layer glass epoxy board with 114.3mm×76.2mm×1.6mm dimension)

●Recommended Operating Range (Ta=25℃)

Parameter	Symbol	Min.	Max.	Unit
Input power supply voltage	V_{CC}	4.5	14.0	V
EN voltage	V_{EN}	0.0	14.0	V
Output voltage setting range	V_O	1.5	13.0	V
Output current	I_O	0.0	0.3	A

●Electrical Characteristics (Unless otherwise specified, Ta=25℃, EN=3V, V_{CC}=6V, R_1=43kΩ, R_2=8.2kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Circuit current at shutdown mode	I_{SD}	-	0	5	μA	V_{EN}=0V, OFF mode
Bias current	I_{CC}	-	600	900	μA	
Line regulation	Reg.I	-1	0.5	1	%	V_{CC}=(V_O+0.9V)→14.0V
Load regulation	Reg I_O	-1.5	0.5	1.5	%	I_O=0→0.3A
Minimum dropout Voltage	V_{CO}	-	0.6	0.9	V	V_{CC}=5V, I_O=0.3A
Output reference voltage(Variable type)	V_{FB}	0.792	0.800	0.808	V	I_O=0A
Output voltage(Fixed type)	V_O	V_O×0.99	V_O	V_O×1.01	V	I_O=0A
EN Low voltage	V_{EN} (Low)	0	-	0.8	V	
EN High voltage	V_{EN} (High)	2.4	-	14.0	V	
EN Bias current	I_{EN}	1	3	9	μA	

●Typical Performance Curves
(Unless otherwise specified, Ta=25℃, EN=3V, V_{CC}=6V, R_1=43kΩ, R_2=8.2kΩ)

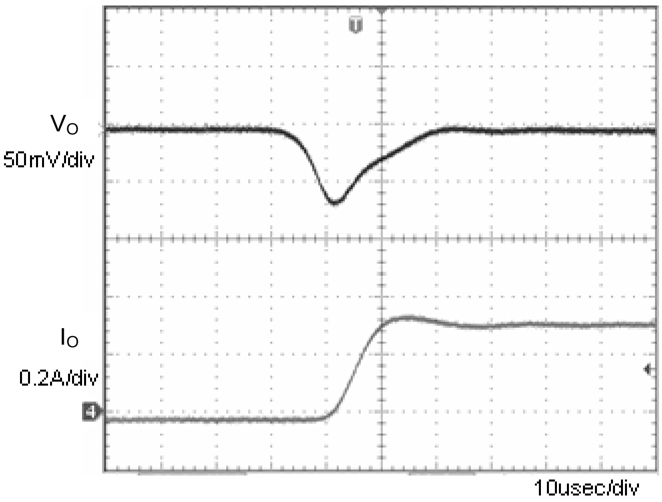


Figure 3.
Transient Response
(0→0.3A)
Co=1µF

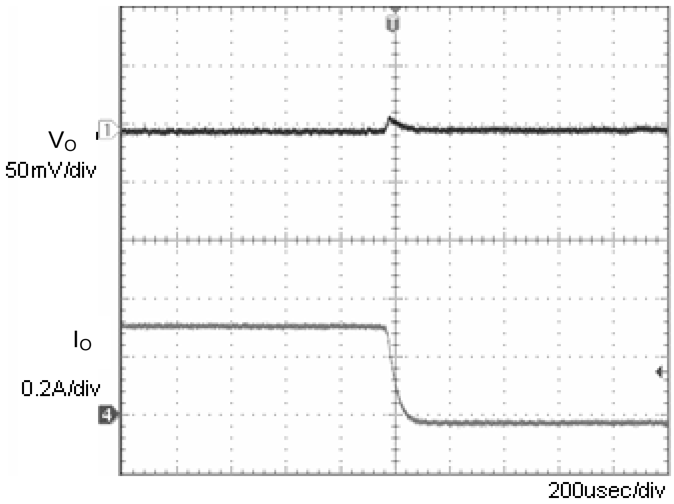


Figure 4.
Transient Response
(0.3→0A)
Co=1µF

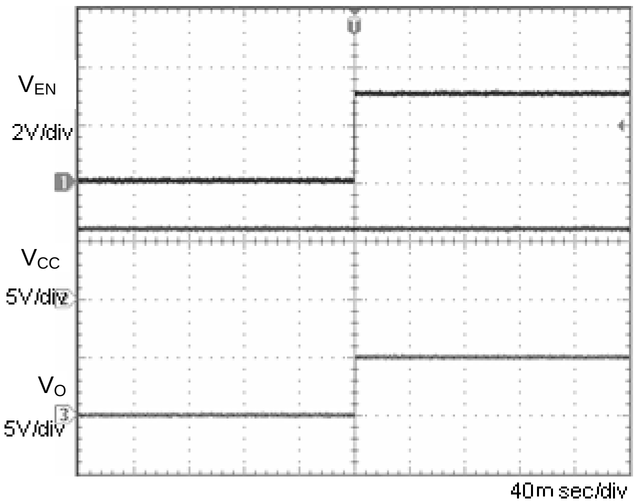


Figure 5.
Input sequence 1
Co=1µF

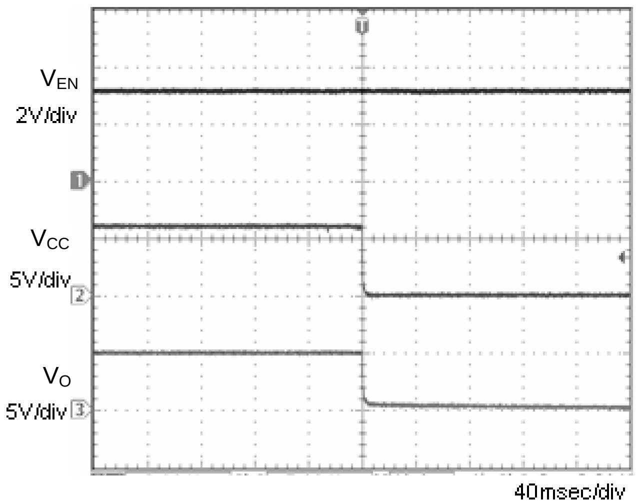


Figure 6.
OFF sequence 1
Co=1µF

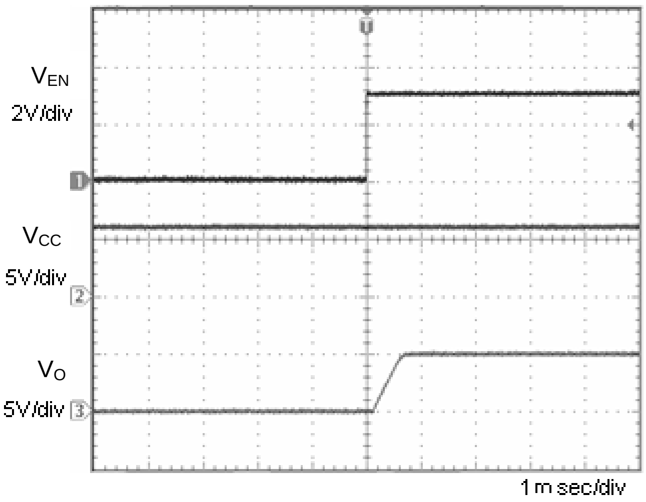


Figure 7.
Input sequence 2
Co=1µF

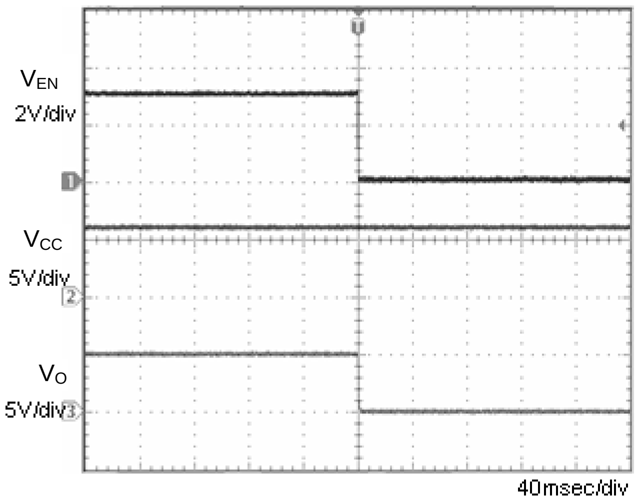


Figure 8.
OFF sequence 2
Co=1µF

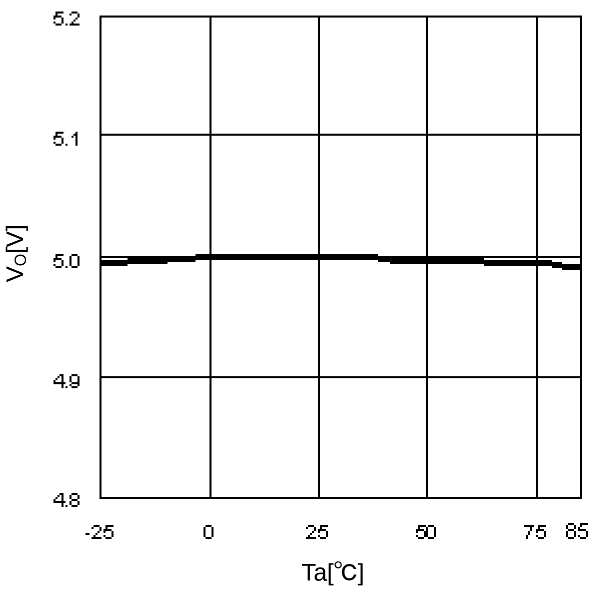


Figure 9.
Ta-V_O (I_O=0mA)

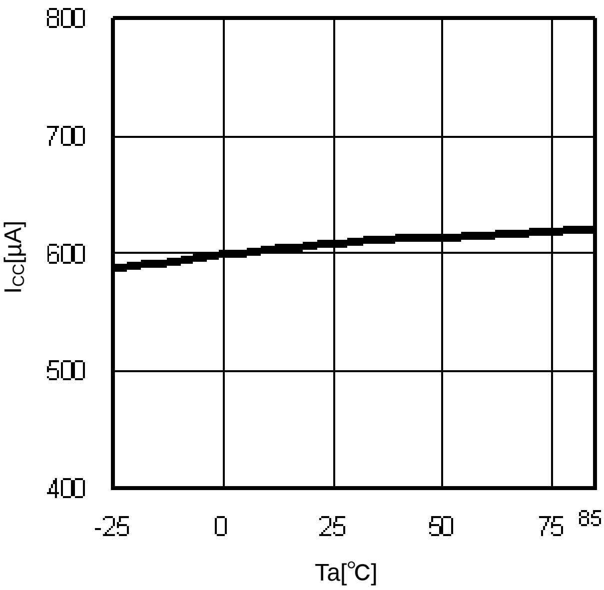


Figure 10.
Ta-I_{CC}

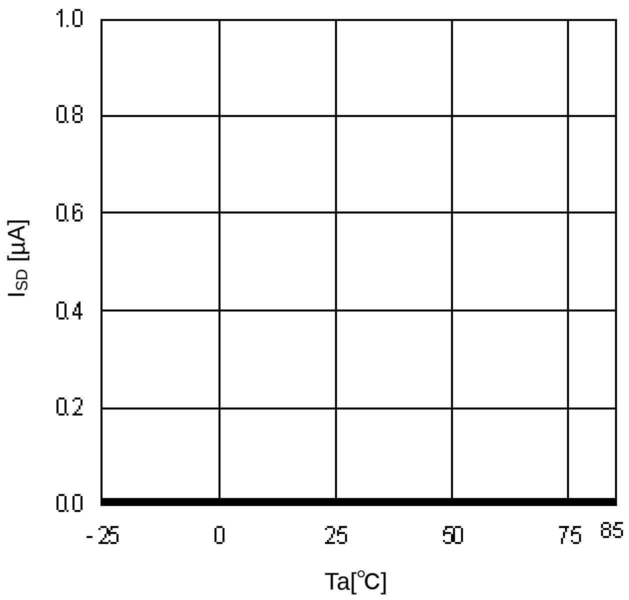


Figure 11.
Ta-I_{SD}
(V_{EN}=0V)

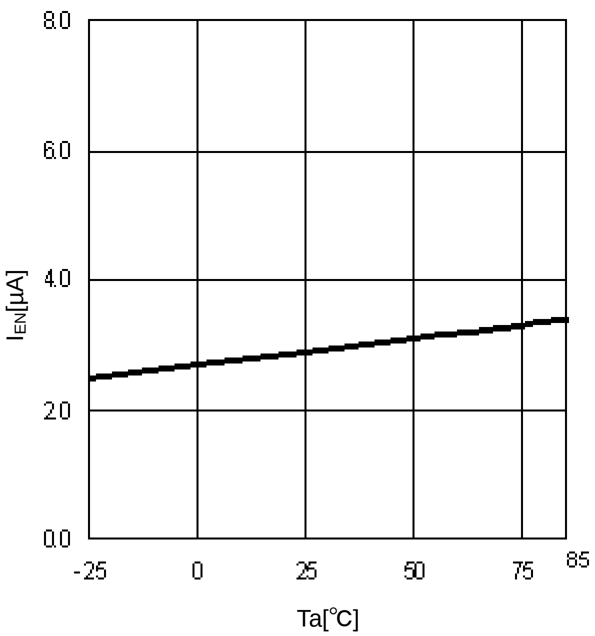


Figure 12.
Ta-I_{EN}

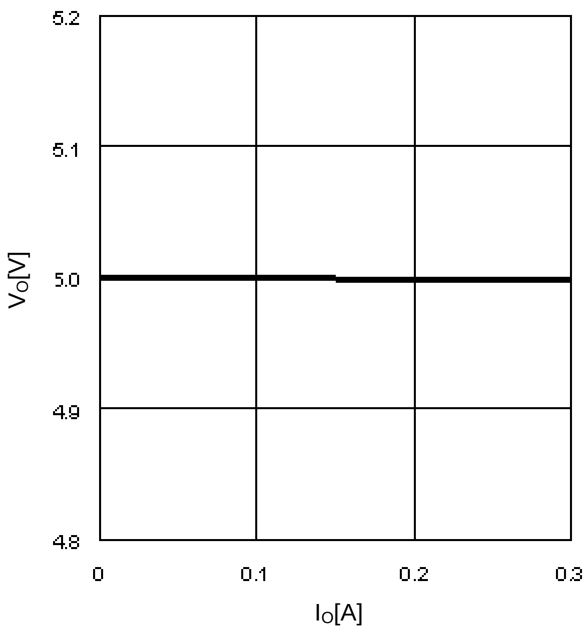


Figure 13.
I_O-V_O

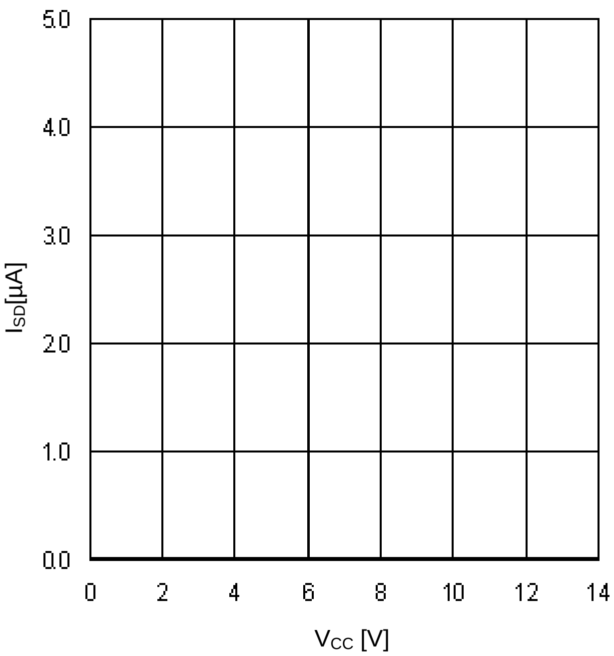


Figure 14.
V_{CC}-I_{SD}
(V_{EN}=0V)

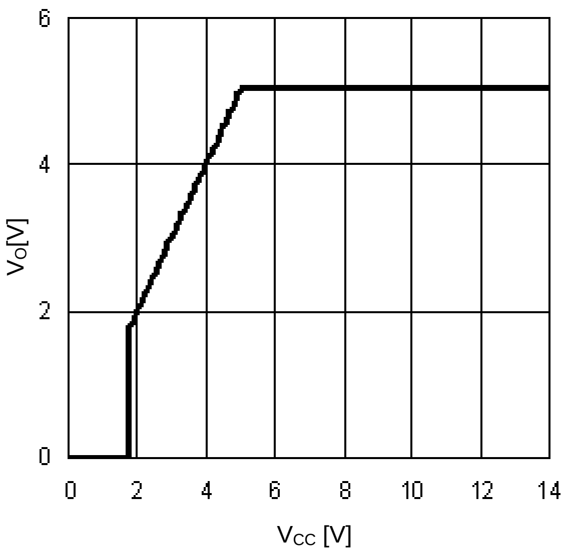


Figure 15.
V_{CC}-V_O (I_O=0mA)

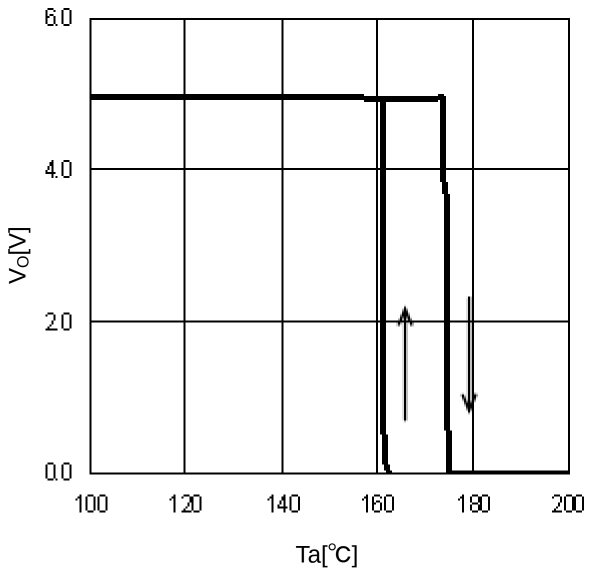


Figure 16.
TSD (I_O=0mA)

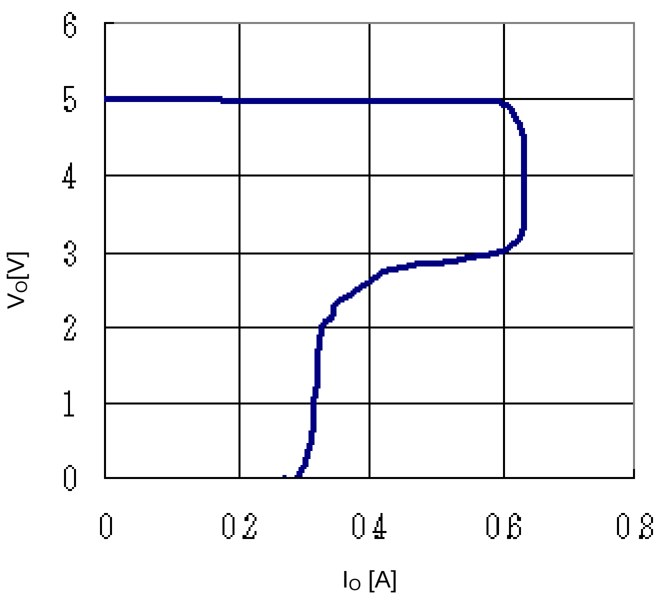


Figure 17.
OCP

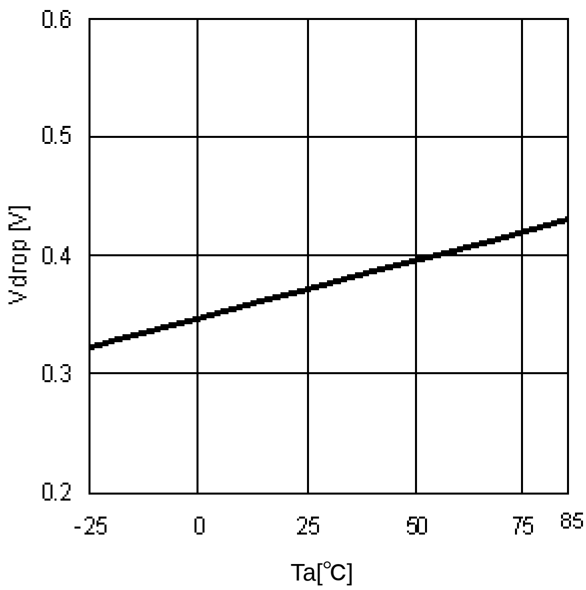


Figure 18.
Minimum dropout Voltage1
（V_{CC}=5V、I_O=0.3A）

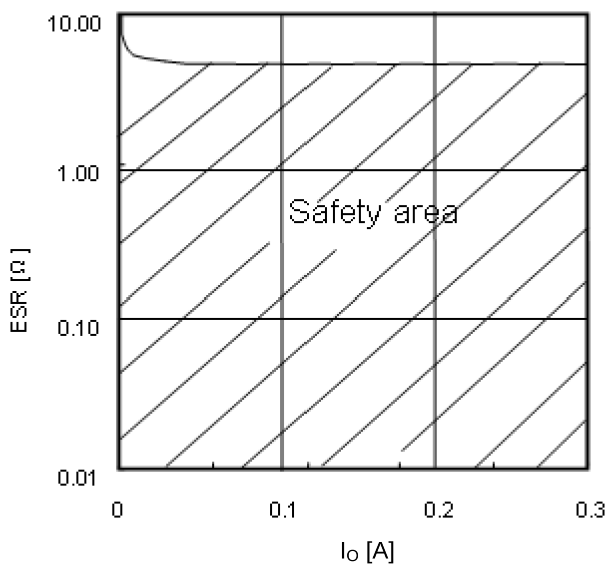


Figure 19.
ESR-Io characteristics

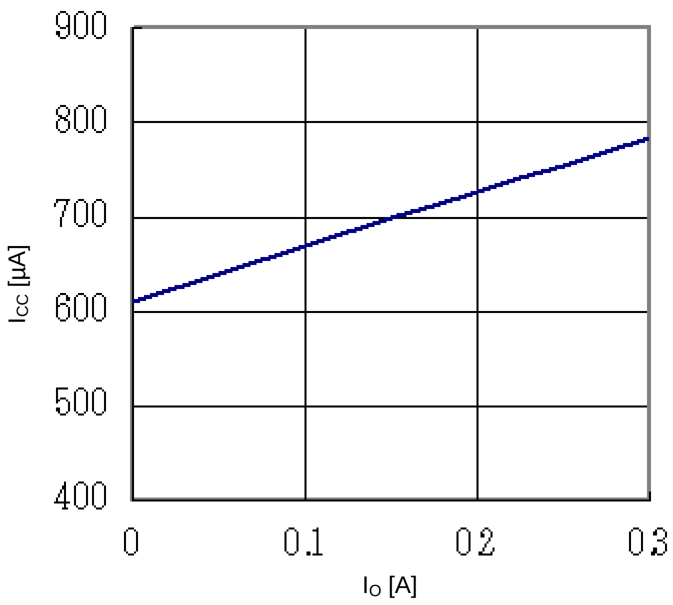


Figure 20.
I_O-I_{CC}

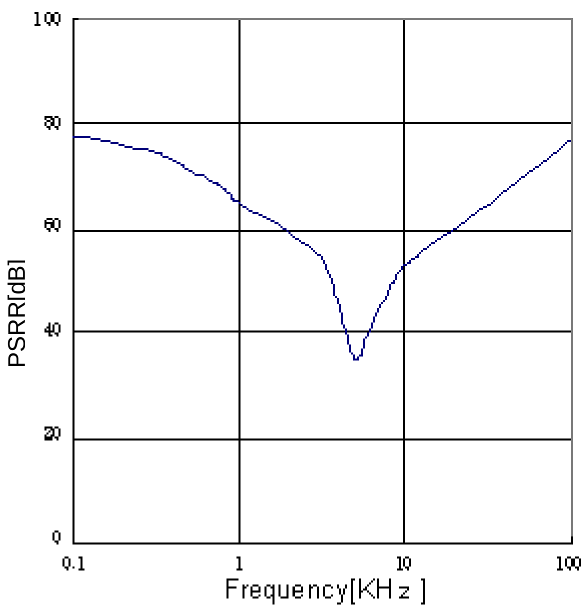


Figure 21.
PSRR (I_O=0mA)

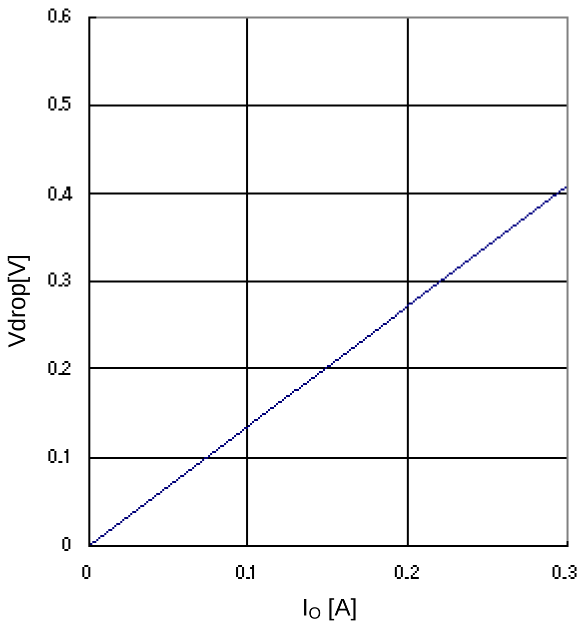


Figure 22.
Minimum dropout Voltage 2
(V_{CC}=4.5V、Ta=25℃)

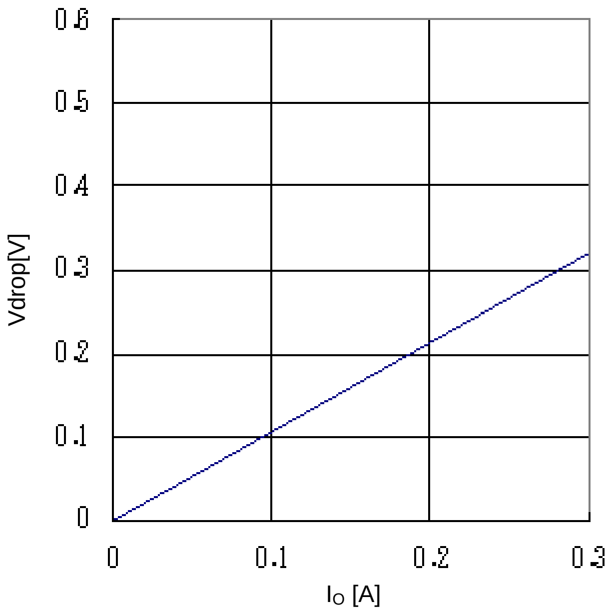


Figure 23.
Minimum dropout Voltage 3
（V_{CC}=6V、Ta=25℃）

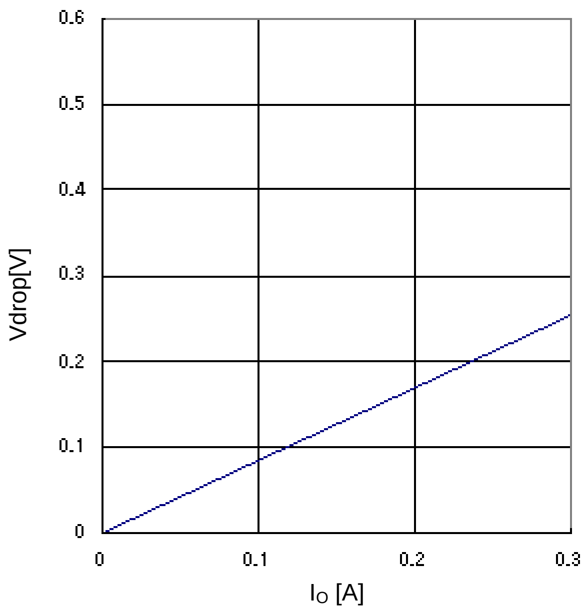


Figure 24.
Minimum dropout Voltage 4
（V_{CC}=8V、Ta=25℃）

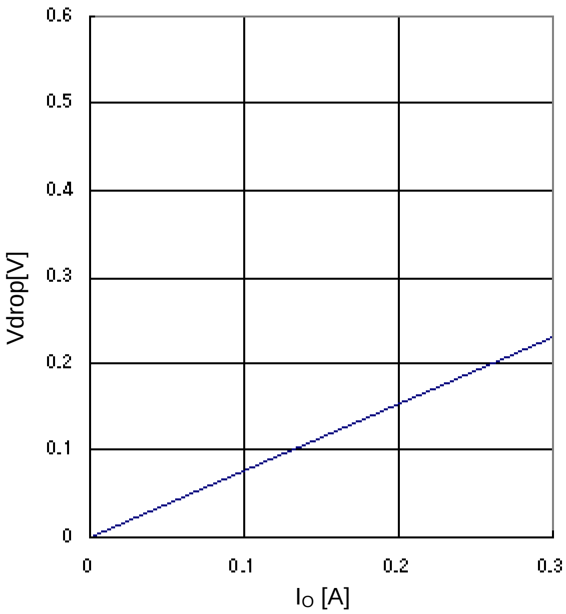


Figure 25.
Minimum dropout Voltage 5
（V_{CC}=10V、Ta=25℃）

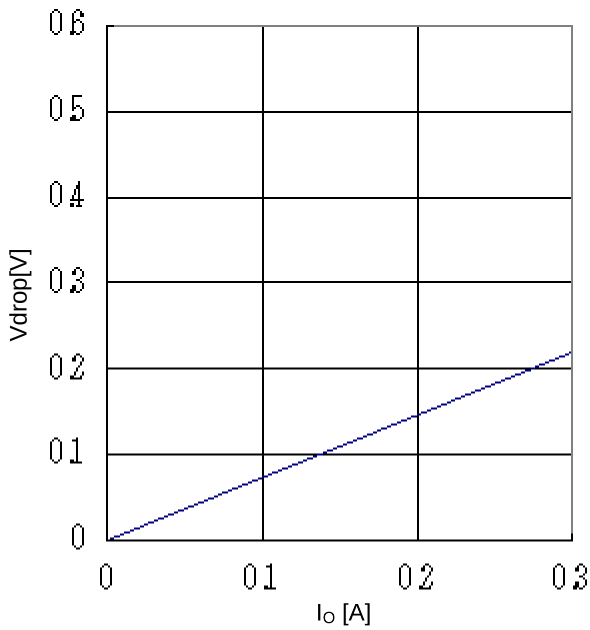
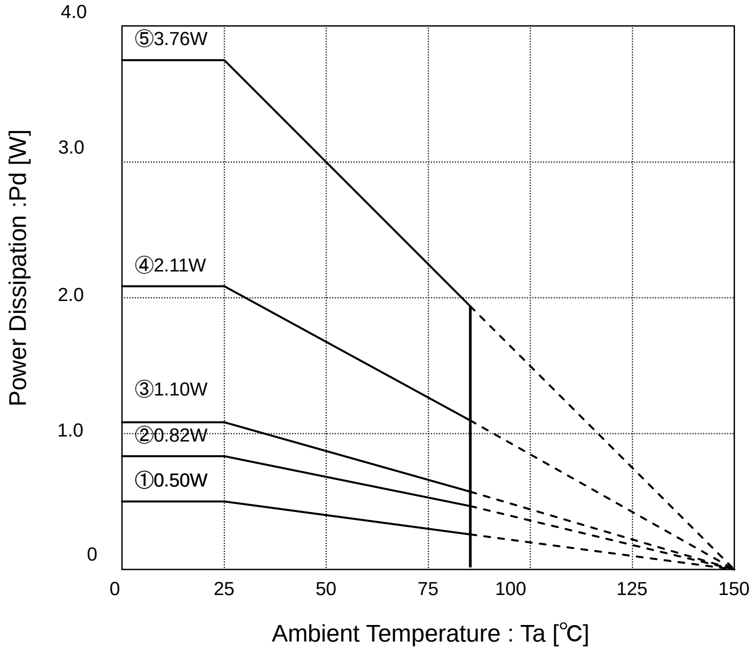


Figure 26.
Minimum dropout Voltage 6
（V_{CC}=12V、Ta=25℃）

●Power Dissipation

◎HTSOP-J8

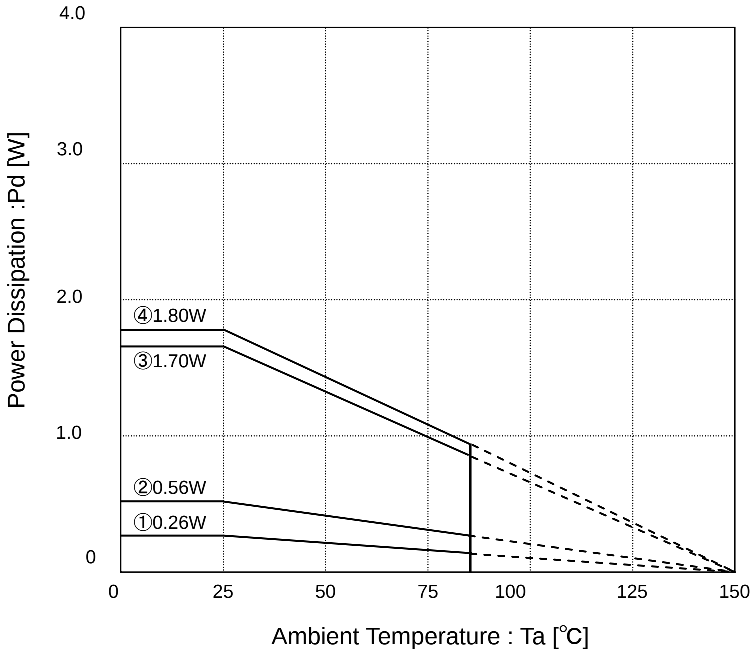


Measurement condition: mounted on a ROHM board

PCB size: 70mm × 70mm × 1.6mm
(PCB with thermal via)
・Solder the thermal pad to Ground

① IC only
θ j-a=249.5℃/W
② 1-layer（copper foil : 0mm×0mm）
θ j-a=153.2℃/W
③ 2-layer（copper foil : 15mm×15mm）
θ j-a=113.6℃/W
④ 2-layer（copper foil : 70mm×70mm）
θ j-a=59.2℃/W
⑤ 4-layer（copper foil : 70mm×70mm）
θ j-a=33.3℃/W

◎VSON008X2030



Measurement condition: mounted on a ROHM board

PCB size: 114.3mm × 76.2mm × 1.6 mm

・Solder the thermal pad to Ground

① IC only
θ j-a=480.8℃/W
② 1-layer（copper foil : $0mm^2$）
θ j-a=223.2℃/W
③ 4-layer（copper foil : $5655mm^2$,
4th layer copper foil : thermal land）
θ j-a=73.5℃/W
④ 4-layer（copper foil at 2nd, 3rd, 4th layers : $5655mm^2$）
θ j-a=69.4℃/W

As the power consumption increases above the maximum allowable power dissipation of the chip, the temperature across the chip also increases. When considering thermal design for the regulator, operation should be maintained within the following conditions:

1. Ambient temperature Ta can be not higher than 85℃.
2. Chip junction temperature (Tj) can be not higher than 150℃.

Chip junction temperature can be determined as follows:

Calculation based on ambient temperature (Ta)

Tj=Ta+θj-a×W

＜Reference values＞

θj-a: HTSOP-J8

153.2℃/W 1-layer PCB(copper foil 0mm×0mm)
113.6℃/W 2-layer PCB(copper foil 15mm×15mm)
59.2℃/W 2-layer PCB(copper foil 70mm×70mm)
33.3℃/W 4-layer PCB (copper foil 70mm×70mm)
PCB size: 70mm×70mm×1.6mm (PCB with thermal via)

θj-a: VSON008X2030

223.2℃/W 1-layer PCB(copper foil $0mm^2$)
73.5℃/W 4-layer PCB (2^{nd}, 3^{rd} copper foil $5655mm^2$, 4^{th} layer copper foil : thermal land)
69.4℃/W 4-layer PCB (copper foil $5655mm^2$)
PCB size: 114.3mm×76.2mm×1.6mm

Most of the heat loss that occurs in the BDxxGA3WEFJ / BDxxGA3WNUX series is generated from the output Pch FET. Power loss is determined by the voltage drop across V_{CC}-V_O and the output current. Be sure to confirm the system's input and output voltages, as well as the output current conditions in relation to the power dissipation characteristics of the V_{CC} and V_O in the design. Bearing in mind that the power dissipation may vary substantially depending on the PCB employed, it is important to consider PCB size based on thermal design and power dissipation characteristics of the chip with the PCB.

Power consumption [W] = $\{$Input voltage (V_{CC}) - Output voltage (V_O)$\}$ × I_O(Ave)

Example: Where V_{CC}=5.0V, V_O=3.3V, I_O (Ave) = 0.1A,

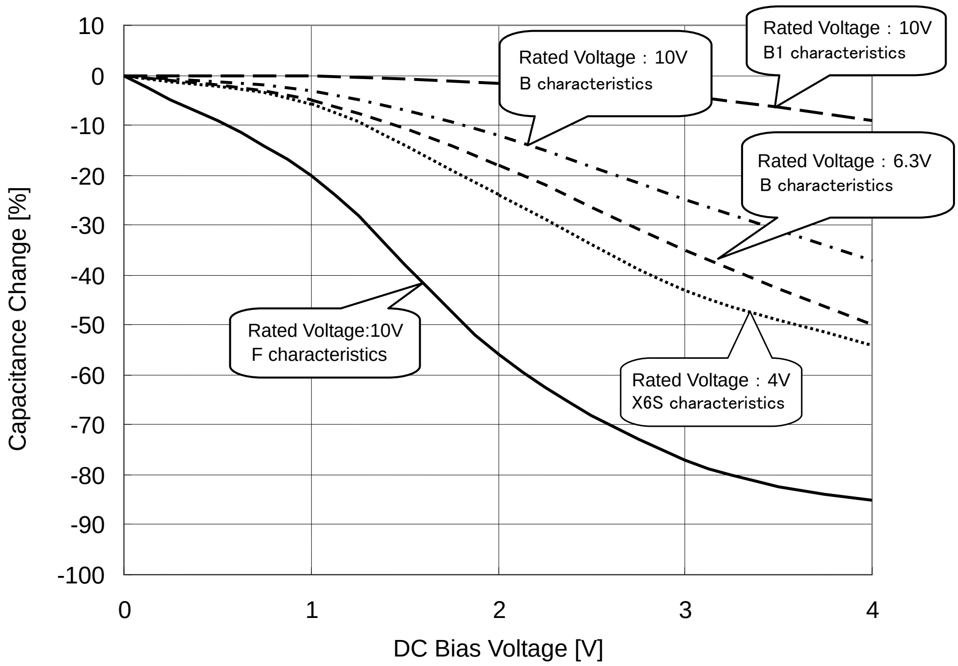
Power consumption [W] = $\{$5.0V - 3.3V$\}$ × 0.1A

=0.17W

●Input and Output Capacitor

It is recommended that a capacitor is placed near pins between input pin and GND as well as output pin and GND. The input capacitor becomes more necessary when the power supply impedance is high or when the PCB trace has significant length. Also, as for a capacitor between output pin and GND, the greater the capacitance, the more stable the output will be depending on the load and line voltage variations. However, please check the actual functionality of this part by mounting on a board for the actual application. Ceramic capacitors usually have different thermal and equivalent series resistance characteristics and may degrade gradually over continued use.

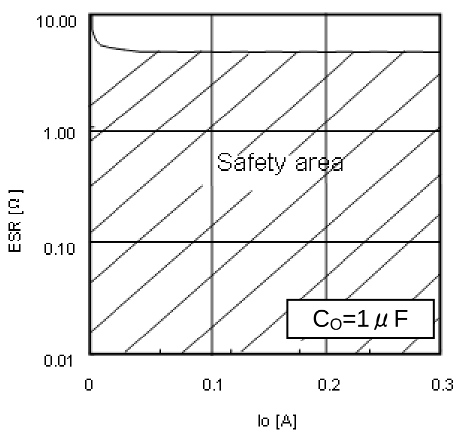
For additional details, please check with the manufacturer and select the best ceramic capacitor for your application.



Ceramic capacitor capacity – DC bias characteristics
(Characteristics example)

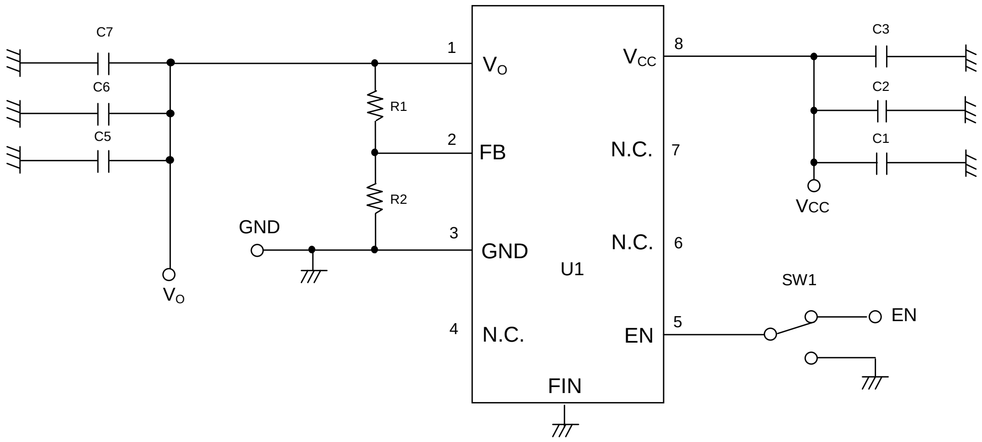
●Equivalent Series Resistance ESR (ceramic capacitor etc.)

To prevent oscillation, please attach a capacitor between V_O and GND. Capacitors usually have ESR (Equivalent Series Resistance). Operation will be stable in ESR-I_O range shown in the right. Ceramic, tantalum and electronic capacitors have different ESR values, so please be sure to use a capacitor that operates in the stable operating region shown in the right. Finally, please evaluate in the actual application.



ESR – I_O characteristics

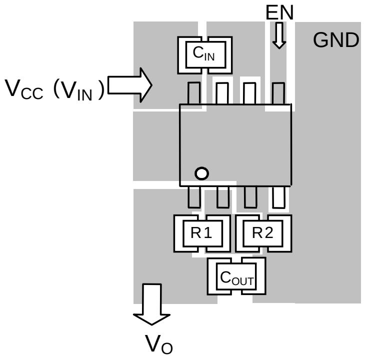
●**Evaluation Board Circuit**



●**Evaluation Board Parts List**

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	43kΩ	MCR01PZPZF4302	ROHM	C4	-	-	-
R2	8.2kΩ	MCR01PZPZF8201	ROHM	C5	1µF	CM105B105K16A	KYOCERA
R3	-	-	-	C6	-	-	-
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	1µF	CM105B105K16A	KYOCERA	C10	-	-	-
C2	-	-	-	U1	-	BDxxGA3WEFJ / BDxxGA3WNUX	ROHM
C3	-	-	-	U2	-	-	-

●**Board Layout**



・Input capacitor C_{IN} connected to V_{CC} (V_{IN}) should be placed as close as possible to V_{CC}(V_{IN}) pin and use wide layout. Output capacitor C_{OUT} should also be placed as close as possible to IC pin. In case connected to inner layer GND plane, please use several through hole.

・FB pin has comparatively high impedance and can be affected by noise, so floating capacitance should be small as possible. Please be careful of this during layout.

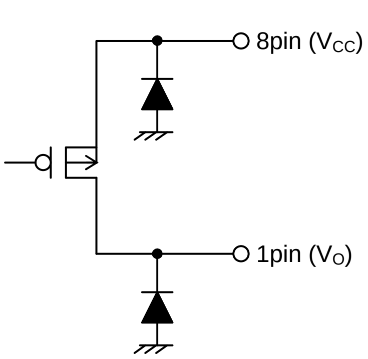
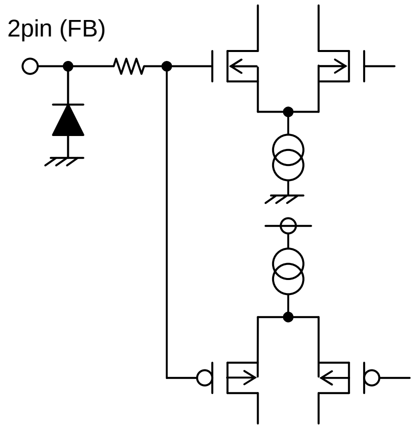
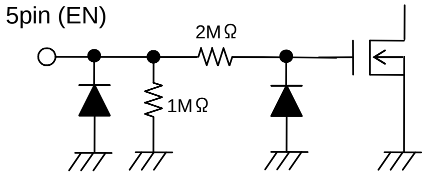
・Please make GND pattern wide enough to handle the power dissipation of the chip.

・For output voltage setting (BD00GA3WEFJ / BD00GA3WNUX)
Output voltage can be set by FB pin voltage（0.800V typ.）and external resistance R1, R2.

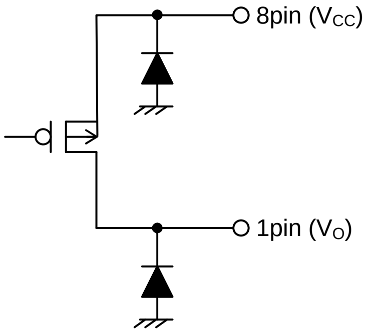
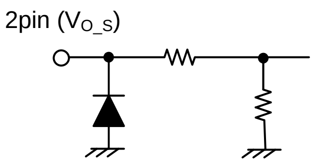
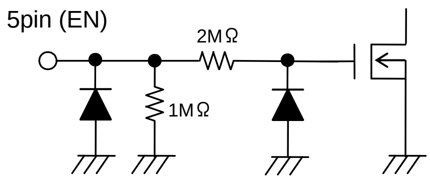
$$V_O = V_{FB} \times \frac{R1+R2}{R2}$$

（The use of resistors with R1+R2=1k to 90kΩ is recommended）

●I/O Equivalent Circuits (Variable type : BD00GA3WEFJ)

8pin (V_{CC}) / 1pin (V_O)	2pin (FB)	5pin (EN)
		

●I/O Equivalent Circuits (Fixed type : BDxxGA3WEFJ)

8pin (V_{CC}) / 1pin (V_O)	2pin (V_{O_S})	5pin (EN)
		

●**Operational Notes**

(1). Absolute maximum ratings

Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

(2). Reverse connection of power supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.

(3). Power supply lines

Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

(4). Ground voltage

The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.

(5). Thermal consideration

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions (Pc≥Pd)

Package Power dissipation : Pd (W)=(Tjmax−Ta)/θja
Power dissipation : Pc (W)=(Vcc−Vo)×Io+Vcc×Ib

Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
Pc : Power dissipation [W], Vcc : Input Voltage, Vo : Output Voltage, Io : Load, Ib : Bias Current

(6). Short between pins and mounting errors

Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.

(7). Operation under strong electromagnetic field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

(8). Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

(9). Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

	TSD ON Temperature[℃] (typ.)	Hysteresis Temperature [℃] (typ.)
BDxxGA3WEFJ / BDxxGA3WNUX	175	15

(10). Testing on application boards

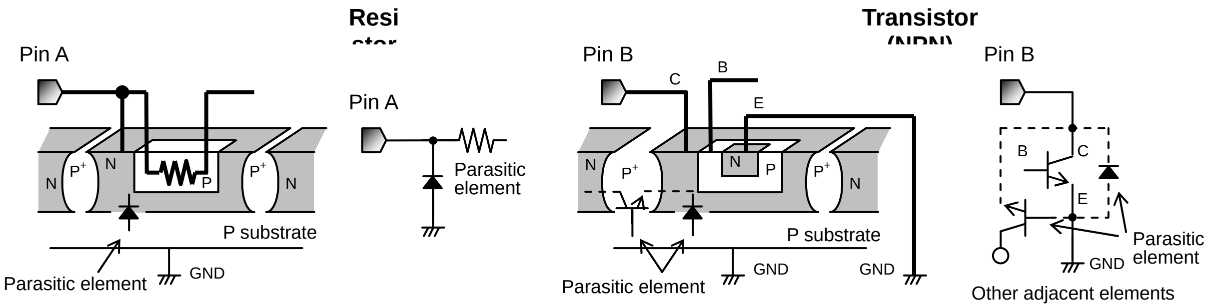
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(11). Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of monolithic IC structure

(12). Ground Wiring Pattern.

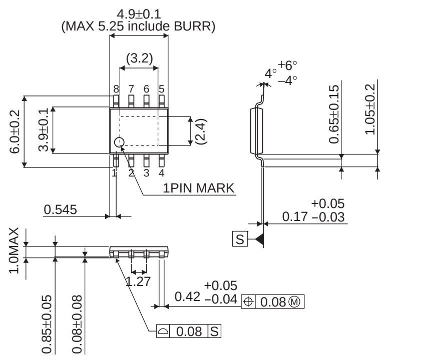
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

Status of this document

The Japanese version of this document is the official specification. If there are any differences in the translated version of this document then official version takes priority.

●Physical Dimension Tape and Reel Information

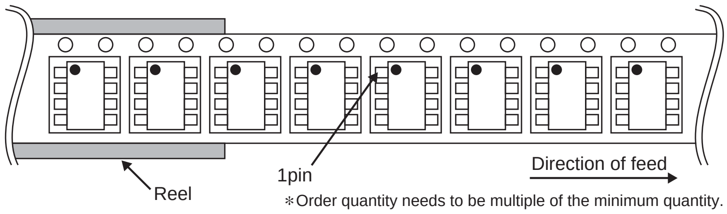
HTSOP-J8



(Unit : mm)

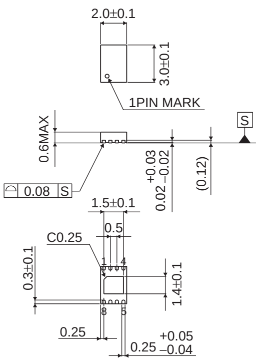
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

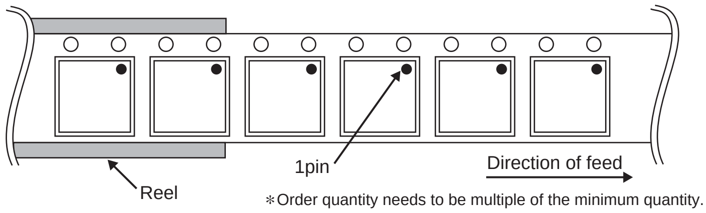
VSON008X2030



(Unit : mm)

<Tape and Reel information>

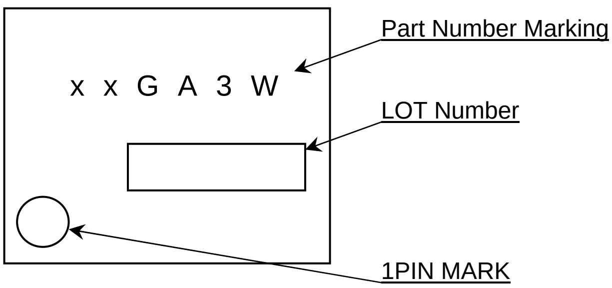
Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



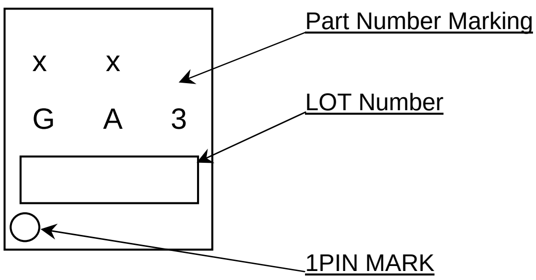
*Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

HTSOP-J8 (TOP VIEW)



VSON008X2030 (TOP VIEW)



●Revision History

Date	Revision	Changes
20.July.2012	001	New Release
03.Dec.2012	002	Improved the English translation and added Package Lineup

Notice

●General Precaution

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   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3) Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

●Precaution for Mounting / Circuit board design

1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

1) If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2) You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

●Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

●Precaution for Storage / Transportation

1) Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

●Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

●Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

●Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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