AIE Adaptive Image Enhancer Series

Real Time Video Processor ICs

BU1572GUW, BU1573KV, BU1574KU

No.09060EBT02

●Description

BU1572GUW/BU1573KV/BU1574KU is AIE : Adaptive Image Enhancer (image processing technology by ROHM's hardware). Camera video images are optimized for maximum visibility.

●Features

1) Compatible with image data from QCIF size (176 × 144) up to WVGA+ size (864 × 480)
2) Compatible with 80-system CPU bus interface and RGB interface.(BU1572GUW/BU1573KV)
3) Compatible with Input/Output data formats with RGB 5:6:5 and 6:6:6.(BU1572GUW/BU1573KV)
4) Multiple operation modes: Image Enhance, Analysis, Through and Sleep. *1
5) Two selectable register settings: indirect addressing through the 80-system CPU bus interface or the 2-wire serial interface (I^2C) *2
6) PWM output for image adjustment LCD backlight control.
7) Built-in edge-enhancement and gamma filters.

*1: BU1574KU is an analysis mode setting interdiction.
*2: BU1574KU becomes only the register set by the two-wire system serial interface.
∗ Extra document is prepared separately about each register setup. Please refer to the Development Scheme on page 10.

●Application

Portable media player, Mobile phone, car display, Car navigation system, and portable DVD etc.

●Lineup

Parameter	Supply power source voltage	Input Interface	Control Interface	Output Interface	PWM Output	Package
BU1572GUW	1.4-1.6(V_{DD}Core) 1.65-3.3(V_{DD}Io)	Supported up to Max WVGA+(864×480)	I^2C BUS (At RGB interface)	18bit RGB interface or bus interface	Image adjustment PWM output	VBGA063W050
BU1573KV	1.4-1.6(V_{DD}Core) 2.7-3.6(V_{DD}Io)	Supported up to Max WVGA+(864×480)	I^2C BUS (At RGB interface)	18bit RGB interface or bus interface	Image adjustment PWM output	VQFP64
BU1574KU	1.4-1.6(V_{DD}Core) 2.7-3.6(V_{DD}Io)	Supported up to Max WVGA+(864×480)	I^2C BUS	8bit YUV=4:2:2 parallel ・ CCIR601 ・ CCIR656	image adjustment PWM output	UQFP64

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply power source voltage 1	VDDIO	-0.3～+4.2	V
Supply power source voltage 2	VDD	-0.3～+2.1	V
Input voltage	VIN	-0.3～VDDIO+0.3	V
Storage temperature range	Tstg	-40～+125	℃
Power dissipation	PD	310 *1	mW

*In the case exceeding 25ºC, 3.1mW should be reduced at the rating 1ºC.
(BU1573KV: 7.5mW / BU1574KU: 7mW should be reduced at the rating.)
*1: BU1573KV is 750mW, and BU1574KU is 700mW.

●Recommended operating range

Parameter	Symbol	Rating	Unit
Supply power source voltage 1 (IO)	VDDIO	1.65～3.30(Typ:2.85V) *1	V
Supply power source voltage 2 (CORE)	VDD	1.40～1.60(Typ:1.50V)	V
Input voltage range	VIN-VDDIO	0～VDDIO	V
Operating temperature range	Topr	-20～+70 *2	℃

*Please supply power source in order of VDD→VDDIO.

*1 : BU1573KV and BU1574KU correspond to 2.70～3.60V(Typ:3.00V)
*2 : BU1573KV and BU1574KU correspond to –40～+85℃

●Electric characteristics

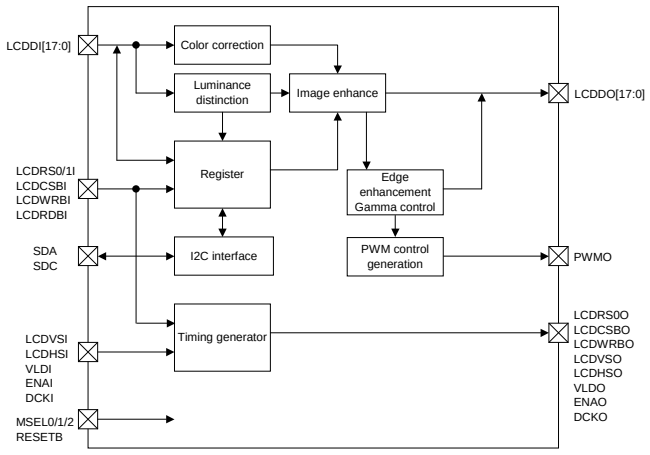
(Unless otherwise specified, VDD=1.50V,VDDIO=2.85V,GND=0.0V,Ta=25℃,f_{IN}=36.0MHz) *1

Parameter	Symbol	Limits			Unit	Condition
		MIN.	TYP.	MAX.		
Input frequency	f_{IN}	-	-	36.0	MHz	DCKI (DUTY45%～55%) *2
Operating consumption current	IDD1	-	24	-	mA	At enhance mode setting (36MHz)
Static consumption current	IDDst	-	-	30	μA	At sleep mode setting, input terminal=GND setting
Input "H" current	IIH	-10	-	10	μA	VIH=VDDIO
Input "L" current	IIL	-10	-	10	μA	VIL=GND
Input "H" voltage 1	VIH1	VDDIO ×0.8	-	VDDIO +0.3	V	Normal input (including input mode of I/O terminal)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO ×0.2	V	Normal input (including input mode of I/O terminal)
Input "H" voltage 2	VIH2	VDDIO ×0.85	-	VDDIO +0.3	V	Hysteresis input *3 (RESETB, DCKI, LCDCSBI/SDA, LCDWRBI/SDC, LCDRDBI/I2CDEV0)
Input "L" voltage 2	VIL2	-0.3	-	VDDIO ×0.15	V	Hysteresis input *4 (RESETB, DCKI, LCDCSBI/SDA, LCDWRBI/SDC, LCDRDBI/I2CDEV0)
Hysteresis voltage width	Vhys	-	0.7	-	V	Hysteresis input *5 (RESETB, DCKI, LCDCSBI/SDA, LCDWRBI/SDC, LCDRDBI/I2CDEV0)
Output "H" voltage	VOH	VDDIO -0.4	-	VDDIO	V	IOH=-1.0mA(DC) (including output mode of I/O terminal)
Output "L" voltage	VOL	0.0	-	0.4	V	IOL=1.0mA(DC) (including output mode of I/O terminal)

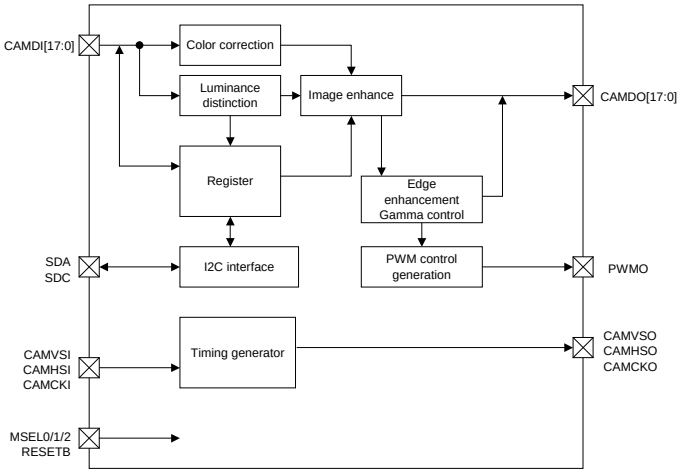
*1 : VDDIO=3.00V in case of BU1573KV / BU1574KU
*2 : CAMCKI in case of BU1574KU
*3,*4,*5 : It corresponds with RESETB CAMCKI SDA SDC I2CDEV0 for BU1574KU

●Block Diagram

(BU1572GUW/BU1573KV)

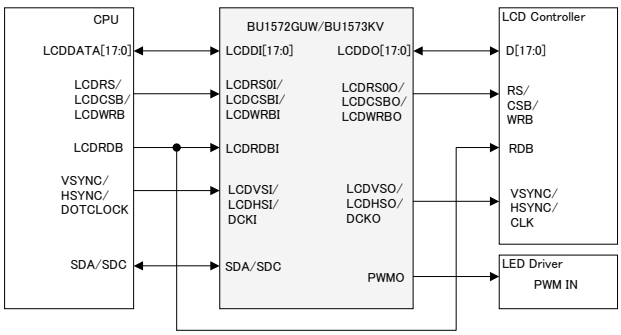


(BU1574KU)

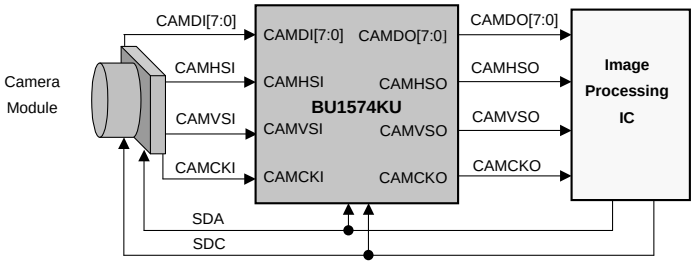


●Recommended Application Circuit

(BU1572GUW/BU1573KV)



(BU1574KU)



●Terminal functions (BU1572GUW/BU1573KV)

PIN No.	PIN Name	Interface Type *1		In/Out	Active Level	Init	Description	In/output type
		TYPE 1	TYPE 2					
1	LCDVSI	LCDVSI	LCDVSI	In	*	-	Vertical timing input	C *1
2	N.C.*2	-	-	-	-	-	-	-
3	LCDHSI/ LCDRS01	*3	LCDHSI	In	*	-	Horizontal timing input/ Register select input signal 0	C *1
4	LCDCSBI/ SDA	LCDCSBI	SDA	In/Out	Low/ DATA	In	Chip select input signal / In/output serial data	G
5	LCDWRDBI/ SDC	LCDWRBI	SDC	In	Low/ CLK	-	Write enable input signal / In/output serial clock	D *1
6	LCDRDBI/ I2CDEV0	LCDRDBI	I2CDEV0	In	Low/ *	-	Read enable input signal / I2C device address setting	D *1
7	LCDDI0	LCDDI0	LCDDI0	In/Out	DATA	In	Data input: bit 0	H *1
8	LCDDI1	LCDDI1	LCDDI1	In/Out	DATA	In	Data input: bit 1	H *1
9	LCDDI2	LCDDI2	LCDDI2	In/Out	DATA	In	Data input: bit 2	H *1
10	LCDDI3	LCDDI3	LCDDI3	In/Out	DATA	In	Data input: bit 3	H *1
11	LCDDI4	LCDDI4	LCDDI4	In/Out	DATA	In	Data input: bit 4	H *1
12	LCDDI5	LCDDI5	LCDDI5	In/Out	DATA	In	Data input: bit 5	H *1
13	LCDDI6	LCDDI6	LCDDI6	In/Out	DATA	In	Data input: bit 6	H *1
14	LCDDI7	LCDDI7	LCDDI7	In/Out	DATA	In	Data input: bit 7	H *1
15	LCDDI8	LCDDI8	LCDDI8	In/Out	DATA	In	Data input: bit 8	H *1
16	LCDDI9	LCDDI9	LCDDI9	In/Out	DATA	In	Data input: bit 9	H *1
17	LCDDI10	LCDDI10	LCDDI10	In/Out	DATA	In	Data input: bit 10	H *1
18	LCDDI11	LCDDI11	LCDDI11	In/Out	DATA	In	Data input: bit 11	H *1
19	LCDDI12	LCDDI12	LCDDI12	In/Out	DATA	In	Data input: bit 12	H *1
20	LCDDI13	LCDDI13	LCDDI13	In/Out	DATA	In	Data input: bit 13	H *1
21	LCDDI14	LCDDI14	LCDDI14	In/Out	DATA	In	Data input: bit 14	H *1
22	LCDDI15	LCDDI15	LCDDI15	In/Out	DATA	In	Data input: bit 15	H *1
23	LCDDI16	LCDDI16	LCDDI16	In/Out	DATA	In	Data input: bit 16	H *1
24	LCDDI17	LCDDI17	LCDDI17	In/Out	DATA	In	Data input: bit 17	H *1
25	ENAI	*3	ENAI	In	*	-	RAM write enable input signal	C *1
26	VLDI	*3	VLDI	In	*	-	VLD input signal	C *1
27	VDDIO	VDDIO	VDDIO	-	PWR	-	DIGITAL IO power source	-
28	DCKI	DCKI	DCKI	In	CLK	-	Clock input	D *1
29	GND	GND	GND	-	GND	-	Common GROUND	-
30	VDD	VDD	VDD	-	PWR	-	CORE power source	-
31	MSEL0/ LCDRS0I	LCDRS0I	MSEL0 *3	In	*	-	Mode select 0/ Register select input signal 0	A
32	MSEL1/ LCDRS1I	LCDRS1I	MSEL1 *3	In	*	-	Mode select 1/ Register select input signal 1	A

※Change by setup by the register is possible for the "*" display in the column of an Active level. Moreover, Init is a pin state under reset.

*1 : It suspends during reset (initial state)

*2 : With no ball(Please connect it with GND for BU1573KV)

*3 : Please connect with GND.

PIN No.	PIN Name	Interface Type *1		In/Out	Active Level	Init	Description	In/output type
		TYPE 1	TYPE 2					
33	MSEL2	MSEL2 *3	MSEL2 *4	In	*	-	Mode select 2	A
34	LCDRS0O/ PWMO1 *5	LCDRS0O/ PWM_O(1)	PWM_O(1)	Out	*	Low	Register select output signal 0/ PWM output for the LCD backlight	E
35	PWMO3 *5/ VLDO	PWM_O(3)	PWM_O(3)/ VLDO	Out	*	Low	PWM output for the LCD backlight/ VLD output signal	E
36	ENAO	-	ENAO	Out	*	Low	RAM write enable output signal	E
37	LCDDO17/ PWMO2 *5	LCDDO17/ PWM_O(2)	LCDDO17/ PWM_O(2)	In/Out	DATA	Low	Data output: bit 17/ PWM output for the LCD backlight	F
38	LCDDO16	LCDDO16	LCDDO16	In/Out	DATA	Low	Data output: bit 16	F
39	LCDDO15	LCDDO15	LCDDO15	In/Out	DATA	Low	Data output: bit 15	F
40	LCDDO14	LCDDO14	LCDDO14	In/Out	DATA	Low	Data output: bit 14	F
41	LCDDO13	LCDDO13	LCDDO13	In/Out	DATA	Low	Data output: bit 13	F
42	LCDDO12	LCDDO12	LCDDO12	In/Out	DATA	Low	Data output: bit 12	F
43	LCDDO11	LCDDO11	LCDDO11	In/Out	DATA	Low	Data output: bit 11	F
44	LCDDO10	LCDDO10	LCDDO10	In/Out	DATA	Low	Data output: bit 10	F
45	LCDDO9	LCDDO9	LCDDO9	In/Out	DATA	Low	Data output: bit 9	F
46	LCDDO8	LCDDO8	LCDDO8	In/Out	DATA	Low	Data output: bit 8	F
47	GND	GND	GND	-	GND	-	Common GROUND	-
48	LCDDO7	LCDDO7	LCDDO7	In/Out	DATA	Low	Data output: bit 7	F
49	LCDDO6	LCDDO6	LCDDO6	In/Out	DATA	Low	Data output: bit 6	F
50	LCDDO5	LCDDO5	LCDDO5	In/Out	DATA	Low	Data output: bit 5	F
51	LCDDO4	LCDDO4	LCDDO4	In/Out	DATA	Low	Data output: bit 4	F
52	LCDDO3	LCDDO3	LCDDO3	In/Out	DATA	Low	Data output: bit 3	F
53	LCDDO2	LCDDO2	LCDDO2	In/Out	DATA	Low	Data output: bit 2	F
54	LCDDO1	LCDDO1	LCDDO1	In/Out	DATA	Low	Data output: bit 1	F
55	LCDDO0	LCDDO0	LCDDO0	In/Out	DATA	Low	Data output: bit 0	F
56	LCDWRBO/ I2CDEV6B	LCDWRBO	I2CDEV6B *3	In/Out	*	High/ In	Write enable output signal	F
57	LCDCSBO	LCDCSBO	"H" *6	Out	*	High	Chip select output signal	E
58	SDA / LCDHSO	-	LCDHSO	Out	*	Low	In/output serial clock/ Horizontal timing output signal	G
59	SDC/ LCDVSO	-	LCDVSO	Out	*	Low	In/output serial clock/ Vertical timing output signal	G
60	RESETB	RESETB	RESETB	In	Low	-	System reset signal	B
61	VDDIO	VDDIO	VDDIO	-	PWR	-	DIGITAL IO power source	-
62	DCKO	DCKO	DCKO	Out	CLK	Low	Clock output	E
63	GND	GND	GND	-	GND	-	Common GROUND	-
64	VDD	VDD	VDD	-	PWR	-	CORE power source	-

※Change by setup by the register is possible for the "*" display in the column of an Active level. Moreover, Init is a pin state under reset.

*3 : Please connect with GND

*4 : Please connect with VDDIO

*5 : It selects it according to PWMCNT register (40h).

*6 : “High”output

●Terminal functions (BU1574KU)

PIN No.	PIN Name	In/ Out	Active Level	Init	Descriptions	In/Output type
1	CAMVSI	In	*	-	Vertical timing input	C *1
2	N.C. *2	-	*	-	-	-
3	CAMHSI	In	*	-	Horizontal timing input	C *1
4	SDA	In/Out	DATA	In	In/Output serial data	G
5	SDC	In	CLK	-	In/Output serial clock	D *1
6	I2CDEV0	In	*	-	I2C device address setting	D *1
7	CAMDI0	In	DATA	-	Data input: bit 0	H *1
8	CAMDI1	In	DATA	-	Data input: bit 1	H *1
9	CAMDI2	In	DATA	-	Data input: bit 2	H *1
10	CAMDI3	In	DATA	-	Data input: bit 3	H *1
11	CAMDI4	In	DATA	-	Data input: bit 4	H *1
12	CAMDI5	In	DATA	-	Data input: bit 5	H *1
13	CAMDI6	In	DATA	-	Data input: bit 6	H *1
14	CAMDI7	In	DATA	-	Data input: bit 7	H *1
15	RESERVEI0 *3	In	*	-	RESERVE	C *1
16	RESERVEI1 *3	In	*	-	RESERVE	C *1
17	RESERVEI2 *3	In	*	-	RESERVE	C *1
18	RESERVEI3 *3	In	*	-	RESERVE	C *1
19	RESERVEI4 *3	In	*	-	RESERVE	C *1
20	RESERVEI5 *3	In	*	-	RESERVE	C *1
21	RESERVEI6 *3	In	*	-	RESERVE	C *1
22	RESERVEI7 *3	In	*	-	RESERVE	C *1
23	RESERVEI8 *3	In	*	-	RESERVE	C *1
24	RESERVEI9 *3	In	*	-	RESERVE	C *1
25	RESERVEI10 *3	In	*	-	RESERVE	C *1
26	RESERVEI11 *3	In	*	-	RESERVE	C *1
27	VDDIO	-	PWR	-	DIGITAL IO power source	-
28	CAMCKI	In	CLK	-	Clock input	D *1
29	GND	-	GND	-	Common GROUND	-
30	VDD	-	PWR	-	CORE power source	-
31	MSEL0 *3	In	*	-	Mode select 0	A
32	MSEL1 *3	In	*	-	Mode select 1	A

※Change by setup by the register is possible for the "*" display in the column of an Active level. Moreover, Init is a pin state under reset.

*1 : It suspends during reset (initial state)

*2 : Please connect with GND

*3 : Please connect with GND.

PIN No.	PIN Name	In/Out	Active Level	Init	Descriptions	In/Output type
33	MSEL2 *4	In	*	-	Mode select 2	A
34	PWMO	Out	*	Low	PWM output for LCD backlight	E
35	RESERVEO11 *5	Out	*	Low	RESERVE	E
36	RESERVEO10 *5	Out	*	Low	RESERVE	E
37	RESERVEO9 *5	Out	*	Low	RESERVE	E
38	RESERVEO8 *5	Out	*	Low	RESERVE	E
39	RESERVEO7 *5	Out	*	Low	RESERVE	E
40	RESERVEO6 *5	Out	*	Low	RESERVE	E
41	RESERVEO5 *5	Out	*	Low	RESERVE	E
42	RESERVEO4 *5	Out	*	Low	RESERVE	E
43	RESERVEO3 *5	Out	*	Low	RESERVE	E
44	RESERVEO2 *5	Out	*	Low	RESERVE	E
45	RESERVEO1 *5	Out	*	Low	RESERVE	E
46	RESERVEO0 *5	Out	*	Low	RESERVE	E
47	GND	-	GND	-	Common GROUND	-
48	CAMDO7	Out	DATA	Low	Data output: bit 7	E
49	CAMDO6	Out	DATA	Low	Data output: bit 6	E
50	CAMDO5	Out	DATA	Low	Data output: bit 5	E
51	CAMDO4	Out	DATA	Low	Data output: bit 4	E
52	CAMDO3	Out	DATA	Low	Data output: bit 3	E
53	CAMDO2	Out	DATA	Low	Data output: bit 2	E
54	CAMDO1	Out	DATA	Low	Data output: bit 1	E
55	CAMDO0	Out	DATA	Low	Data output: bit 0	E
56	I2CDEV6B *3	In	*	-	RESERVE	A
57	RESERVEO12 *5	Out	*	High	RESERVE	E
58	CAMHSO	Out	*	Low	Horizontal timing output signal	E
59	CAMVSO	Out	*	Low	Vertical timing output signal	E
60	RESETB	In	Low	-	System reset signal	B
61	VDDIO	-	PWR	-	DIGITAL IO power source	-
62	CAMCKO	Out	CLK	Low	Clock output	E
63	GND	-	GND	-	Common GROUND	-
64	VDD	-	PWR	-	CORE power source	-

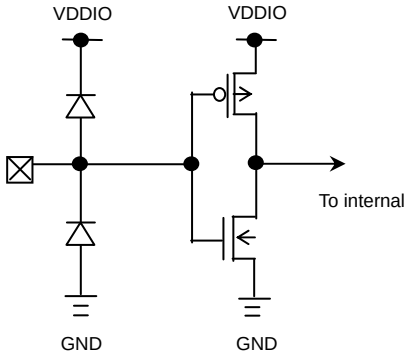
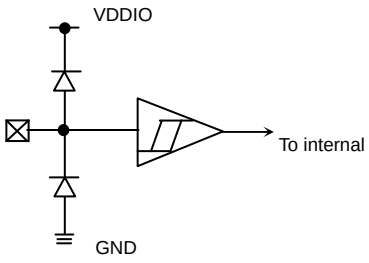
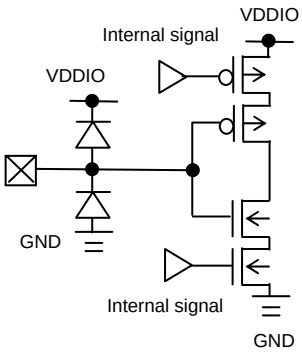
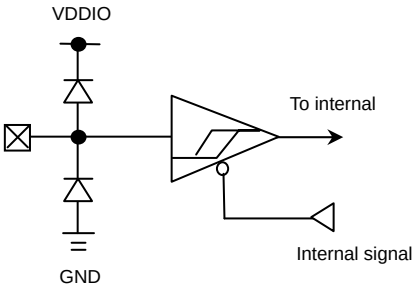
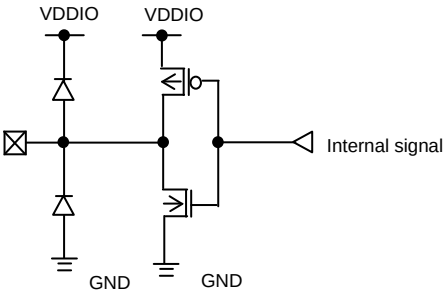
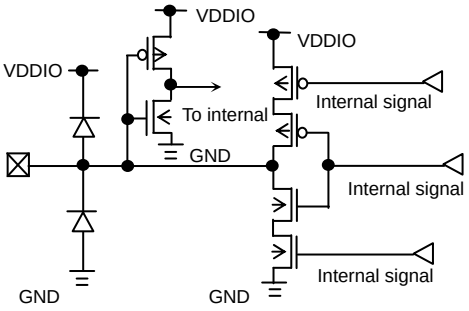
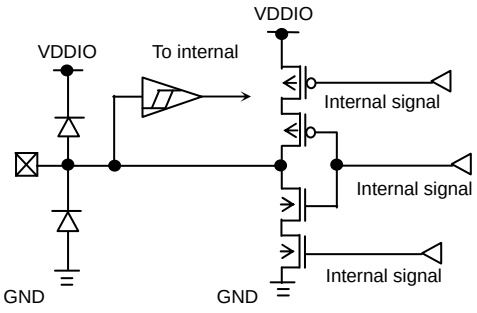
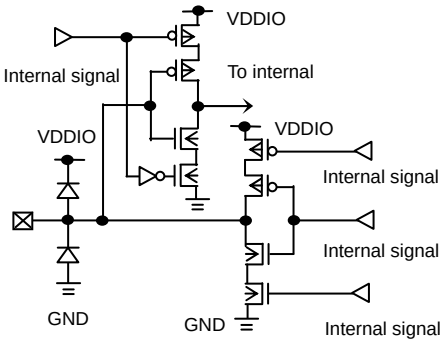
※Change by setup by the register is possible for the "*" display in the column of an Active level. Moreover, Init is a pin state under reset.

*3 : Please connect with GND

*4 : Please connect with VDDIO

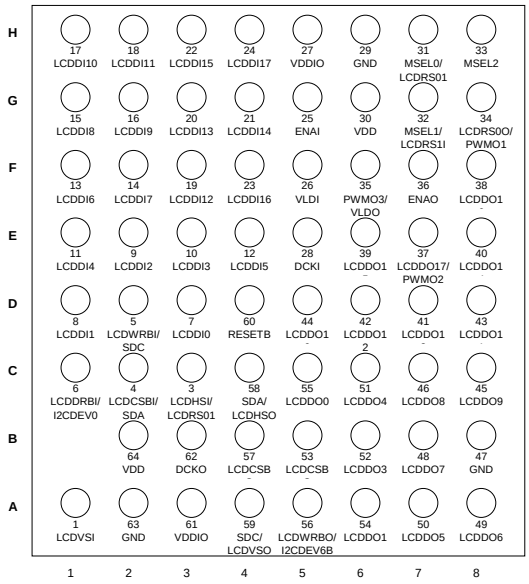
*5 : Please leave OPEN

●Equivalent Circuit Structures of input / output pins

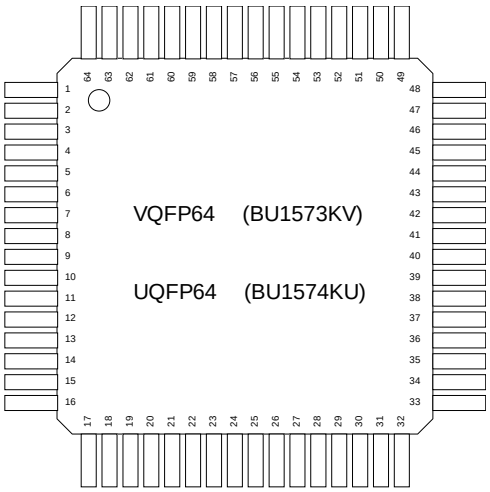
Type	The equivalent circuit structure	Type	The equivalent circuit structure
A	 Input pin	**B**	 Input pin with the hysteresis function
C	 Input pin with the suspend function	**D**	 Input pin with the hysteresis and suspend functions
E	 Output pin	**F**	 In/output pin
G	 In/output pin with the hysteresis function	**H**	 In/output pin with the suspend function

●Terminal Layout

(BU1572GUW Bottom View)



(BU1573KV/BU1574KU Top View)



∗ The terminal arrangement follows terminal function table of P.3-6.

● Timing Chart

1. I2C interface

1.1 I2C interface timing

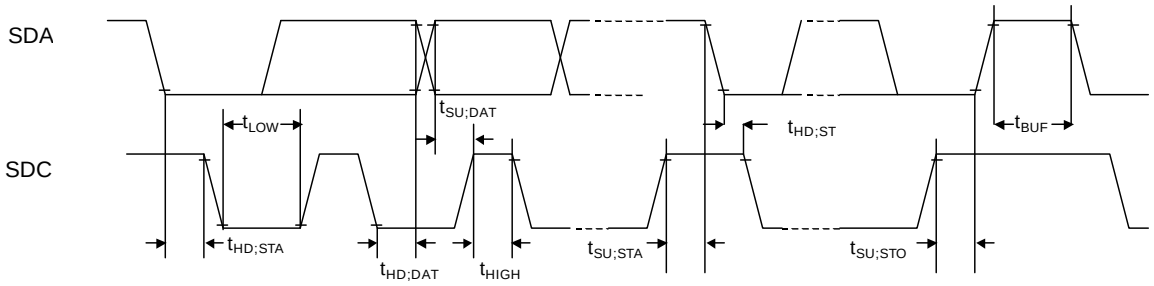


Table 1.1-1 I2C Interface timing

Symbol	Parameter	MIN.	TYP.	MAX.	Unit
f_{SCL}	SDC Clock Frequency	0	-	400	kHz
$t_{HD;STA}$	Hold-time(repetition)『START』conditions (The first clock pulse is generated after this period.)	0.6	-	-	us
f_{LOW}	The "L" period of SDC clock	1.3	-	-	us
t_{HIGH}	The "H" period of SDC clock	0.6	-	-	us
$t_{SU;STA}$	Setup time of repetitive 『START』conditions	0.6	-	-	us
$t_{HD;DAT}$	Hold time of SDA	0	-		us
$t_{SU;DAT}$	Setup time of SDA	100	-	-	ns
$t_{SU;STO}$	Setup time of the 『STOP』conditions	0.6	-	-	us
t_{BUF}	Bus free time between『STOP』conditions and the『START』conditions	1.3	-	-	us

2. RGB interface

2.1. RGB interface timing

The input timing of image signal on RGB I/F is shown in Table 2.1-1.

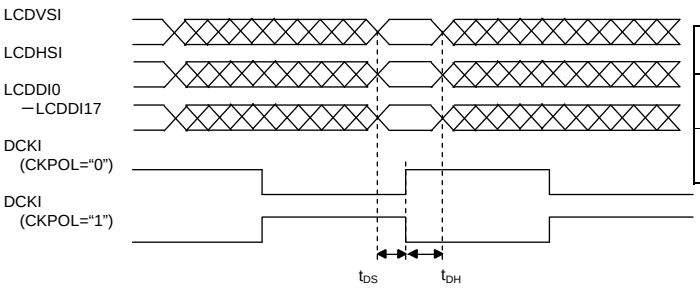


Table 2.1-1 BU1572GUW/BU1573KV RGB interface input timing

Symbol	Explanation	MIN.	TYP.	MAX	UN
t_{DS}	Camera setup period (between the DCKI rising and falling edges)	8	-	-	ns
t_{DH}	Camera holding period (between the DCKI rising and falling edges)	8	-	–	ns

The output timing of image signal on RGB I/F is shown in Table 2.1-2.

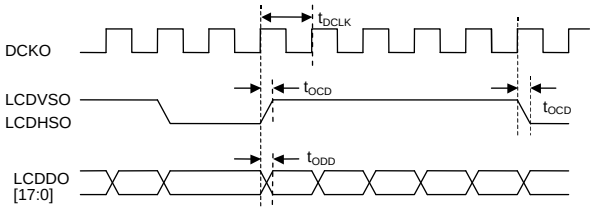


Table 2.1-2 BU1572GUW/BU1573KV Image signal output timing

Symbol	Explanation	MIN.	TYP.	MAX.	UNIT
t_{DCLK}	Clock Cycle	27.7	-	-	ns
d_{DCLK}	Clock Duty	40	50	60	%
t_{ODD}	Decision of LCDDO from DCKO	-	-	5	ns
t_{OCD}	Decision of LCDVSO or LCDHSO from DCKO	-	-	5	ns

3. YUV interface

3.1. YUV interface timing

The input timing of image signal on YUV I/F is shown in Table 3.1-1.

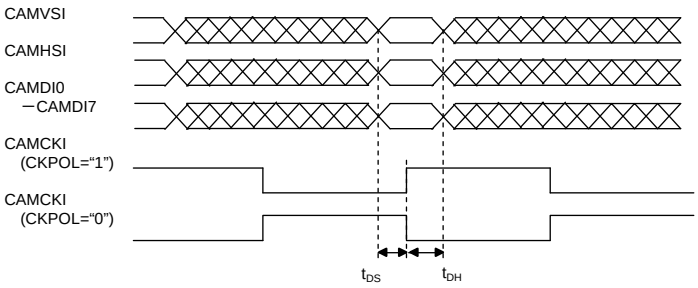


Table 3.1-1 BU1574KU YUV interface input timing

Symbol	Explanation	MIN.	TYP	MAX	UNI
t_{DS}	Camera setup period (between the CAMCKI rising and falling edges)	8	-	-	ns
t_{DH}	Camera holding period (between the CAMCKI rising and falling edges)	8	-	–	ns

The output timing of image signal on YUV I/F is shown in Table 3.1-2.

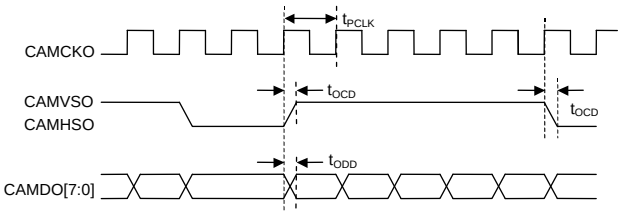


Table 3.1-2 BU1574KU Image signal output timing

Symbol	Explanation	MIN.	TYP.	MAX.	UNIT
t_{PCLK}	Clock Cycle	27.7	-	-	ns
d_{PCLK}	Clock Duty	40	50	60	%
t_{ODD}	Decision of CAMDO from CAMCKO	-	-	5	ns
t_{OCD}	Decision of CAMVSO or CAMHSO from CAMCKO	-	-	5	ns

●Development Scheme

This technical note is aimed at trying the connectivity in the hardware between customer's system and our AIE Adaptive Image Enhancer series.
We prepare various data and tools for every development STEP as follows other than this technical note, please contact the sales staff in your duty also including the support system.

(1) Demonstration STEP

(You can try the standard image processing functions by the standard Demonstration kit at once.)

You can confirm on TV screen what carried out AIE processing of a camera image and the DVD video image.

・Standard Demonstration board kit

◎Demonstration board(TV-IN→BU1573KV→TV-OUT board)
◎Demonstration board operation manual
◎Demonstration software
If the software for the trial board is installed in your Windows PC(Windows 2000/XP), more detailed setting is possible.
◎USB cable

(2) Confirmation STEP

(We will respond to customer's camera module.)

・Specifications
We will provide specifications for AIE Adaptive Image Enhancer according to customer's requirements.

・Function explanation
We will deliver you the function explanation describing detailed functions, register settings, external interfaces, timing, and so forth of AIE Adaptive Image Enhancer according to your requests.

・Application note
We will deliver you the detailed explanation data on application development of AIE Adaptive Image Enhancer according to your requests.

(3) System check STEP

(You can check the application operation as a system by the kit of system check tools and your camera module.)

You can check the interface with your camera module and the application operation on the system check board using the tools for user's only.

・System check tools kit

◎Board for system evaluation
◎Manual for system evaluation
◎Macro command file for reference

*You can check the detailed functions of the application operation by your PC using the macro command file.

(4) Integrated check STEP with user's system

(You can check the application operation as a system on your system check board using the integrated check software.)

You can check the application operation on the sample LSI-equipped system check board by your camera module using the integrated check software.

・On line Support ; We will answer your questions about the software development.

●Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.
In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5)GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6)Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7)Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8)Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10)Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11)External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

●Order Model Name Selection

B U	1 5 7 2	G U W	—	E 2
ROHM model name	Product number	Package type		Taping model name

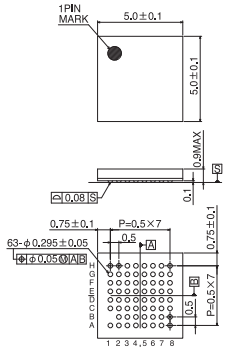
GUW: VBGA063W050
KV: VQFP64
KU: UQFP64

E2: Embossed reel tape
None: Tray

●Tape and Reel information

VBGA063W050

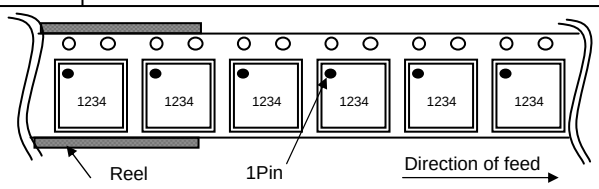
<Dimension>



(Unit:mm)

<Tape and Reel information>

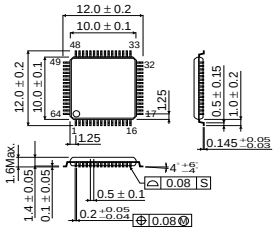
Tape	Embossed carrier tape (With dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.)



※When you order , please order in times the amount of package quantity.

VQFP64

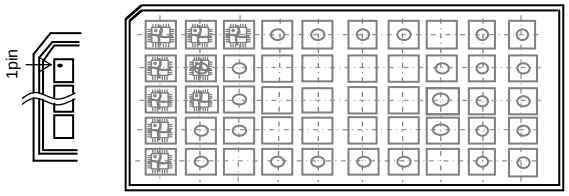
<Dimension>



(Unit:mm)

<Packing information>

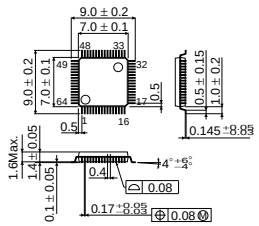
Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



※When you order , please order in times the amount of package quantity.

UQFP64

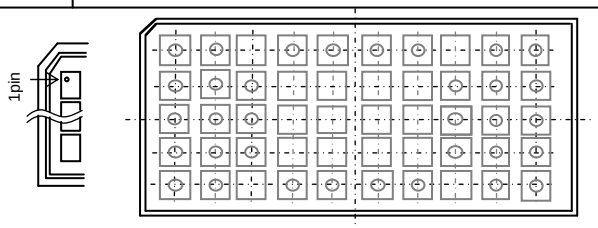
<Dimension>



(Unit:mm)

<Packing information>

Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



※When you order , please order in times the amount of package quantity.

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