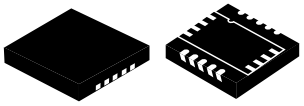
A6984

36 V, 400 mA automotive synchronous step-down switching regulator

Datasheet - production data



VFDFPN10 4 x 4 x 1.0 mm

Features

- AEC-Q100 qualified
- 400 mA DC output current
- 4.5 V to 36 V operating input voltage
- Synchronous rectification
- Low consumption mode or low noise mode
- 75 µA I_Q at light load (LCM V_{OUT} = 3.3 V)
- 13 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} (250 kHz - 600 kHz)
- Output voltage adjustable from 0.9 V
- No resistor divider required for 3.3 V V_{OUT}
- V_{BIAS} maximizes efficiency at light load
- 350 mA valley current limit
- Constant on-time control scheme
- PGOOD open collector
- Thermal shutdown

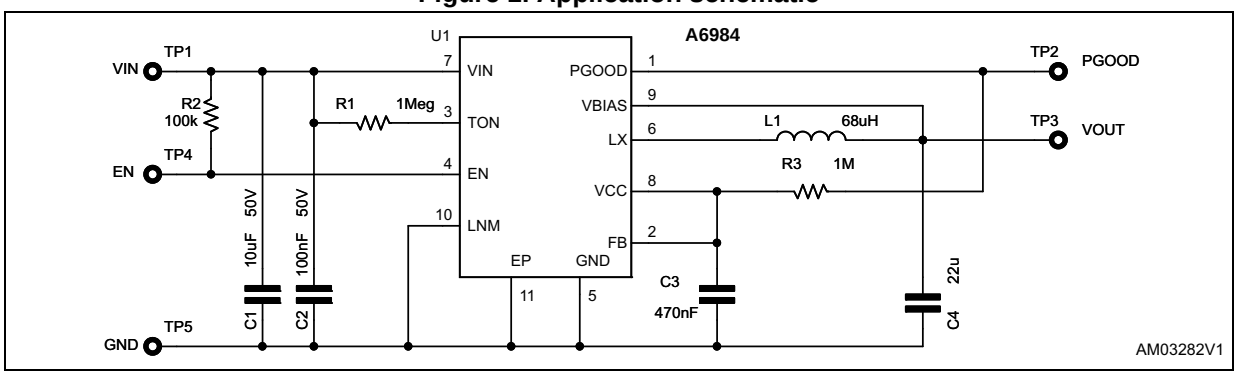
Applications

- Car body and ADAS applications (LCM)
- Car audio and low noise applications (LNM)

Description

The A6984 is a step-down monolithic switching regulator able to deliver up to 400 mA DC. The output voltage adjustability ranges from 0.9 V. The fixed 3.3 V VOUT requires no external resistor divider. The “low consumption mode” (LCM) is designed for applications active during car parking, so it maximizes the efficiency at light load with controlled output voltage ripple. The “low noise mode” (LNM) makes the switching frequency almost constant over the load current range, serving low noise application specifications such as car audio/sensors. The PGOOD open collector output can implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium-heavy load, and the high switching frequency capability make the size of the application compact. Pulse-by-pulse current sensing on the low-side power element implements effective constant current protection. The package lead finishing guarantees side solderability, thus allowing visual inspection during manufacturing.

Figure 1. Application schematic

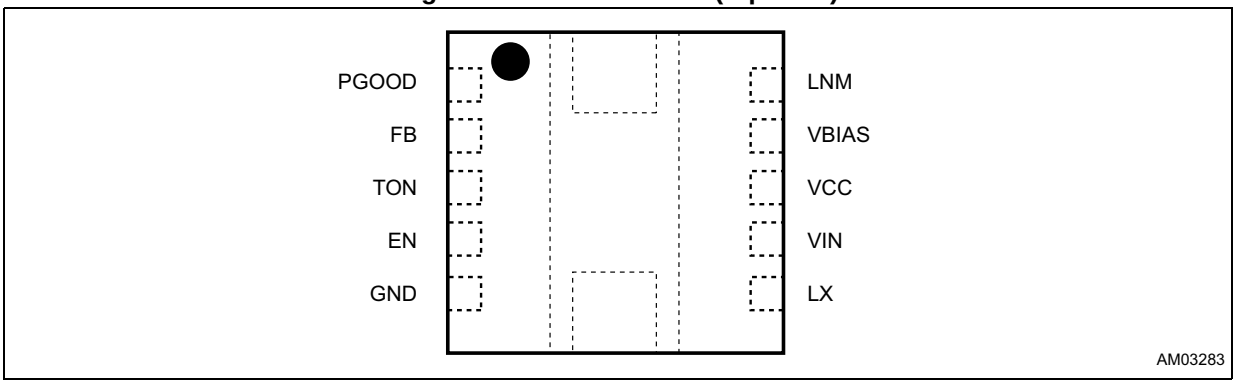


Contents

1 Pin settings

1.1 Pin connection

Figure 2. Pin connection (top view)



1.2 Pin description

Table 1. Pin description

N°	Pin	Description
1	PGOOD	The open collector output is driven low when the FB voltage is below the $V_{PGD\ L}$ threshold (see *Table 5*).
2	FB	Inverting input of the error amplifier
3	TON	A resistor connected between this pin and V_{IN} sets the switching frequency.
4	EN	Enable pin. A logical active high signal enables the device. Connect this pin to V_{IN} if not used.
5	GND	Power GND
6	LX	Switching node
7	VIN	DC input voltage
8	VCC	Embedded regulator output that supplies the main switching controller. Connect an external 1 µF capacitor for proper operation. An integrated LDO regulates VCC = 3.3 V if VBIAS voltage is < 2.4 V. VCC is connected to VBIAS through a MOSFET switch if VBIAS > 3.2 V and the embedded LDO is disabled to increase the light load efficiency.
9	VBIAS	Typically connected to the regulated output voltage. An external voltage reference can be used to supply the analog circuitry to increase the efficiency at light load. Connect to GND if not used.
10	LNM	Connect to V_{CC} for low noise mode (LNM) / to GND for low consumption mode (LCM) operation.

1.3 Maximum ratings

Stressing the device above the rating listed in *Table 2: Absolute maximum ratings* may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5* of this specification is not implied.

Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
dV_{IN}/dt (1)	Input slew rate	-	0.1	V/µs
V_{IN}	-	-0.3	38	V
LX	device ON		V_{IN} + 0.3	
	device OFF		25	
EN	see *Table 1*		V_{IN} + 0.3	
TON				
V_{CC}			6	
V_{BIAS}				
PGOOD			V_{CC} + 0.3	
FB				
LNM				
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-	-55 to 150	
T_{LEAD}	Lead temperature (soldering 10 sec.)	-	260	
I_{HS}, I_{LS}	High-side / low-side RMS switch current	-	400	mA

1. Maximum slew rate should be limited as detailed in *Section 5.1*.

1.4 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ JA}$	Thermal resistance junction ambient (device soldered on STMicroelectronics evaluation board)	50	°C/W

1.5 ESD protection

Table 4. ESD protection

Symbol	Test condition	Value	Unit
ESD	HBM	2	KV
	MM	200	V
	CDM	500	V

2 Electrical characteristics

T_J = -40 to 125 °C, V_{IN} = V_{EN} = 12 V, V_{BIAS} = 3.3 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range		-	4.5		36	V
V_{IN_UVLO}	UVLO thresholds	Rising edge V_{CC} regulator V_{BIAS} = GND	-	3.1	3.8	4.5	
		Falling edge V_{CC} regulator V_{BIAS} = GND	-	2.9	3.6	4.3	
V_{OUT}	Fixed output voltage valley regulation	FB = V_{CC}, no load	-	3.23	3.3	3.37	
V_{FB}	Adjustable output voltage valley regulation	No load	-	0.88	0.9	0.92	
$R_{DSON\ HS}$	High-side RDSON	I_{SW} = 0.1 A	-	0.6	1.3	2.2	Ω
$R_{DSON\ LS}$	Low-side RDSON	I_{SW} = 0.1 A	-	0.4	1.0	1.9	
T_{OFF}	Minimum Low-side conduction time	V_{IN} = V_{EN} = 4.5 V	-	100	200	400	ns
Current limit and zero crossing comparator							
I_{VY}	Valley current limit	-	-	350	400	470	mA
I_{ZCD}	Zero crossing current threshold	-	(1)	12	27	46	
VCC regulator							
V_{CC}	VCC voltage	V_{FB} = 1 V, V_{BIAS} = GND	-	3	3.8	4.6	V
V_{BIAS}	V_{BIAS} falling threshold	-	-	2.4	2.6	2.8	
	V_{BIAS} rising threshold	-	-	2.6	2.9	3.2	
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	EN = GND	-	3	13	22	µA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	11	26	41	µA
		LCM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = GND	(2)	90	160	230	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V	-	11	26	42	
		LNM - NO SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = GND	-	200	320	440	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM - SWO** $V_{REF} < V_{FB} < V_{OVP}$ (SLEEP) V_{BIAS} = 3.3 V	(2)	80	150	200	
		LNM - SWO $V_{REF} < V_{FB} < V_{OVP}$ V_{BIAS} = 3.3 V	-	180	300	390	
Enable							
EN	EN thresholds	Device inhibited	-	1.1	-	-	V
		Device enabled	-	-	-	2.6	
	EN hysteresis	-	(3)	-	650	-	mV
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})	Rising edge		18	23	28	%
PGOOD							
$V_{PGD\ L}$	Power good LOW threshold	V_{FB} rising edge (PGOOD high impedance)	(3)	-	90	-	%
		V_{FB} falling edge (PGOOD low impedance)	-	84	88	92	
$V_{PGD\ H}$	Power good HIGH threshold	Internal FB rising edge (PGOOD low impedance) $V_{FB} = V_{CC}$	-	118	123	128	
		Internal FB falling edge (PGOOD high impedance) $V_{FB} = V_{CC}$	(3)	-	100	-	
V_{PGOOD}	PGOOD open collector output	$V_{IN} > V_{IN\_UVLO\_H}$, V_{FB}=GND 4 mA sinking load	-	-	-	0.6	V
		$2.9 < V_{IN} < V_{IN\_UVLO\_H}$ 100 µA sinking load	-	-	-	0.6	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature	-	(3)	-	150	-	°C
T_{HYS}	Thermal shutdown hysteresis	-	(3)	-	20	-	°C

1. Parameter tested in static condition during testing phase. Parameter value may change over dynamic application condition.
2. LCM enables SLEEP mode (part of the internal circuitry is disabled) at light load.
3. Not tested in production.

3 Datasheet parameters over the temperature range

100% of the population in the production flow is tested at three different ambient temperatures (-40 °C; 25 °C, 125 °C) to guarantee datasheet parameters within the junction temperature range (-40 °C to 125 °C).

Device operation is guaranteed when the junction temperature is within the -40 °C to 150 °C temperature range. The designer can estimate the silicon temperature increase with respect to the ambient temperature evaluating the internal power losses generated during the device operation.

However, the embedded thermal protection disables the switching activity to protect the device in case the junction temperature reaches the T_{SHTDWN} (+150 °C min) temperature.

All the datasheet parameters can be guaranteed to a maximum junction temperature of +125 °C to avoid triggering the thermal shutdown protection during the testing phase due to self-heating.

4 Device description

The A6984 device is based on a “Constant On-Time” (COT) control scheme with frequency feed-forward correction over the V_{IN} range. As a consequence the device features fast load transient response, almost constant switching frequency operation over the input voltage range and simple stability control.

The switching frequency can be adjusted in the 250 kHz - 600 kHz range.

The LNM (low noise mode) implements constant PWM control to minimize the voltage ripple over the load range, the LCM (low consumption mode) pulse skipping technique to increase the efficiency at the light load.

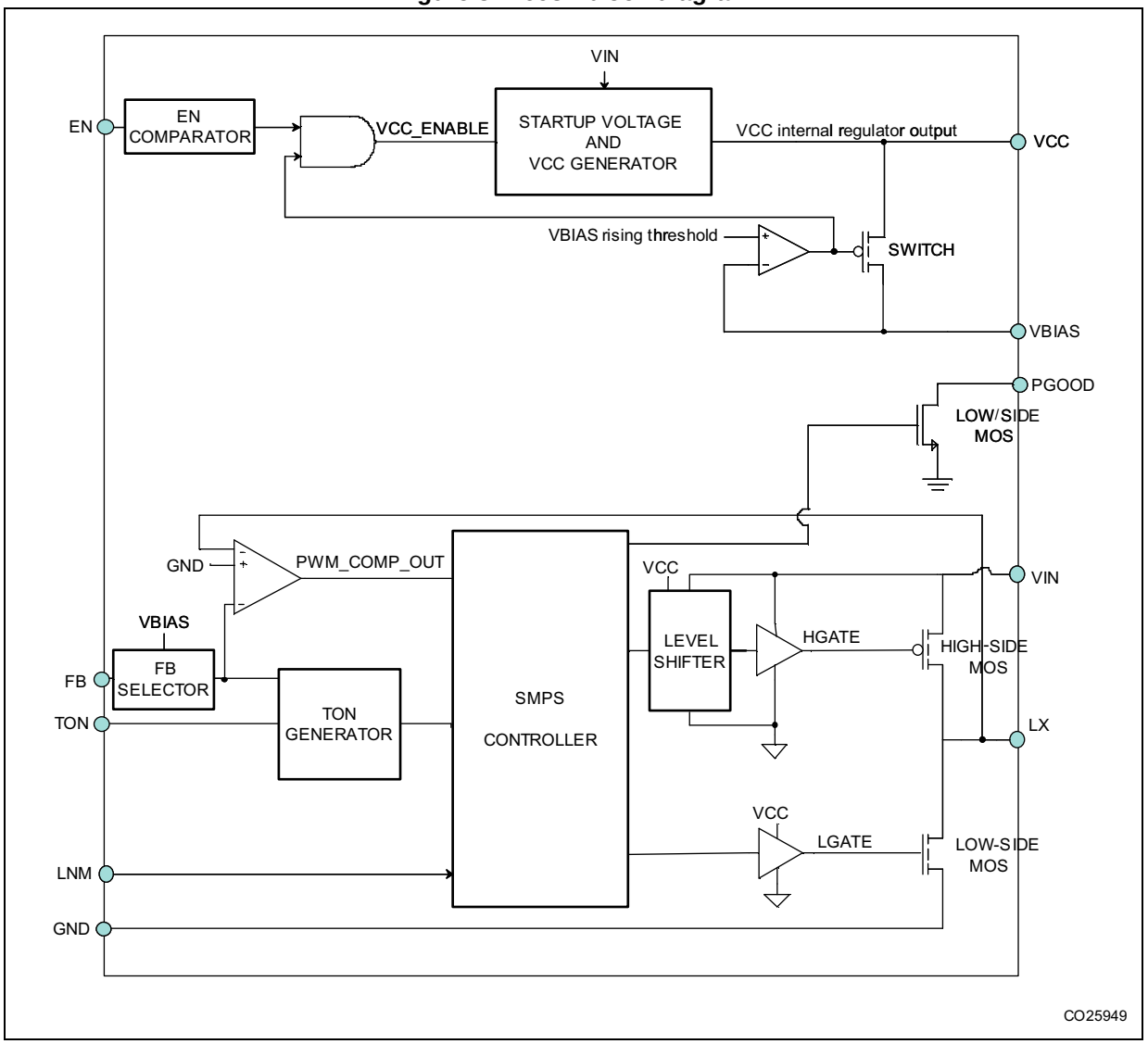
No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider implements the output voltage adjustability.

The switchover capability of the internal regulator derives a portion of the quiescent current from an external voltage source (V_{BIAS} pin is typically connected to the regulated output voltage) to maximize the efficiency at the light load.

The device main internal blocks are shown in the block diagram in *Figure 6 on page 15*:

- The bandgap reference voltage
- The on-time controller
- A “pulse width modulation” (PWM) comparator and the driving circuitry of the embedded power elements
- The SMPS controller block
- The soft-start block to ramp the current limitation
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the VBIAS pin is connected to an external output voltage
- The current limitation circuit to implement the constant current protection, sensing pulse-by-pulse low-side switch current.
- A circuit to implement the thermal protection function
- LNM pin strapping sets the LNM/LCM mode
- The PG (“Power Good”) open collector output
- The thermal protection circuitry

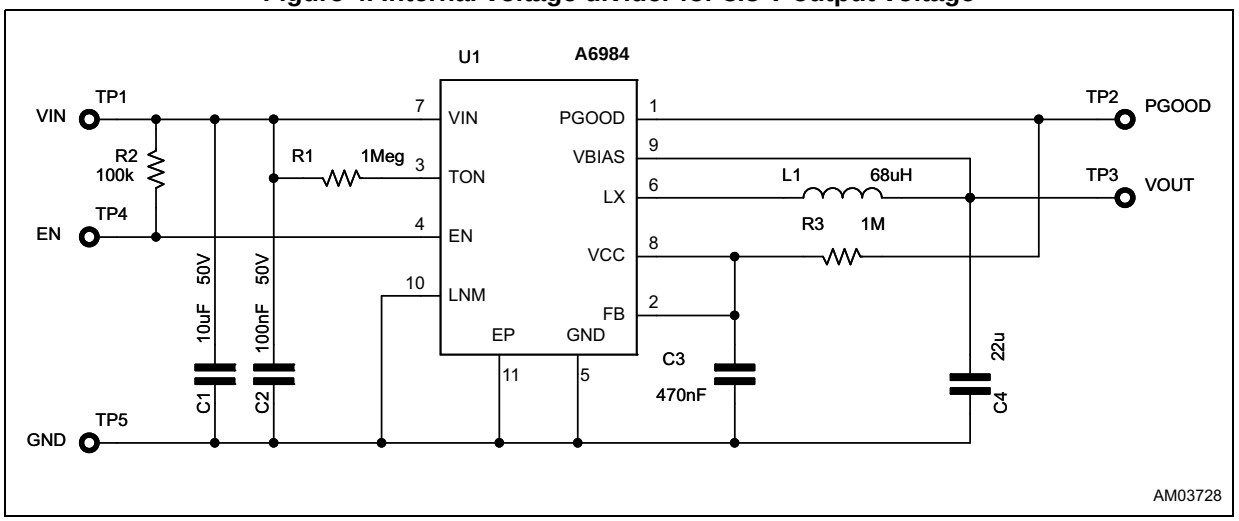
Figure 3. A6984 block diagram



4.1 Output voltage adjustment

No external resistor divider is required to regulate fixed 3.3 V output voltage, connecting FB to the V_{CC} pin and V_{BIAS} to the regulated output voltage (see *Figure 1 on page 1*). An external voltage divider otherwise implements the output voltage adjustability.

Figure 4. Internal voltage divider for 3.3 V output voltage



The error amplifier reference voltage is 0.9 V typical.

The output voltage is adjusted accordingly with the following formula (see *Figure 6*):

Equation 1

$$V_{OUT} = 0.9 \cdot \left(1 + \frac{R_3}{R_2}\right)$$

4.1.1 Maximum output voltage

The constant on-time control scheme naturally requires a minimum cycle-by-cycle off time to sense the feedback voltage and properly driving the switching activity.

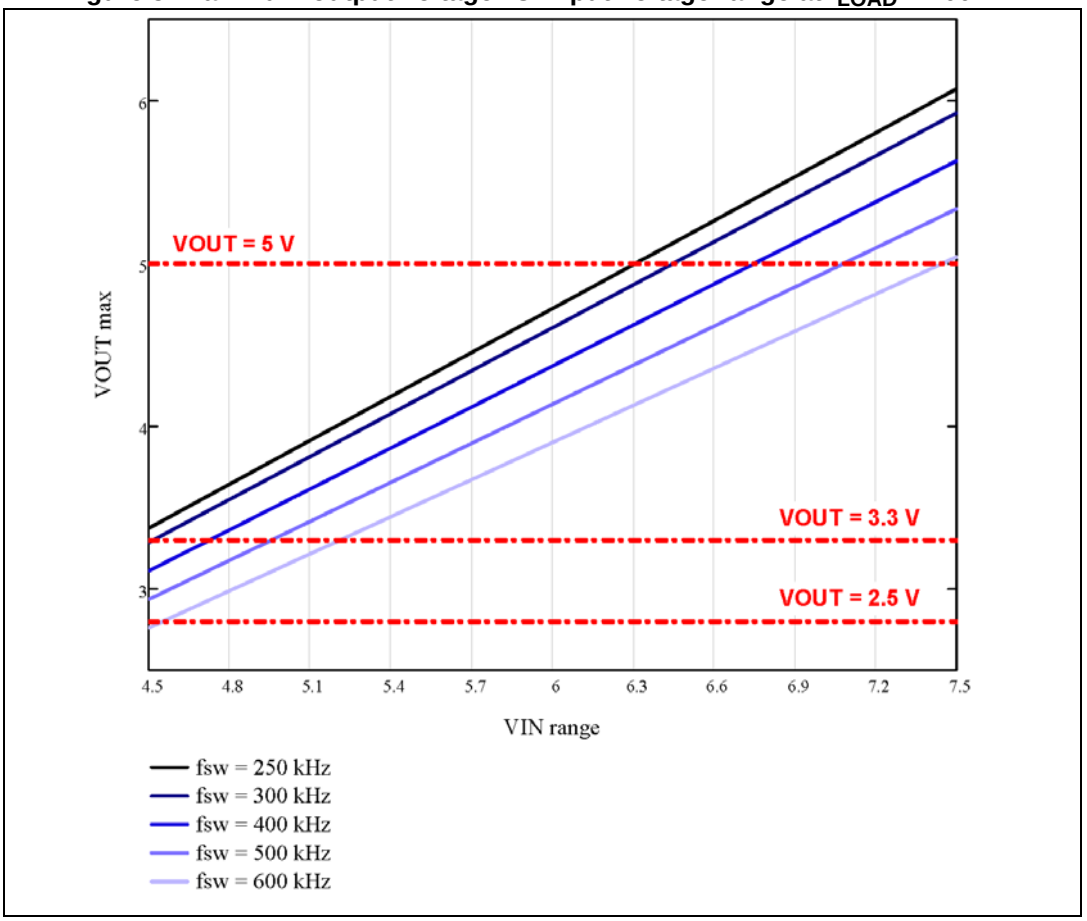
The A6984 minimum off time, as reported in *Table 2 on page 5*, is 300 nsec typical and 400 nsec max.

The control loop generates the proper PWM signal to regulate the programmed output voltage over the application conditions. Since the power losses are proportional to the delivered output power, the duty cycle increases with the load current request.

The fixed minimum off time limits the maximum duty cycle, so the maximum output voltage, depending on the selected switching frequency (see *Section 4.2*).

Figure 5 shows the worst case scenario for maximum output voltage limitation over the input voltage range, that happens at the maximum current request and considering the upper datasheet limit time for the minimum off time parameter.

Figure 5. Maximum output voltage vs. input voltage range at I_{LOAD} = 400 mA



4.1.2 Leading network

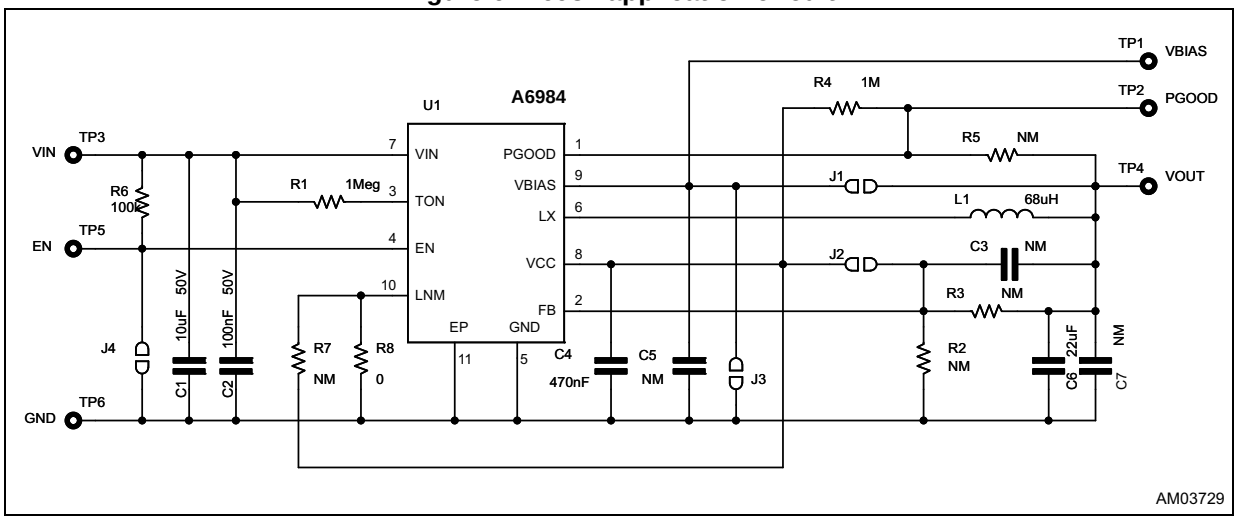
The small signal contribution of a simple voltage divider is:

Equation 2

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3}$$

A small signal capacitor in parallel to the upper resistor (see C3 in *Figure 6*) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$) that can improve the dynamic regulation for boundary application conditions (high f_{SW} / high duty cycle conversion) and improves the SNR for the feedback comparator operation, entirely coupling the high frequency output voltage ripple without the resistive divider attenuation.

Figure 6. A6984 application circuit



Laplace transformer of the leading network:

Equation 3

$$G_{DIV}(s) = \frac{R_2}{R_2 + R_3} \cdot \frac{(1 + s \cdot R_3 \cdot C_{R3})}{\left(1 + s \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}\right)}$$

where:

Equation 4

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_3 \cdot C_{R3}}$$

$$f_P = \frac{1}{2 \cdot \pi \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_{R3}}$$

$$f_Z < f_P$$

The R2, R3 compose the voltage divider. C_{R3} is calculated as (see *Section 5.3.2: COUT specification and loop stability on page 39* for C_{OUT} selection):

Equation 5

$$C_{R3} = 28 \cdot 10^{-3} \cdot \frac{V_{OUT} \cdot C_{OUT}}{R_3}$$

4.2 Control loop

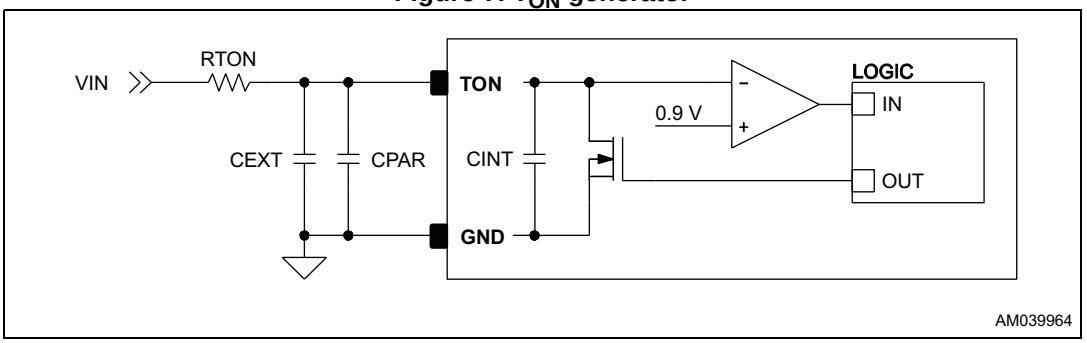
The A6984 device is based on a constant on-time control loop with frequency feed-forward correction over the input voltage range. As a consequence the on-time generator compensates the input voltage variations in order to adapt the duty cycle and so keeping the switching frequency almost constant over the input voltage range.

The general constraint for converters based on the COT architecture is the selection of the output capacitor with an ESR high enough to guarantee a proper output voltage ripple for the noiseless operation of the internal PWM comparator. The A6984 innovative control loop otherwise supports the output ceramic capacitors with the negligible ESR.

The device generates a T_{ON} duration switching pulse as soon as the voltage ripple drops below the valley voltage threshold.

The A6984 on-time is internally generated as shown in *Figure 7*.

Figure 7. T_{ON} generator



where R_{TON} represents the external resistor connected between the V_{IN} and T_{ON} pins, C_{INT} is the integrated capacitor, C_{PAR} the pin parasitic capacitor of the board trace at the pin 3.

The overall contribution of the C_{PAR} and C_{INT} for the A6984 device soldered on the STMicroelectronics evaluation board is 7.5 pF typical but the precise value depends on the parasitic capacitance connected at the pin 3 (TON) that may depend on the implemented board layouts.

As a consequence, a further fine tune of the R_{TON} value with the direct scope measurement is required for precise f_{SW} adjustment accordingly with the designed board layout.

The ON time can be calculated as:

Equation 6

$$T_{ON} = \frac{0.9 \cdot R_{TON} \cdot C_{TON}}{V_{IN}} = \frac{0.9 \cdot R_{TON} \cdot (C_{INT} + C_{PAR})}{V_{IN}} \cong \frac{0.9 \cdot R_{TON} \cdot 7.5pF}{V_{IN}}$$

The natural feedforward of the generator in *Figure 7* corrects the fixed T_{ON} time with the input voltage to achieve almost constant switching frequency over the input voltage range.

On the other hand, the PWM comparator (see *Figure 3 on page 12*) in the closed loop operation modulates the T_{OFF} time, given the programmed T_{ON}, to compensate conversion losses (i.e. conduction, switching, inductor losses, etc.) that are proportional to the output current.

As a consequence the switching frequency slightly depends on the conversion losses:

Equation 7

$$f_{SW}(I_{OUT}) = \frac{D_{REAL}(I_{OUT})}{T_{ON}}$$

where D_{REAL} is the real duty cycle accounting conduction losses:

Equation 8

$$D_{REAL}(I_{OUT}) = \frac{V_{OUT} + (R_{ON\_LS} + DCR) \cdot I_{OUT}}{V_{IN} + (R_{ON\_LS} - R_{ON\_HS}) \cdot I_{OUT}}$$

R_{ON_HS} and R_{ON_LS} represent the RDSON value of the embedded power elements (see *Table 5 on page 7*) and DCR the equivalent series resistor of the selected inductor.

Finally from *Equation 7* and *Equation 8*:

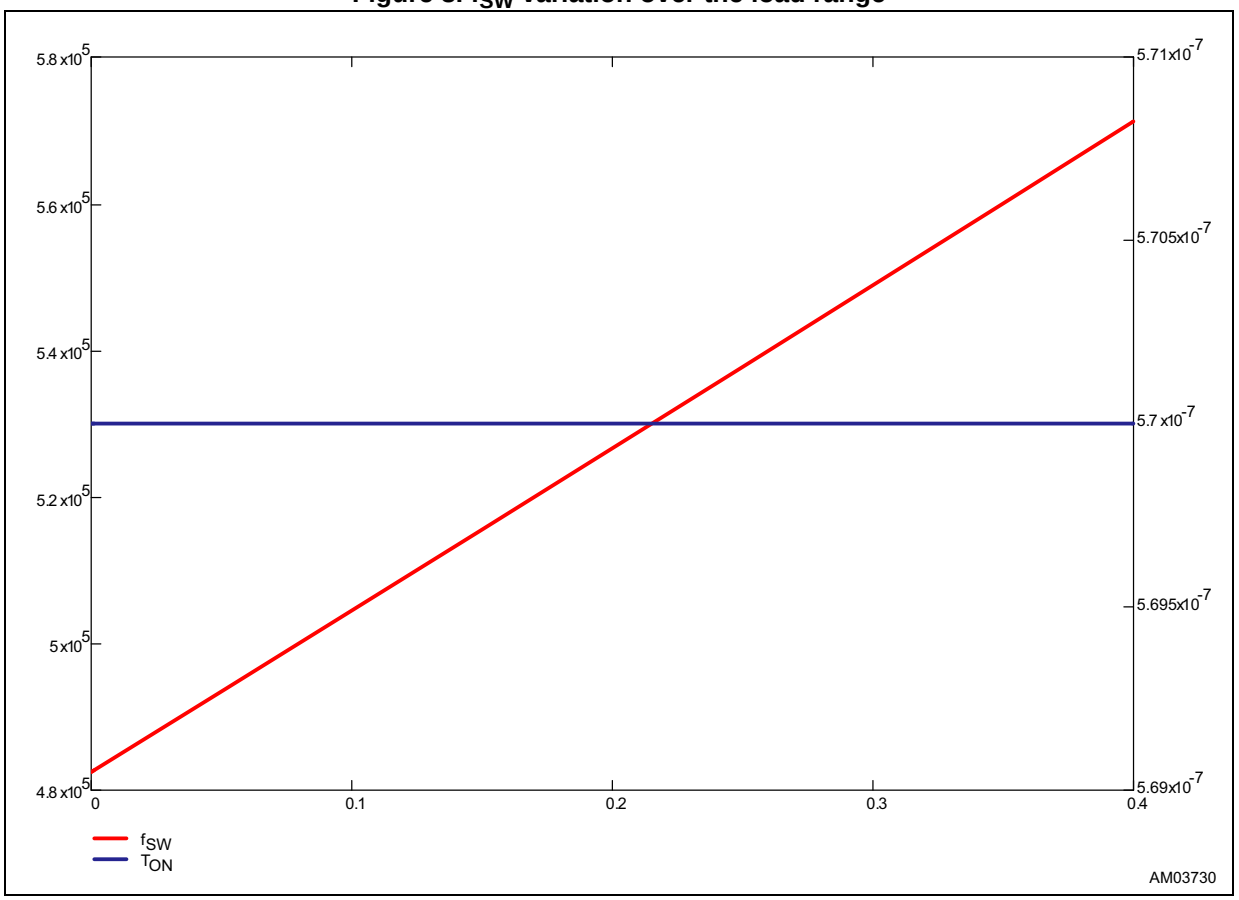
Equation 9

$$R_{TON} = \frac{1}{0.9} \cdot \frac{V_{IN} \cdot D_{REAL}(I_{OUT})}{f_{SW} \cdot C_{TON}}$$

where f_{SW} is the desired switching frequency at a certain I_{OUT} load current level.

Figure 8 shows the estimated f_{SW} variation over the load range assuming the typical RDSON of the power elements, DCR = 420 mΩ (see *Section 6 on page 40* for details on the selected inductor for the reference application board.) and R_{TON} = 1 M.

Figure 8. f_{SW} variation over the load range



A general requirement for applications compatible with humid environments, is to limit the maximum resistor value to minimize the resistor variation determined by the leakage path.

An optional external capacitor C_{TON} >> (C_{INT} + C_{PAR}) connected as shown in *Figure 9* helps to limit the R_{TON} value and also minimizes the f_{SW} variation with the p.c.b. parasitic components C_{PAR}.

Figure 9. T_{ON} generator with optional capacitor

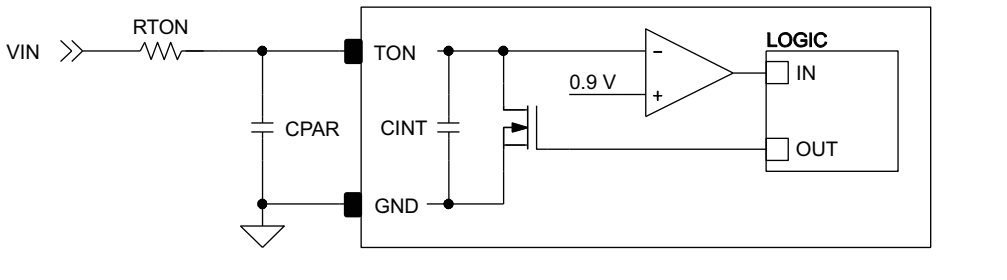


Figure 10, *Figure 11*, *Figure 12*, and *Figure 13* show the numeric example to program the switching frequency accordingly with the R_{TON}, C_{TON} pair selection.

The eDesignSuite online tool supports the A6984 and R_{TON}, C_{TON} dimensioning for proper switching frequency selection, see http://www.st.com/content/st_com/en/support/resources/edesign.html).

Figure 10. Example to select R_{TON}, C_{TON} for V_{OUT} = 1.8 V

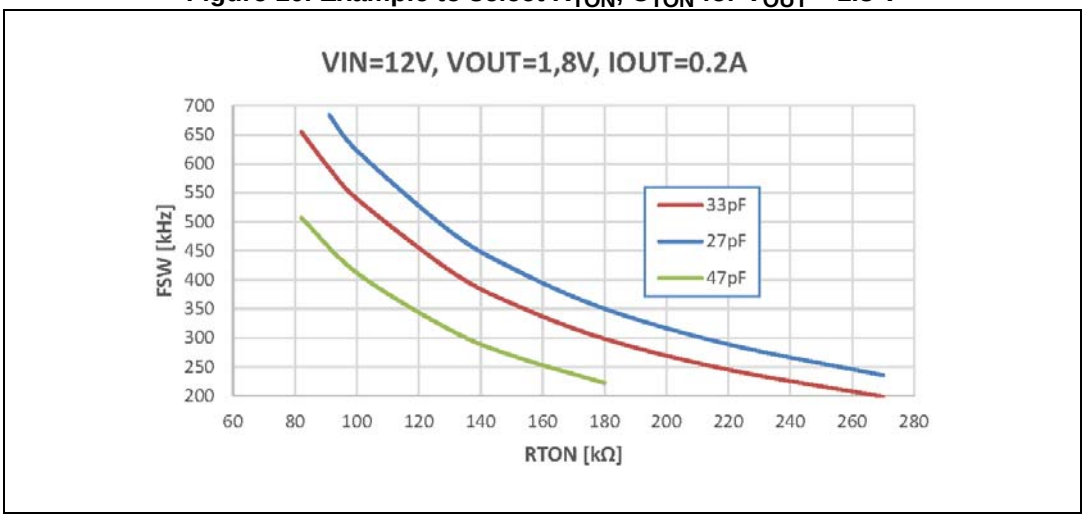


Figure 11. Example to select R_{TON}, C_{TON} for V_{OUT} = 3.3 V

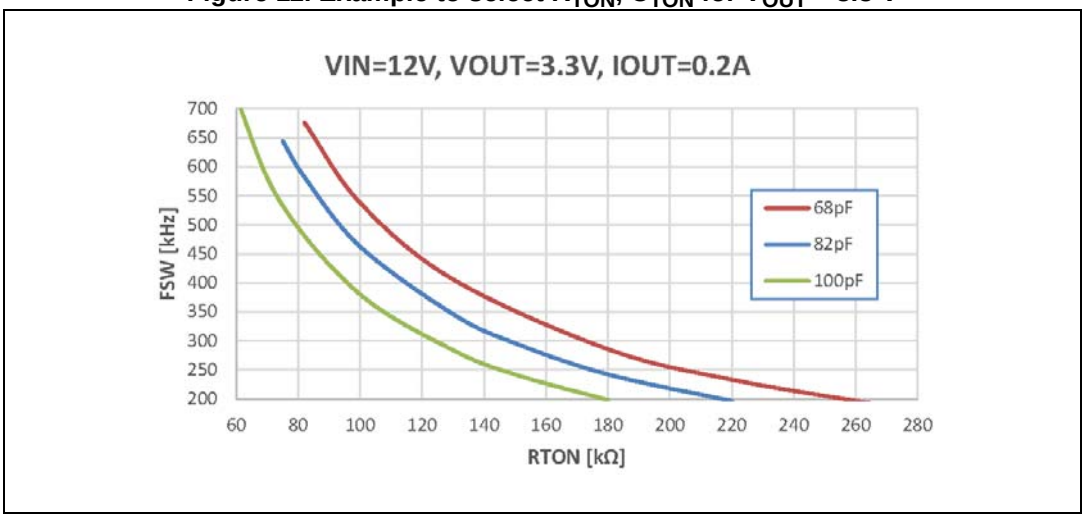


Figure 12. Example to select R_{TON}, C_{TON} for V_{OUT} = 5 V

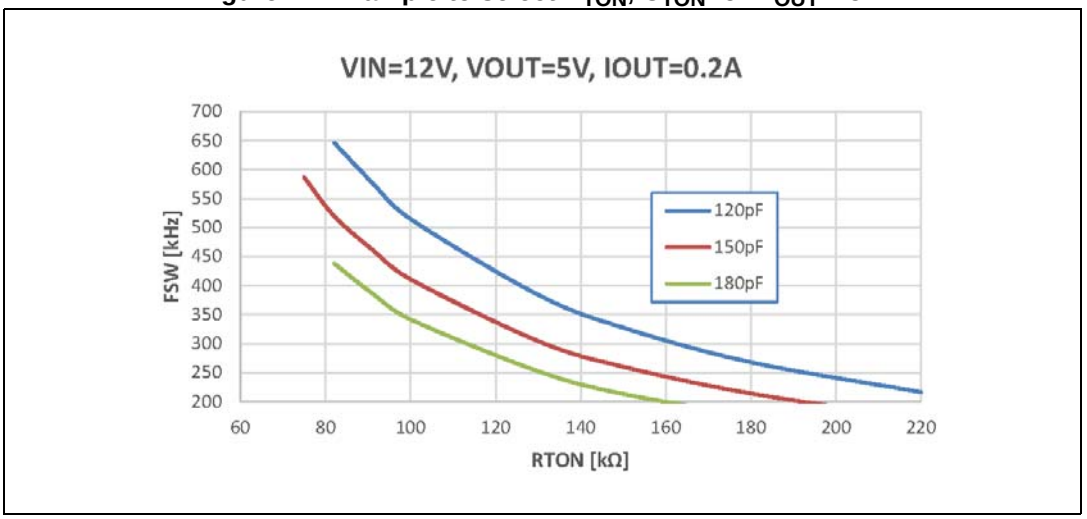
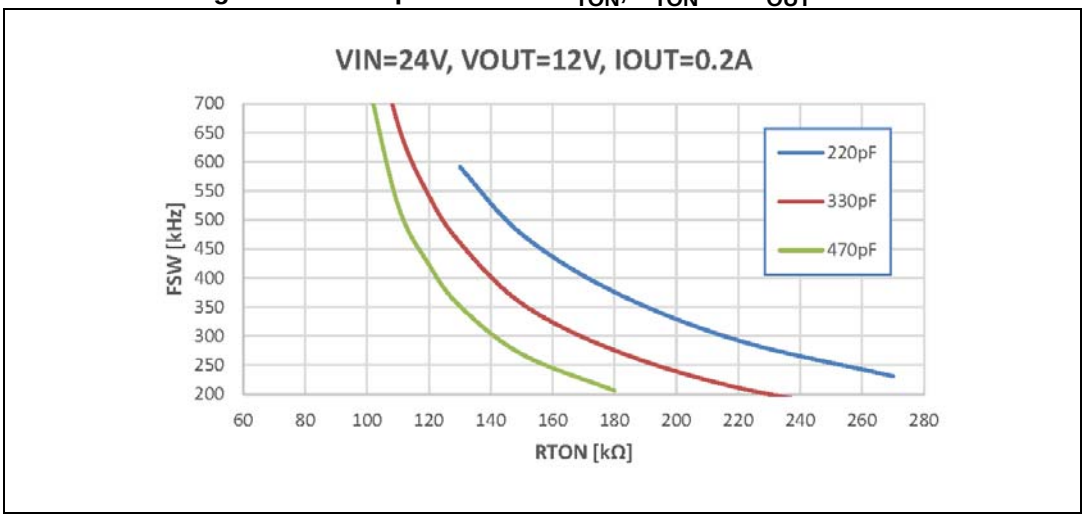


Figure 13. Example to select R_{TON}, C_{TON} for V_{OUT} = 12 V



4.3 Optional virtual ESR network

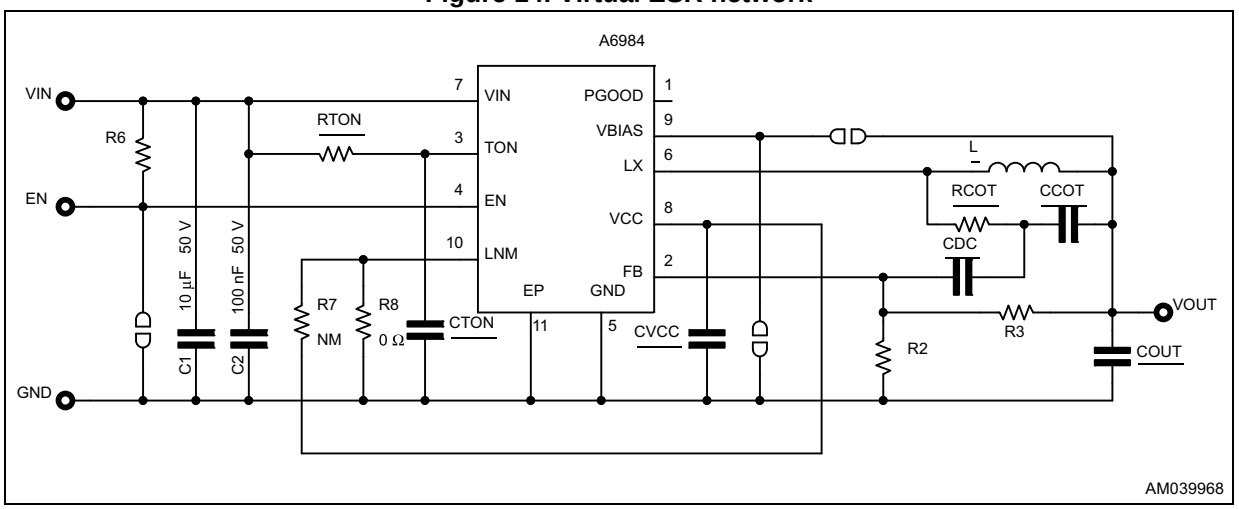
A standard COT loop requires a high ESR output capacitor to generate a proper PWM signal.

The A6984 architecture naturally supports output ceramic capacitors with the negligible ESR generating an internal voltage ramp proportional to the inductor current to emulate a high ESR output capacitor for the proper PWM comparator operation.

The control scheme is designed to guarantee the minimum signal for the PWM comparator cycle-by-cycle operation with controlled duty cycle jitter, that is a natural duty cycle dithering that helps to reduce the switching noise emission for EMC.

If required, an optional external virtual ESR network (see *Figure 14* can be designed to generate a higher signal for the PWM comparator operation and remove the duty cycle dithering. This network requires the external voltage divider to set the output voltage and supports the LNM and LCM device operation.

Figure 14. Virtual ESR network

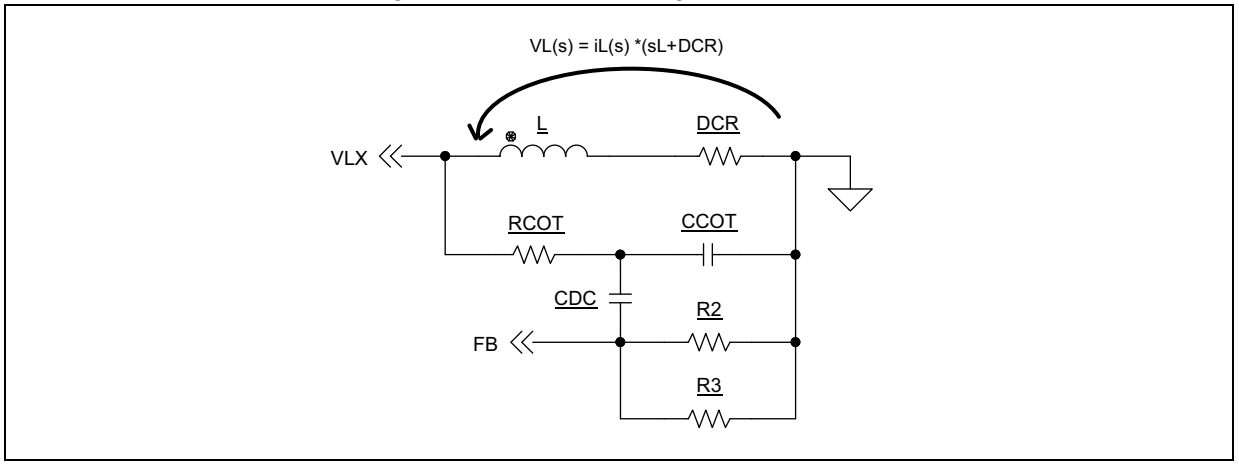


The C_{DC} capacitor decouples the feedback DC path through the R_{COT} so the output voltage is adjusted accordingly with *Section 4.1 on page 13*.

Basically the network R_{COT}, C_{COT} generates a voltage signal proportional to the inductor current ripple and superimposed with the real partitioned output voltage that increases the SNR at the input of the PWM comparator. As a consequence the PWM converter commutation is clean, removing the duty cycle dithering.

For the purpose of the signal generated by the R_{COT} and C_{COT} the output capacitor represents a virtual ground so the equivalent small signal circuit of the output of the virtual ESR network is shown in *Figure 15.*

Figure 15. Virtual ESR equivalent circuit



The switching activity drives the inductor voltage so the small signal transfer function can be calculated as:

Equation 10

$$H(s) = \frac{vFB(s)}{iL(s)} = \frac{(s \cdot L + DCR)}{R_{COT} + \frac{1}{s \cdot C_{COT} + \frac{1}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}}} \cdot \frac{1}{s \cdot C_{COT} + \frac{1}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}} \cdot \frac{\frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}{\frac{1}{s \cdot C_{DC}} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}}$$

Equation 10 can be simplified as follows:

Equation 11

$$H(s) = \frac{vFB(s)}{iL(s)} = \frac{(s \cdot L + DCR) \cdot s}{\left[1 + s \cdot \left(R_{COT} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}}\right) \cdot C_{DC}\right] \cdot \left[1 + s \cdot \left(\frac{1}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_{COT}}}\right) \cdot C_{COT}\right]} \cdot \frac{C_{DC}}{\frac{1}{R_2} + \frac{1}{R_3}}$$

The pole splitting is guaranteed by the condition:

Equation 12

$$C_{DC} > 10 \cdot C_{COT}$$

$$R_{COT} > 10 \cdot \left(\frac{R_2 x R_3}{R_2 + R_3}\right)$$

In case:

Equation 13

$$f_z = \frac{1}{2 \cdot \pi} \cdot \frac{L}{DCR} \ll fsw$$

$$f_{PL} = \frac{1}{2 \cdot \pi \cdot R_{COT} + \frac{1}{\frac{1}{R_2} + \frac{1}{R_3}} \cdot C_{DC}} \ll fsw$$

$$f_{PH} = \frac{1}{2 \cdot \pi \cdot \left(\frac{1}{\frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_{COT}}}\right) \cdot C_{COT}} \ll fsw$$

Equation 10 can be simplified as:

Equation 14

$$ESR_{VRT} = H(s)_{s \to (2 \cdot \pi \cdot fsw)} = \left(\frac{vFB(s)}{iL(s)}\right)_{s \to (2 \cdot \pi \cdot fsw)} = \frac{L}{R_{COT} \cdot C_{COT}}$$

which represents the virtual ESR of the network in *Figure 14*.

As a consequence, the injected triangular voltage ripple in the FB is:

Equation 15

$$VFB_{RIPPLE}(V_{IN}) = IL_{RIPPLE} \cdot ESR_{VRT} = \frac{V_{IN} - V_{OUT}}{R_{COT} \cdot C_{COT}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{fsw}$$

that does not depend on the R_2, R_3, C_{DC}, L and DCR.

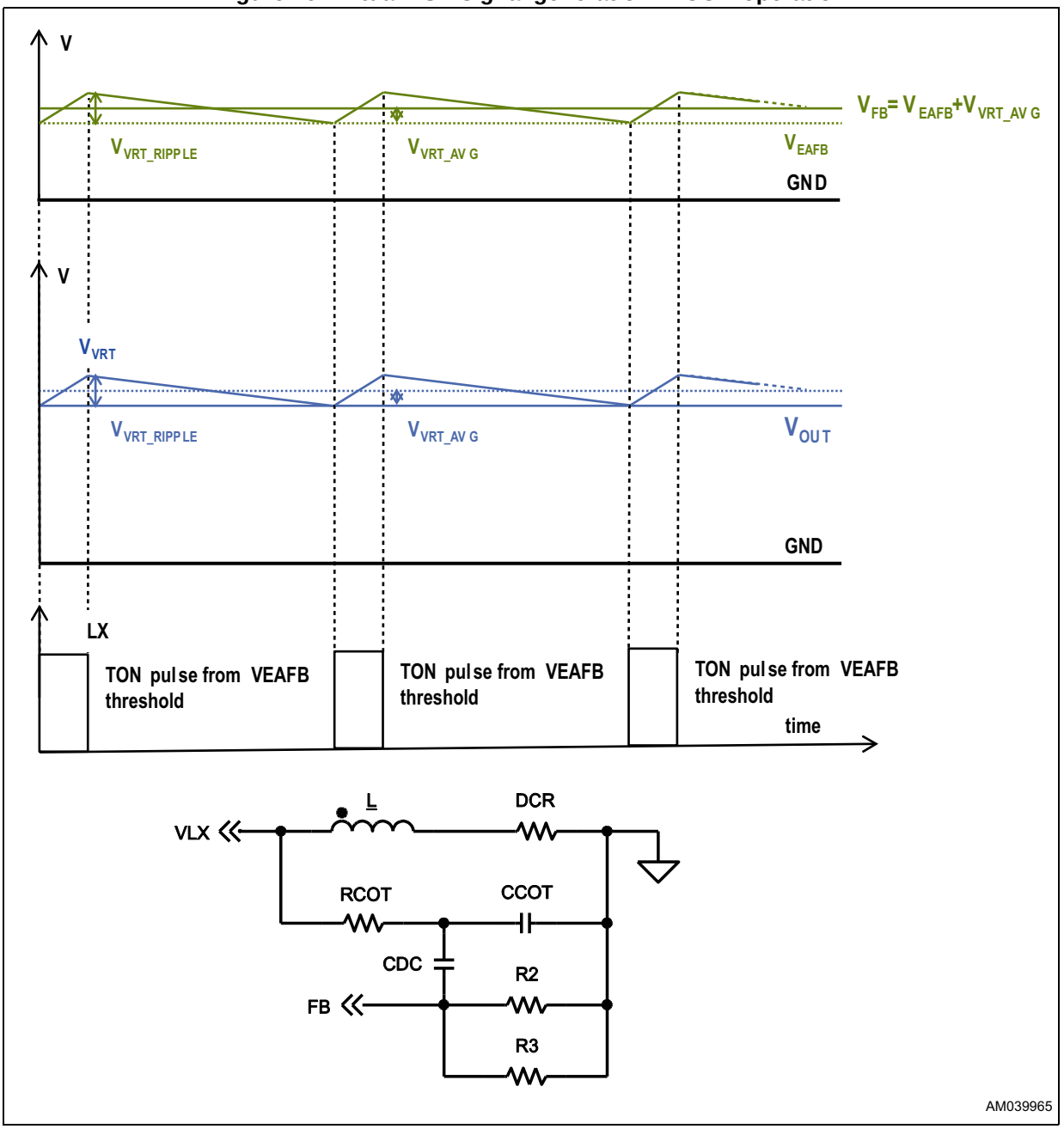
A virtual ESR network able to guarantee a peak-to-peak signal higher than 20 mV at the FB pin removes any duty cycle dithering at the switching node.

Output voltage accuracy and optimized resistor divider

The constant on-time control scheme implements valley output voltage regulation: the internal comparator monitors the FB voltage cycle-by-cycle and generates a fixed T_{ON} pulse if the sensed voltage drops below the internal voltage reference (V_{EAFB} = 0.9 V typical).

The virtual ESR network generates a signal proportional to the inductor current that is AC coupled to the FB pin through the C_{DC} capacitor (refer to *Section 4.3* for dimensioning rules) and superimposed on the voltage divider contribution as shown in *Figure 16*.

Figure 16. Virtual ESR signal generation in CCM operation



In the CCM operation, the average value for the triangular signal in *Equation 15* is:

Equation 16

$$VFB_{AVG}(V_{IN}) = \frac{1}{2} \cdot \frac{V_{IN} - V_{OUT}}{R_{COT} \cdot C_{COT}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{fsw}$$

so the output voltage is calculated as:

Equation 17

$$V_{OUT} = (0.9 + VFB_{AVG}(V_{IN})) \cdot \left(1 + \frac{R_3}{R_2}\right)$$

that shows the average injected ripple entered in the divider calculation.

In addition, since the virtual FB ripple depends on the input voltage (the switching frequency is almost constant, see *Section 4.2 on page 16*) its contribution affects the average output voltage regulation.

In the low noise mode (for LNM operation refer to *Section 4.6.2 on page 32*) the regulator operates in the forced PWM over the load range so:

Equation 18

$$\begin{cases} V_{OUTMIN} = (0.9 + VFB_{AVG}(V_{INMIN})) \cdot \left(1 + \frac{R_3}{R_2}\right) \\ V_{OUTMAX} = (0.9 + VFB_{AVG}(V_{INMAX})) \cdot \left(1 + \frac{R_3}{R_2}\right) \end{cases}$$

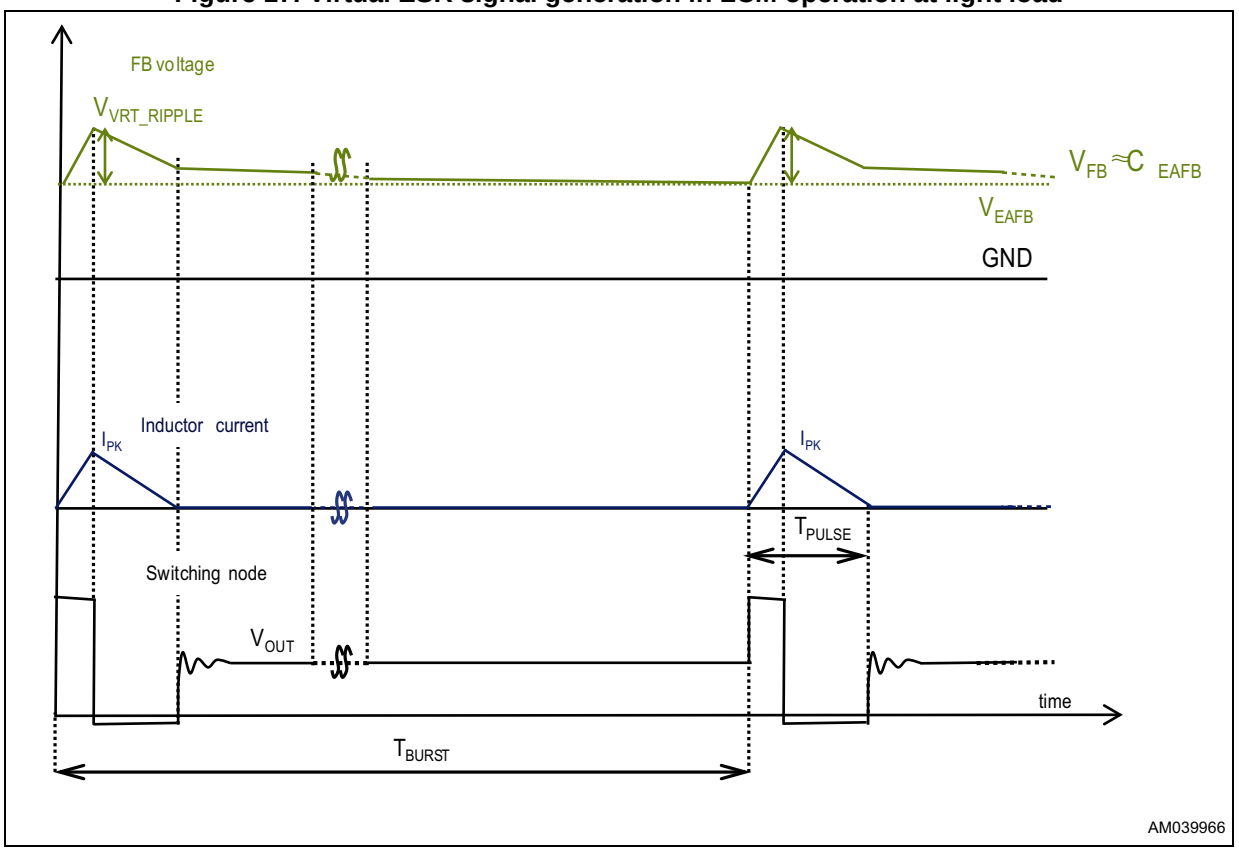
and the accuracy can be estimated as:

Equation 19

$$\Delta V_{OUT-LNM} = \left(\frac{1}{2} \cdot \frac{V_{OUT}}{fsw \cdot R_{COT} \cdot C_{COT}}\right) \cdot \left(\frac{V_{INMAX} - V_{OUT}}{V_{INMAX}} - \frac{V_{INMIN} - V_{OUT}}{V_{INMIN}}\right) \cdot \left(1 + \frac{R_3}{R_2}\right)$$

In the low consumption mode (for LCM operation refer to *Section 4.6.1 on page 32*) the regulator skips pulses at light load to increase the efficiency.

Figure 17. Virtual ESR signal generation in LCM operation at light load



In LCM operation the virtual ripple contributes to the regulated output voltage as follows:

Equation 20

$$\begin{cases} V_{OUTMIN} = \left(0.9 + \frac{1}{2} \cdot VFB_{RIPPLE}(V_{IN}) \cdot \frac{T_{PULSE}}{T_{BURST}}\right) \cdot \left(1 + \frac{R_3}{R_2}\right) \approx 0.9 \cdot \left(1 + \frac{R_3}{R_2}\right) \\ V_{OUTMAX} = (0.9 + VFB_{AVG}(V_{INMAX})) \cdot \left(1 + \frac{R_3}{R_2}\right) \end{cases}$$

since $T_{PULSE} << T_{BURST}$ at zero loading condition.

So the accuracy can be calculated as:

Equation 21

$$\Delta V_{OUT-LCM} = VFB_{AVG}(V_{INMAX}) \cdot \left(1 + \frac{R_3}{R_2}\right)$$

Equation 18, *Equation 19* for the LNM and *Equation 20*, *Equation 21* for the LCM allows proper dimensioning of the FB voltage divider and virtual ESR contribution given the acceptable output voltage accuracy over the application input voltage range.

The eDesignSuite on-line simulation tool (see http://www.st.com/content/st_com/en/support/resources/edesign.html) supports the design based on the A6984 device by inserting the required electrical specifications of the final application. The interface is based on a fully annotated and interactive schematic and the output provides a complete set of the analysis diagram to estimate the electrical, thermal and efficiency performance.

Moreover, it is possible to design the optional virtual ESR network based on the output voltage specification in terms of accuracy over the input voltage range.

4.4 Soft-start

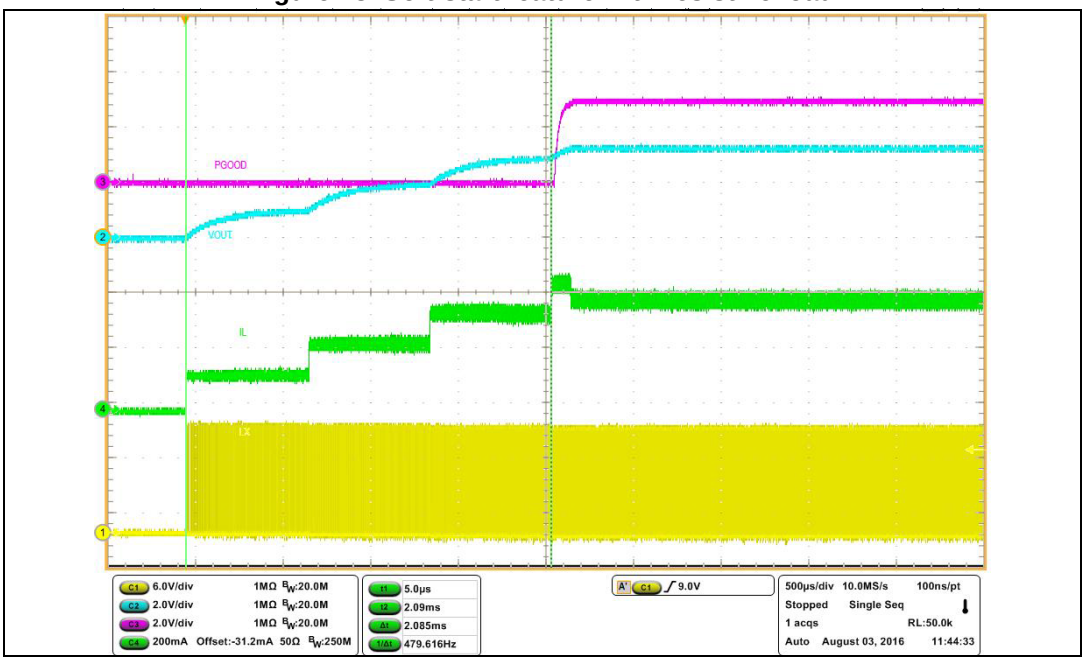
The soft-start feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The A6984 implements the soft-start, clamping the device current limitation in four different steps in 2 msec time.

During normal operation, a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- EN pin rising

Figure 18 shows the soft-start feature. The green trace represents the inductor current which shows different current protection thresholds.

Figure 18. Soft-start feature with resistive load



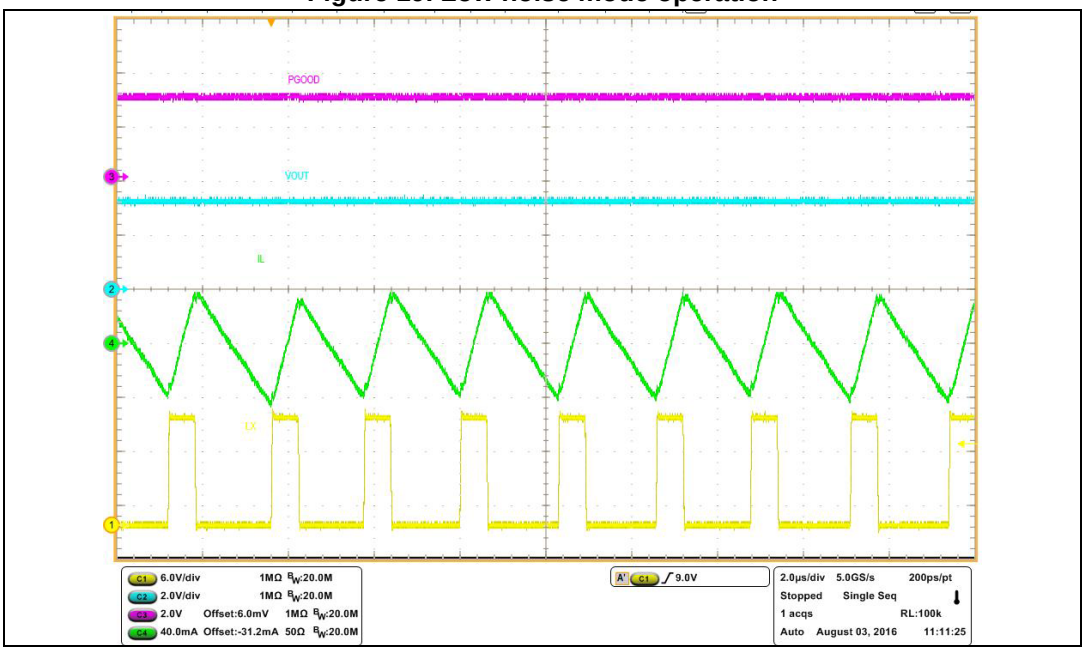
4.5 Light load operation

The LNM pinstrapping during the power-up phase determines the light load operation.

4.5.1 Low noise mode (LNM)

Low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}. The regulator in steady loading condition never skips pulses and it operates in continuous conduction mode (CCM) over the different loading conditions.

Figure 19. Low noise mode operation



Typical applications for LNM operation are car audio and sensors.

4.5.2 Low consumption mode (LCM)

The low consumption mode maximizes the efficiency at the light load. As soon as the output voltage drops, the regulator generates a pulse to have the FB back in regulation. In order to minimize the current consumption in the LCM part of the internal circuitry is disabled in the time between bursts.

Figure 20. LCM operation at zero load

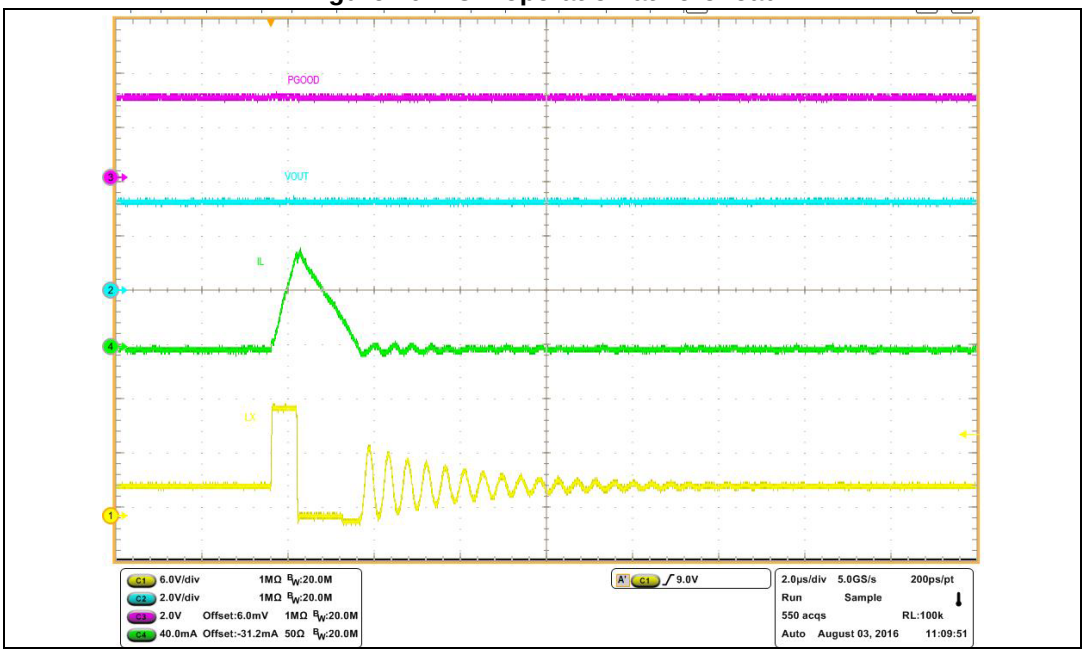
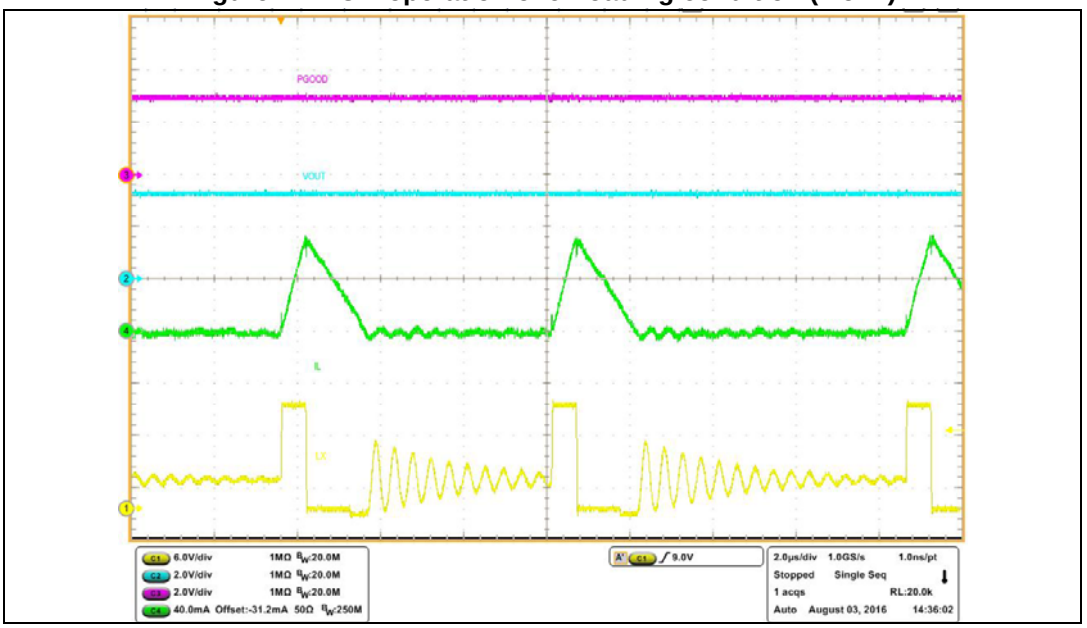


Figure 21. LCM operation over loading condition (1 of 2)

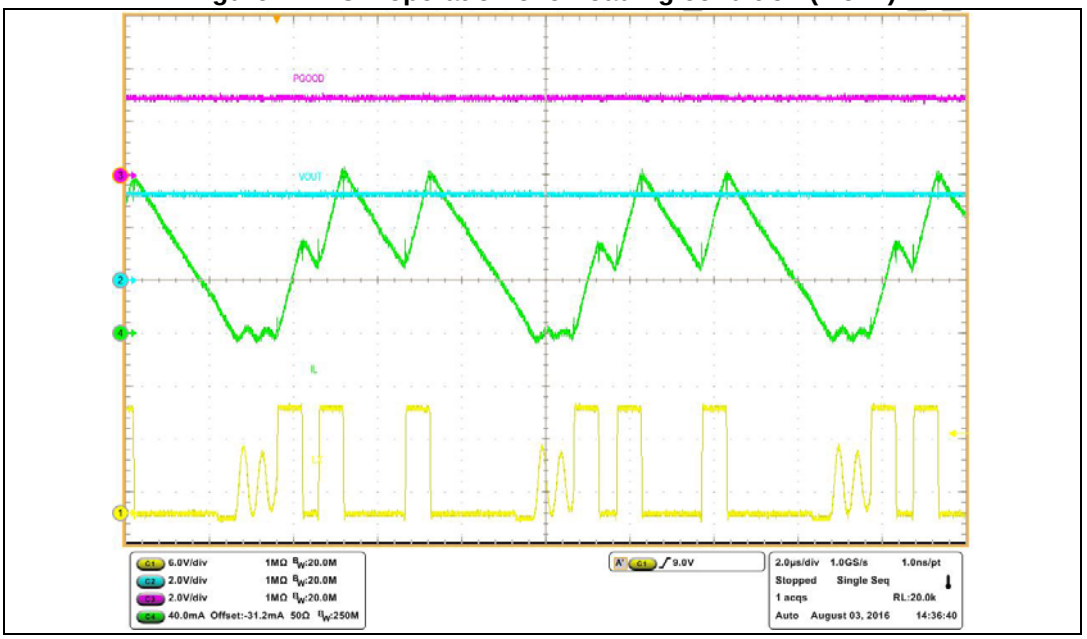


Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

Equation 22

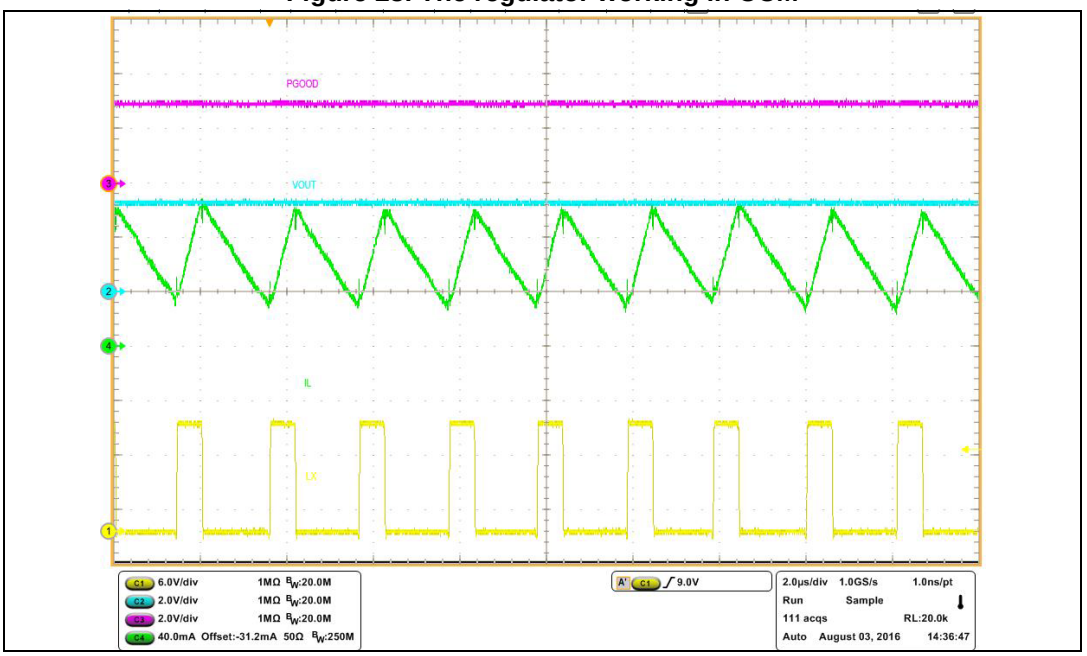
$$V_{OUT\ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (i_L(t) \cdot dt)}{C_{OUT}}$$

Figure 22. LCM operation over loading condition (2 of 2)



When the load current is higher, the $I_{RIPPLE}/2$ the regulator works in CCM.

Figure 23. The regulator working in CCM



4.6 Switchover feature

The switchover maximizes the efficiency at the light load that is crucial for LCM applications.

The main switching controller is supplied by the VCC pin regulator

An integrated LDO regulates VCC = 3.3 V if VBIAS voltage is < 2.4 V.

VCC is connected to VBIAS through a MOSFET switch if VBIAS > 3.2 V and the embedded LDO is disabled to increase the light load efficiency.

4.6.1 LCM

LCM operation satisfies the requirements of battery-powered applications where it is crucial to increase efficiency at the light load.

In order to minimize the regulator quiescent current request from the input voltage, the VBIAS pin can be connected to an external voltage source in the range 3 V < V_{BIAS} < 5.5 V.

In case the VBIAS pin is connected to the regulated output voltage (V_{OUT}), the total current drawn from the input voltage can be calculated as:

Equation 23

$$I_{Q\ VIN} = I_{Q\ OP\ VIN} + \frac{1}{\eta_{A6984}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{Q\ OP\ VBIAS}$$

where $I_{Q\ OP\ VIN}$, $I_{Q\ OP\ VBIAS}$ are defined in *Table 5: Electrical characteristics on page 7* and η_{A6984} is the efficiency of the conversion in the working point.

4.6.2 LNM

Equation 23 is also valid when the device works in LNM and it can boost the efficiency at medium load since the regulator always operates in continuous conduction mode.

4.7 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum current (see *Table 5: Electrical characteristics on page 7*) in overcurrent condition.

The low-side switch pulse-by-pulse current sensing, called “valley”, implements the constant current protection. In overcurrent condition the internal logic keeps the low-side switch conducting as long as the switch current is higher than the valley current threshold.

As a consequence, the maximum DC output current is:

Equation 24

$$I_{MAX} = I_{VALLEY\_TH} + \frac{I_{RIPPLE}}{2} = I_{VALLEY\_TH} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON}$$

Figure 24. Constant current operation in dynamic short-circuit

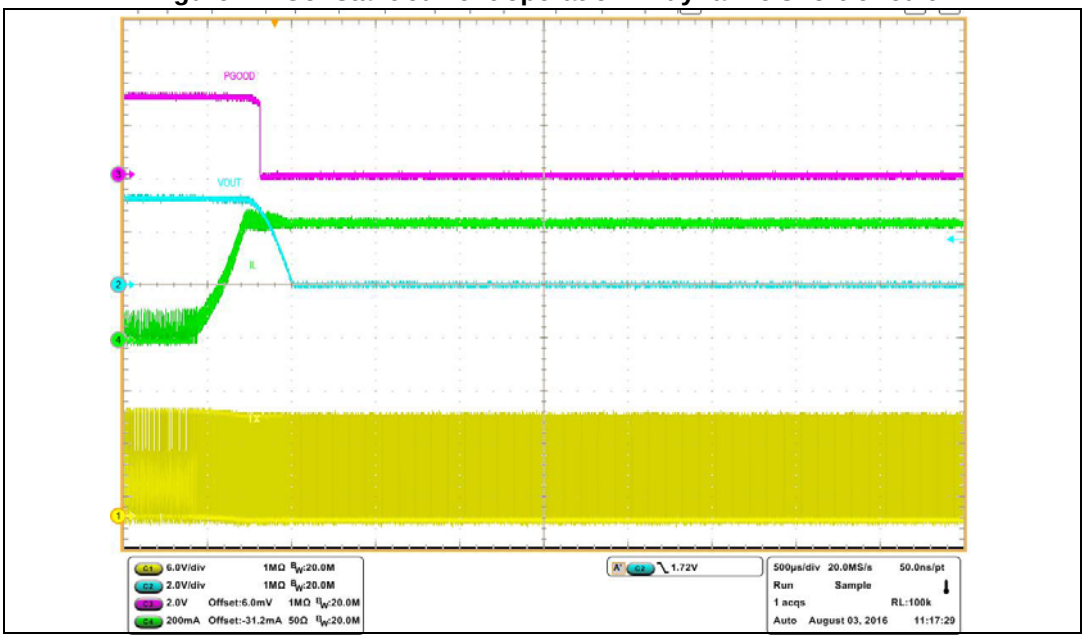
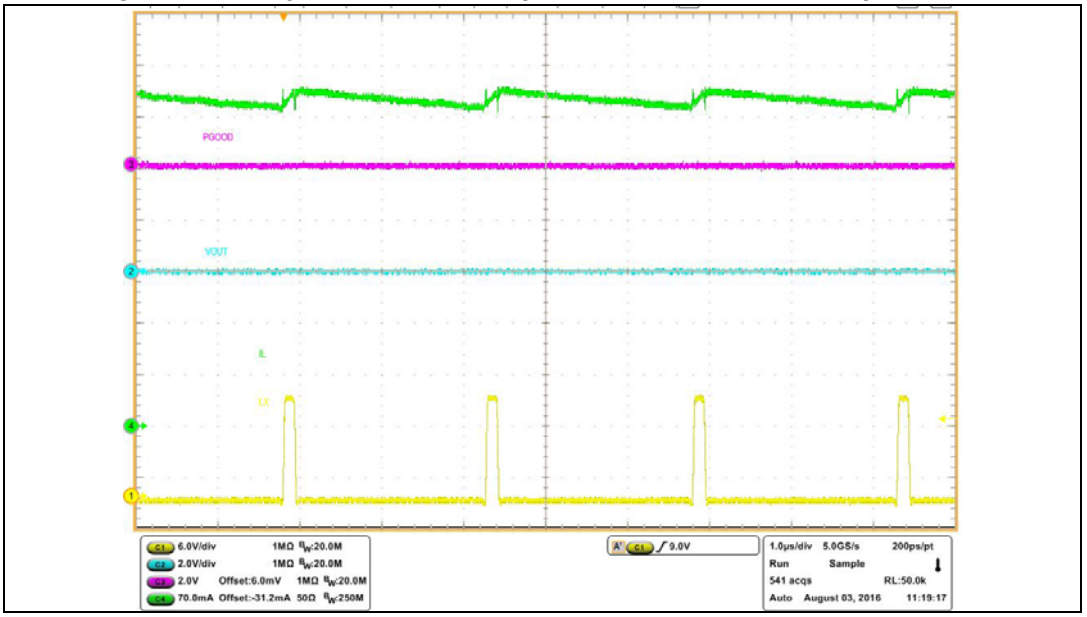


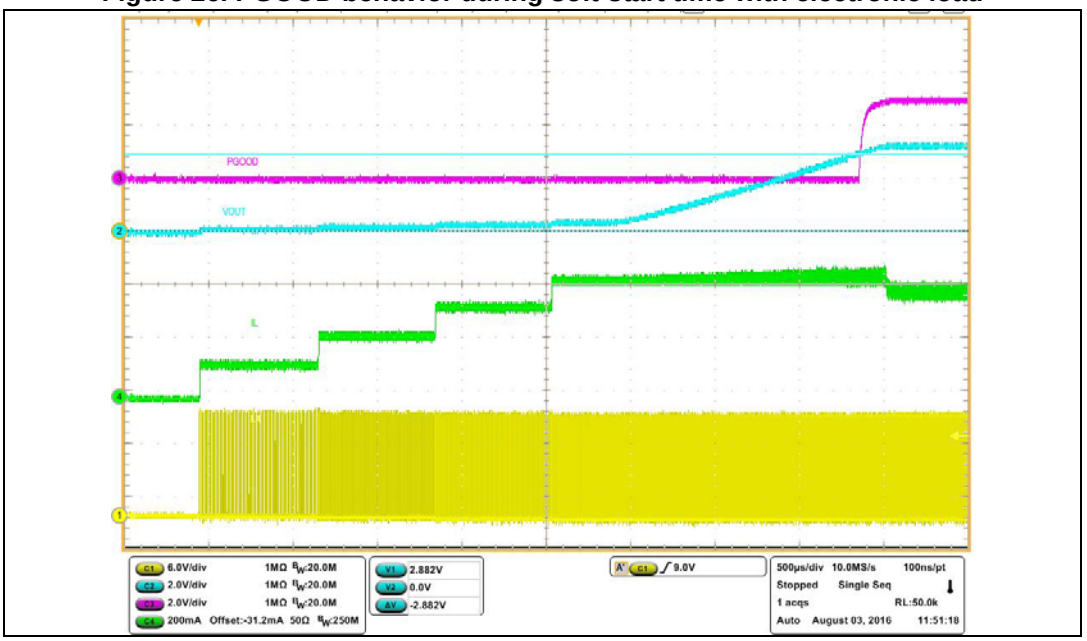
Figure 25. Valley current sense implements constant current protection



4.8 PGOOD

The internal circuitry monitors the regulated output voltage and keeps the PGOOD open collector output in low impedance as long as the feedback voltage is below the $V_{PGD\ L}$ threshold (see *Table 5 on page 7*).

Figure 26. PGOOD behavior during soft-start time with electronic load



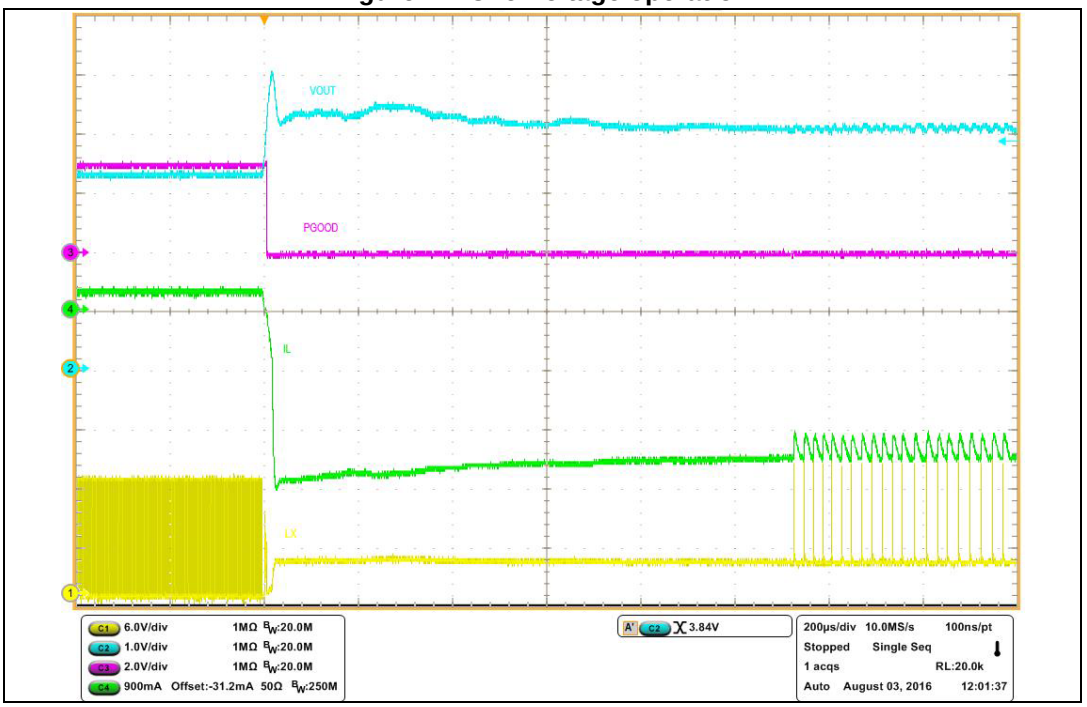
The PGOOD is driven low impedance if $V_{FB} = V_{CC}$ (internal voltage divider, see *Section 4.1 on page 13*) and $V_{BIAS} > V_{PGD\ H}$ threshold (see *Table 5*).

The $V_{PGD\ H}$ threshold has no effect on PGOOD behavior in case the external voltage divider is being used.

4.9 Overvoltage protection

The overvoltage protection monitors the FB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value. A new soft-start takes place after the OVP event ends.

Figure 27. Overvoltage operation



The OVP feature is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance should guarantee an output voltage regulation within the overvoltage threshold even during the worst case scenario in term of load transitions.

The protection is reliable and also able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. As a consequence the output voltage regulation would be affected.

In *Figure 27* the PGOOD output is driven in low impedance (refer to *Section 4.8*) as long as the OVP event is present ($V_{FB} = V_{CC}$, that is an internal resistor divider for $V_{OUT} = 3.3$ V).

4.10 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (150 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 20 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

5 Design of the power components

5.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depend on the ESR value, so usually low ESR capacitors (like multilayer ceramic capacitors) have a higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

Equation 25

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where I_O is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering $\eta = 1$, it is equal to $I_O/2$.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

Equation 26

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMIN} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

and

Equation 27

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOW\_SIDE}}{V_{INMAX} + \Delta V_{LOW\_SIDE} - \Delta V_{HIGH\_SIDE}}$$

Where ΔV_{HIGH_SIDE} and ΔV_{LOW_SIDE} are the voltage drops across the embedded switches.

The input filter value must be dimensioned to safely handle the input RMS current and to limit the V_{IN} ramp-up slew-rate to 0.1 V/µs maximum.

The peak-to-peak voltage across the input filter can be calculated as:

Equation 28

$$V_{PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right] + ESR \cdot I_O$$

In case of negligible ESR (MLCC capacitor) the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

Equation 29

$$C_{IN} = \frac{I_O}{V_{PP} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

Considering $\eta = 1$ this function has its maximum in D = 0.5:

Equation 30

$$C_{IN\_MIN} = \frac{I_O}{2 \cdot V_{PP\_MAX} \cdot f_{SW}}$$

Typically C_{IN} is dimensioned to keep the maximum peak-to-peak voltage across the input filter in the order of 5% V_{IN_MAX}.

Table 6. Input capacitors

Manufacture	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	C3225X7S1H106M	1210	10	50
	C3216X5R1H106M	1206		
Taiyo Yuden	UMK325BJ106MM-T	1210		

5.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple (please refer to *Section 5.3: Output capacitor selection*). Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by the following equation:

Equation 31

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF}$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed $V_{OUT,}$ is obtained at maximum T_{OFF} that is at minimum duty cycle (see *Section 5.1* to calculate minimum duty). So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

Equation 32

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{MAX}} \cdot \frac{1 - D_{MIN}}{F_{SW}}$$

where F_{SW} is the switching frequency $1/(T_{ON} + T_{OFF})$.

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_O = 0.4 A and F_{SW} = 600 kHz the minimum inductance value to have ΔI_L = 30% of I_O is about 33 µH.

The peak current through the inductor is given by:

Equation 33

$$I_{L,PK} = I_O + \frac{\Delta I_L}{2}$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In *Table 7* some inductor part numbers are listed.

Table 7. Inductors

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	LPS6225	47 to 150	0.98 to 0.39
	LPS5030	10 to 47	1.4 to 0.5

5.3 Output capacitor selection

5.3.1 Output voltage ripple

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). As a consequence the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

Equation 34

$$\Delta V_{OUT} = ESR \cdot \Delta I_{MAX} + \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}}$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multilayer ceramic capacitor (MLCC).

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, ΔI_L = 0.12 A, f_{SW} = 600 kHz (resulting by the inductor value) and C_{OUT} = 4.7 µF MLCC:

Equation 35

$$\frac{\Delta V_{OUT}}{V_{OUT}} \cong \frac{1}{V_{OUT}} \cdot \frac{\Delta I_{MAX}}{8 \cdot C_{OUT} \cdot f_{SW}} = \left(\frac{1}{3.3} \cdot \frac{0.12}{8 \cdot 4.7\mu F \cdot 600kHz}\right) = \frac{5mV}{3.3} = 0.15\%$$

The output capacitor value has a key role to sustain the output voltage during a steep load transient. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. In case the final application specifies a high slew rate load transient, the system bandwidth must be maximized and the output capacitor has to sustain the output voltage for time response shorter than the loop response time.

In *Table 8* some capacitor series are listed.

Table 8. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	< 5
	GRM31	10 to 47	6.3 to 25	< 5
PANASONIC	ECJ	10 to 22	6.3	< 5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	< 5

5.3.2 C_{OUT} specification and loop stability

Output capacitor value

A minimum output capacitor value is required for the COT loop stability:

Equation 36

$$C_{OUT} \geq \frac{35}{V_{OUT} \cdot f_{SW}}$$

Equivalent series resistor (ESR)

The maximum ESR of the output capacitor is:

Equation 37

$$ESR_{MAX} \leq 2.8 \cdot 10^{-3} \cdot V_{OUT}$$

6 Application board

The reference evaluation board schematic is shown in *Figure 28*.

Figure 28. Evaluation board schematic

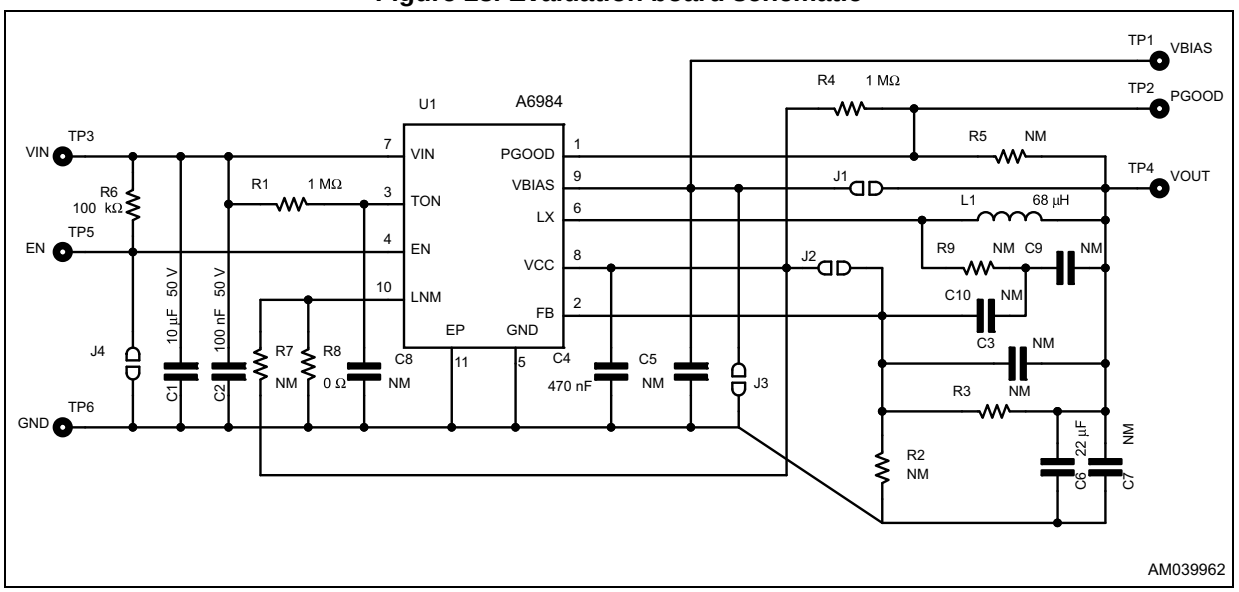


Table 9. Bill of material

Reference	Part number	Description	Manufacturer
C1	CGA5L3X5R1H106K160AB	10 µF - 50 V - 1206	TDK
C2	-	100 nF - 50 V - 0805	-
C4	-	470 nF - 10 V - 0603	-
C6	CGA5L1X5R1C226M160AC	22 µF - 16V - 1206	TDK
L1	MSS6132-683MLC	68 µH	Coilcraft
R1	-	1 MΩ - 1% - 0603	-
R4	-	1 MΩ - 5% - 0603	-
R6	-	100 kΩ - 5% - 0603 V	-
R8	-	0 Ω - 0603	-
U1	A6984	-	ST
J1	-	JUMPER - CLOSED	-
J2	-	JUMPER - CLOSED	-
J3	-	JUMPER - OPEN	-
J4	-	JUMPER - OPEN	-
R2, R3, R5, R7, R9, C3, C5, C7, C8, C9, C10	-	NOT MOUNTED	-
TP1, TP2, TP3, TP4, TP5, TP6, TP7	-	VBIAS, PGOOD, VIN, VOUT, EN, GND, GND	-

Figure 29. Top layer 4 x 4 DFN evaluation board

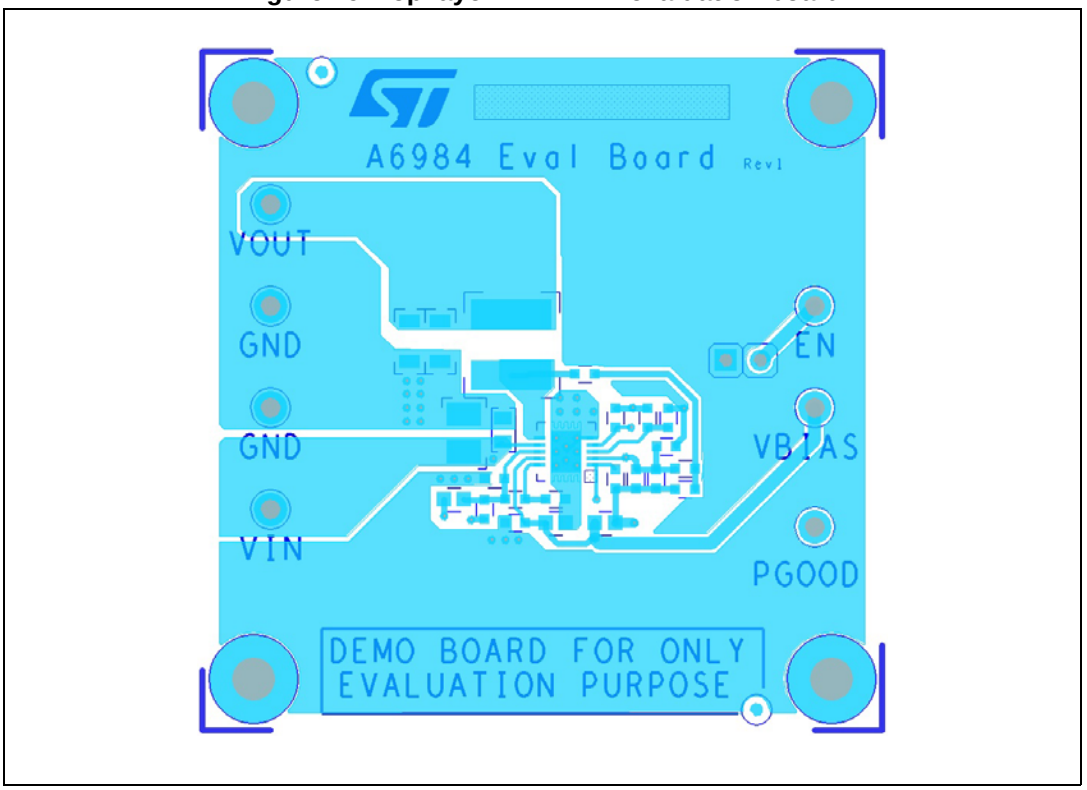
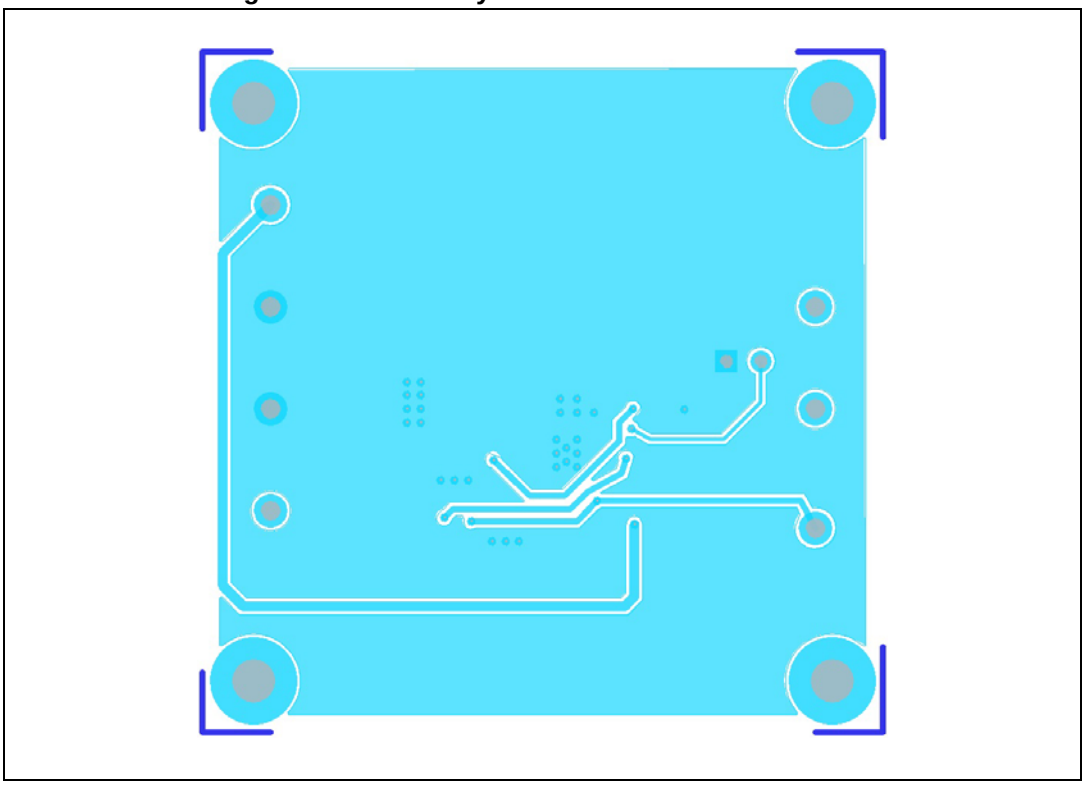


Figure 30. Bottom layer 4 x 4 DFN evaluation board



7 Efficiency curves

Figure 31. VIN 12 V - VOUT 5 V (linear scale)

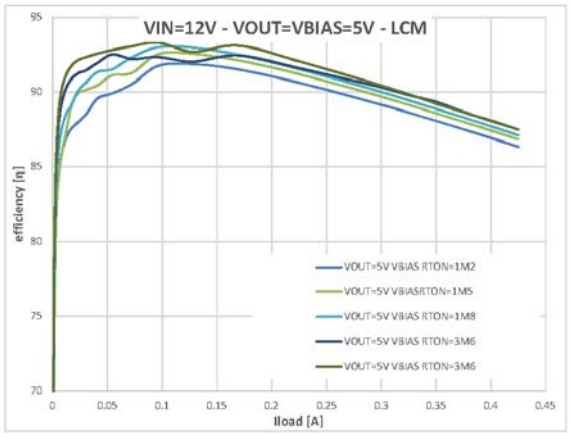


Figure 32. VIN 24 V - VOUT 5 V (linear scale)

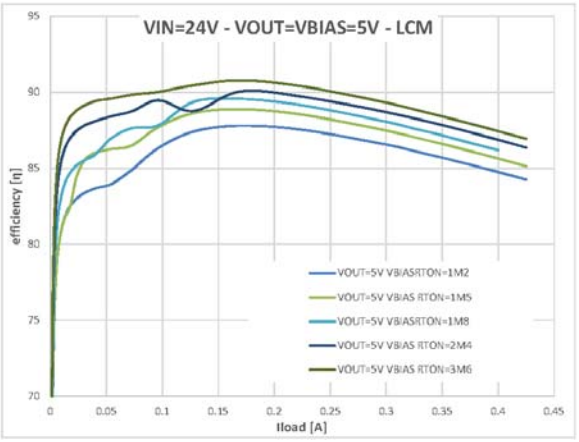


Figure 33. VIN 12 V - VOUT 3.3 V (linear scale)

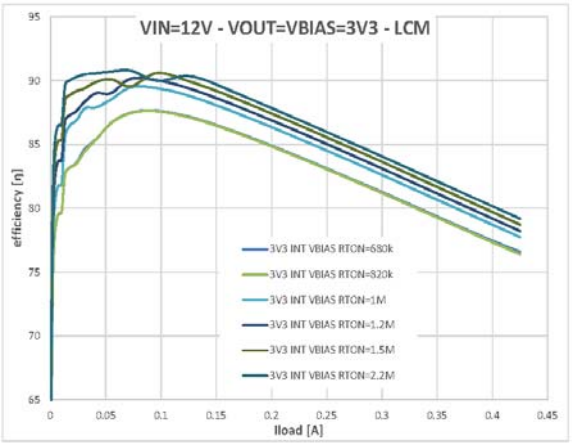


Figure 34. VIN 12 V - VOUT 5 V (log scale)

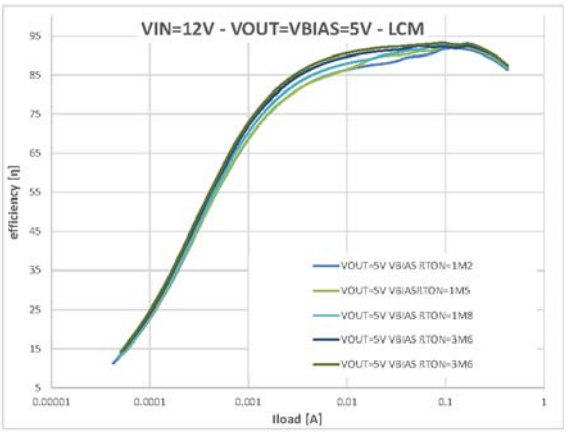


Figure 35. VIN 24V - VOUT 5 V (log scale)

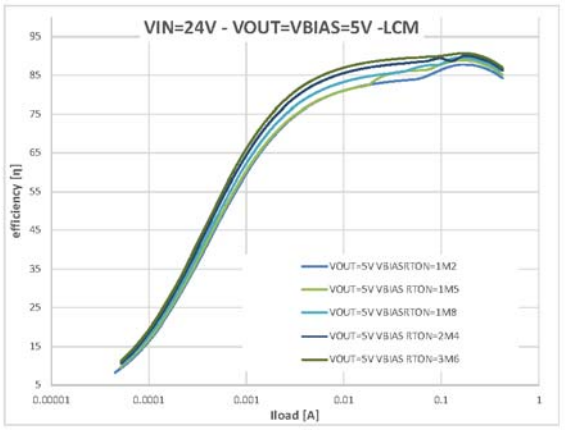


Figure 36. VIN 12 V - VOUT 3.3 V (log scale)

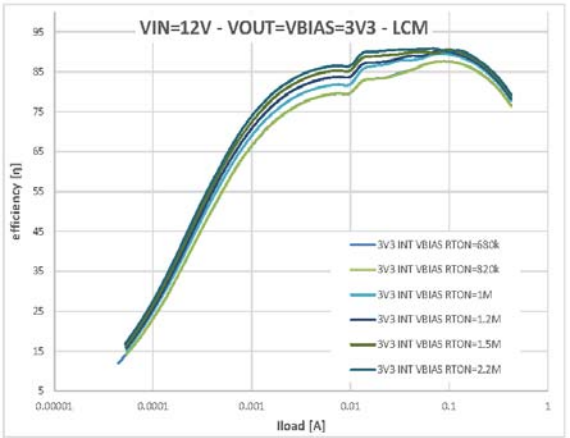


Figure 37. VIN 24 V - VOUT 3.3 V (linear scale)

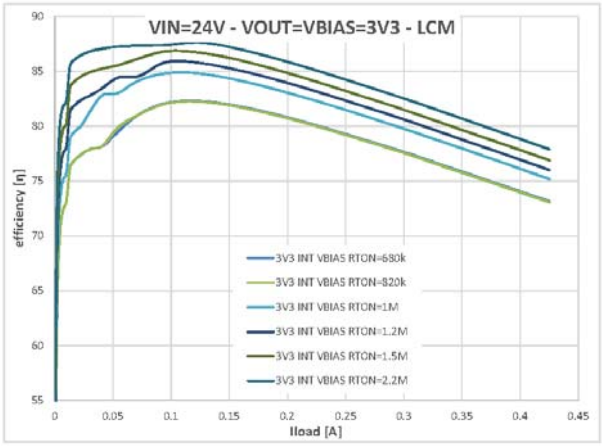


Figure 38. VIN 12 V - VOUT 2.5 V (linear scale)

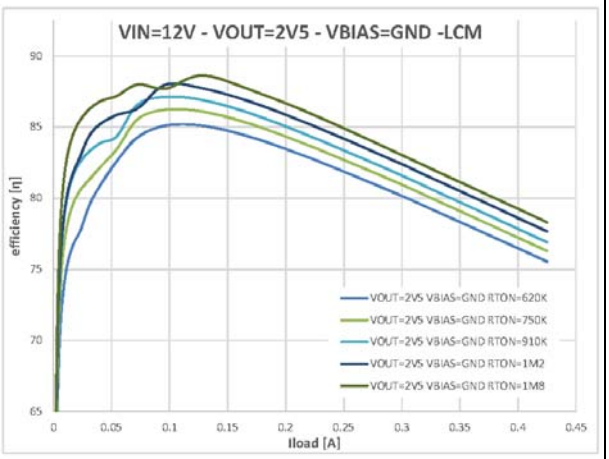


Figure 39. VIN 24V - VOUT 2.5 V (linear scale)

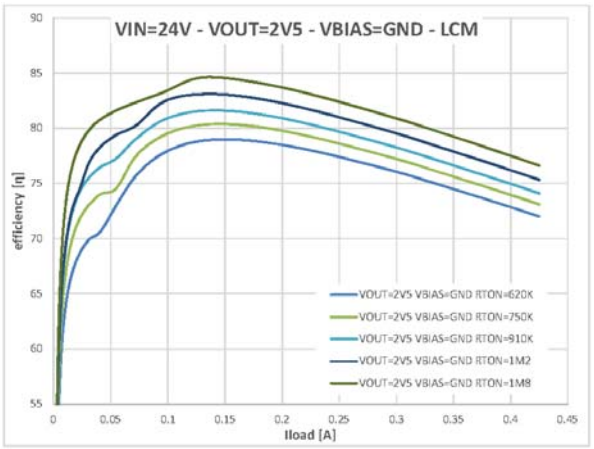


Figure 40. VIN 24V - VOUT 3.3 V (log scale)

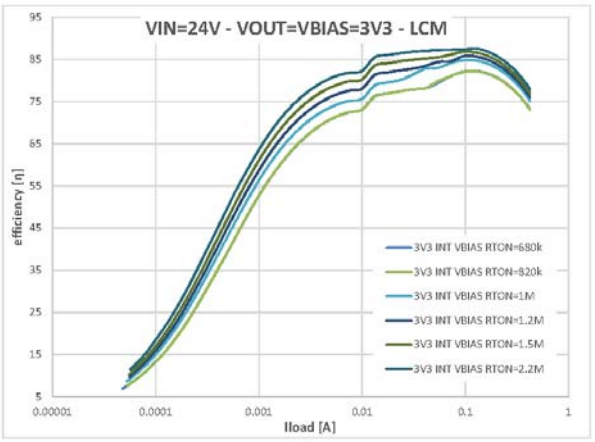


Figure 41. VIN 12 V - VOUT 2.5 V (log scale)

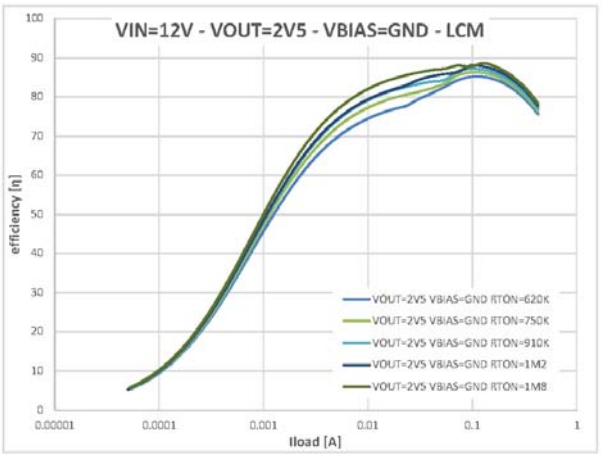
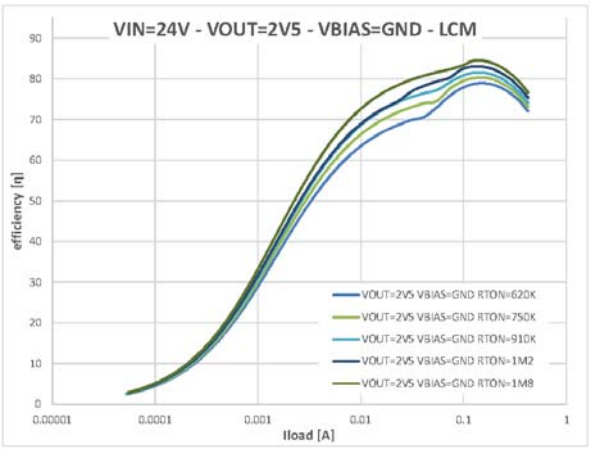


Figure 42. VIN 24 V - VOUT 2.5 V (log scale)



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

8.1 VFDFPN10 4 x 4 x 1.0 mm package information

Figure 43. VFDFPN10 4 x 4 x 1.0 mm package outline

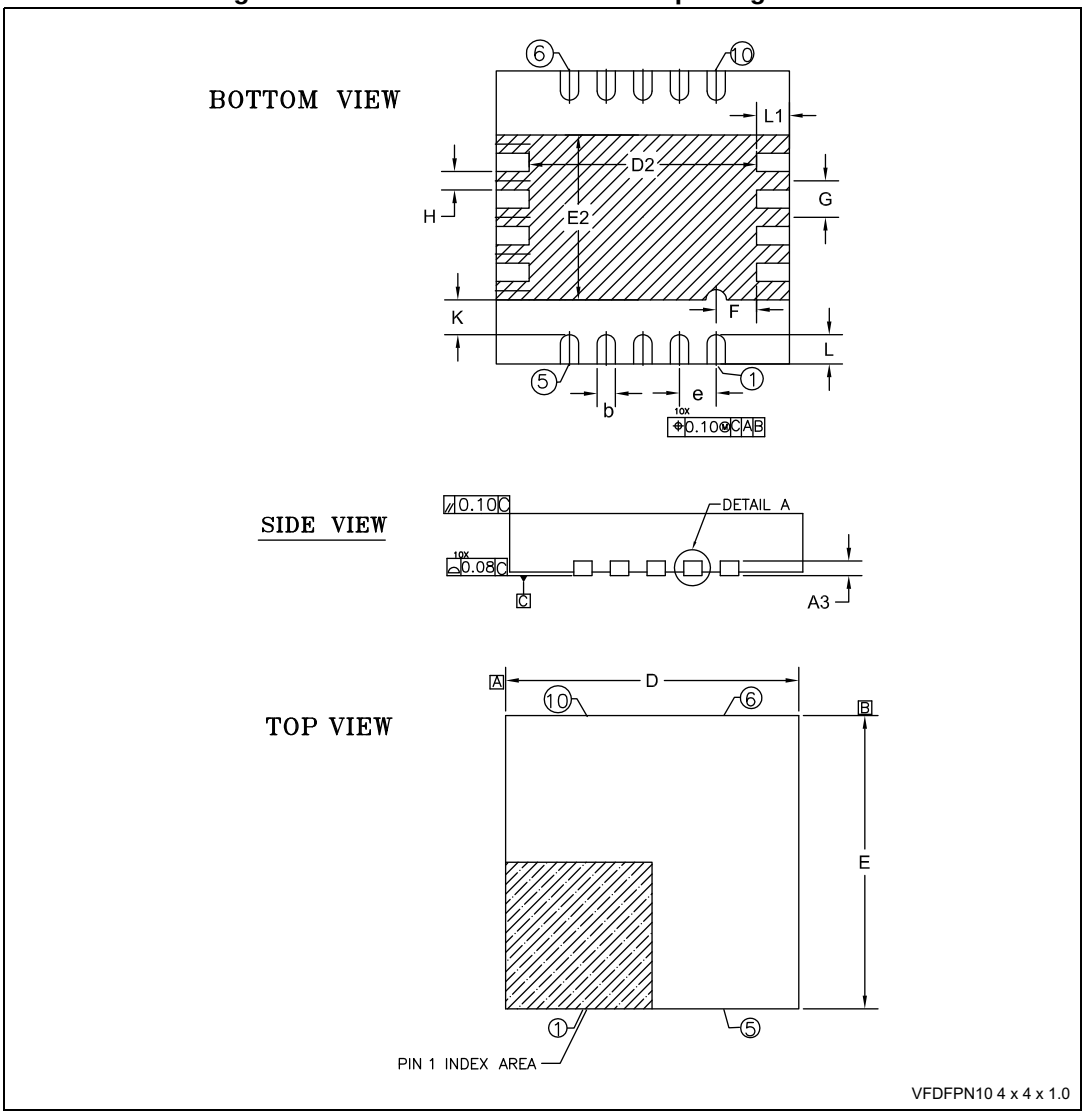


Table 10. VFDFPN10 4 x 4 x 1.0 mm package mechanical data[1], [2], [3]

Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	0.80	0.85	0.90
A1	0.0	-	0.05
A3		0.20 REF.	
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	3.00	3.10	3.20
e		0.50 BSC	
E	3.90	4.00	4.10
E2	2.15	2.25	2.35
F		0.55 REF.	
G		0.50 BSC	
H		0.25 REF.	
L	0.30	0.40	0.50
L1		0.45 REF.	
K		0.475 REF.	
N		10	

1. All dimensions are in mm, angles in degrees.
2. Coplanarity applies to the exposed pad as well as the terminals. Coplanarity shall not exceed 0.08 mm.
3. Warpage shall not exceed 0.10 mm.

Figure 44. VFDFPN10 4 x 4 x 1.0 mm package detail A

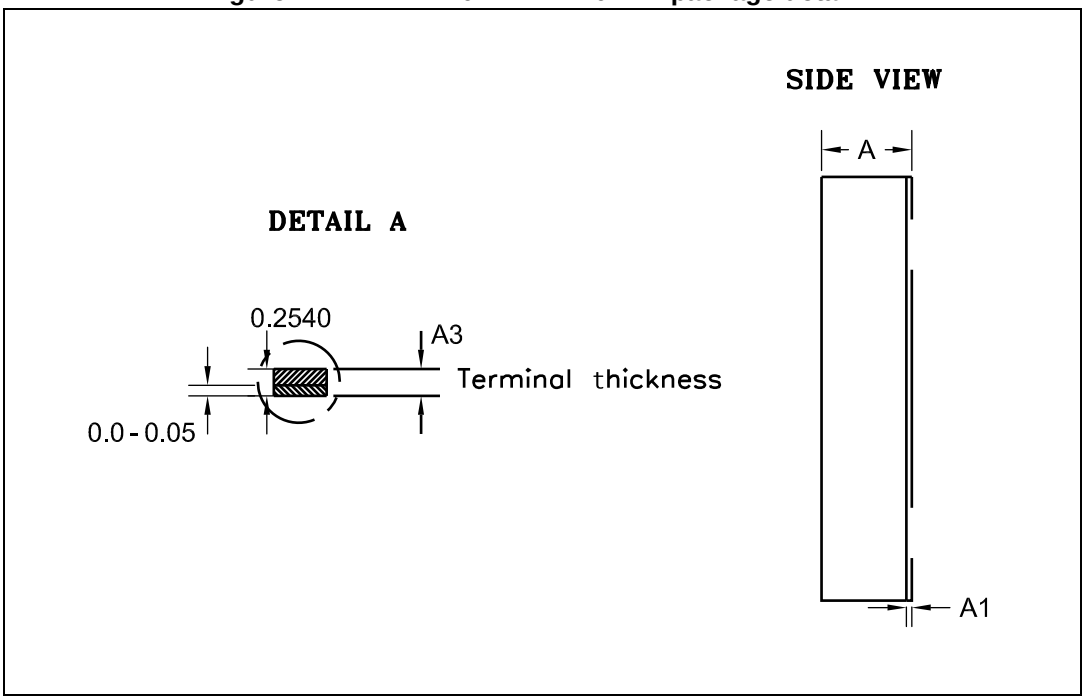
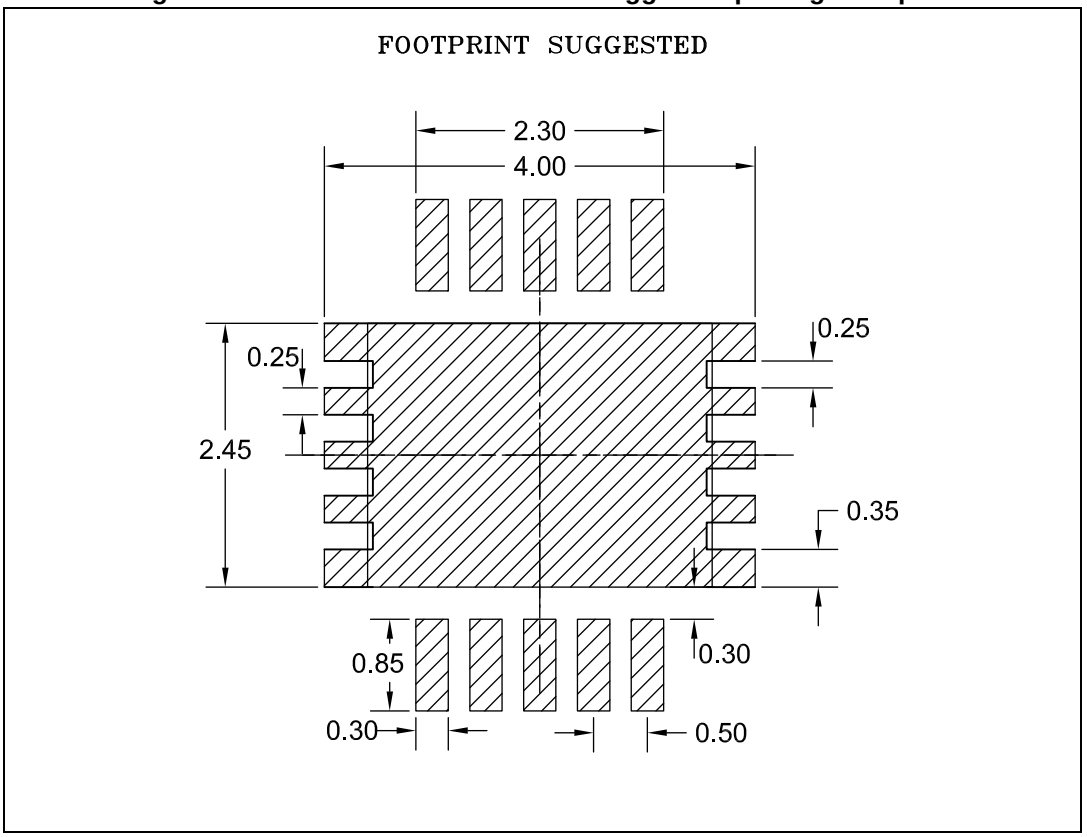


Figure 45. VFDFPN10 4 x 4 x 1.0 mm suggested package footprint



9 Ordering information

Table 11. Order codes

Part number	Package	Packaging
A6984	VFDFPN10 4 x 4	Tube
A6984TR	VFDFPN10 4 x 4	Tape and reel

10 Revision history

Table 12. Document revision history

Date	Revision	Changes
02-Mar-2017	1	Initial release
19-Dec-2017	2	Added sentence between *Equation 27* and *Equation 28*.
11-May-2018	3	Updated: Features on the cover page, *Figure 15*, *Equation 12* and sentence between *Equation 27* and *Equation 28*. Added: new item dV_{IN}/dt and footnote on *Table 2*.