SPZB32W1x1.4

802.15.4 long range modules based on the STM32W chipset

Datasheet – production data

Features

- 2.4 GHz IEEE 802.15.4-compliant SMD modules based on the ST STM32W chipset solution featuring:
  - Integrated 2.4 GHz transceiver
  - PHY and MAC IEEE 802.15.4 features
  - Integrated ARM® Cortex-M3 core
  - Integrated embedded Flash and RAM
  - Integrated encryption (AES-128) accelerator
- Power amplified RF performances:
  - Up to 20 dBm nominal TX output power
  - Up to 105 dBm RX sensitivity
- Robust Wi-Fi and Bluetooth® coexistence
- 16 channels (IEEE 802.15.4 channel 11 to 26)
- Multiple configurable interfaces available (UART, SPI, I^2C, ADC, GPIOs)
- Industry standard JTAG programming
- Onboard 24 MHz and 32.768 kHz stable Xtal
- Less than 2 µA typ. power consumption in deep sleep mode (32.768 Xtal)
- Multiple antenna options: integrated antenna or integrated UFL connector
- Multiple protocol stack options
- Single voltage supply (2.1 to 3.6 V)
- FCC and CE compliant qualified
- Small form factor: 16.4 x 26.5 mm
- Operating temperature range: -40 °C to +85 °C.

AM02872v1

Contents

1 Description

The SPZB32W1x.4 is a ready-to-use device, compliant with IEEE 802.15.4 and power amplified RF modules optimized for embedded applications. It requires low data rate communication and high transmission range capabilities based on the STM32W single chip, which integrates a 2.4 GHz, IEEE 802.15.4-compliant transceiver together with an ARM® Cortex embedded processor.

The modules are very compact and enable OEMs to easily add wireless capabilities to electronics devices by optimizing time-to-market, cost, size, and consumption of their target applications. No RF experience or expertise is required to add this powerful networking capability to the final product.

24 MHz high stability Xtal is available onboard the modules to perform the timing requirements as per IEEE 802.15.4 specifications; additionally a 32.768 kHz Xtal is also provided onboard for low power operation.

A single supply voltage is requested to power the modules. The supply is in the range of 2.1 to 3.6 V. The voltage supply also determines the I/O ports level allowing an easy interface with additional peripherals.

An advanced solution integrating PA and LNA in a single package is onboard to ensure excellent power transmission and receiver sensitivity performances.

To support user defined applications, a number of peripherals such as GPIO, UART, I^2C, ADC and general purpose timers are available and user selectable.

The size and footprint of this series of modules is equivalent to that of the series SPZB32W1x2.4 to facilitate the evaluation of the different range options on the target application.

The SPZB32W1x1.4 is based on the STM32W108CB chipset integrating 128 kB of embedded flash memory and 8 kB of RAM available for data and program storage.

For technical details on the STM32W108CB chipset refer to the related datasheet. For technical details on the supported stacks refer to the related user guides and application notes available on the ST website.

2 RoHS compliance

ST modules are RoHS compliant and comply with ECOPACK® norms.

3 Application

- Smart energy applications
- Machine2Machine industrial control
- Wireless sensor networks
- Home/building automation
- Smart appliances
- Wireless alarms and security systems
- Lighting control
- Remote monitoring

4 Block diagram

Figure 1. SPZB32W1A1.4 block diagram

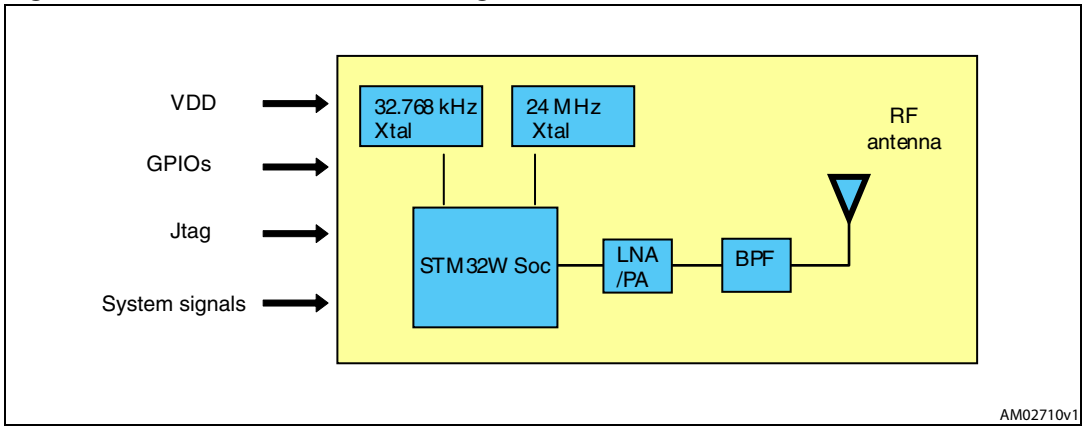
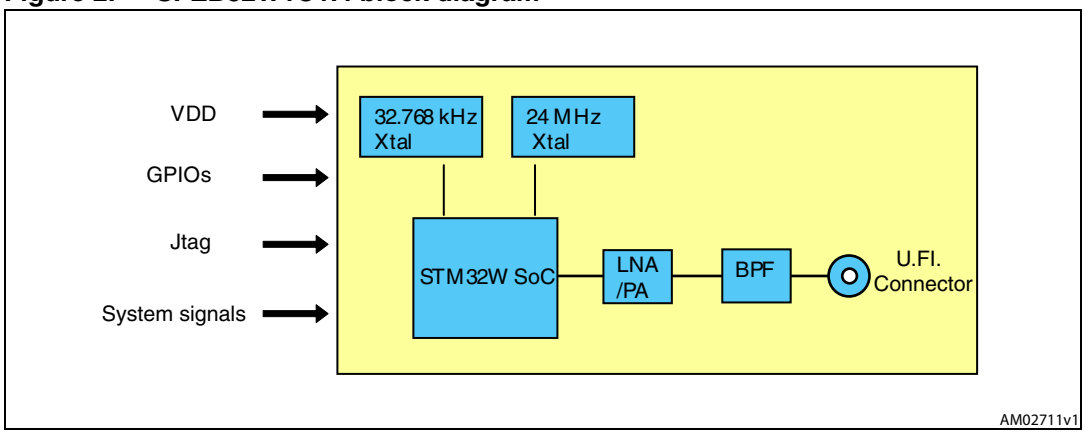


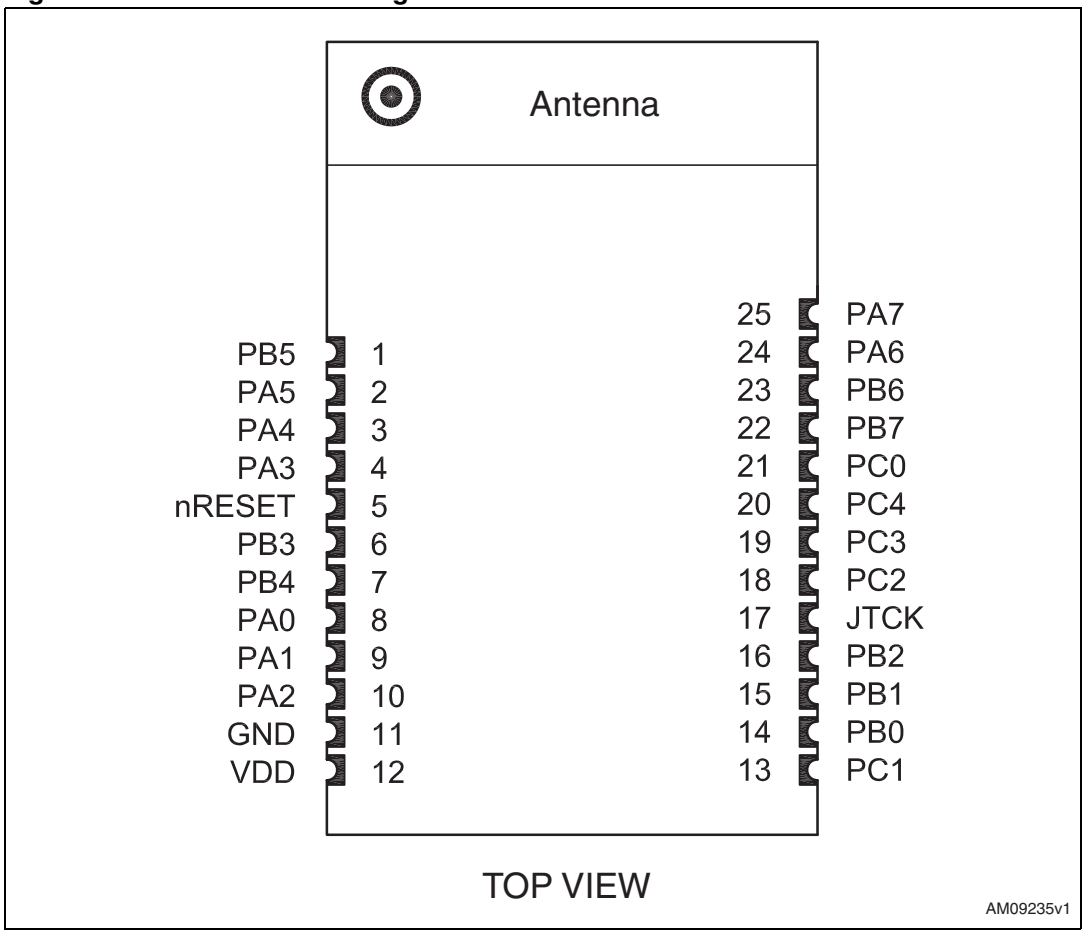
Figure 2. SPZB32W1C1.4 block diagram



5 Pin settings

5.1 Pin connections

Figure 3. Pin connection diagram



5.2 Pin description

Table 1. Pin description

Module pin n°	Pin name	Direction	STM32W pin	Description
1	PB5	I/O	43	Digital I/O
	ADC0	Analog	43	ADC input 0
	TIM2CLK	I	43	Timer 2 external clock input
	TIM1MSK	I	43	Timer 1 external clock mask input
2	PA5	I/O	27	Digital I/O
	ADC5	Analog	27	ADC input 1
	PTI_DATA	O	27	Frame signal of PTI (packet trace interface)
	nBOOTMODE	I	27	Embedded serial bootloader activation out of reset
	TRACEDATA3	0	27	Synchrounus CPU trace data bit 3
3	PA4	I/O	26	Digital I/O
	ADC4	Analog	26	ADC input 0
	PTI_EN	O	26	Frame signal of PTI (packet trace interface)
	TRACEDATA2	O	26	Synchrounus CPU trace data bit 2
4	PA3	I/O	25	Digital I/O
	SC2nSSEL	I	25	SPI SLAVE SELECT of serial controller 2
	TIM2_CH2	I/O	25	Timer 2 channel 2 output (or input - disable remap with TIM2_OR[5])
	TRACECLK	O	25	Synchrounus CPU trace clock
5	nRESET	I	12	Active low reset (an internal pull-up of 30 kohm typ. is provided)
6	PB3	I/O	19	Digital I/O
	UART_CTS	I	19	UART CTS handshake of serial controller 1
	SC1SCLK	I/O	19	SPI slave clock of serial controller SC1 / SPI master clock of serial controller SC1
	TIM2_CH3	I/O	19	Timer 2 channel 3 input / timer 2 channel 3 output
7	PB4	I/O	20	Digital I/O
	UART_RTS	O	20	UART RTS handshake of serial controller 1
	TIM2_CH4	I/O	20	Timer 2 channel 4 input / timer 2 channel 4 output
	SC1nSSEL	I	20	SPI slave select of serial controller 1
8	PA0	I/O	21	Digital I/O
	SC2MOSI	O	21	SPI master data out of serial controller 2
	SC2MOSI	I	21	SPI slave data in of serial controller 2
	TIM2_CH1	I/O	21	Timer 2 channel 1 input / timer 2 channel 1 output

Table 1. Pin description (continued)

Module pin n°	Pin name	Direction	STM32W pin	Description
9	PA1	I/O	22	Digital I/O
	SC2MISO	I	22	SPI master data in of serial controller 2
	SC2MISO	O	22	SPI slave data out of serial controller 2
	SC2SDA	I/O	22	TWI (I^2C) data of serial controller 2
	TIM2_CH3	I/O	22	Timer 2 channel 3 input / timer 2 channel 3 output
10	PA2	I/O	24	Digital I/O
	SC2SCLK	O	24	SPI master clock of serial controller 2
	SC2SCLK	I	24	SPI slave clock of serial controller 2
	SC2SCL	I/O	24	TWI (I^2C) clock of serial controller 2
	TIM2_CH4	I/O	24	Timer 2 channel 4 input / timer 2 channel 4 output
11	GND	--	49	Ground
12	VDD	Power	16,23,28, 37	Input power supply
13	PC1	I/O	38	Digital I/O
	ADC3	Analog	38	ADC Input 3
	SWO	O	38	Serial wire output synchronous trace output to debugger
	TRACEDATA0	O	38	Synchronous CPU trace data bit 0
14	PB0	I/O	36	Digital I/O
	VREF (O/I)	Analog	36	ADC reference output / ADC reference input
	TIM1CLK	I	36	Timer 1 external clock input
	TIM2MSK	I	36	Timer 2 external clock mask input
	IRQA	I	36	External interrupt source A
	TRACECLK	O	36	Synchronous CPU trace clock
15	PB1	I/O	30	Digital I/O
	SC1TXD	O	30	UART transmit data of serial controller 1
	SC1MOSI / SC1MISO	O	30	SPI master data out of serial controller 1 / SPI slave data out of serial controller 1
	SC1SDA	I/O	30	TWI (I^2C) data of serial controller 1
	TIM2_CH1	I/O	30	Timer 2 channel 1 input / timer 2 channel 1 output
16	PB2	I/O	31	Digital I/O
	SC1RXD	I	31	UART receive data of serial controller 1
	SC1MISO / SC1MOSI	I	31	SPI master data in of serial controller SC1 / SPI slave data in of serial controller 1
	SC1SCL	I/O	31	TWI (I^2C) clock of serial controller 1
	TIM2_CH2	I/O	31	Timer 2 channel 2 input / timer 2 channel 2 output

Table 1. Pin description (continued)

Module pin n°	Pin name	Direction	STM32W pin	Description
17	JTCK	I	32	JTAG clock input from debugger
	SWCLK	I/O	32	Serial wire clock input/output with debugger
18	PC2	I/O	33	Digital I/O
	JTDO	O	33	JTAG data out to debugger
	SWO	O	33	Serial wire output asynchronous trace output to debugger
19	PC3	I/O	34	Digital I/O
	JTDI	I	34	JTAG data in from debugger
20	PC4	I/O	35	Digital I/O
	JTMS	I	35	JTAG mode select from debugger
	SWDIO	I/O	35	Serial wire bidirectional data to/from debugger
21	PC0	I/O	40	Digital I/O (high current)
	JRST	I	40	JTAG reset input from debugger
	TRACEDATA1	O	40	Synchronous CPU trace data bit 1
	IRQD	I	40	External interrupt source D
22	PB7	I/O	41	Digital I/O
	TIM1_CH2	O	41	Timer 1 channel 2 output
	TIM1 _CH2	I	41	Timer 1 channel 2 input
	IRQC	I	41	External interrupt source C
	ADC2	I	41	ADC input 2
23	PB6	I/O	42	Digital I/O
	TIM1_CH1	O	42	Timer 1 channel 1 output
	TIM1_CH1	I	42	Timer 1 channel 1 input
	IRQB	I	42	External interrupt source B
	ADC1	Analog	42	ADC input 1
24	LNA/ENABLE	I	29	Digital input, module firmware dependent, externally forced by the user dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L internal LNA. (HIGH= internal LNA enabled, LOW= internal LNA disabled).
	PA6/LNA_ENABLE	O	29	Digital output, module firmware dependent, internally forced by application dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L internal LNA. (HIGH= internal LNA enabled, LOW= internal LNA disabled).

Table 1. Pin description (continued)

Module pin n°	Pin name	Direction	STM32W pin	Description
25	RF_STANDBY	I	18	Digital input, module firmware dependent, externally forced by the user dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L front-end STANDBY state. (HIGH= front-end enabled, LOW= front-end forced into STANDBY state).
	PA7/RF_STANDBY	O	18	Digital output, module firmware dependent, internally forced by application dedicated firmware. This signal is dedicated to manage the SIGE-SE2432L front-end STANDBY state. (HIGH= front-end enabled, LOW= front-end forced into STANDBY state).

6 Electrical characteristics

6.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
VDD	Module supply voltage	- 0.3	3.6	V
V_{in}	Input voltage on any digital pin	- 0.3	VDD + 0.3	V
T_{stg}	Storage temperature	-40	+85	°C
T_{sold}	Soldering temperature < 10s		250	°C

6.2 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Module supply voltage	-40 °C < T < +85 °C	2.1	3.3	3.6	V
T_{stg}	Operating ambient temperature		-40		+85	°C

6.3 DC electrical characteristics

Table 4. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IRX	RX current	VDD = 3.3 V, T= 25 °C	-	20	-	mA
ITX	TX current	Po = 18 dBm, VDD = 3.3 V, T = 25 °C, F= 2450 MHz	-	120	-	mA
IDS	Deep sleep current (32.768 kHz oscillator)	VDD = 3.3 V, T = 25 °C	-	1.3	-	mA

6.4 Digital I/O specifications

Table 5. Digital I/O specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	2.1 < VDD < 3.6 V	0		0.5 x VDD	V
V_{IH}	High level input voltage	2.1 < VDD < 3.6 V	0.62 x VDD		VDD	V
I_{il}	Input current for logic 0	2.1 < VDD < 3.6 V			-0.5	mA
I_{ih}	Input current for logic 1	2.1 < VDD < 3.6 V			0.5	mA
R_{ipu}	Input pull-up resistor			30		kΩ
R_{ipd}	Input pull-down resistor			30		kΩ
V_{OL}	Low level output voltage		0		0.18 x VDD	V
V_{OH}	High level output voltage		0.82 x VDD		VDD	V
I_{OHS}	Output source current (standard)				4	mA
I_{OLS}	Output sink current (standard)				4	mA
I_{OHH}	Output source current (high current)				8	mA
I_{OLH}	Output sink current (high current)				8	mA
I_{OTot}	Total output current for I/O				40	mA

6.5 RF electrical characteristics

Table 6. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
	Frequency range	VDD = 3.3 V, T= 25 °C	2405		2480	MHz
TX	Output power	VDD = 3.3 V, T= 25 °C			20	dBm
RX	Sensitivity	VDD = 3.3 V, 1% PER			-105	dBm
	Adjacent channel rejection	±5 MHz ±10 MHZ		35 40		dBm

7 Mechanical dimensions

Figure 4. Mechanical dimensions

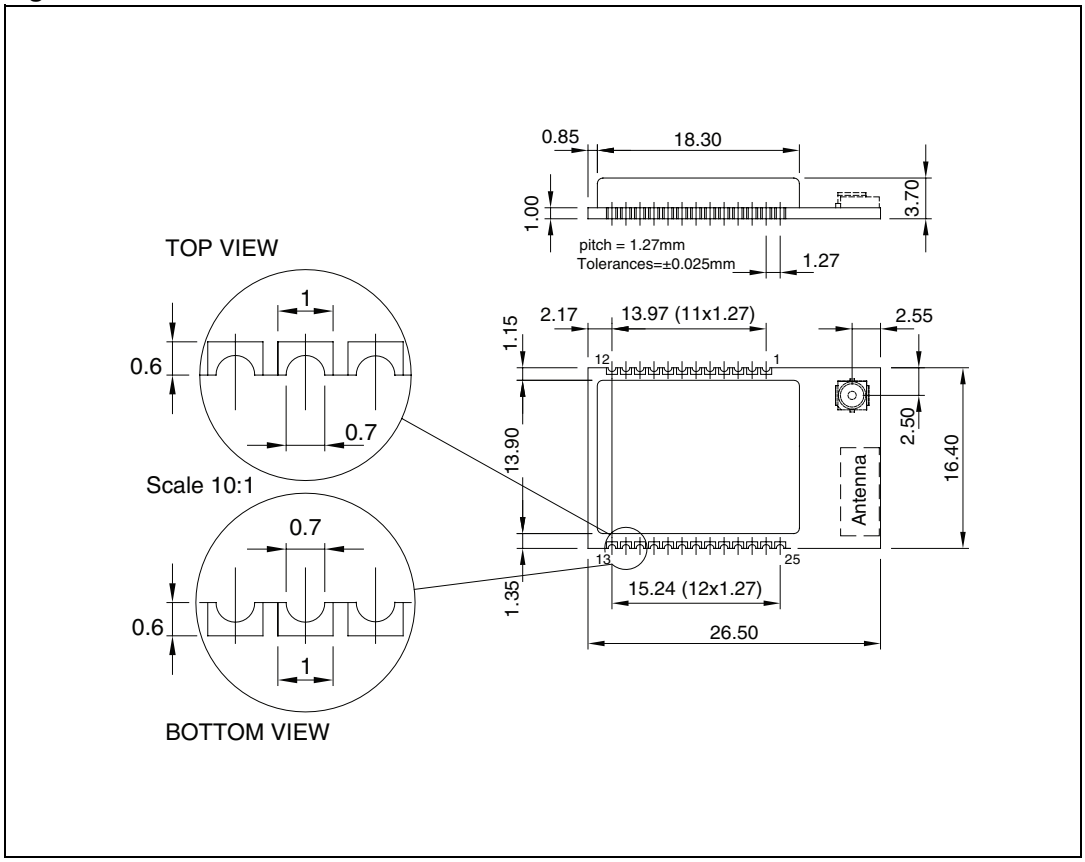
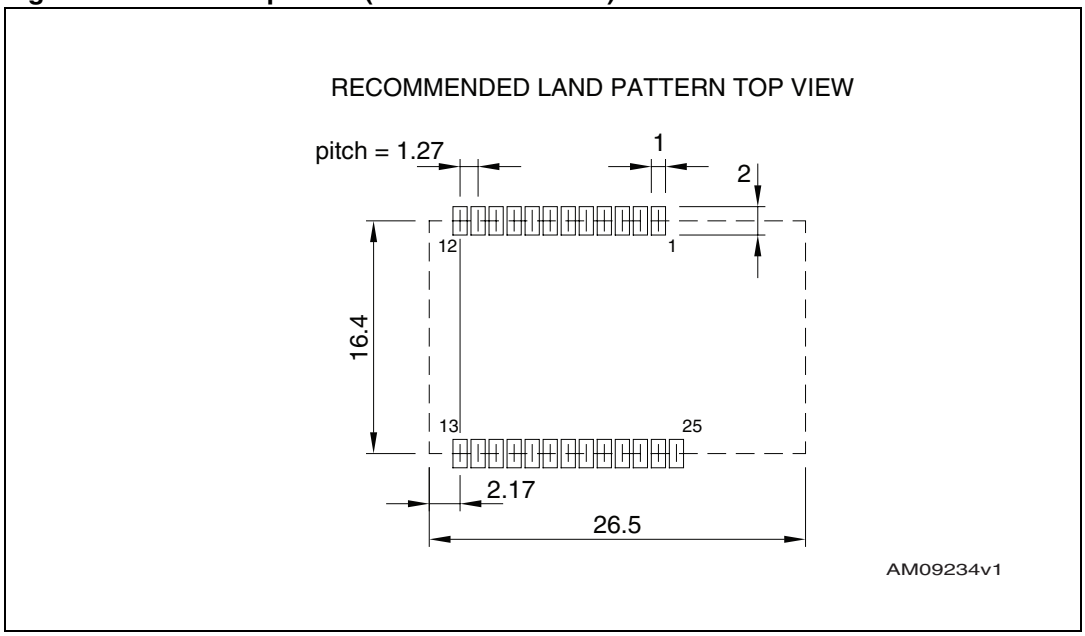


Figure 5. Pin land pattern (dimensions in mm)



8 Soldering

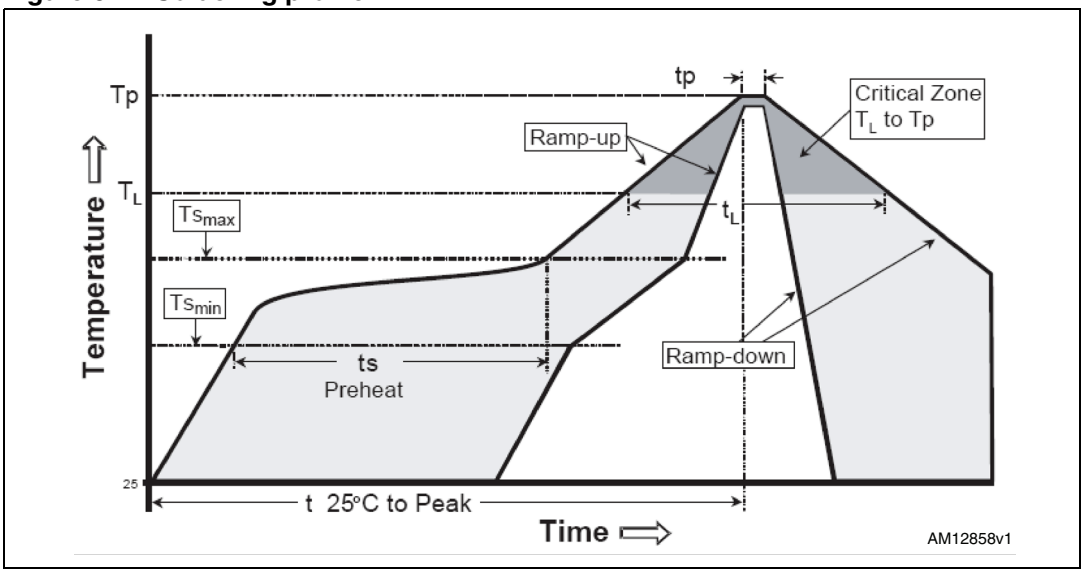
The soldering phase must be carefully executed; in order to avoid undesired melting phenomenon, particular attention must be paid to the set-up of the peak temperature.

Below are some suggestions for the temperature profile based on IPC/JEDEC J-STD-020C, July 2004 recommendations.

Table 7. Soldering

Profile feature	PB free assembly
Average ramp-up rate (T_{SMAX} to T_P)	3 °C / sec max.
Preheat Temperature min. ($T_{S\ MIN}$) Temperature max. ($T_{S\ MAX}$) Time ($T_{S\ MIN}$ to $T_{S\ MAX}$) (t_S)	 150 °C 200 °C 60 – 100 sec
Time maintained above: Temperature T_L Time t_L	 217 °C 40 – 70 sec
Peak temperature (T_p)	240 + 0 °C
Time within 5 °C of actual peak temperature (t_P)	10 – 20 sec
Ramp-down rate	6 °C / sec
Time from 25 °C to peak temperature	8 minutes max.

Figure 6. Soldering profile



9 Product approval

These modules have been designed to meet national regulations for world wide use. They are mechanically and electrically equivalent to the modules SPZB32W1A1.1[a] and SPZB32W1C1.1[a], differing only in terms of the SW that they are enabled to run. This fact is explicated with the last digit of the device part number. CE and FCC certifications have been obtained for SPZB32W1A1.1 and SPZB32W1C1.1 as models representative of the complete series SPZB32Wxyz1.t of 802.15.4/Zigbee RF modules. Each representative of the series does not degrade the characteristics granted by the certification organisms on the indicated model used during the certification process.

9.1 FCC approval

The SPZB32W1A1.1 device, with integrated antenna, as well as the SPZB32W1C1.1, with the antenna specified in *Table 8*, have been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference does not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

Consult the dealer or an experienced radio/TV technician for help.

Module type: ZigBee® module *SPZB32W1A1.1 / SPZB32W1C1.1*

FCC-ID: S9NZB32C1

Modular type: single modular

Table 8. Antenna used for FCC approvals

ITEM	Part N°	Manufacturer
1	2010B4844-01 (Titanis Antenna)	Antenova

Any changes or modifications not expressly approved by the part responsible for compliance may cause the module to cease to comply with FCC rules part 15, and therefore void the user's authority to operate the equipment.

a. Device used for testing only and is not available for purchase.

While the user of a device into which the SPZB32W1A1.1 or the SPZB32W1C2.1, with the antenna specified in *Table 8*, is installed, they are not required to obtain new authorization for the module, this does not preclude the possibility that some other form of authorization or testing may be required for the end product.

9.1.1 FCC labeling requirements

When integrating the *SPZB32W1A1.1 / SPZB32W1C1.1* into the final product, it must be ensured that the FCC labelling requirements, as specified below, are satisfied.

Based on the public notice from FCC, the product into which the transmitter module is installed must display a label referring to the enclosed module.

The label should use wording such as “Contains Transmitter module FCC ID: S9NZB32C1 or “Contains FCC ID: S9NZB32C1”, any similar wording that expresses the same meaning may be used.

For example:

Contains FCC ID: S9NZB32C1

9.2 European certification

SPZB32W1A1.1 and SPZB32W1C2.1 devices are CE certified:

CE 0051

Expert opinion N. 0420-ARAL00045 released by IMQ refers to the following normative:

Art. 3.1a Health : EN 62311 : 2008

Art .3.1a Safety : EN 60950-1:2006 + A11:2009 + A1:2010

Art. 3.1b EMC: EN 301 489-1 V.1.8.1:2008 / EN 301 489- 17 V 2.1.1:2009

Art.3.2 Radio Spectrum: EN 300 328: V1.7.1:2006

10 Ordering information scheme

Table 9. Ordering information scheme

SPZB 32Wx y 1 .z

802.15.4 / ZigBee modules

Memory options:

1: 128 kB Flash; 8 kB RAM

Antenna options:

x --> A: Integrated ceramic antenna

x --> C: Integrated UFL connector

1: Long TX range

Firmware options:

4: SimpleMAC

Note: Check availability of the different versions with your ST sales representative.

11 Revision history

Table 10. Document revision history

Date	Revision	Changes
07-May-2012	1	Initial release.

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