

## 40V 4A DOUBLE POWER HALF BRIDGE

### 1 FEATURES

- MULTIPOWER BCD TECHNOLOGY
- MINIMUM INPUT OUTPUT PULSE WIDTH DISTORTION
- 200mΩ  $R_{dsON}$  COMPLEMENTARY DMOS OUTPUT STAGE
- CMOS COMPATIBLE LOGIC INPUTS
- THERMAL PROTECTION
- THERMAL WARNING OUTPUT
- UNDER VOLTAGE PROTECTION

### 2 DESCRIPTION

STA502 is a monolithic dual half bridge stage in Multipower BCD Technology.

Figure 1. Package



Table 1. Order Codes

Part Number	Package
STA502	PowerSO36 (Slug Up)

The device is particularly designed to make the output stage of a mono All-Digital High Efficiency (DDX™) amplifier capable to deliver 60W @ THD = 10% at  $V_{CC}$  32V output power on 8Ω load. The input pins have threshold proportional to  $V_L$  pin voltage.

Figure 2. Block Diagram

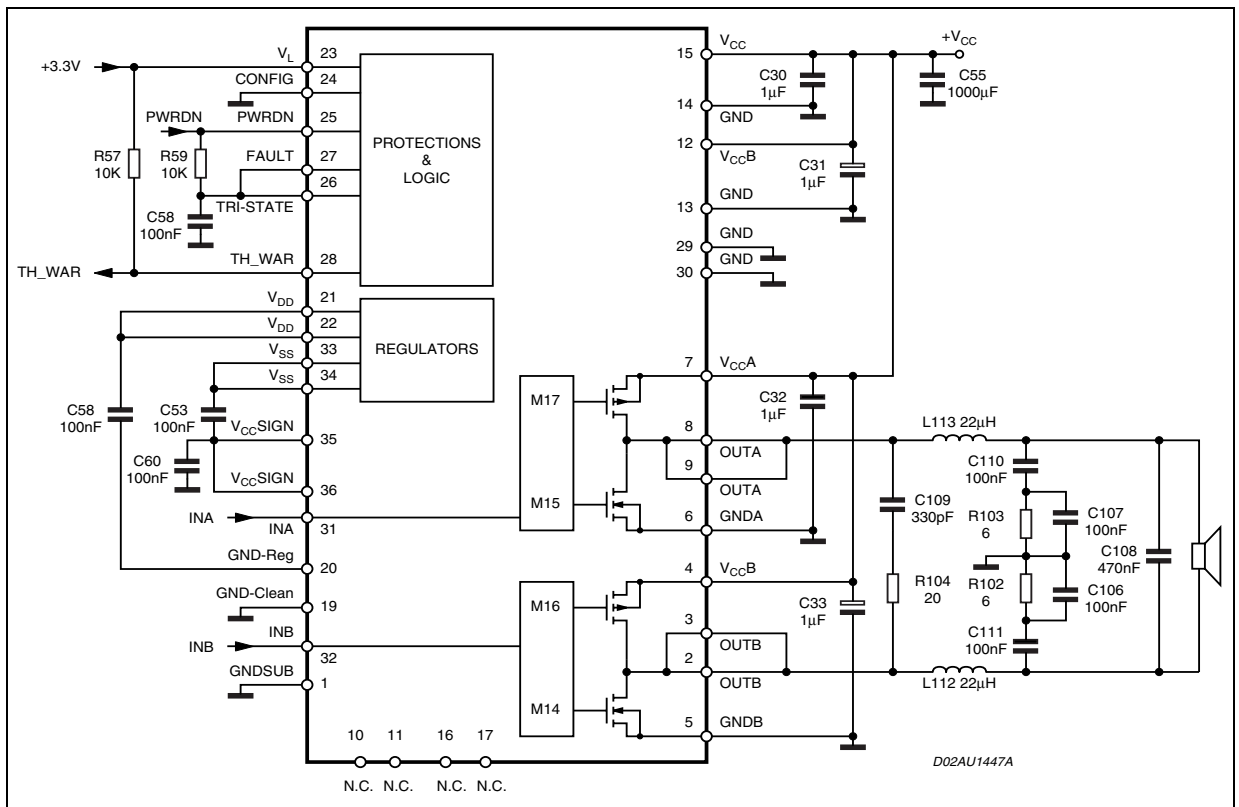


Table 2. Pin Description

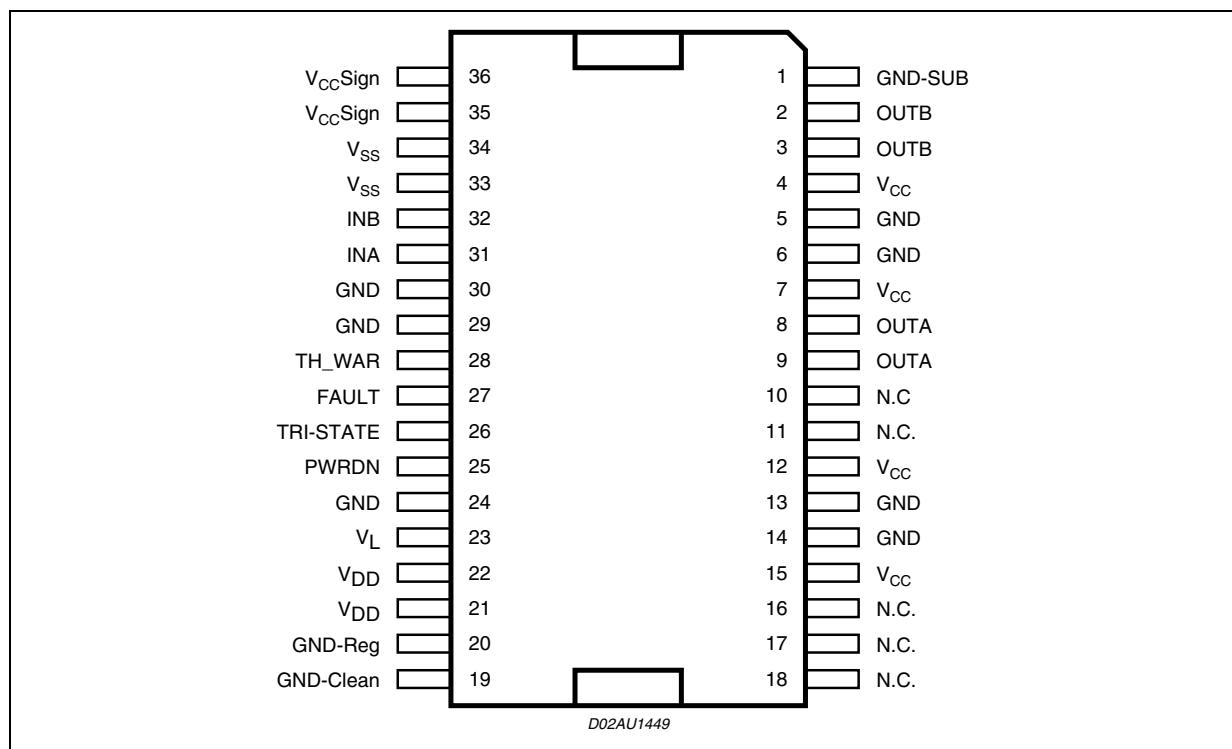
N°	Pin	Description
1	GND-SUB	Substrate ground
2 ; 3	OUTB	Output half bridge
4	V <sub>CC</sub>	Positive Supply
5	GND	Negative Supply
6	GND	Negative Supply
7	V <sub>CC</sub>	Positive Supply
8 ; 9	OUTA	Output half bridge
10 ; 11	N.C.	
12	V <sub>CC</sub>	Positive Supply
13	GND	Negative Supply
14	GND	Negative Supply
15	V <sub>CC</sub>	Positive Supply
16 ; 17	N.C.	
18	NC	Not connected
19	GND-Clean	Logical ground
20	GND-Reg	Ground for regulator V <sub>dd</sub>
21 ; 22	V <sub>dd</sub>	5V Regulator referred to ground
23	V <sub>L</sub>	High logical state setting voltage
24	GND	
25	PWRDN	Stand-by pin
26	TRI-STATE	Hi-Z pin
27	FAULT	Fault pin advisor
28	TH-WAR	Thermal warning advisor
29	GND	
30	GND	
31	INA	Input of half bridge
32	INB	Input of half bridge
33 ; 34	V <sub>SS</sub>	5V Regulator referred to + V <sub>CC</sub>
35 ; 36	V <sub>CC</sub> Sign	Signal Positive supply

**Table 3. FUNCTIONAL PIN STATUS**

PIN NAME	Logical value	IC -STATUS
FAULT	0	Fault detected (Short circuit, or Thermal ..)
FAULT *	1	Normal Operation
TRI-STATE	0	All powers in Hi-Z state
TRI-STATE	1	Normal operation
PWRDN	0	Low absorption
PWRDN	1	Normal operation
THWAR	0	Temperature of the IC =130°C
THWAR*	1	Normal operation

\* : The pin is open collector. To have the high logic value, it needs to be pulled up by a resistor.

**Figure 3. PIN CONNECTION**



**Table 4. ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Pin 4,7,12,15)	40	V
V <sub>max</sub>	Maximum Voltage on pins 23 to 32	5.5	V
P <sub>tot</sub>	Power Dissipation (T <sub>case</sub> = 70°C)	50	W
T <sub>op</sub>	Operating Temperature Range	0 to 70	°C
T <sub>stg</sub> , T <sub>j</sub>	Storage and Junction Temperature	-40 to 150	°C

**Table 5. THERMAL DATA**

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>j-case</sub>	Thermal Resistance Junction to Case (thermal pad)			2.5	°C/W
T <sub>jSD</sub>	Thermal shut-down junction temperature		150		°C
T <sub>warn</sub>	Thermal warning temperature		130		°C
t <sub>hSD</sub>	Thermal shut-down hysteresis		25		°C

**Table 6. Electrical Characteristics** (V<sub>L</sub> = 3.3V; V<sub>CC</sub> = 30V; T<sub>amb</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
R <sub>dsON</sub>	Power Pchannel/Nchannel MOSFET RdsON	I <sub>d</sub> =1A;		200	270	mΩ
I <sub>dss</sub>	Power Pchannel/Nchannel leakage I <sub>dss</sub>	V <sub>CC</sub> =35V;			50	μA
g <sub>N</sub>	Power Pchannel RdsON Matching	I <sub>d</sub> =1A;	95			%
g <sub>P</sub>	Power Nchannel RdsON Matching	I <sub>d</sub> =1A;	95			%
Dt <sub>s</sub>	Low current Dead Time (static)	see test circuit no.1; see fig. 14		10	20	ns
Dt <sub>d</sub>	High current Dead Time (dynamic)	L=22μH; C = 470nF; R <sub>l</sub> = 8 Ω I <sub>d</sub> =3.5A; see fig. 3			50	ns
t <sub>d ON</sub>	Turn-on delay time	Resistive load			100	ns
t <sub>d OFF</sub>	Turn-off delay time	Resistive load			100	ns
t <sub>r</sub>	Rise time	Resistive load; as fig.14			25	ns
t <sub>f</sub>	Fall time	Resistive load; as fig. 4			25	ns
V <sub>CC</sub>	Supply voltage operating voltage		10		36	V
V <sub>IN-High</sub>	High level input voltage				V <sub>L</sub> /2 +300mV	V
V <sub>IN-Low</sub>	Low level input voltage		V <sub>L</sub> /2 - 300mV			V
I <sub>IN-H</sub>	High level Input current	Pin voltage = V <sub>L</sub>		1		μA

**Table 6. Electrical Characteristics** (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{IN-L}$	Low level input current	Pin voltage = 0.3V		1		$\mu A$
$I_{PWRDN-H}$	High level PWRDN pin input current	$V_L = 3.3V$		35		$\mu A$
$V_{Low}$	Low logical state voltage $V_{Low}$ (pin PWRDN, TRISTATE) (note 1)	$V_L = 3.3V$	0.8			V
$V_{High}$	High logical state voltage $V_{High}$ (pin PWRDN, TRISTATE) (note 1)	$V_L = 3.3V$			1.7	V
$I_{VCC-PWRDN}$	Supply current from $V_{cc}$ in Power Down	PWRDN = 0			3	mA
$I_{FAULT}$	Output Current pins FAULT -TH-WARN when FAULT CONDITIONS	$V_{pin} = 3.3V$		1		mA
$I_{VCC-hiz}$	Supply current from $V_{cc}$ in Tri-state	Tri-state=0;		22		mA
$I_{VCC}$	Supply current from $V_{cc}$ in operation (both channel switching)	Input pulse width = 50% Duty; Switching Frequency = 384KHz; No LC filters;		50		mA
$I_{out-sh}$	Isc (short circuit current limit)		4	6	8	A
$V_{UV}$	Undervoltage protection threshold			7		V
$t_{pw-min}$	Output minimum pulse width	No Load	70		150	ns

**Table 7.**

$V_L$	$V_{Low\ min}$	$V_{High\ max}$	Unit
2.7	0.7	1.5	V
3.3	0.8	1.7	V
5	0.85	1.85	V

Notes: 1. The following table explains the  $V_{Low}$ ,  $V_{High}$  variation with  $V_L$

**Table 8. Logic Truth** (see fig. 5)

TRI-STATE	INA	INB	Q1	Q2	Q3	Q4	OUTPUT MODE
0	x	x	OFF	OFF	OFF	OFF	Hi-Z
1	0	0	OFF	OFF	ON	ON	DUMP
1	0	1	OFF	ON	ON	OFF	NEGATIVE
1	1	0	ON	OFF	OFF	ON	POSITIVE
1	1	1	ON	ON	OFF	OFF	Not used

Figure 4. Test Circuit.

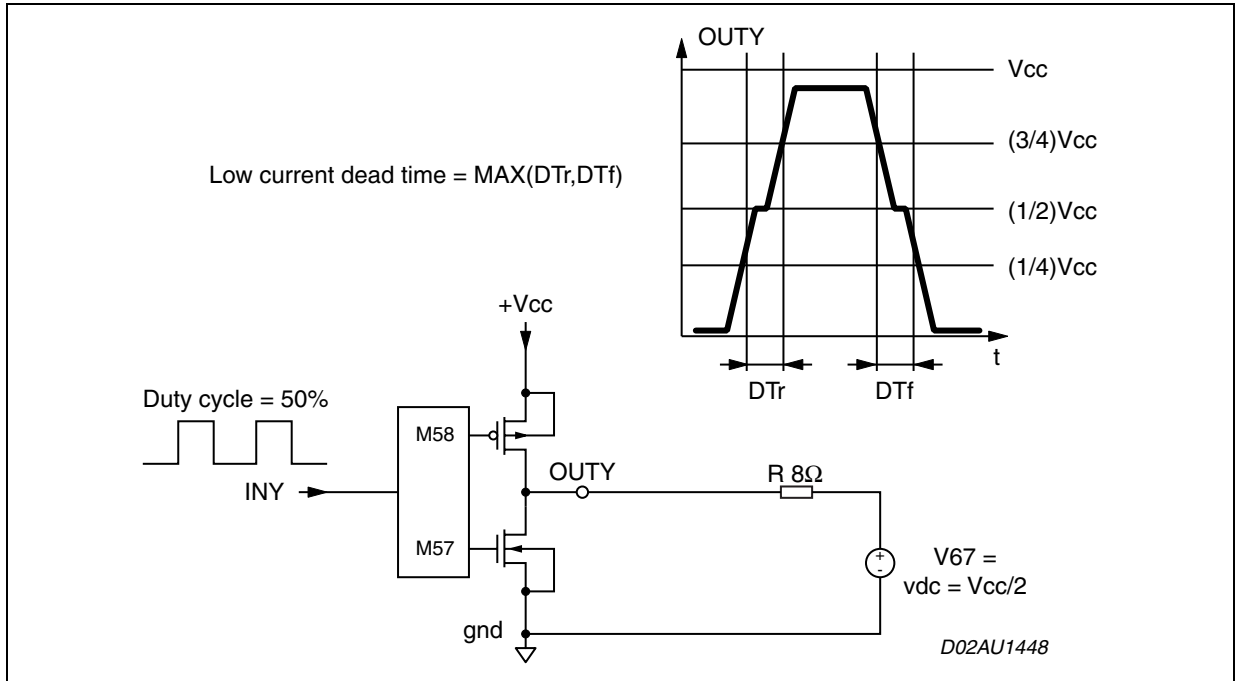


Figure 5.

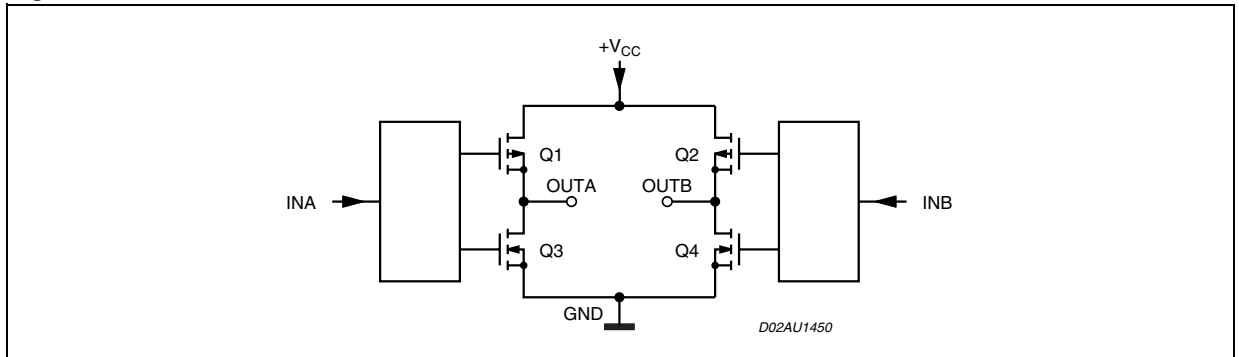


Figure 6.

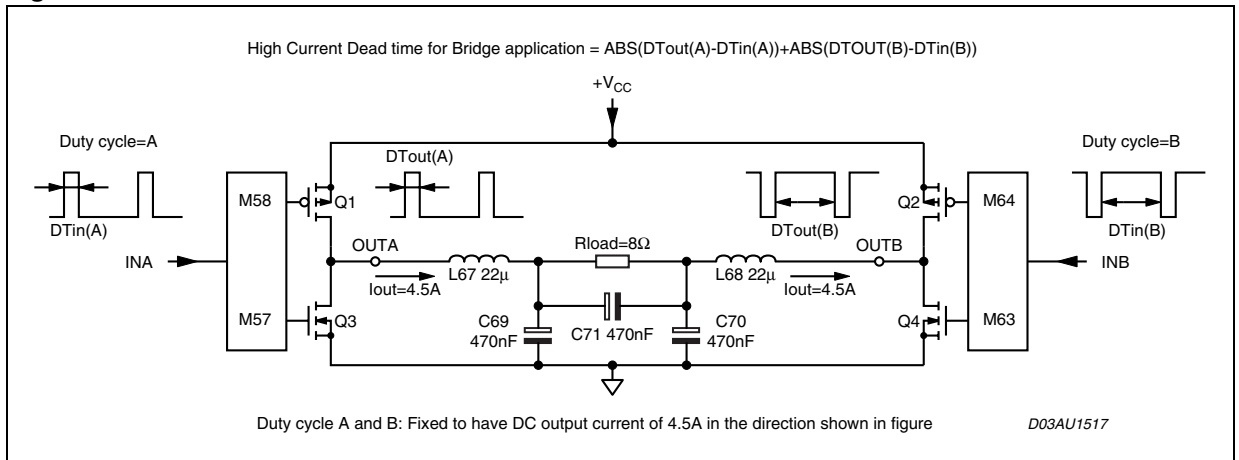
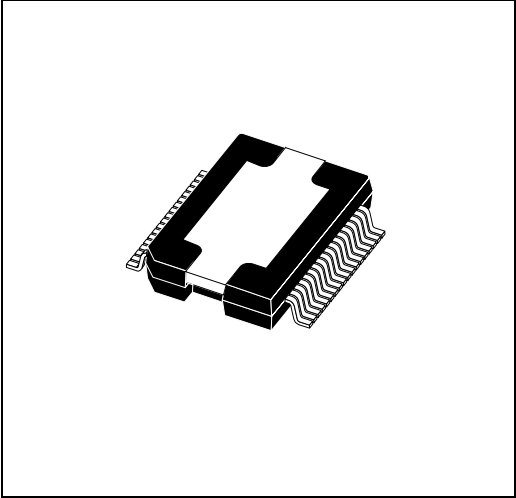


Figure 7. Power SO36 (SLUG UP) Mechanical Data & Package Dimensions

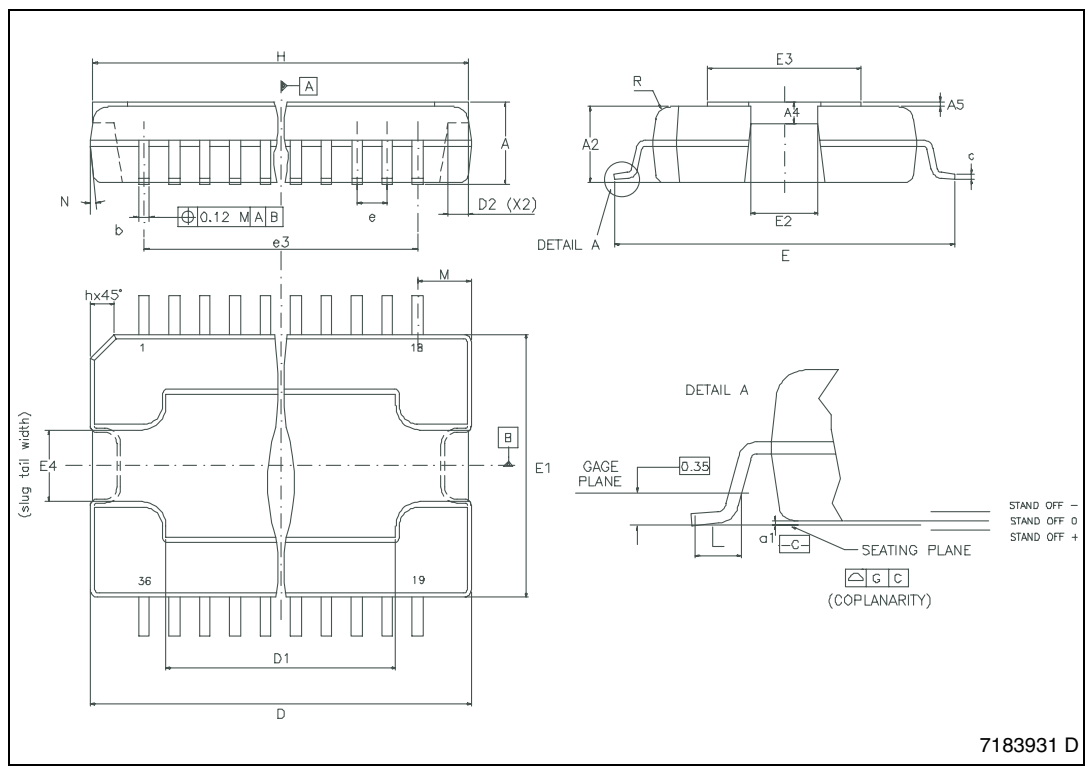
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.25		3.43	0.128		0.135
A2	3.1		3.2	0.122		0.126
A4	0.8		1	0.031		0.039
A5		0.2			0.008	
a1	0.030		-0.040	0.0011		-0.0015
b	0.22		0.38	0.008		0.015
c	0.23		0.32	0.009		0.012
D	15.8		16	0.622		0.630
D1	9.4		9.8	0.37		0.38
D2		1			0.039	
E	13.9		14.5	0.547		0.57
E1	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
E4	2.9		3.2	0.114		1.259
e		0.65			0.026	
e3		11.05			0.435	
G	0		0.075	0		0.003
H	15.5		15.9	0.61		0.625
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N			10°			10°
s			8°			8°

**OUTLINE AND MECHANICAL DATA**



**PowerSO36 (SLUG UP)**

- (1) "D and E1" do not include mold flash or protusions.  
Mold flash or protusions shall not exceed 0.15mm (0.006")
- (2) No intrusion allowed inwards the leads.



**Table 9. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
May 2004	1	First Issue
November 2004	2	Modificated the fig2; changed lbias pin to V <sub>L</sub> pin.



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