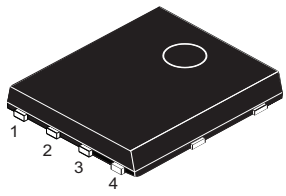
STL130N8F7

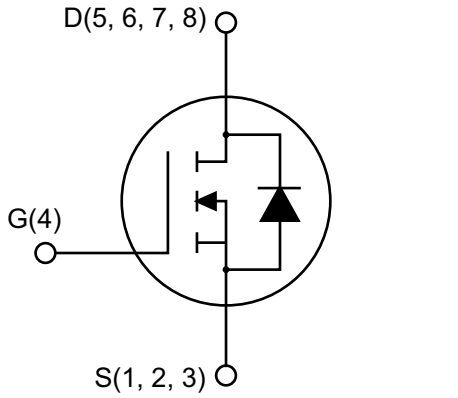
N-channel 80 V, 3 mΩ, 130 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



PowerFLAT™ 5x6

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D	P_{TOT}
STL130N8F7	80 V	3.6 mΩ (V_{GS}=10 V)	130 A	135 W

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL130N8F7	130N8F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	± 20	
I_D(1)	Drain current (continuous) at T_C = 25 °C	130	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	93	
I_D(2)	Drain current (continuous) at T_{pcb} = 25 °C	26	
I_D(2)	Drain current (continuous) at T_{pcb} = 100 °C	19	
I_{DM}(1)(3)	Drain current (pulsed)	560	
I_{DM}(2)(3)	Drain current (pulsed)	104	
P_{TOT}(1)	Total dissipation at T_C = 25 °C	135	W
P_{TOT}(2)	Total dissipation at T_{pcb} = 25 °C	4.8	W
E_{AS}(4)	Single pulse avalanche energy	515	mJ
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. This value is rated according to $R_{thj\text{-}c}$.
2. This value is rated according to $R_{thj\text{-}pcb}$.
3. Pulse width is limited by safe operating area.
4. Starting T_J=25°C, I_D=18.5 A, V_{DD}=50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	31.3	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.1	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_J = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS}= 0, I_D = 250 µA	80			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0, V_{DS} = 80 V			1	µA
		V_{GS} = 0, V_{DS} = 80 V, T_J = 125 °C			10	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS}= 10 V, I_D= 13 A		3	3.6	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
C_{iss}	Input capacitance	V_{GS}=0, V_{DS} = 40 V, f=1 MHz	-	6340	-	pF
C_{oss}	Output capacitance		-	1195	-	pF
C_{rss}	Reverse transfer capacitance		-	105	-	pF
Q_g	Total gate charge	V_{DD}=40 V, I_D = 26 A V_{GS} =10 V	-	96	-	nC
Q_{gs}	Gate-source charge		-	29	-	nC
Q_{gd}	Gate-drain charge		-	26	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD}=40 V, I_D= 13 A, R_G=4.7 Ω, V_{GS}=10 V	-	26	-	ns
t_r	Rise time		-	51	-	ns
$t_{d(off)}$	Turn-off delay time		-	82	-	ns
t_f	Fall time		-	44	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
I_{SD}	Source-drain current		-		26	A
I_{SDM}(1)	Source-drain current (pulsed)		-		104	
V_{SD}(2)	Forward on voltage	V_{GS}=0, I_{SD} = 26 A	-		1.2	V
t_{rr}	Reverse recovery time	I_{SD} = 26 A, di/dt = 100 A/µs, V_{DD}=60 V, T_J 150 °C	-	58		ns
Q_{rr}	Reverse recovery charge		-	92		nC
I_{RRM}	Reverse recovery current		-	3.2		A

1. Pulse width is limited by safe operating area.
2. Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

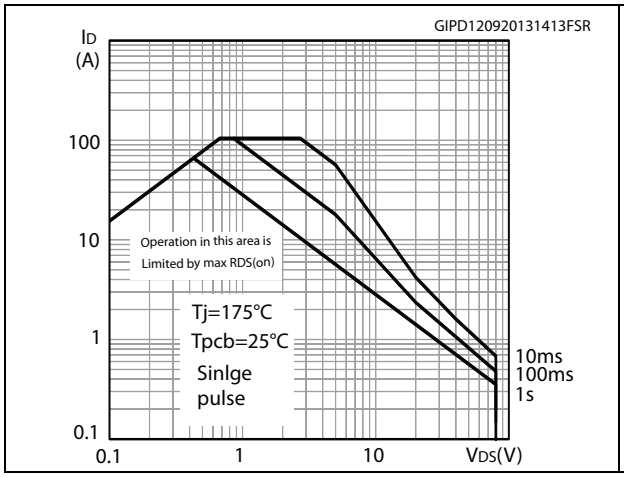


Figure 3. Thermal impedance

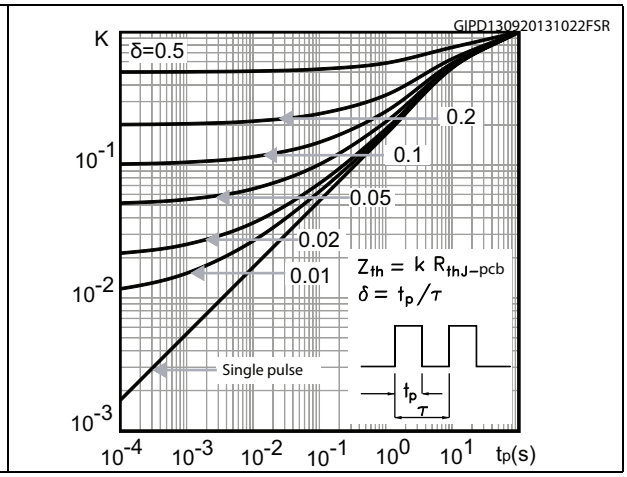


Figure 4. Output characteristics

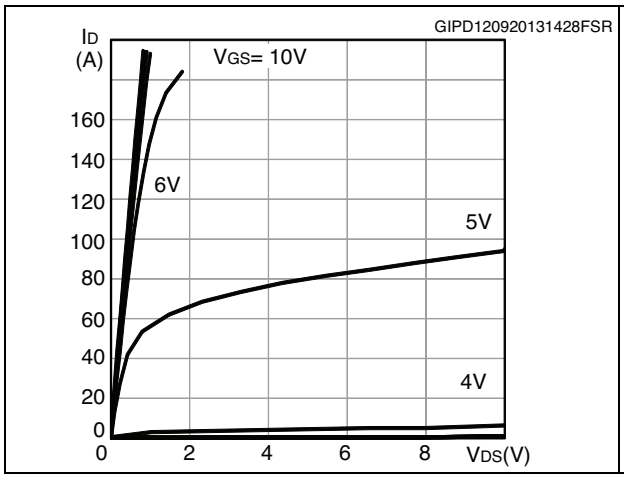


Figure 5. Transfer characteristics

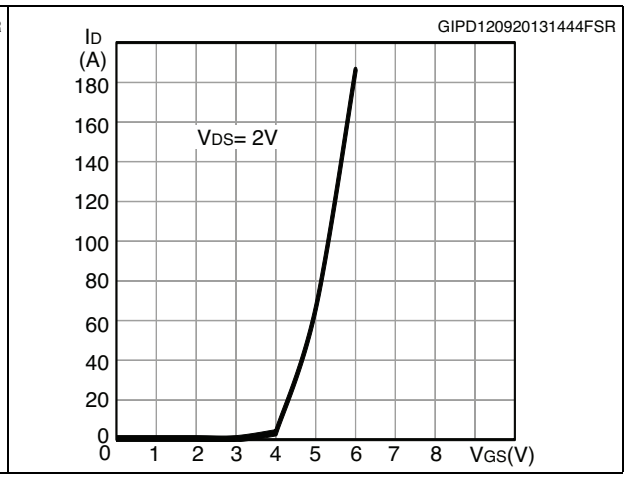


Figure 6. Gate charge vs gate-source voltage

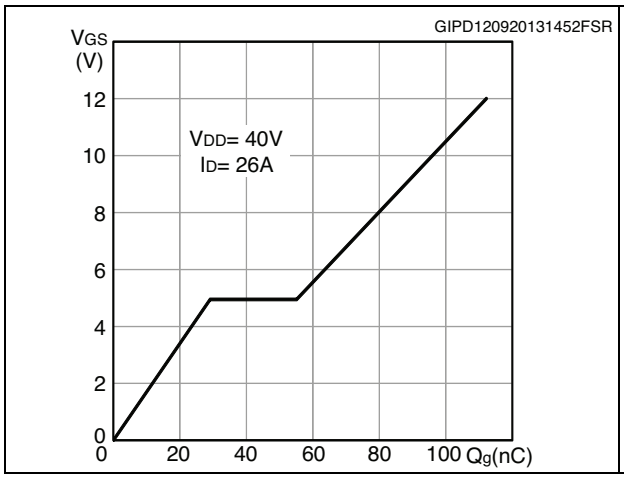


Figure 7. Static drain-source on-resistance

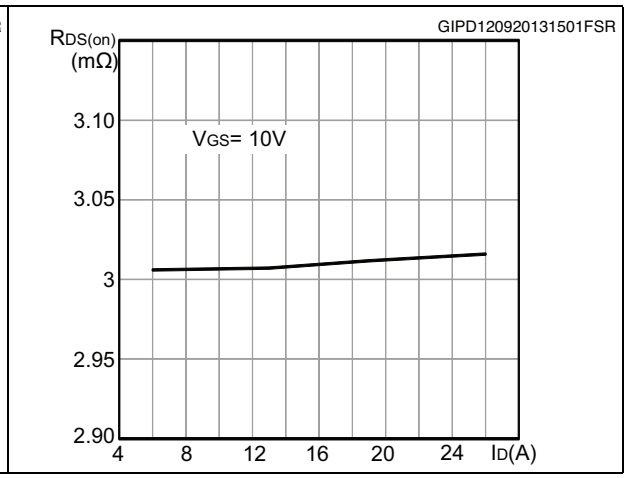


Figure 8. Capacitance variations

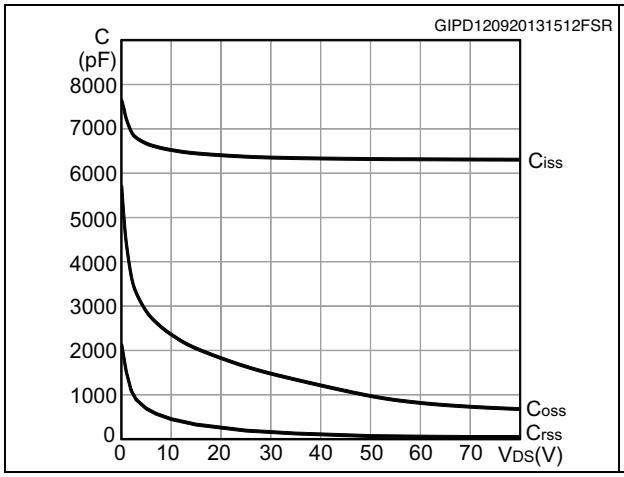


Figure 9. Normalized $V_{(BR)DSS}$ vs temperature

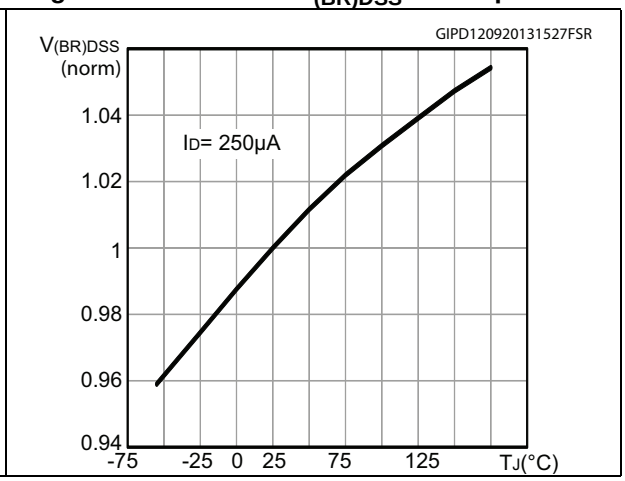


Figure 10. Normalized gate threshold voltage vs temperature

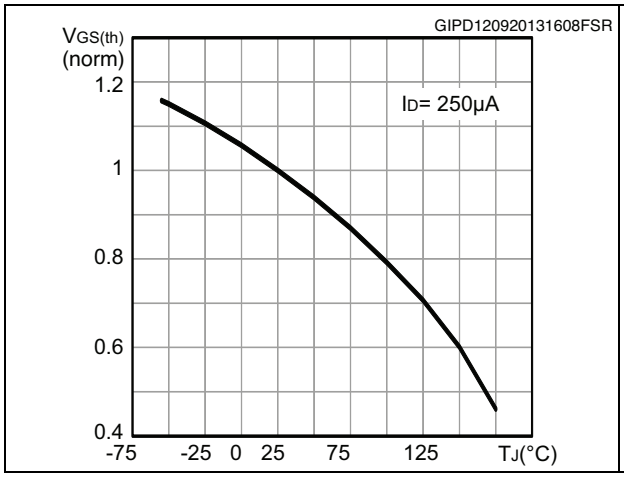


Figure 11. Normalized on-resistance vs temperature

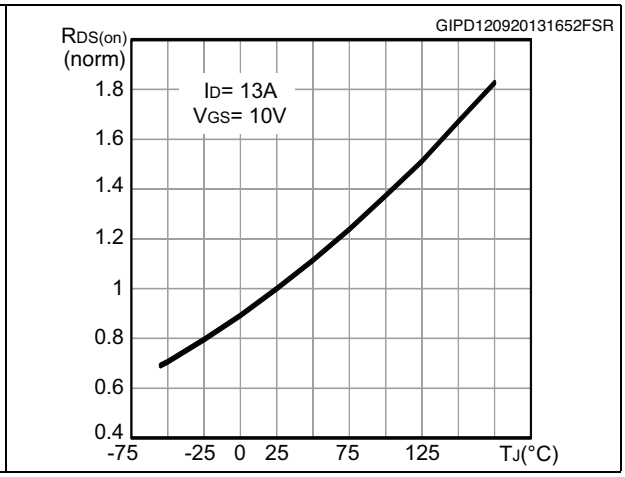
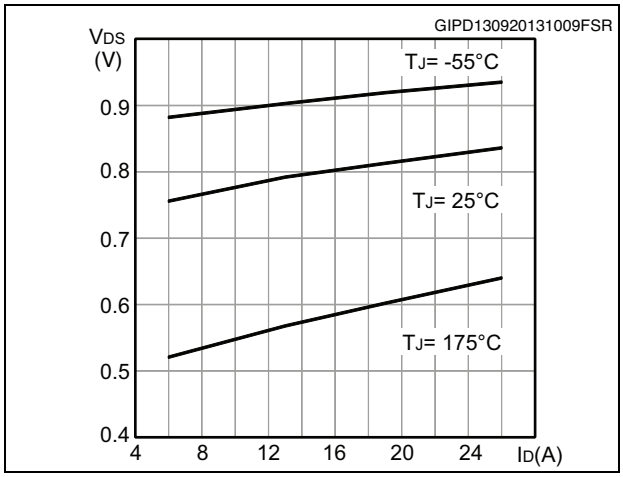


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

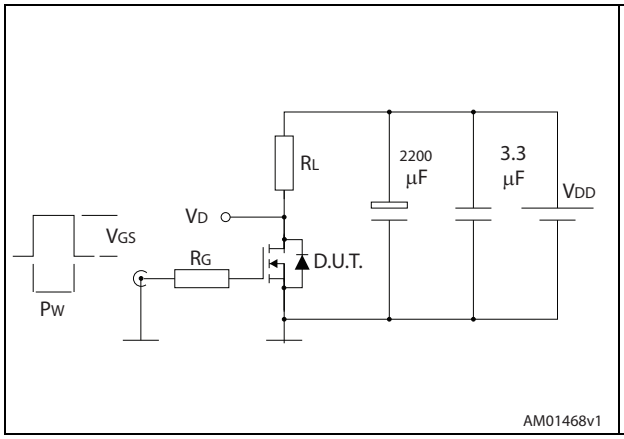


Figure 14. Gate charge test circuit

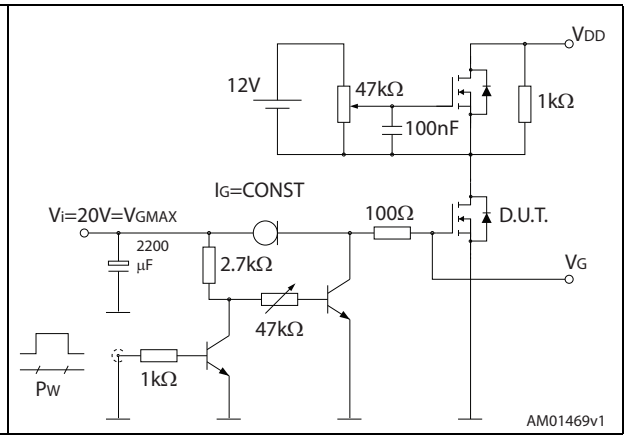


Figure 15. Test circuit for inductive load switching and diode recovery times

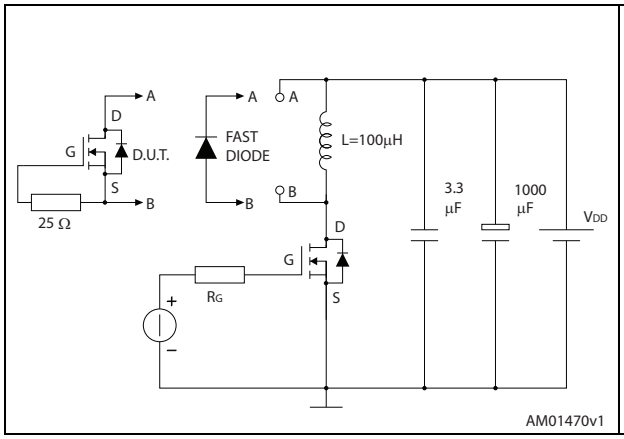


Figure 16. Unclamped inductive load test circuit

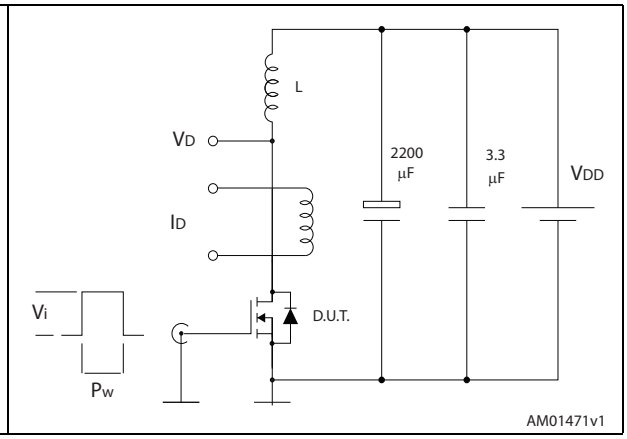


Figure 17. Unclamped inductive waveform

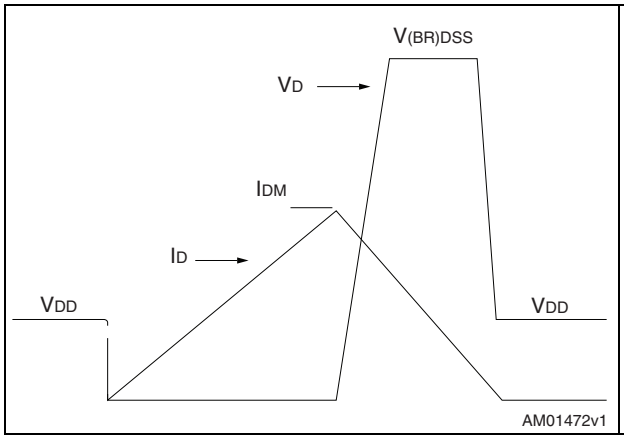
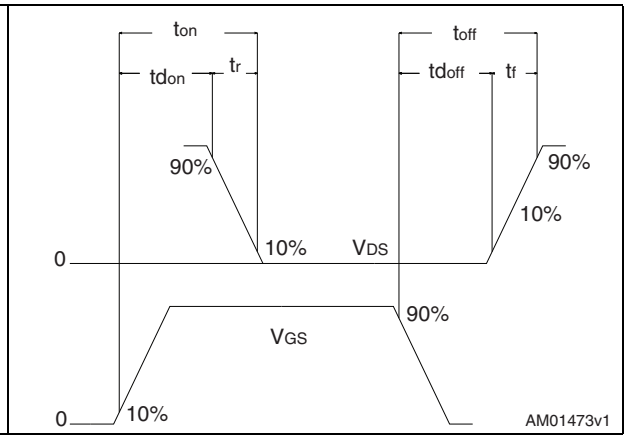


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 19. PowerFLAT™ 5x6 type S-C mechanical data

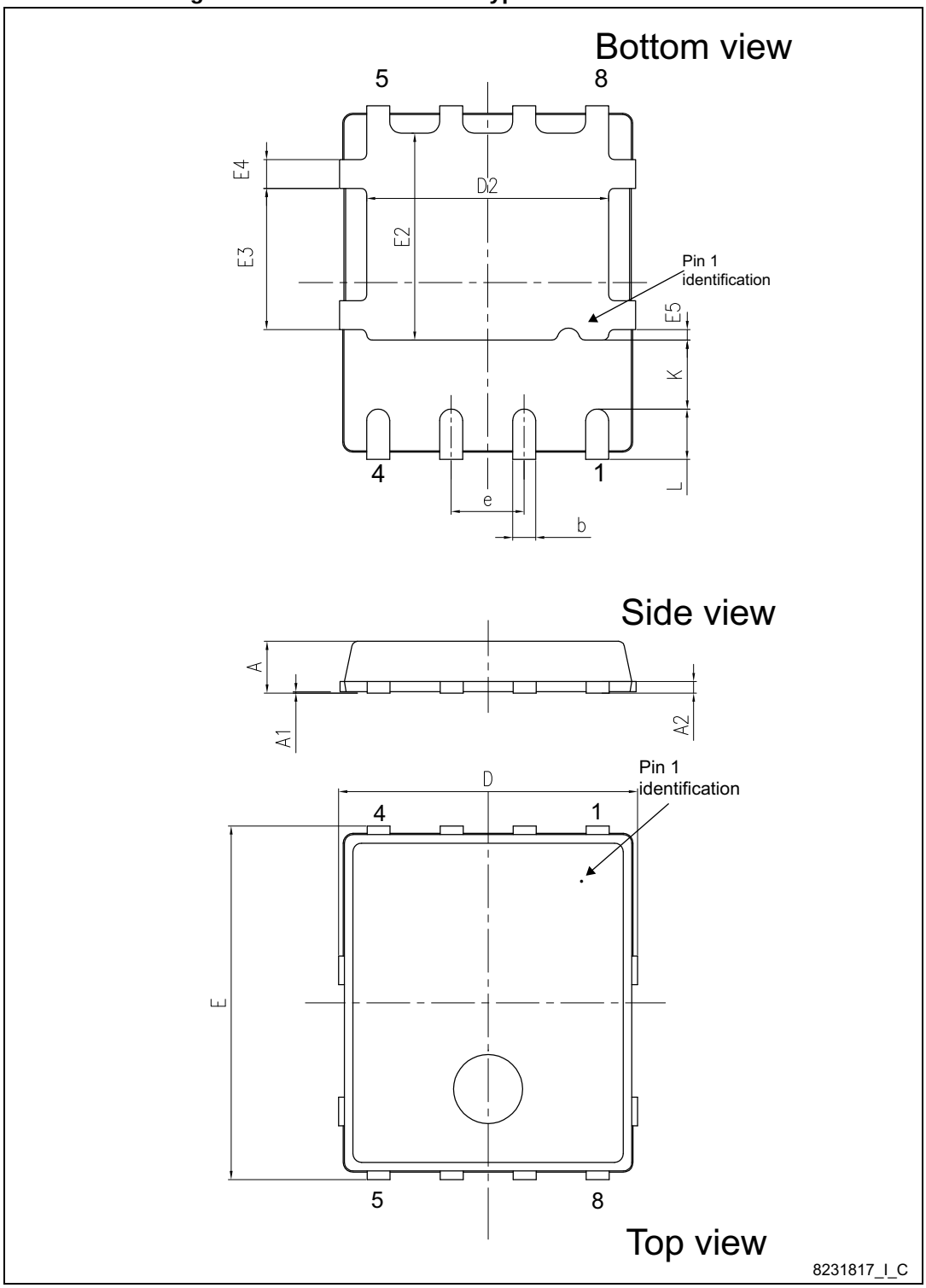
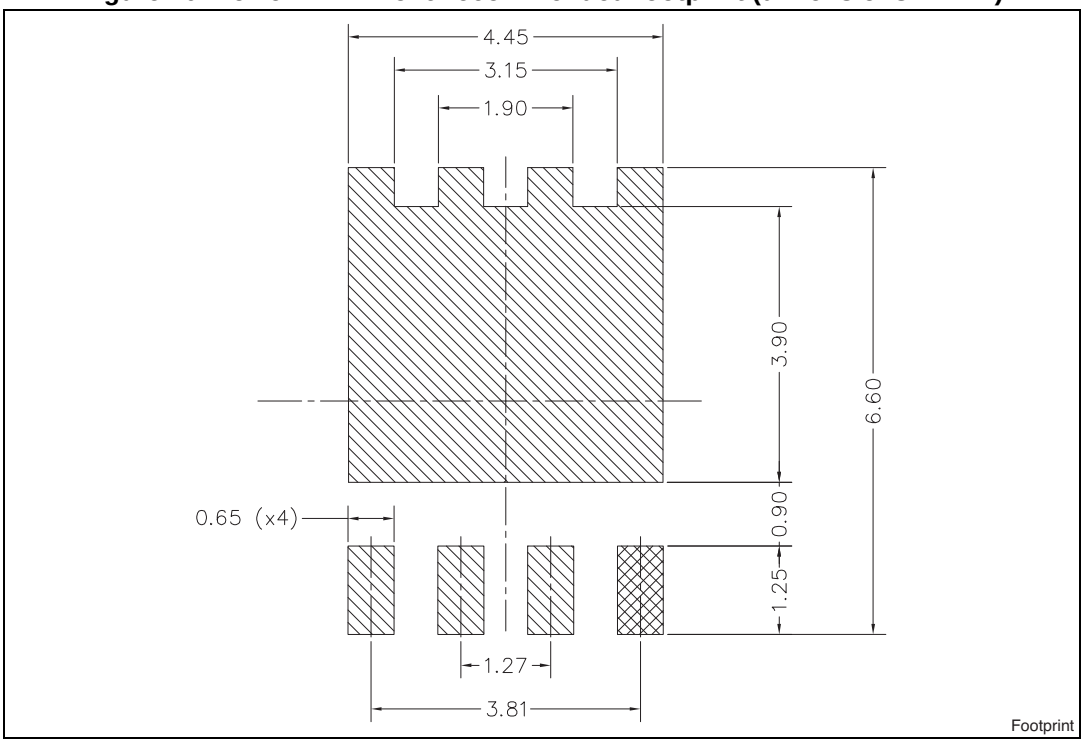


Table 8. PowerFLAT™ 5x6 type S-C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
D2	4.11		4.31
E		6.15	
e		1.27	
e1		0.65	
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
K	1.05		1.35
L	0.715		1.015

Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape[a]

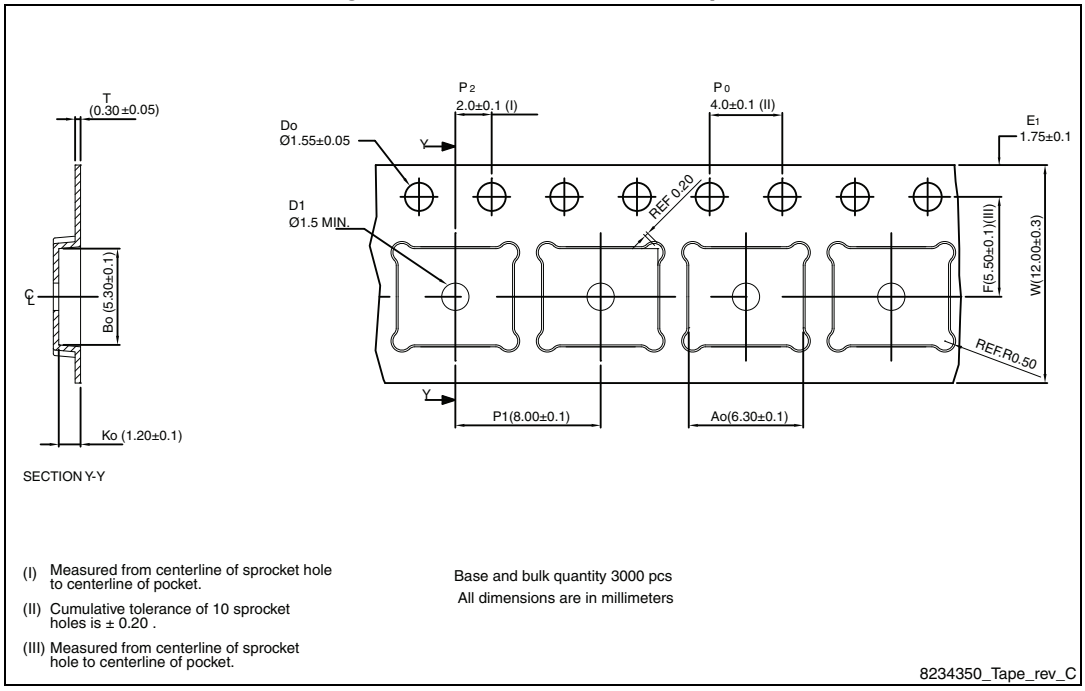
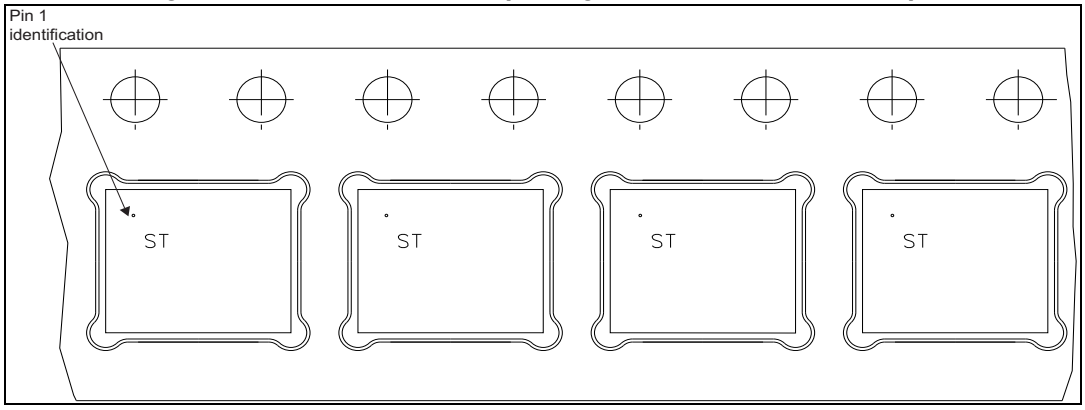
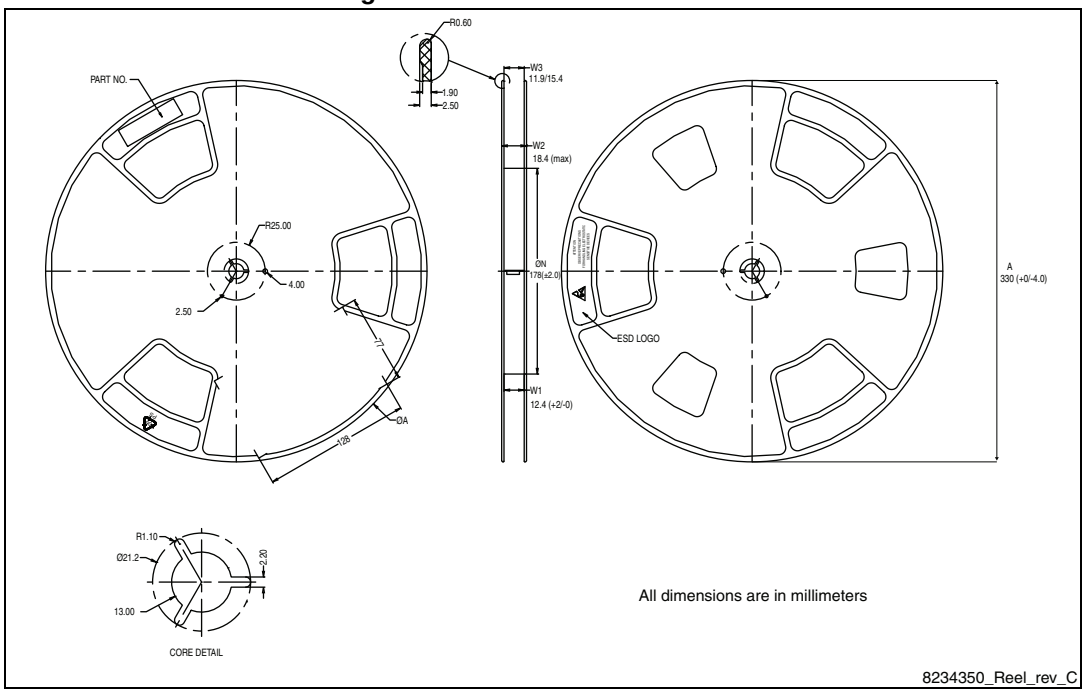


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
21-May-2013	1	First release.
23-Sep-2013	2	Document status promoted form preliminary to production data. Inserted *Section 2.1: Electrical characteristics (curves)*.
25-Jul-2014	3	– Modified: title and description – Modified: I_D and P_{TOT} values in cover page – Updated: *Figure 13*, *14*, *15* and *16* – Updated: *Section 4: Package mechanical data* – Minor text changes