STLC60844 - STLC60845
STLC60133 - STLC60243

COPPERWING ADSL CENTRAL OFFICE CHIPSET

DATA BRIEFING

The 8-channel ADSL Chip set from STMicroelectronics provides a complete low-power, cost saving solution for Central Office (CO) ADSL technology. The CopperWing chipset integrates all ADSL functions from Utopia to line in three board-area saving devices:

- **STLC60845**: octal channel ADSL data pump (DMT Transceiver)
- **STLC60844**: octal channel ADSL AFE (Analog Front End) with integrated receiver
- Line driver options:
  - **STLC60133**: single channel class AB line driver
  - **STLC60243**: dual channel class G line driver

The new ADSL chipset takes advantage of the STMicroelectronics large experience and deployment of the previous ADSL TOSCA chip set.

The Modem Control Software runs entirely on the DMT Transceiver: the line card host controller is in charge only of high-level management operation.

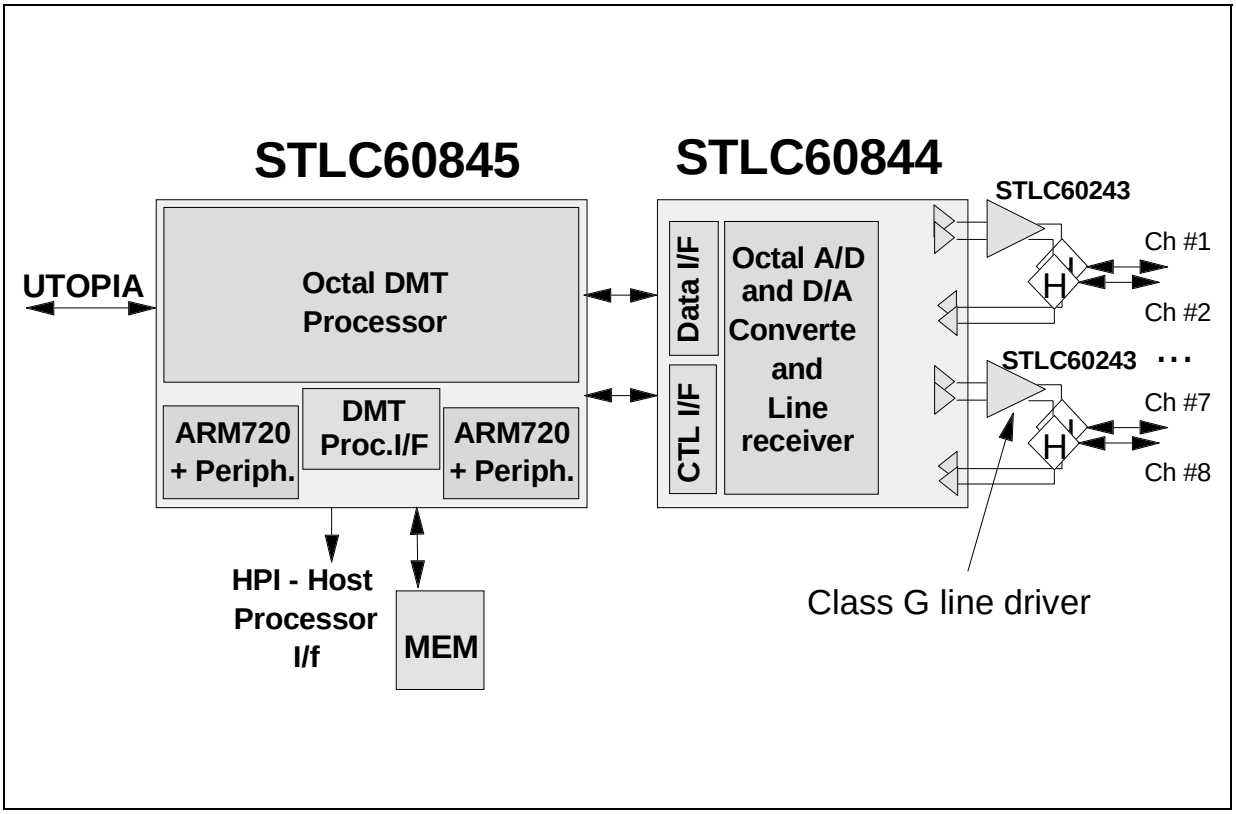
The chipset + the embedded SW are able to support all current ADSL standards, including ITU-T G.994.1 (G.hs), G.992.1 Annex A (G.dmt ADSL over POTS), G.992.1 Annex B (G.dmt ADSL over ISDN), G.992.2 (G.lite) and ANSI T1.413 Issue 2.

Thanks to its low power consumption and high integration, the CopperWing chip set is suitable for all CO applications like Digital Subscriber Line Multiplexer (DSLAM), Digital Loop Carrier (DLC), and CO line card architectures.

With only 1.2 square inches and less than 1.1 Watt per channel, the CopperWing chipset is one of the most competitive solutions for CO ADSL application.

An efficient Power Management mechanism and a Tone Activation feature are the complements of the overall solution.

BLOCK DIAGRAM



SOLUTION OVERVIEW

The **STLC60845** is an 8 channel ADSL Data Pump with integrated controller and direct interface to the 8 channel AFE STLC60844.

The two ARM720T processors embedded into the STLC60845 take care of the real-time modem control SW for the eight lines; the line card controller deals only with the higher level modem management (de/ activation, performance collection, notification, etc.).

From a Software point of view, the STLC60845 isolates the Modem Control Software (MCS), running on the internal ARMs, and the Customer's board management software running on the line-card processor.

The two functions of the low speed Host Processor Interface (HPI) on the STLC60845 device are the following:

- MCS SW download at boot time
- Inter-processor communication channel for Management, Fault detection, and life maintenance

The **STLC60844** Octal channel AFE is completely controlled by the STLC60845 through a dedicated interface. The STLC60844 implements eight analog transceiver functions required for a central office modem. It connects the digital modem chip with the line driver and hybrid balance circuit. This 8 channel AFE has been designed with high dynamic range and low noise, in order to greatly reduce the external filter requirements. In particular it allows for direct interfacing to the hybrid circuitry in RX path, saving the need of an external receiver. A per line tone detection function is also provided.

The **STLC60243** is a dual channel class G line driver. Key feature of this line driver is the very low power consumption, in the range of 0.65W per channel. Package is a EQFP48 7x7mm.

The **STLC60133** is a single channel class AB line driver available in a HTSSOP28 package (4x9mm).

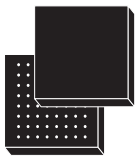
Combining the tone detection function of the AFE chip with the several power down facilities of the solution, the whole chipset can be kept in power down with an extremely low power consumption, also on a per-line basis, when not in use. This allows for effective system level power saving, still with quick power-up also in case of remote activation (CPE modem).

STLC60845

8 CHANNEL DMT ADSL DATA PUMP

PRODUCT PREVIEW

- 8 Channel DMT ADSL Data Pump
- 2 Embedded ARM720T controllers
- External System Bus Interface (SDRAM)
- Host Processor Interface
- Compliant with ITU992.1 (Annex A and B) and 992.2 (Annex A)
- Per Channel Power Down and Activation Feature
- Dedicated AFE Interface
- Utopia Level2 Interface (8-bit, single CLAV, polling mechanism)
- HCMOS8 Technology @ 1.8V (I/O @ 3.3)
- 292PBGA Package (27x27mm)



PBGA292 (27x 27mm)

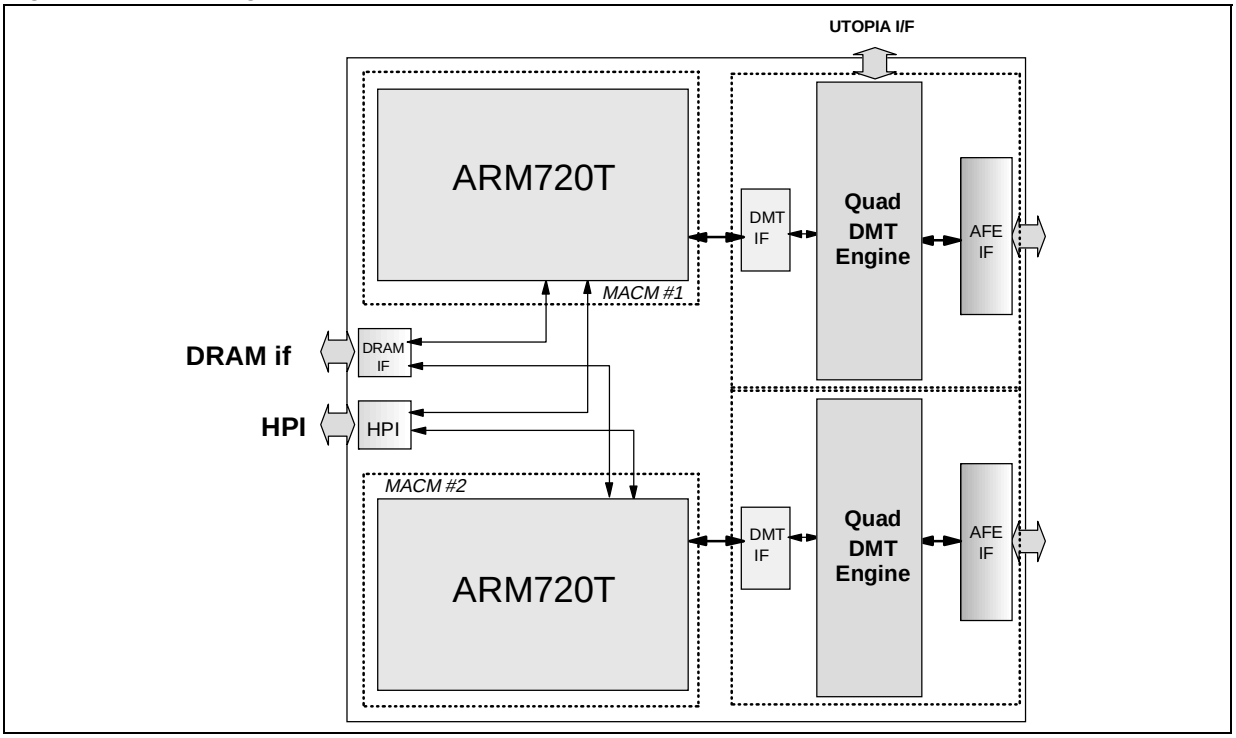
FUNCTIONAL DESCRIPTION

The STLC60845 is an 8 channel ADSL Data Pump with integrated controller and direct interface with the STLC60844 (8 channel AFE). An UTOPIA level 2 interface is also provided for the data interface.

The two ARM720T processors embedded into the STLC60845 take care of the real-time modem control Software for the eight lines; the line-card controller deals only with the higher level modem management (de/activation, performance collection, notification, etc.).

From a Software point of view, the STLC60845 isolates the Modem Control Software (MCS), running on the internal ARMs, and the Customer's software running on the line-card processor.

Figure 1. Block Diagram



ARCHITECTURE DESCRIPTION

Fig. 1 reports the high level view of the STLC60845 device. It has two main blocks:

- Data pump block
- Multi Channel ARM Control Module (MACM)

Data Pump Block

The Data Pump section is based on the Quad DMT engine macro-block; two identical macro-blocks are embedded in the device and are connected through an internal bus to the MACM block.

The internal AFE interface, coming from the Quad DMT engine macro-block, brings the samples coming from the data pump and presents them to the STLC60844 on a 16 bits interface.

The two DMT blocks share the same UTOPIA port.

MACM Block

The MACM block is based on the ARM720T core and is connected to the Data Pump block through an internal bus. The two ARMs are used to run the Modem Control Software based on embedded VxWorks RTOS (supplied by Wind River). The MACM #1 manages the channels from #0 to #3 while the MACM #2 manages the channels from #4 to #7. There is no direct connection between the two MACM blocks, but they share the same HPI and the memory interface controller.

INTERFACES

DRAM interface

The DRAM interface is used to access the external DRAM. This interface supports SDRAM interfaces with enough flexibility to be used with several DRAM chips available on the market. On top of the DRAM controller itself, this block includes also an arbiter so that the ARMs can share the single external DRAM. It is possible to support up to 4 external chip select space with x8, x16, x32 data bus width. Each chip-select address space is up to 32 Mbyte deep, so that a standard 32 Mbyte DRAM device fits easily. It is responsibility of the ARM code to properly configure the DRAM interface and to initialize the DRAM at the startup, with minimum DRAM-type information from the line-card controller.

HPI interface

A Host Processor Interface (HPI) is provided to allow the STLC60845 communicate with an external MCU. The design has been optimized for the Motorola MPC860. The external MCU sees the two MACM blocks at two different base addresses.

AFE interface

A direct interface to the 8-channel AFE device (STLC60844) is available in the STLC60845. Each 4 logical channels are grouped together, so there are four separate buses (two for the data samples and two for the control). The data sample bus is 16-bit wide in both TX and RX direction; 16*4=64 data lines in total between the AFE and the data pump. The STLC608445 receives also the master clock from the STLC60844.

UTOPIA interface

The STLC60845 implements an Utopia level2 interface (8 bit); it is a multi-PHY interface and is therefore an optimal solution for CO application The Utopia2 port provides access to both two data streams (fast and slow) for each line, making them available at two separate Utopia addresses (with a total of 8 addresses per chip, to be assigned).

The Utopia2 is fully working @ 25MHz.

Clock interface

Here below the clock interfaces of the STLC60845

- MCLK @ 35.238MHz coming from the STLC60844
- HPI input clock (host processor clock) up to 50MHz
- SDRAM output clock (MCLK)
- Utopia clock up to 25MHz (two lines, one per direction)

General

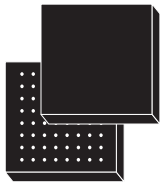
The STLC60845 is designed in HCMOS8 technology, 0.18um. The power supply of the internal core is 1.8V while the power supply of the external I/Os is 3.3V (3.3V level compliance).

STLC60844

8 CHANNEL ADSL AFE

PRODUCT PREVIEW

- Tx Path
  - 14bit DAC
  - 1st order low pass filter
  - Programmable Gain Amplifier (PGA)
- Rx Path
  - 12bit ADC
  - Programmable Attenuator
  - Internal Low Noise Amplifier (LNA)
- ITU-T and ANSI Tone Detection per line
- Per channel Power Down Function
- Fully Programmable through the DataPump Interface
- 196-pin LFBGA package (12x12mm)
- BiCMOS6 technology (0.35um)
- Single 3.3V supply
- Extended temperature range



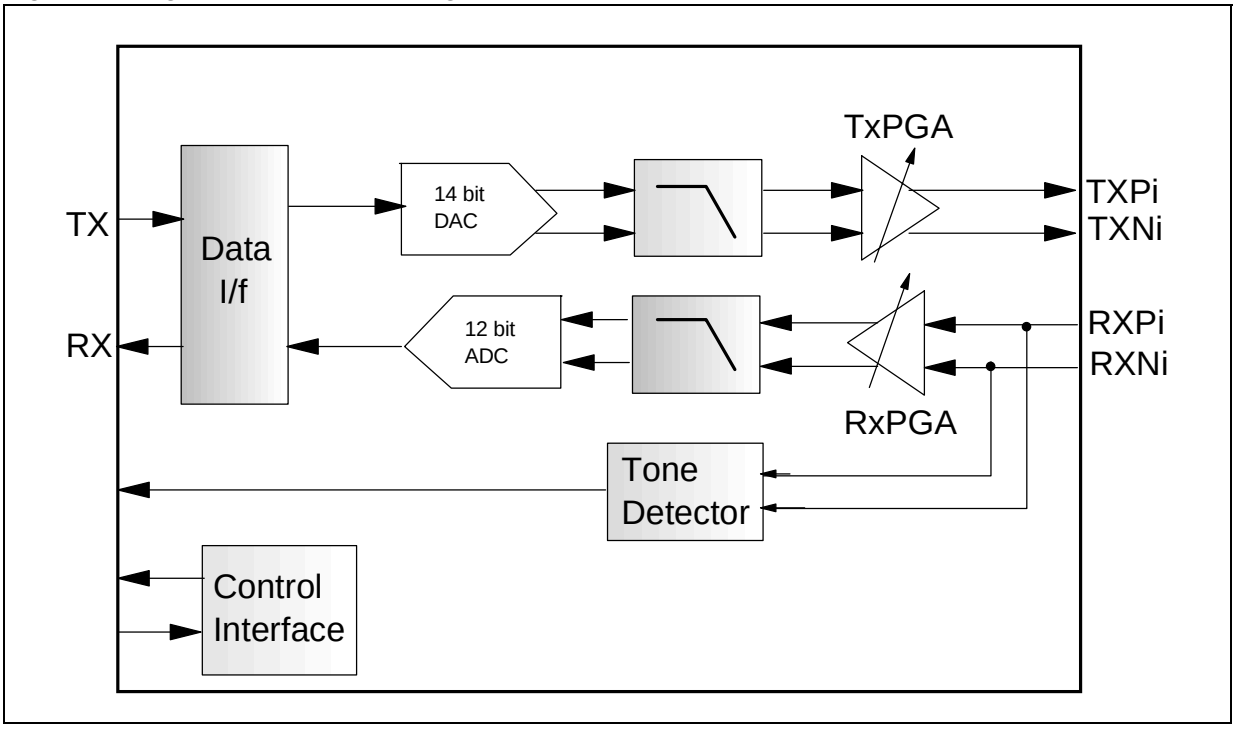
LFBGA196 (12 x 12mm)

FUNCTIONAL DESCRIPTION

The STLC60844 is a 4 channel ADSL AFE. It implements eight analog transceiver functions required for a central office modem. It connects the digital modem chip with the line driver and hybrid balance circuit. This 8 Ch AFE has been designed with high dynamic range in order to greatly reduce the external filter requirements. Each single channel can be put in power down mode and provides a tone detection function for remote activation.

No external receiver is required.

Figure 2. Single Channel Block Diagram



ARCHITECTURE DESCRIPTION

The STLC60844 has two separate sections: the Analog section and the Digital one.

The Analog section includes:

- in the Transmit path (downstream), a Programmable Gain Amplifier (PGA) and a final amplifier stage per channel;
- in the Receive path (upstream), a programmable attenuator, a low noise amplifier (LNA) and an antialias filter.

The Digital section includes:

- in the Transmit path, a digital interpolator per channel.
- A 12-bit DAC and a 14-bit ADC constitute the core of the device.

It is part of the Digital section also a Control Interface that allows the STLC60845 to configure the STLC60844, by means of a serial interface (with read/write capability for all the registers).

The digital data interface is made of two separate (one per direction) 16-bit buses, where data words from/to the 4 channels are multiplexed in a fixed pattern.

In Fig.1 is shown the internal block diagram of the STLC60844 related to a single channel.

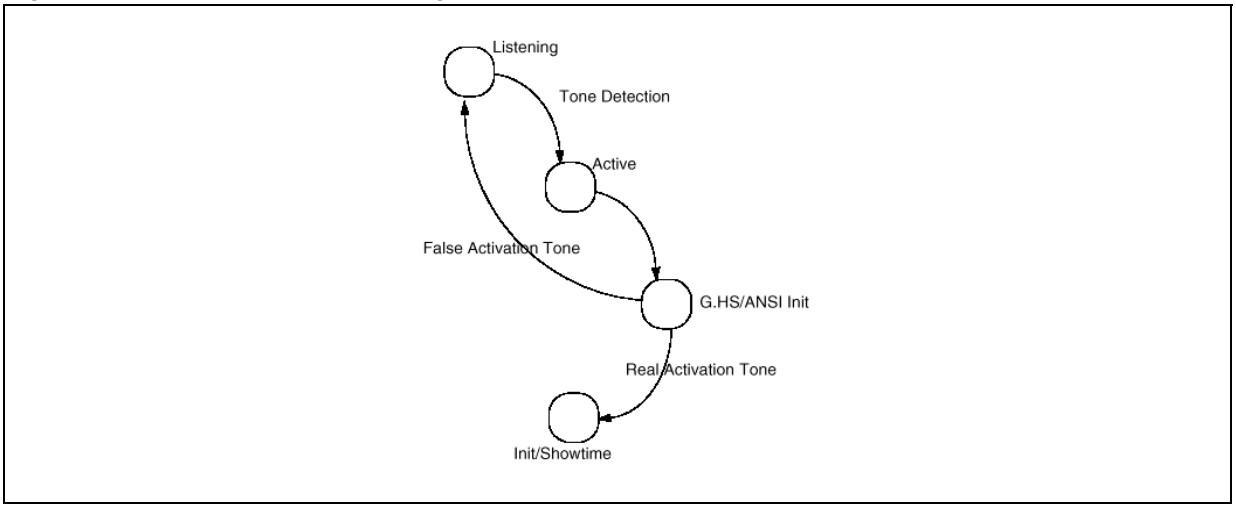
RECEIVE PATH DESCRIPTION

The receive path contains a programmable gain amplifier (RxPGA), a low pass anti-aliasing filter and a 12-bit ADC. The RxPGA is digitally programmable from 0 to 31dB in 1dB steps. The receive path is fully differential.

Tone activation

In the receive path also a tone detection block is present. Purpose of this block is the remote activation and is enabled during the power down mode of the single channel.

Figure 3. Tone activation state diagram



The Tone Detection block is able to detect the wakeup tone according to the selected standard(s): ITU and ANSI, over POTS and over ISDN. When activity is detected on a specific tone, an external signal (ACTD) is activated, allowing the corresponding channel to wake up. The DMT companion chip must read a specific register to know which channel is waked up.

TRANSMIT PATH DESCRIPTION

The transmit path contains a 14-bit DAC necessary to generate the TX signal from a 14-bit digital input word.

The TX signal is then scaled by a programmable gain amplifier (TxPGA) from 0 to -15dB in 1dB steps. Also the transmit path is fully differential.

INTERFACE

Digital Data interface

To facilitate the data transfer between the STLC60844 and STLC60845 a double 16 bit parallel port (one for the downstream and one for the upstream) is provided. Each port consists of the data interface plus the control signals required to transmit and receive the data.

Control Serial interface

There is a 5 pins serial digital interface that is used to load one of the 8 12-bit control register that controls all the programmable features of the STLC60844. In order to program separately each channel, 3 pins are dedicated to address them.

POWER DOWN MODE

The device has several Power-Down features. A control pin allows to put in power-down the complete STLC60844 device.

Through the control interface, it is instead possible to selectively put in power-down every single logical line of the STLC60844. In particular, each ADSL channel has a dedicated power-down register in the AFE, with 4 separate bits to put in power-down the DAC, the ADC, the LNA and the PGA. In this case, the Tone Activation block remains always active.

GENERAL

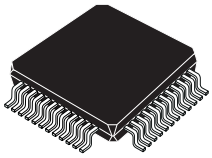
The STLC60844 is designed in BiCMOS6M technology, 0.35um. It is a single 3.3V supply device.

STLC60243

DUAL CHANNEL ADSL LINE DRIVER

PRODUCT PREVIEW

- Class G ADSL line driver
- Low power consumption
- Low distortion
  - -70dBc @ f =1MHz, Vout =-40Vpp (differential), 50W load
- 500mA minimum output current into a 50W load
- Digitally programmable gain: 13-28dB, step 1dB
- Single channel termal shutdown
- Low-Power mode
  - 85mW with active impedance synthesis
  - 5mW with passive impedance synthesis
- Over current and over temperature protection with per channel fault indication
- Minimal external components
- TQFP48 7x7mm package with slug
- ±-5V and ±15V supply



TQFP48 (7x7mm)

GENERAL DESCRIPTION

The STLC60243 is a dual channel ADSL line driver that has very low power consumption. It accepts differential input signals from the AFE and can be used for both full-rate (G.dmt) or G.lite application. Thanks to its small package is also an extremely space saving device.

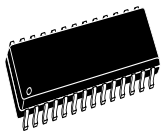
The main concept behind the improved consumption performances is the dual external power supply: normally at ±5V, the power supply is automatically switched to ±15V when required, to properly follow the signal peaks (depending of the statistic of the DMT signal). No external power supply switch command is required.

STLC60133

DUAL CHANNEL ADSL LINE DRIVER

PRODUCT PREVIEW

- Class G ADSL line driver
- Low noise
  - 4nV/(Hz)1/2
- Low single tone distortion
  - -60dBc @ f =1MHz, 18Vp, 100Ω load
- 500mA minimum output current into a 50Ω load
- Thermal and over load protections
- High speed
  - 100MHz bandwidth (-3dB), Gain = 6
  - 30MHz Gain Flatness
  - 400V/us Slew Rate
- Low Power operation
  - From ±5V to ±15V
  - 12.5mA/A Total supply current
  - Power-reduced stand by current of 4.5 mA/A
- Minimal external components
- HTSSOP28 4x9mm package with slug
- From ±5V to ±15V voltage supply range



HTSSOP28 with slug up (4x9mm)

GENERAL DESCRIPTION

The STLC60133 is a single channel ADSL line driver that has very low power consumption. It accepts differential input signals from the AFE and can be used for both full-rate (G.dmt) or G.lite application.

Two digital bits allow the line driver to be capable of full performances, an output "stand-by" state, or two intermediate bias states. The Stand-by state biases the output stage in order to provide a low impedance for back termination.

Thanks to its small package (HTSSOP28 with exposed leadframe) is also an extremely space saving device.