STPTIC

Parascan™ tunable integrated capacitor

Datasheet – production data

Features

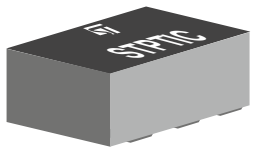
- High power capability (+36 dBm)
- High tuning range (3.5/1)
- High quality factor (Q)
- High linearity device
- Low leakage current
- Capacitor bias is DC blocked
- Frequency of operation from DC to 3 GHz
- 7 values available: 2.7pF, 3.3 pF, 3.9 pF, 4.7 pF, 5.6 pF, 6.8 pF and 8.2 pF
- Analog control voltage
- Compatible with high voltage control IC (STHVDAC series)
- Available in plastic molded package:
  - µQFN package 1.2 x 1.6 x 0.9 mm
  - Flip Chip 0.65 x 1.2 x 0.3 mm
- ECOPACK®2 compliant component

Benefit

- RF tunable passive implementation in mobile phones to optimize antenna radiated performances.

Applications

- Cellular Antenna tunable matching network in multi-band GSM/WCDMA/LTE mobile phone
- Tunable RF filters
- Cellular tunable antenna
- LTE band tuning
- VSWR correction circuit



µQFN

Flip Chip

Description

The ST integrated tunable capacitor, offers excellent RF performance, low power consumption and high linearity required in adaptive RF tuning applications. The fundamental building block of PTIC is a tunable material called Parascan which is a version of barium strontium titanate (BST) developed by Paratek microwave.

BST capacitances are tunable capacitances intended for use in mobile phone application, and dedicated to RF tunable applications. These tunable capacitances are controlled through a bias voltage ranging from 2 to 20 V. The use of BST tunable capacitance in mobile phones enables significant improvement in terms of radiated performances making the performance almost insensitive to the external environment.

TM: Parascan is a trade mark of Paratek microwave Inc.

1 Functional characteristics

Figure 1. PTIC functional block diagram

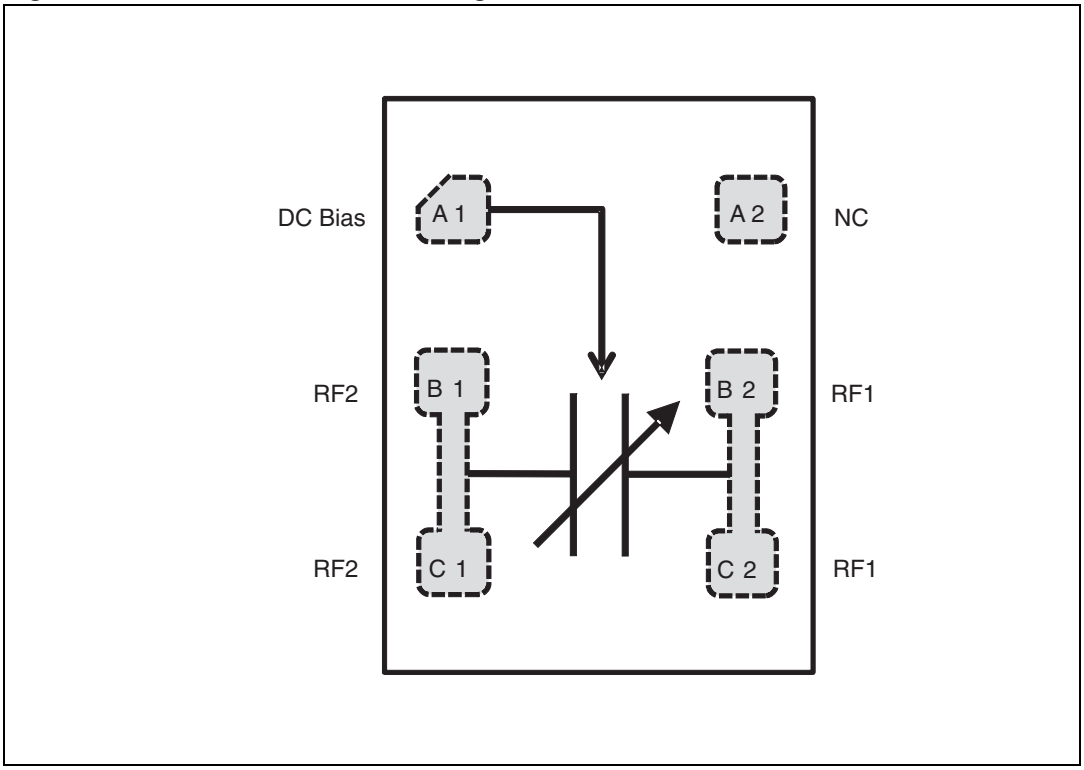


Table 1. Signal descriptions

Ball/Pad number	Pin name	Description
A1	DC BIAS	DC Bias voltage
B1	RF2	RF Input / output
C1	RF2	RF Input / output
A2	NC	Not Connected
B2	RF1	RF Input / output
C2	RF1	RF Input / output

2 Electrical characteristics

Table 2. Absolute maximum ratings (limiting values)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P_{IN}	Input peak power RF_{IN} (CW mode)/all RF ports			36	dBm
$V_{ESD(HBM)}$	Human model (JESD22-A114-B), all I/O		class 1A(1)		V
$V_{ESD(MM)}$	Machine model (JESD22-A114-B), all I/O	100			
T_{device}	Device temperature			125	°C
T_{stg}	Storage temperature	-55 to +150			
V_x	Bias voltage	25			V

1. Class 1A defined as passing 250 V

Table 3. Recommended operating conditions

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
P_{IN}	RF input power (50% duty cycle mode) RF_{IN} (LB) RF_{IN} (HB)			 35 33	dBm
F_{OP}	Operating frequency	700		3000	MHz
T_{device}	Device temperature			100	°C
T_{OP}	Operating temperature	-30		85	
V_x	Bias voltage	2		20	V

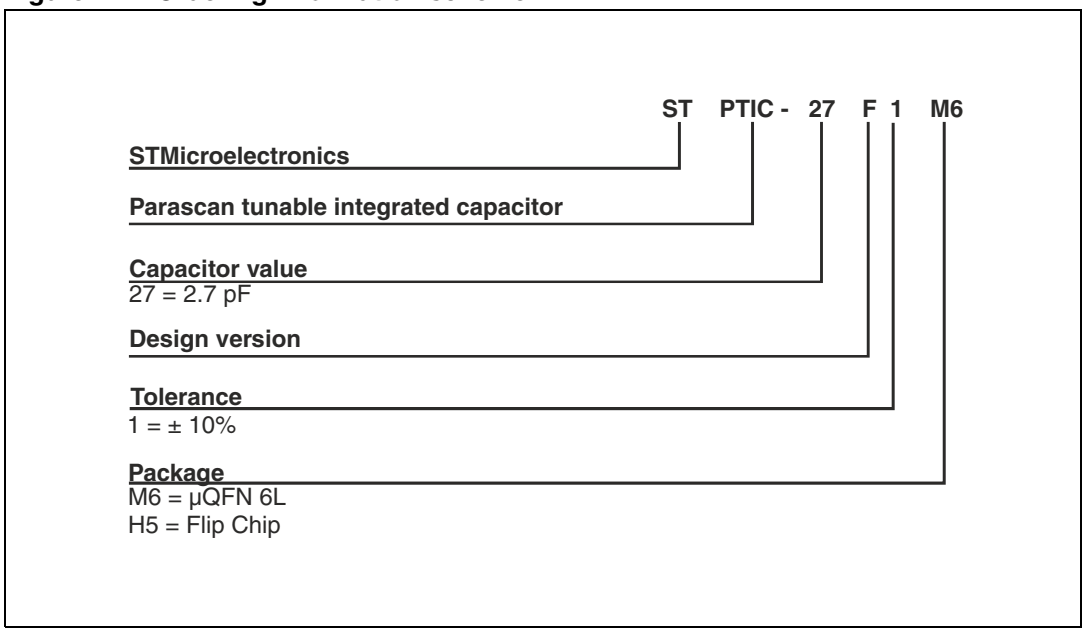
Table 4. Representative performances (T_{amb} = 25 °C)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
C_{2V}	Capacitance at 2V bias	STPTIC-27	2.43	2.7	2.97	pF
		STPTIC-33	2.97	3.3	3.63	pF
		STPTIC-39	3.51	3.9	4.29	pF
		STPTIC-47	4.23	4.7	5.17	pF
		STPTIC-56	5.04	5.6	6.16	pF
		STPTIC-68	6.12	6.8	7.48	pF
		STPTIC-82	7.38	8.2	9.02	pF
I_L	Leakage current	Measured with Vbias = 20 V			100	nA
ΔC	Tuning range	Ratio between C_{2V}/C_{20V} measured at 100 kHz	2.6/1	3.5/1		
Q_{LB}	Quality factor	Measured at 900 MHz		65		
Q_{HB}	Quality factor	Measured at 1800 MHz		45		
IP3	Third order intercept point	Vbias = 2 V(1) and (3)		60		dBm
		Vbias = 20 V(1) and (3)		70		dBm
H2	Second harmonic	Vbias = 2 V(2) and (3)		-65		dBm
		Vbias = 20 V(2) and (3)		-65		dBm
H3	Third harmonic	Vbias = 2 V(2) and (3)		-45		dBm
		Vbias = 20 V(2) and (3)		-45		dBm
t_T	Transition time	From Cmin to Cmax (4)		135		µs
		From Cmax to Cmin(4)		100		µs

1. f_1 = 894 MHz, f_2 = 849 MHz, P_1 = 20 dBm, P_2 = -15 dBm, $2f_1 - f_2$ = 939 MHz
2. 894 MHz, P_{in} = 34 dBm
3. IP3 and harmonics are measured in the shunt/series configuration in a 50 Ω environment
4. One or both of RFin and RFout must be connected to DC ground

3 Ordering information scheme

Figure 2. Ordering information scheme



4 Package information

- Epoxy meets UL94, V0
- Lead-free package

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK® is an ST trademark.

Figure 3. µQFN package dimension

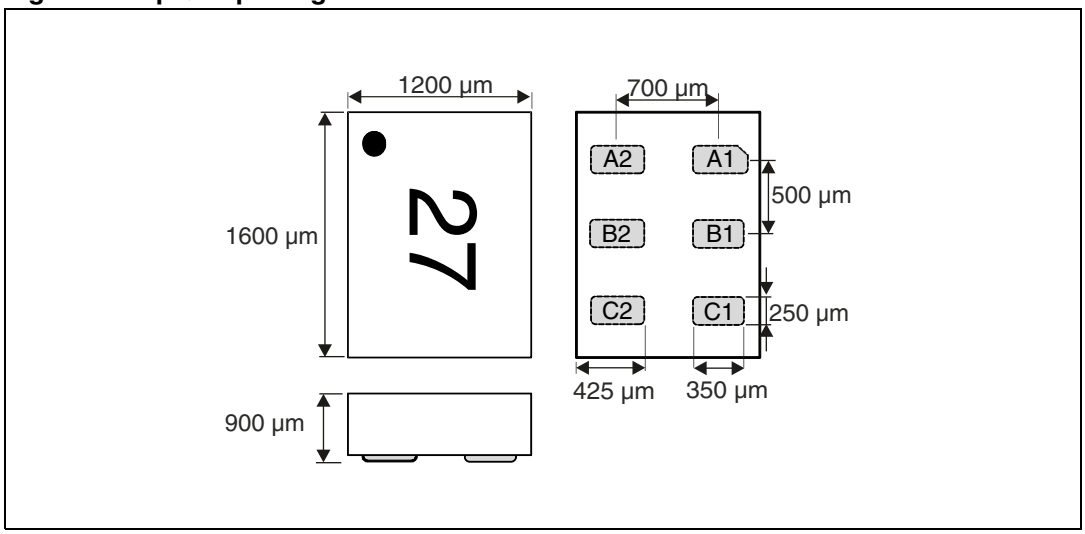


Figure 4. Recommended PCB land pattern for µQFN package

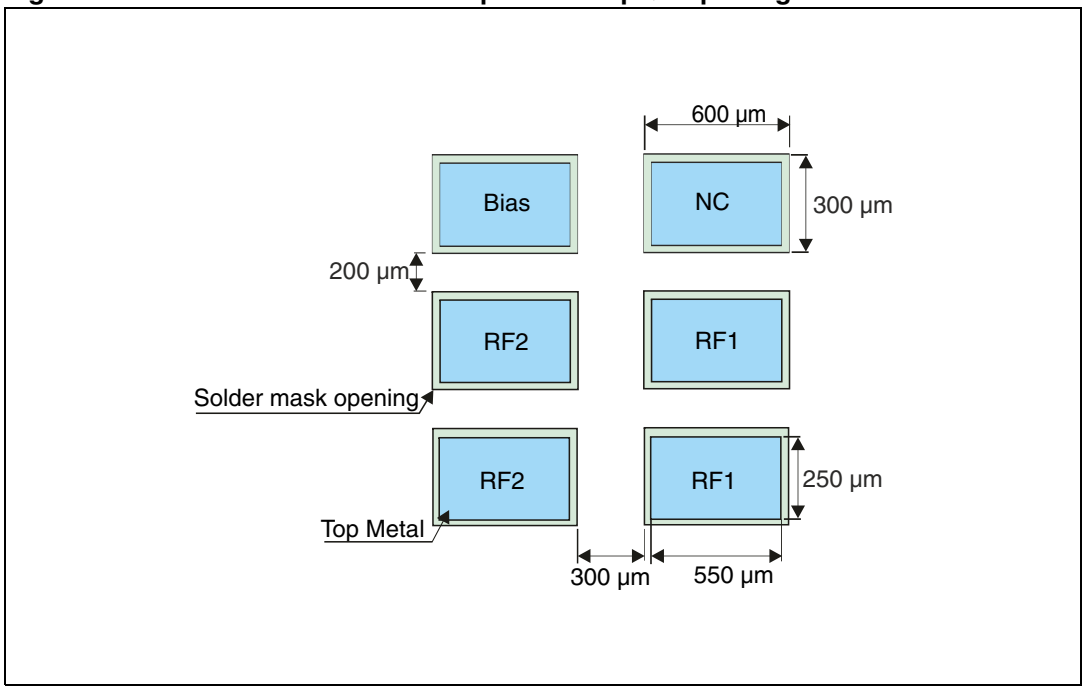


Figure 5. Flip Chip dimensions (size for 2p7, 3p3)

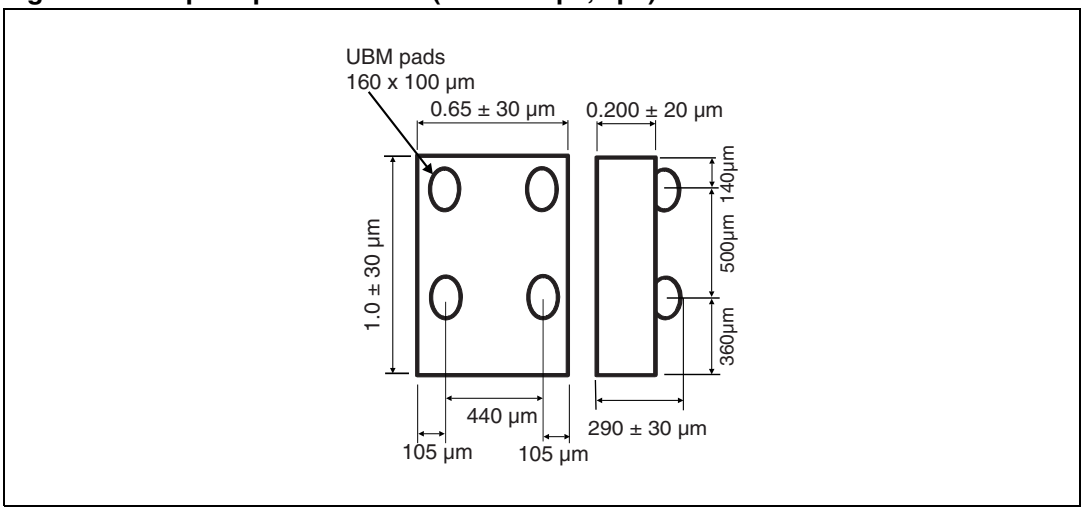


Figure 6. Flip Chip dimensions (size for 3p9, 4p7)

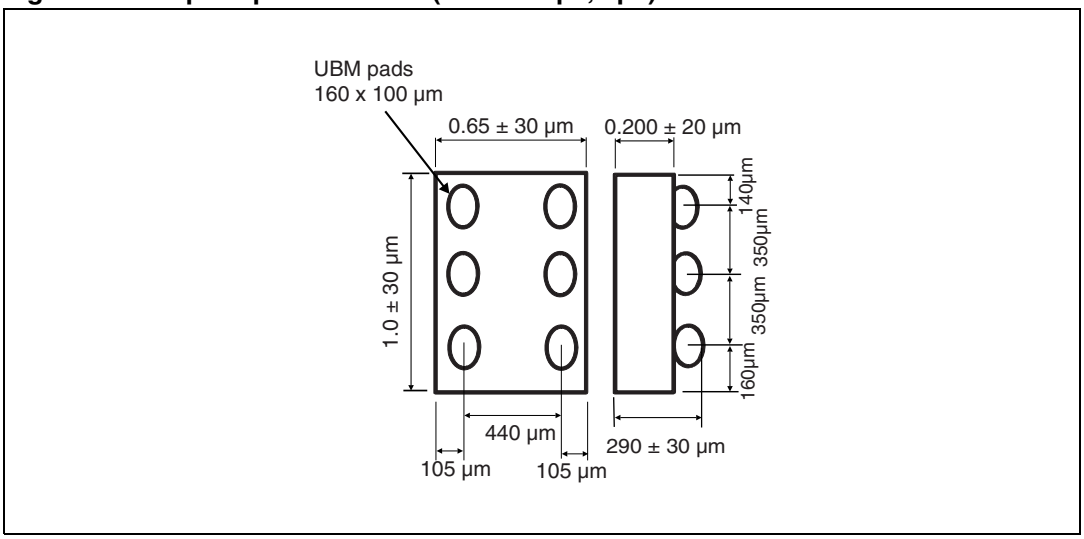


Figure 7. Flip Chip dimensions (size for 5p6, 6p8, 8p2)

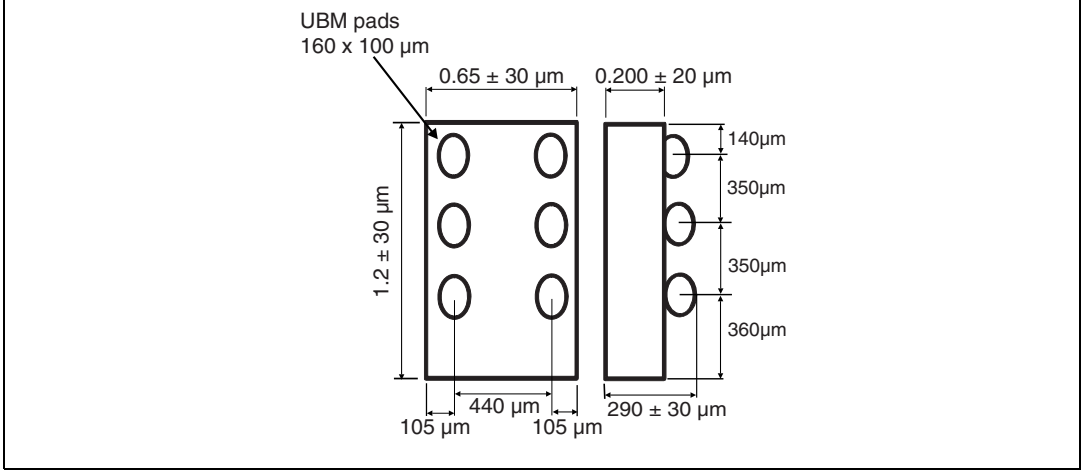


Figure 8. Recommended PCB land pattern for Flip Chip package (metal defined pads, solder mask 25 µm larger)

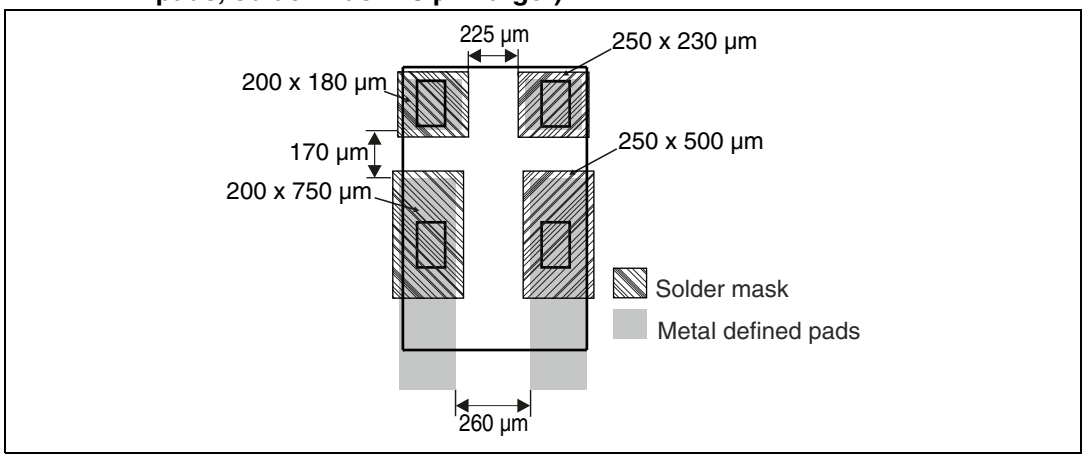


Figure 9. Recommended PCB land pattern for Flip Chip PTIC (die size 650x1000)

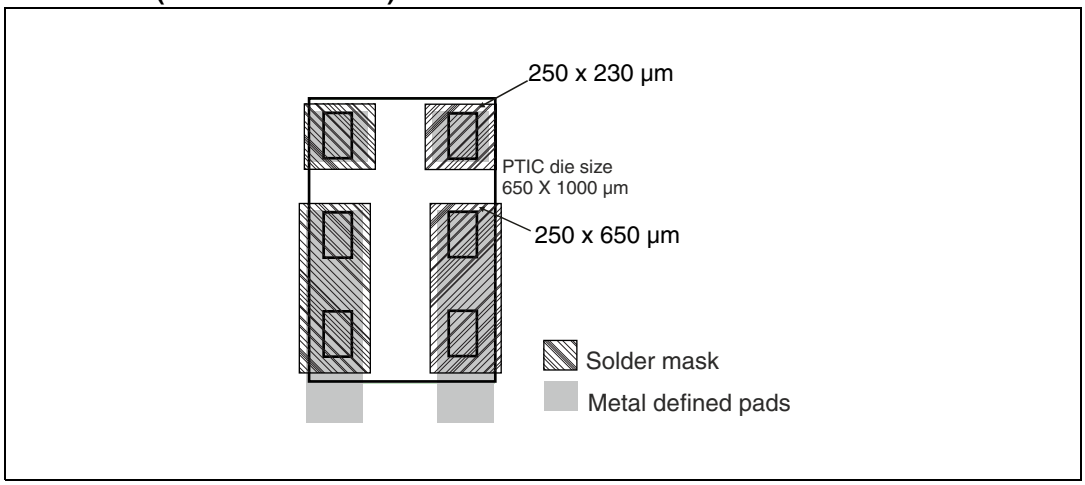


Figure 10. Recommended PCB land pattern for Flip Chip PTIC (die size 650x1200)

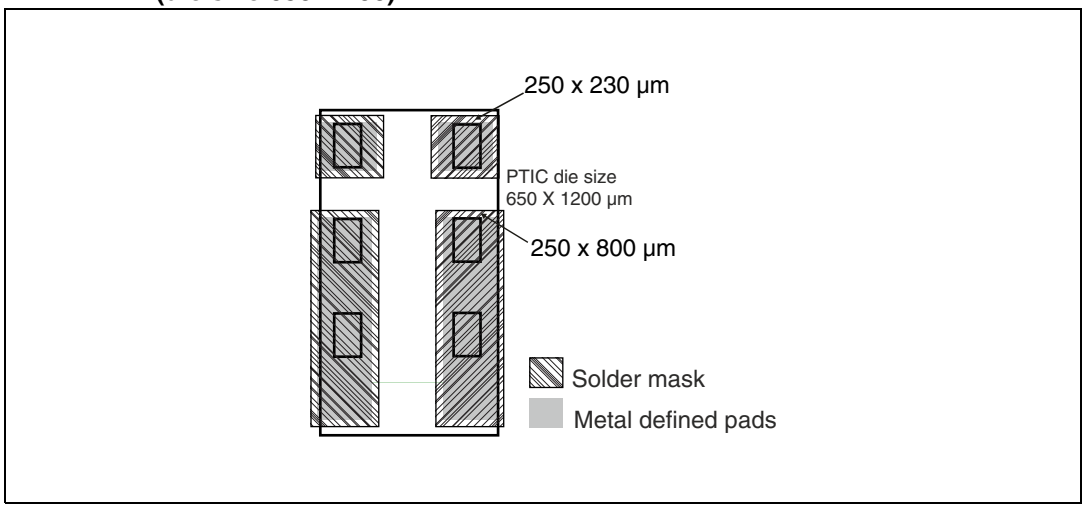


Figure 11. µQFN marking

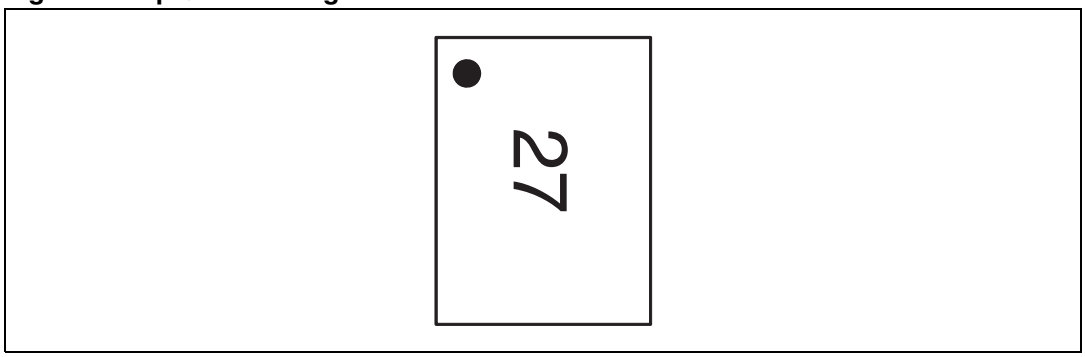


Figure 12. Flip Chip marking (bump side view)

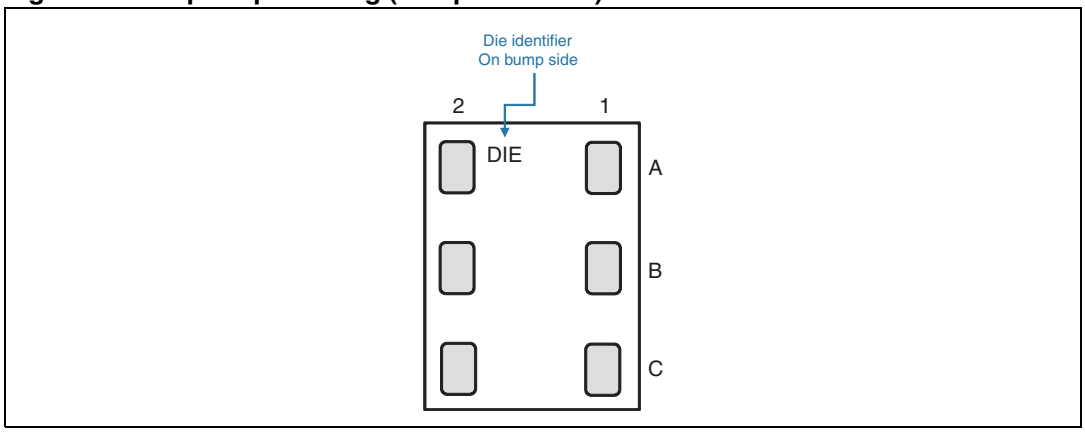


Figure 13. µQFN tape and reel specification

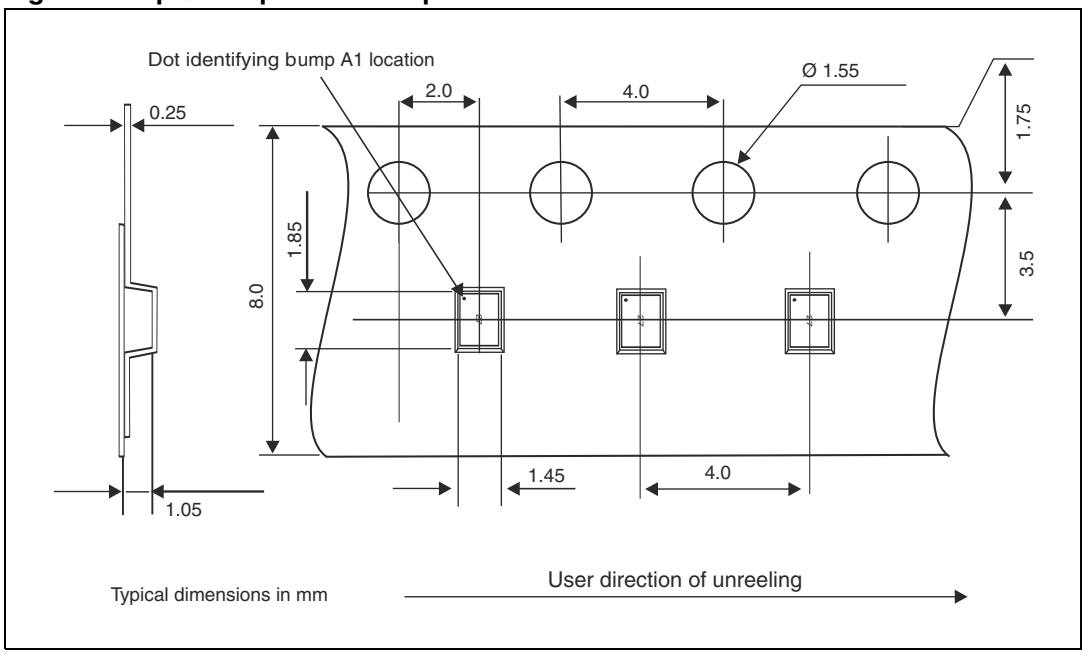
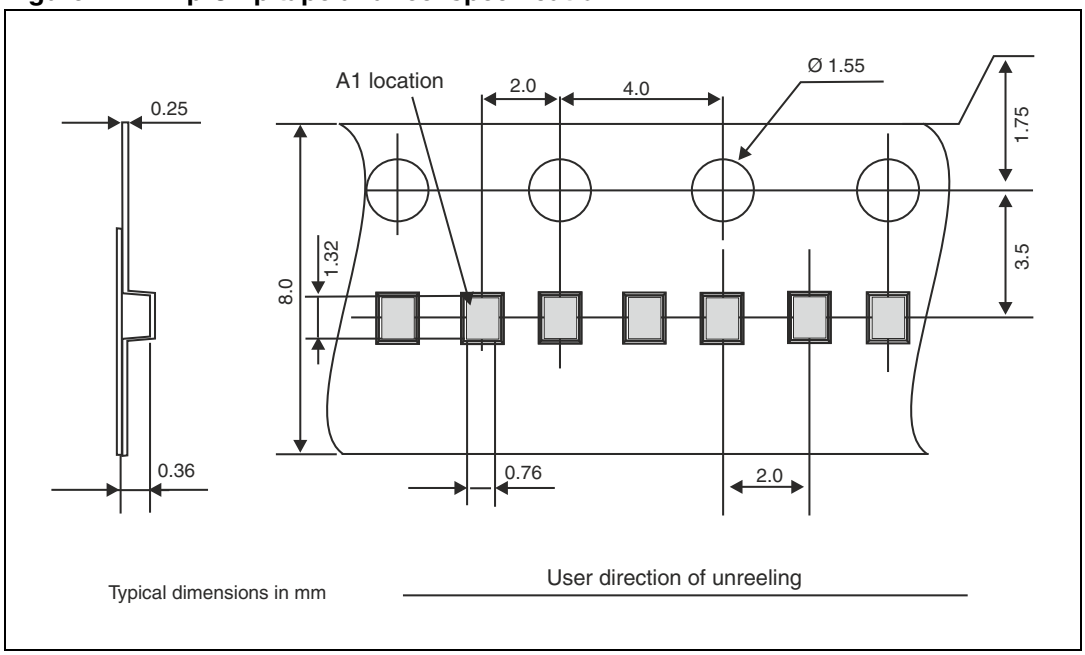
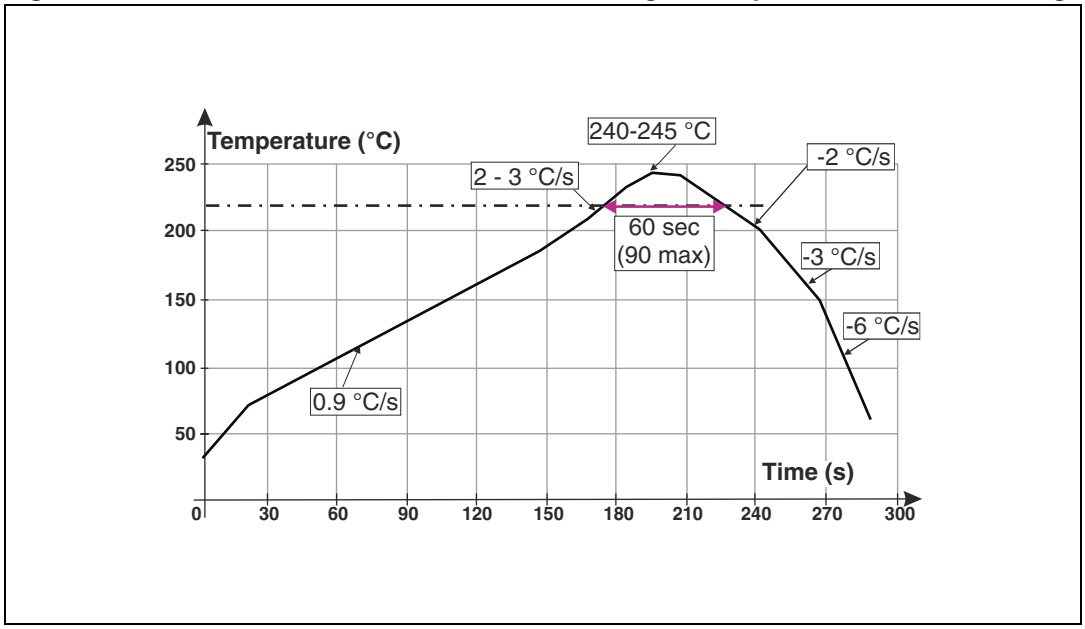


Figure 14. Flip Chip tape and reel specification



5 Recommendation on PCB assembly

Figure 15. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

Table 5. Recommended (value)

Profile	Value	
	Typical	Max.
Temperature gradient in preheat (T = 70-180 °C)	0.9 °C/s	3 °C/s
Temperature gradient (T = 200-225 °C)	2 °C/s	3 °C/s
Peak temperature in reflow	240-245 °C	260 °C
Time above 220 °C	60 s	90 s
Temperature gradient in cooling	-2 to -3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

6 Ordering information

Table 6. Ordering information

Part Number	Marking	Weight	Base Qty	Delivery Mode
STPTIC-27F1M6	27		3000	Tape and reel
STPTIC-33F1M6	33		3000	Tape and reel
STPTIC-39F1M6	39		3000	Tape and reel
STPTIC-47F1M6	47		3000	Tape and reel
STPTIC-56F1M6	56		3000	Tape and reel
STPTIC-68F1M6	68		3000	Tape and reel
STPTIC-82F1M6	82		3000	Tape and reel
STPTIC-27G1H5	I1x		15000	Tape and reel
STPTIC-33G1H5	I3x		15000	Tape and reel
STPTIC-39G1H5	I2x		15000	Tape and reel
STPTIC-47G1H5	I5x		15000	Tape and reel
STPTIC-56G1H5	I4x		15000	Tape and reel
STPTIC-68G1H5	I7x		15000	Tape and reel
STPTIC-82G1H5	I6x		15000	Tape and reel

7 Revision history

Table 7. Document revision history

Date	Revision	Changes
02-Nov-2012	1	Initial release.

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