SHARP

Reference

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To;

S P E C I F I C A T I O N S

Product Type 6 Segment LED Driver IC

IR2E53Y7

Model No.

※ This specifications contains 53 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMERS ACCEPTANCE

DATE :

BY :

PRESENTED

BY : H. Fujita

H. Fujita
Dept. General Manager

REVIEWED BY : H. Morikawa

PREPARED BY : A. Tokura

Engineering Dept. IV
Opto-Analog Devices Division
Electronic Components Group
SHARP Corporation

● When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting form failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) These contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

● Please direct all queries regarding the products covered herein to a sales representative of the company.

Content

1. General Description

This IC incorporates LED driver for illumination with animated control.
This IC is equipped with 3-colum driver and 6 segment driver circuit. And This IC can controll 6-RGB LED or 18-single LED in maximum.
All LED brightness can continuously be changed with internal animation logic circuit.
This IC is equipped with charge pump DC/DC converter to drive LED.
This IC supports I^2C-Bus interface.
This product is optimum for use as the illumination LED driver IC for cellular phone and PDA applications, etc.

2. Features

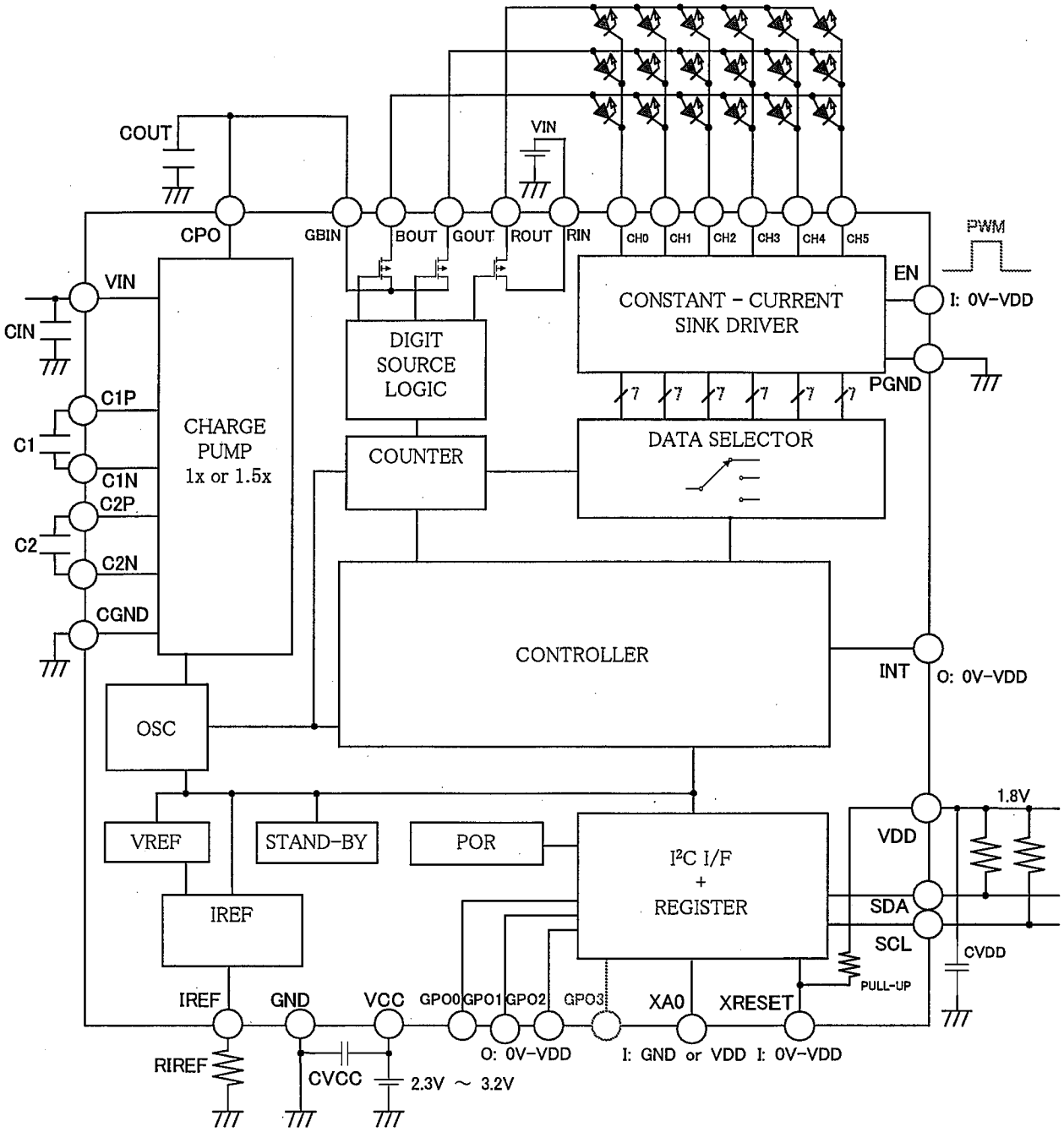
- Supply Voltage Range: VIN=3.0V to 4.5V, VCC=2.3V to 3.2V
- Supports I^2C-Bus interface
- Supports I^2C Extend address
- SCL pin and SDA pin are installed with noise filters.
- 6Ch Sink-type variable constant current driver for LED (maximum current 25.9mA)
- Control logic circuit for animated illumination embedded
- Output-enable circuit embedded
- 1x/1.5x Modes Charge Pump: Automatically Selected
- Voltage reference embedded
- Power-on-reset circuit embedded
- Soft-Start Limits Inrush Current
-

Radiation resistance designing:	No
Package:	35-pin WL-CSP package (3.57mm x 3.57mm)
Chip material and wafer board type:	P-type silicon substrate monolithic IC
Lead surface finish:	Lead-free
Process:	CMOS

3. Terminal name

Pin No	Pin name	Description
A1	U1A	Non-connect. This terminal is connected to pin No. F6 (U2F).
A2	VDD	Supply voltage for I/O buffer of I^2C, GPO and INT pin.
A3	IREF	Resistor connection terminal for reference current setting of LED drivers.
A4	XRESET	Hard reset terminal.
A5	SCL	I^2C clock input.
A6	GPO0	General purpose output.
B1	GBIN	Source terminal of column driver for ROUT and GOUT pin.
B2	GPO2	General purpose output.
B3	VCC	Power supply terminal.
B4	SDA	I^2C data Input/Output terminal.
B5	EN	Enable for all LED
B6	CH1	Constant current output terminal.
C1	GOUT	Column driver terminal to anode terminal of green LED
C2	INT	Interrupt output terminal.
C4	GPO3	General purpose output.
C5	CH0	Constant current output terminal.
C6	PGND	LED driver ground.
D1	RIN	Source terminal of column driver for ROUT pin.
D2	BOUT	Column driver terminal to anode terminal of blue LED
D3	GND	Ground terminal for control.
D4	XA0	I^2C address configuration input.
D5	CH2	Constant current output terminal.
D6	CH3	Constant current output terminal.
E1	VIN	Power supply terminal for charge pump.
E2	ROUT	Column driver terminal to anode terminal of red LED.
E3	C1N	Flying capacitor 1 negative connection.
E4	CH4	Constant current output terminal.
E5	CH5	Constant current output terminal.
E6	CGND	Ground terminal for charge pump.
F1	GPO1	General purpose output.
F2	C1P	Flying capacitor 1 positive connection.
F3	CPO	Output voltage terminal of charge pump.
F4	C2P	Flying capacitor 2 positive connection.
F5	C2N	Flying capacitor 2 negative connection.
F6	U2F	Non-connect. This terminal is connected to pin No. A1 (U1A).

4. Block Diagram



5. Pin Assignment

	1	2	3	4	5	6
A	U1A	VDD	IREF	XRESET	SCL	GPO0
B	GBIN	GPO2	VCC	SDA	EN	CH1
C	GOUT	INT		GPO3	CH0	PGND
D	RIN	BOUT	GND	XA0	CH2	CH3
E	VIN	ROUT	C1N	CH4	CH5	CGND
F	GPO1	C1P	CPO	C2P	C2N	U2F

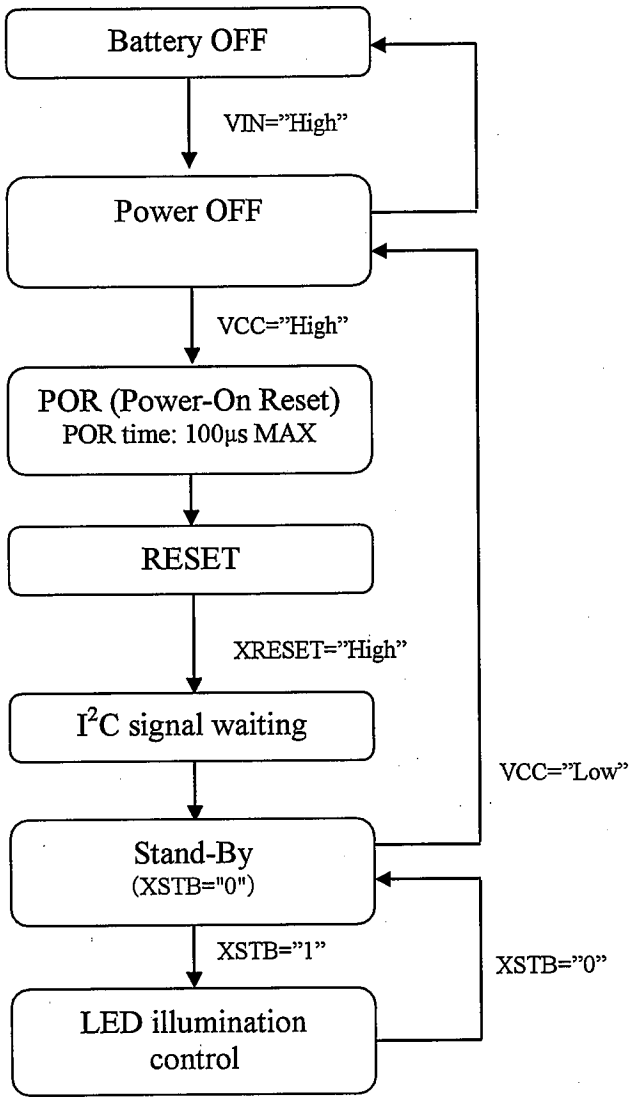
Note: Pins are located on the underside.

6. Peripheral Parts List

Type	Name	Maximum applied voltage(V)	Parts	Value
Smoothing capacitor	CVIN	6V	Temperature characteristICs code:B	1.0μF
Smoothing capacitor	CVCC	4.5V	Temperature characteristICs code:B	1.0μF
Smoothing capacitor	CVDD	3.3V	Temperature characteristICs code:B	1.0μF
Smoothing capacitor	COUT	8V	Temperature characteristICs code:B	2.2μF
Flying capacitor	C1	4.5V	Temperature characteristICs code:B	1.0μF
Flying capacitor	C2	4.5V	Temperature characteristICs code:B	1.0μF
Reference resistance	RIREF	-	Tolerance:±1%	13kΩ
Light-emitting diode	LED	-	GN1WA55320A	-

7. Function Operation

This IC is equipped with the LED driver circuit, the charge pump DC/DC converter that supply electricity to LED, I²C interface and general purpose outputs.
The operation of the IC can be set by the built-in register through the I²C interface.
I²C interface can use standby state or LED driver control mode.



7.1 Constant current driver

This IC is equipped with a sink-type variable constant current driver for LED.
This IC is connectable to 6-RGB LED or 18-single LED for illumination.
The maximum current of a constant current driver is the value set up by peripheral resistance. It is also possible to perform the ON/OFF control using the enable/disable pin (EN pin).
Connect driver terminal to VCC when LED is unconnected.

7.1.1 ON/OFF control of constant current driver

Constant current driver is also possible to perform the ON/OFF control using the EN pin.
EN pin can be disabled with the EXT_EN register.
The logic of EN pin can be reversed. with the EN_XEN register.

EN pin is an input terminal that controls ON/OFF of the Constant current driver.

Pin Name	Setting	Description(as EN_XEN=0)
EN	High	ON(output)
	Low	OFF(no output)

"EXT_EN" is a register that enables or disables the EN pin.

Symbol	Initial Value	Setting	Description
EXT_EN	0	1	EN pin enabled
		0	EN pin disabled

"EN_XEN" is a register that reverses the logic of EN pin.

Symbol	Initial Value	Setting	Description
EN_XEN	0	1	Constant current driver is enabled in terminal EN=H
		0	Constant current driver is enabled in terminal EN=L.

Truth tabe of the constant current driver pin

I^2C register			EN pin	Constant current driver
XSTB	EXT_EN	EN_XEN		
0	*	*	*	OFF
1	1	1	High	ON
1	1	1	Low	OFF
1	1	0	High	OFF
1	1	0	Low	ON
1	0	*	*	ON

Note: "*" indicates that the selection dose not matter.

7.1.2 Current setting of constant current driver

The output current from each driver can be varied to 16 steps. The variable range is 0 to 25.9mA with a step of about 1.8mA.

In the ANIME mode, the redundancy bit is added to achieve a smooth current change in the animated illumination, and it changes into 128 steps.

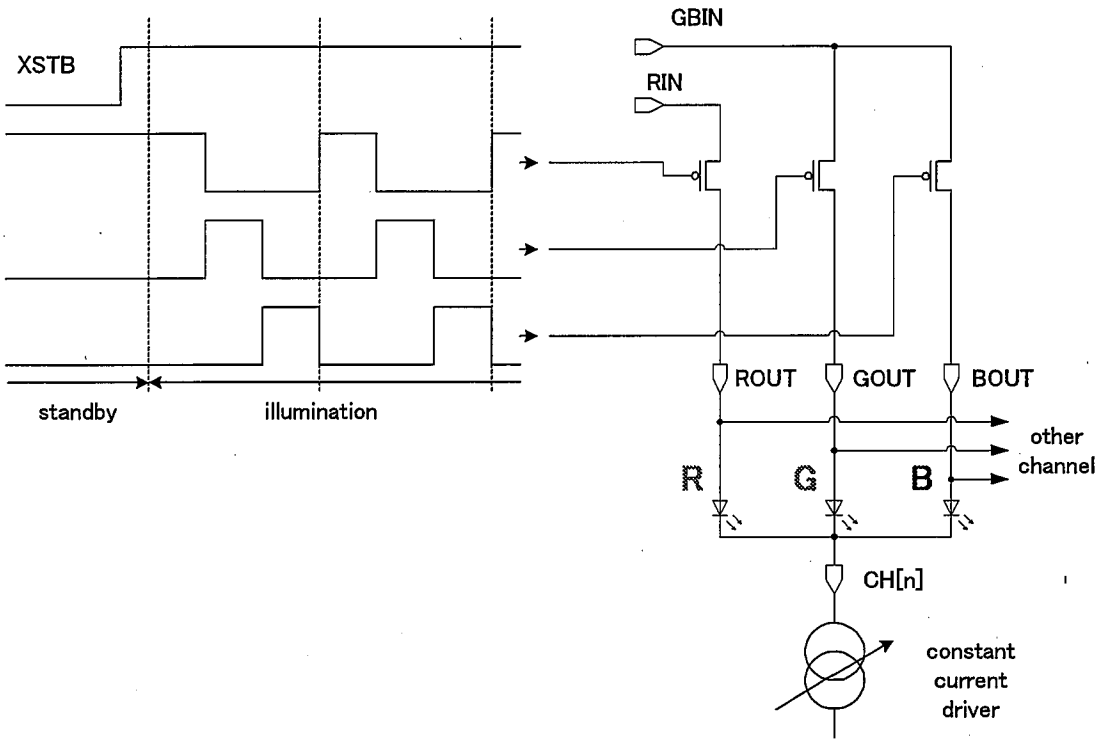
The starting point and the ending point of the animated illumination are set by 16 steps as well as the NORMAL mode and the BLINK mode.

CH[RGB][n][3:0] a register that sets the CH0,CH1,CH2,CH3,CH4 and CH5 pin current.

Symbol	Description	Setting			Inital Value	Value	Unit
		BINAA	DECCC	HEXXX			
CH[RGB][n][3:0]	Constant current driver output current	0000	0	00H	00H	0.0	mA
		0001	1	01H		1.9	
		0010	2	02H		3.6	
		0011	3	03H		5.4	
		0100	4	04H		7.1	
		0101	5	05H		8.8	
		0110	6	06H		10.5	
		0111	7	07H		12.2	
		1000	8	08H		13.9	
		1001	9	09H		15.6	
		1010	10	0AH		17.3	
		1011	11	0BH		19.0	
		1100	12	0CH		20.8	
		1101	13	0DH		22.5	
		1110	14	0EH		24.2	
		1111	15	0FH		25.9	

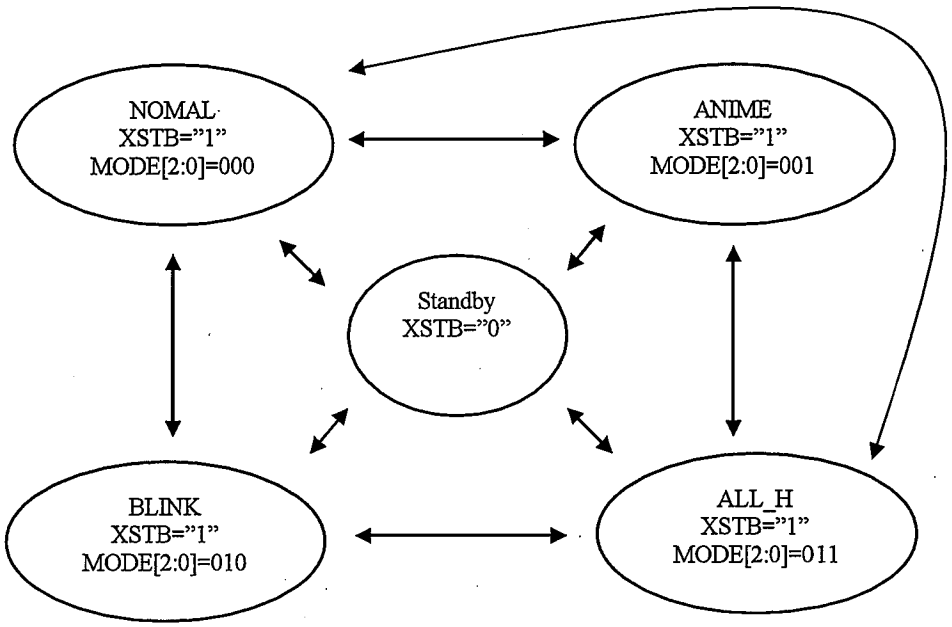
7.2 Column driver

Three column drivers are built into this IC. RGBLED for each one current driver or three single LED can be driven by timesharing by connecting the anode of LED with ROUT, GOUT, and BOUT. The column driver of ROUT is always turned on at the standby state.



7.3 Illumination mode select

This IC has 4 LED illumination mode, various illuminations can be displayed.
The illumination mode is selected from MODE[2:0] register.



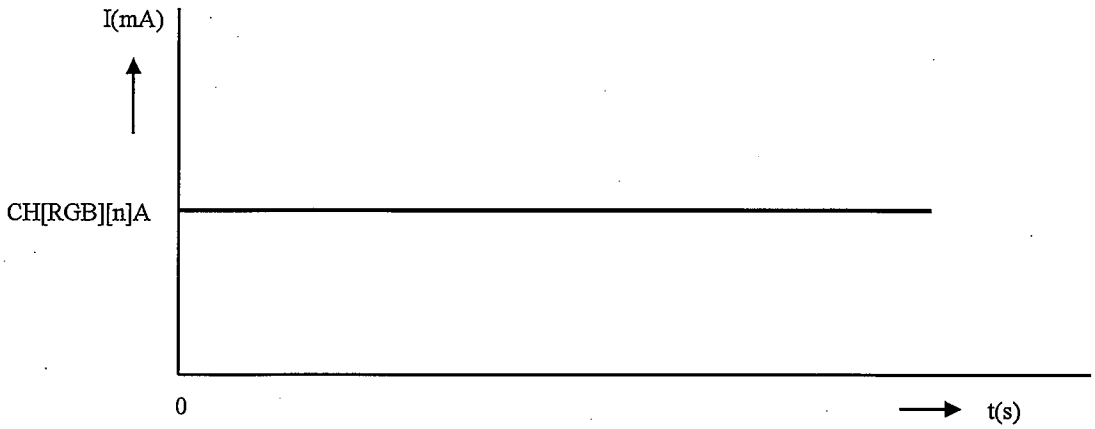
Note: The arrow is a mode that is possible to change.

MODE[2:0] a register that sets illumination mode. Do not set it from 100 to 111.

Symbol	Description	Setting			Initial Value	Value	Unit
		BIN	DEC	HEX			
MODE[2:0]	illumination mode	000	0	00H	00H	NOMAL	-
		001	1	01H		ANIME	
		010	2	02H		BLINK	
		011	3	03H		ALL_H	
		100	4	04H		inhibit	
		101	5	05H		inhibit	
		110	6	06H		inhibit	
		111	7	07H		inhibit	

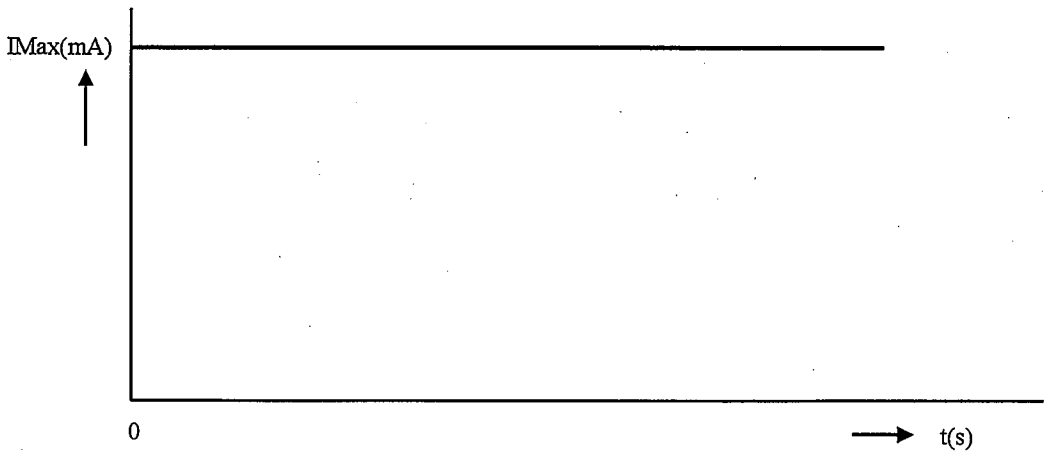
7.3.1 Normal mode

In Normal mode, current value written in CH[RGB][n]A register is outputted to the constant current driver.



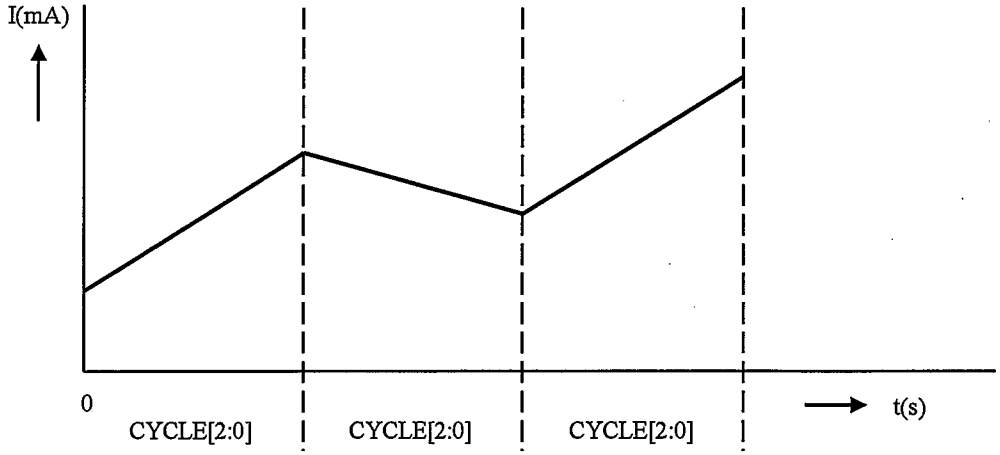
7.3.2 ALL_H mode

In ALL_H mode, MAX current value is output to all constant current driver.



7.3.3 ANIME mode

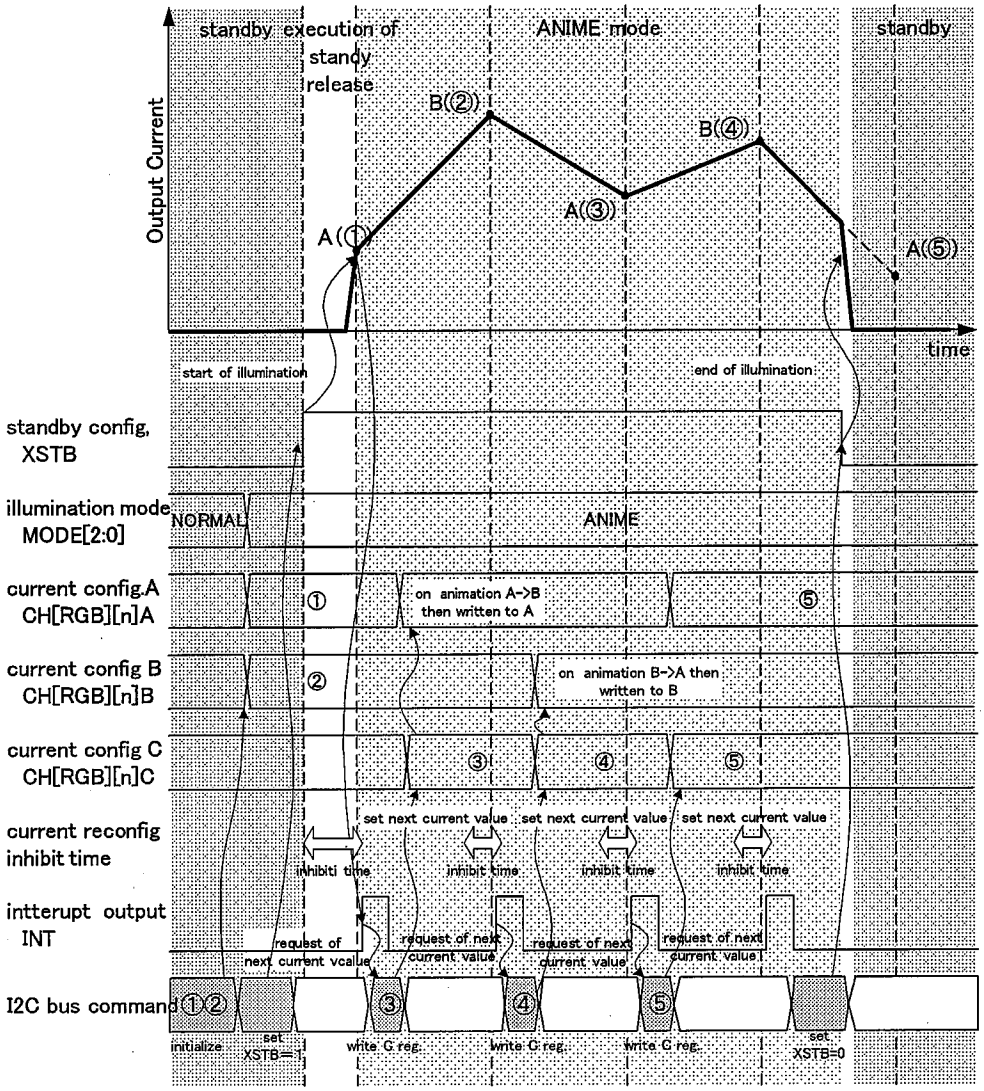
In ANIME mode, CH[RGB][n]A, CH[RGB][n]B, CH[RGB][n]A, and the current change gradually.
Timing to which the setting of the current of the driver is changed is time set with CYCLE[2:0].



CH[RGB][n]A1 → CH[RGB][n]B1 → CH[RGB][n]A2 → CH[RGB][n]B2

7.3.3.1 Basic operation on ANIME mode

In the ANIME mode, first of all, the current of the starting point and the following point is set to CH[RGB][n]A and CH[RGB][n]B. The current of the following respect is one by one set to CH[RGB][n]C register every cycle continuously set with CYCLE[3:0] register. The current in which LED is driven can be continuously changed by this operation.
When it becomes possible the setting of the following value, the INT signal is output, and this IC demands the setting from the host side.
The substance of CH[RGB][n]C register is either CH[RGB][n]A and CH[RGB][n]B. It is automatically allocated in the point of the next cycle while displaying it. Therefore, it is possible to set it consciously of a present display continuously.



7.3.3.2 ANIME mode Initialization

The following setting is necessary for the ANIME mode operation.

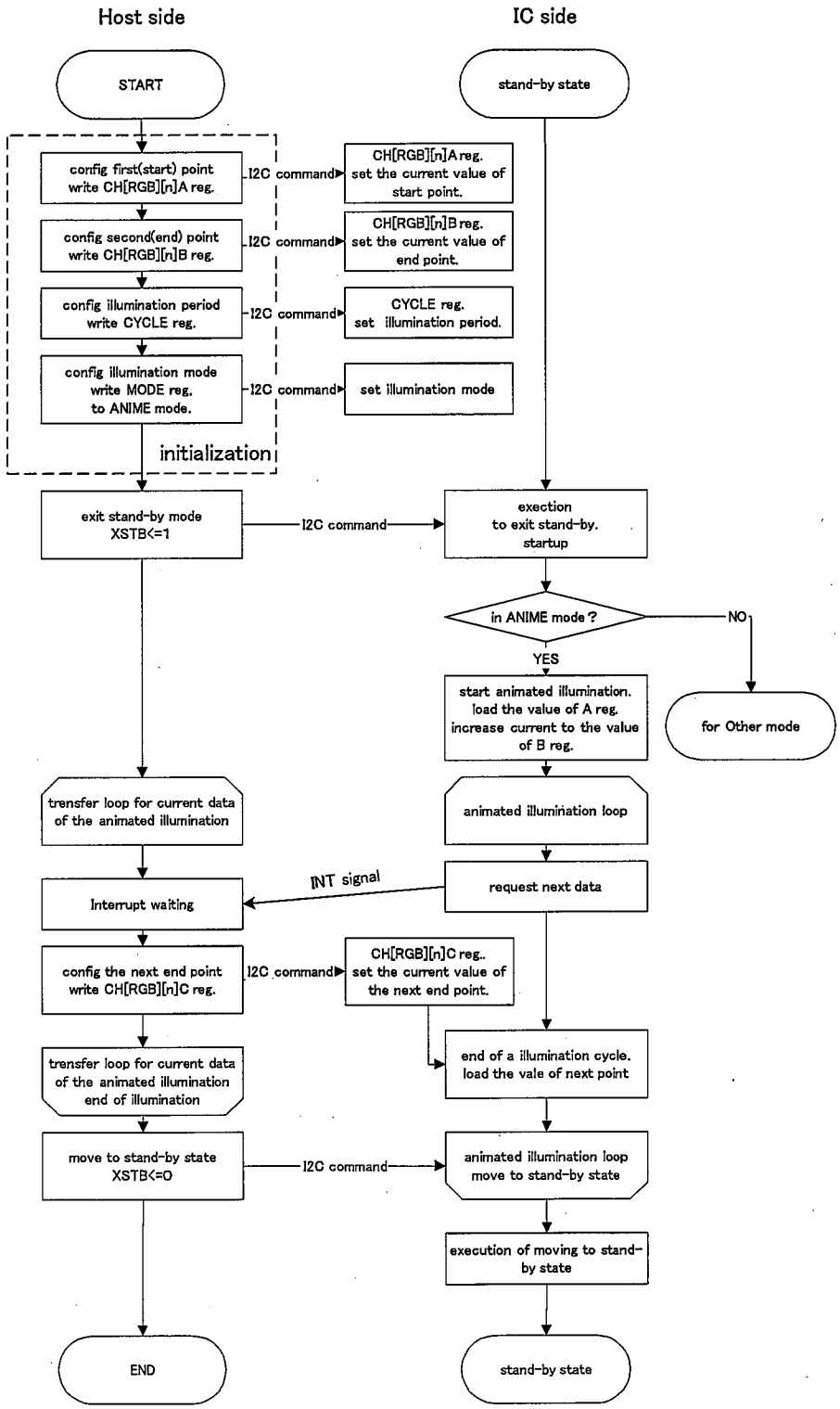
- MODE[2:0] Set ANIME mode [001].
- CYCLE[2:0] Set one illumination cycle period.
- CH[RGB][n]A Set the output current of the first illumination point.
- CH[RGB][n]B Set the output current of the second illumination point.
- XSTB This is the trigger to exit standby state. After the above-configuration is set, the standby is released when XSTB is assumed to be 1 and illumination is begun.

7.3.3.3 Animated Illumination Flow

The following setting is necessary to display animated illumination at each next data demand by the INT signal.

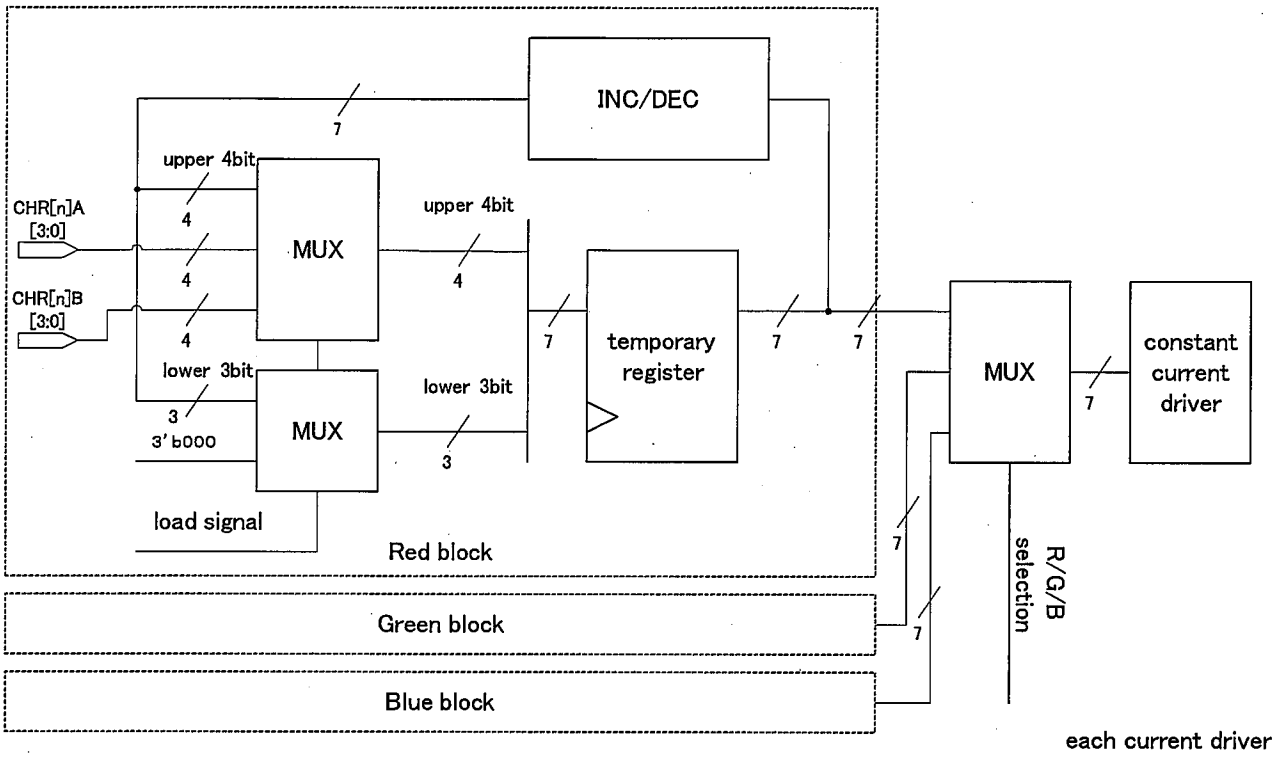
- CH[RGB][n]C set the output current value of the next end point of one display period

The example of the flow to one by one change the LED drive current by using the ANIME mode is shown as follows.



7.3.3.4 ANIME mode and Output Precision

In the ANIME mode, to achieve the illumination that changes smoothly, control logic circuit of animated illumination outputs current value by the redundancy bit addition and seven bit accuracy.



7.3.3.5 Limitations

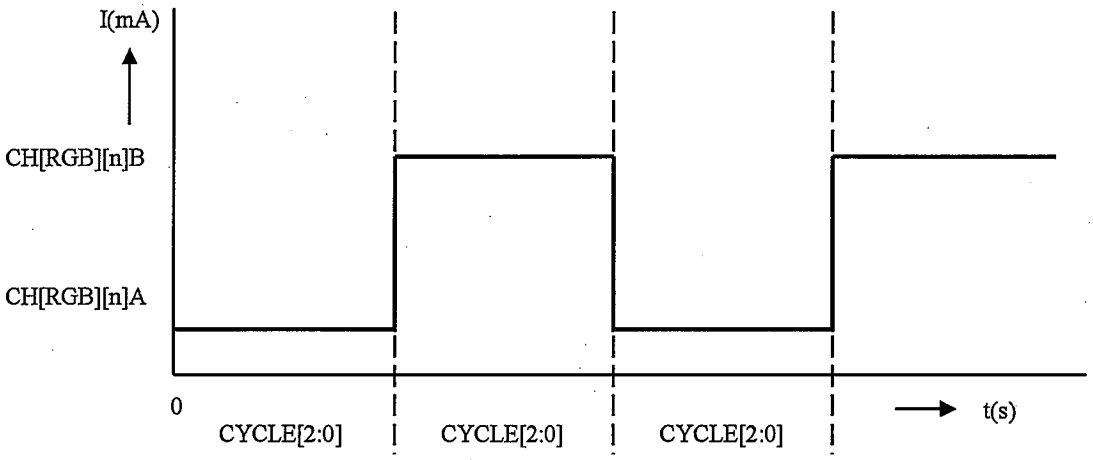
- Mode change under illumination
  The mode change between the ANIME mode and other modes under illumination is not recommended.
  Change in standby state.
  Behavior when the mode is changed in the illumination is as follows.

current mode	new mode	Behavior
ANIME,BLINK	NORMAL,ALL_H	Shift new mode immediately and output new value.
NORMAL,ALL_H	ANIME,BLINK	Start illumination from the CH[RGB][n]A value
ANIME	BLINK	The output at one CYCLE[1:0] period is not guaranteed from the change. The output returns to the normal performance at the next cycle.
BLINK	ANIME	

- Behavior when INT signal is output and CH[RGB][n]A, CH[RGB][n]B or CH[RGB][n]C are not replaced.
  The illumination is executed considering the previous value to be the following value when the CH[RGB][n]A, CH[RGB][n]B or CH[RGB][n]C register will not be updated in one illumination cycle after the INT signal is output.
- Setup/Hold time between INT signal and CH[RGB][n]A, CH[RGB][n]B and CH[RGB][n]C registers.
  It is necessary to keep to the time provided for according to the AC timing between the INT signal and the CH[RGB][n]A, CH[RGB][n]B and CH[RGB][n]C register.
  Do not update the CH[RGB][n]A, CH[RGB][n]B or CH[RGB][n]C register for the period from the standby release to positive edge of the first INT signal.
  When updating it outside timing, the SETUP/HOLD time cannot be defended, and the output might become irregular.

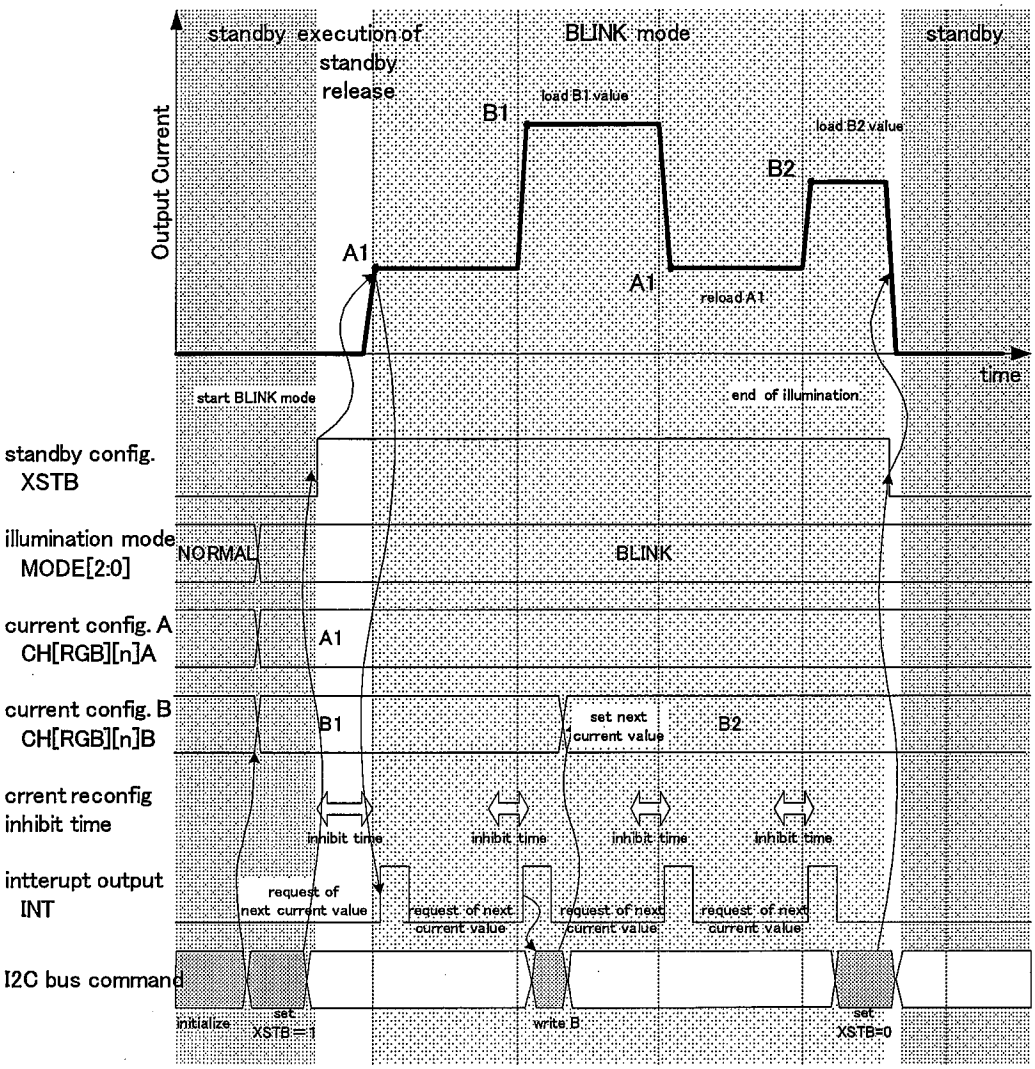
7.3.4 BLINK mode

In BLINK mode, CH[RGB][n]A and CH[RGB][n]B are alternately set to the constant current driver.
Timing to which the setting of the current of the driver is changed is time set with CYCLE[2:0]



7.3.4.1 Basic operation on BLINK mode

As for the BLINK mode, it is the same as the ANIME mode not interpolating linearly.
The output current value is updated every CYCLE[2:0] cycle if the value is set at each positive-edge of the INT signal.
The CH[RGB][n]A value and the CH[RGB][n]B value are repeatedly output every CYCLE[2:0] period if the register value is fixed.



7.4 Setting of the frequency of the RGB column drivers

The frequency of RGB column drivers can be set by the matrix of DOSC[1:0] and OSC[2:0]. The combination of the settings is as follows.

However, the oscillation frequency of the charge pump changes, too, when OSC[2:0] is changed. The value of OSC[2] doesn't influence the frequency of RGB column drivers.

"DOSC[2:0]" is a register that sets the oscillator frequency of column driver.

Symbol	Description	Setting			Initial Value	the frequency at each value of OSC[2:0] register				Compared with frequency	Unit
		BIN	DEC	HEX		*00	*01	*10	*11		
DOSC[1:0]	the frequency of the RGB column divers	00	0	00H	00H	1146	1016	859	694	1	Hz
		01	1	01H		2292	2031	1719	1389	2	
		10	2	02H		859	762	645	521	0.75	
		11	3	03H		1719	1523	1289	1042	1.5	

Note: "*" indicates that the selection dose not matter.

7.5 Setting of the period of a cycle of illumination

The cycle used at the ANIME mode and the BLINK mode can be set by the CYCLE[2:0] register.

"CYCLE[2:0]" is a register that sets the period of a cycle of illumination

Symbol	Description	Setting			Initial Value	time	the period at each value of DOSC[1:0] register when OSC[2:0] register is *00(BIN)				Unit
		BIN	DEC	HEX			00	01	10	11	
CYCLE[2:0]	the period of illumination cycle	000	0	00H	00H	128/DOSC	0.112	0.056	0.149	0.074	sec
		001	1	01H		256/DOSC	0.223	0.112	0.298	0.149	
		010	2	02H		512/DOSC	0.447	0.223	0.596	0.298	
		011	3	03H		1024/DOSC	0.894	0.447	1.192	0.596	
		100	4	04H		2048/DOSC	1.787	0.894	2.383	1.192	
		101	5	05H		4096/DOSC	3.575	1.787	4.766	2.383	
		110	6	06H		8192/DOSC	7.149	3.575	9.533	4.766	
		111	7	07H		16384/DOSC	14.299	7.149	19.065	9.533	

Note1: The illumination cycle changes at the same time, too, when the frequency of the column drivers is changed by the OSC[1:0] register and the DOSC[1:0] register.

Note2: "*" indicates that the selection dose not matter.

7.6 Configuration of BLINKHD

After the value of the CH[RGB][n]A register is loaded, the BLINK operation is held when changing to the BLINK mode after the BLINKHD register is set to one. The skew is generated at the update time of each current value because the setting of the current value is updated in the NORMAL mode at the time of each writing the register. However, if BLINKHD is used, the setting of all current value can be updated at the same time.

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Symbol	Initial Value	Setting	Description
BLINKHD	0	0	BLINK mode operation
		1	Hold after load the CH[RGB][n]A register value.

Concrete flow is as follows.

1. Release XSTB after set BLINKHD=1 and the BLINK mode.
2. Write the current value to CH[RGB][n]A register after wait time of release standby mode
3. Change to the NORMAL mode. The current setting is updated at the same time.
4. Change to the BLINK mode after wait time longer then 2*DOSC period.
5. Write the next current value to CH[RGB][n]A register after wait time longer then 2*DOSC period.
6. After arbitrary waiting time, go to 3.

※Please do not make it to the ANIME mode with BLINKHD set to 1. Operation when setting it is not guaranteed.

7.7 LED connected pin voltage monitoring and automatic select 1x or 1.5x charge pump mode

This IC monitors the voltage of all constant current driver pins. Charge pump boost ratio is selected automatically 1x mode in the minimum voltage is more than setting voltage, or 1.5x mode in the minimum voltage is less than setting voltage.

Charge and discharge cycle is 660 kHz (TYP.).

Oscillating frequency of charge pump can be changed by OSC[2:0] register.

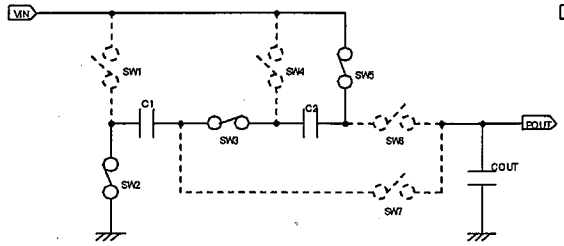


Fig.1 charge

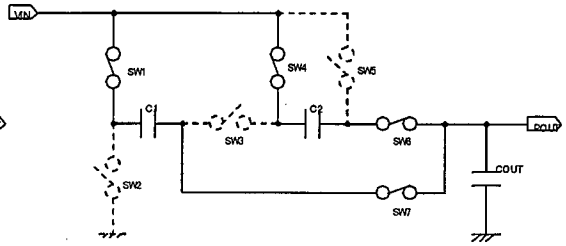


Fig.2 discharge

7.7.1 Oscillating frequency of charge pump

The register performs control of the oscillator frequency of charge pump.

Efficiency is optimized by changing the oscillation frequency of a charge pump.

When oscillation frequency is set up low, the efficiency of a charge pump increases, and output ripple becomes large.

When oscillation frequency is set up high, the efficiency of a charge pump falls, and output ripple becomes small.

When output ripple is large, the voltage monitoring function starts earlier than the case of output ripple is small, and changes 1x mode to 1.5x mode.

The adjustment of the oscillation frequency is effective to obtain the maximum efficiency.

Change OSC 2:0 register at the standby state.

"OSC[2:0]" is a register that sets the oscillator frequency of charge pump.

Symbol	Description	Setting			Initial Value	Value	Unit
		BIN	DEC	HEX			
OSC[2:0]	Oscillating frequency	000	0	00H	00H	660	kHz
		001	1	01H		585	
		010	2	02H		495	
		011	3	03H		400	
		100	4	04H		1320	
		101	5	05H		1170	
		110	6	06H		990	
		111	7	07H		800	

7.7.2 Slow start time of charge pump

This IC is provided a slow start circuit in the charge pump unit.
The register performs control of the slow start time of charge pump.
When slow start time is set up long, the rushes current decrease, and starting time becomes large.
When oscillation frequency is set up high, the rushes current increase, and starting time becomes short.

"SS[1:0]" is a register that sets the slow start time of charge pump.

Symbol	Description	Setting			Initial Value	Value	Unit
		BIN	DEC	HEX			
SS[1:0]	Slow start time	00	0	00H	00H	1.5	μs
		01	1	01H		3.0	
		10	2	02H		6.1	
		11	3	03H		12.2	

Note: The slow starting time changes with change of oscillation frequency.

7.8 GPO Interface

This IC has 4-port general purpose output (GPO) interface.
GPO interface usually operates at the standby state.
If reset enters, all registers are cleared to 0.
When "High" is output, the voltage at the VDD level is output from the GPO pin.

GPO0 is a register that sets the output data of the terminal GPO0.

Symbol	Initial Value	Setting	Description
GPO0	0	0	GPO0 pin Low
		1	GPO0 pin High

GPO1 is a register that sets the output data of the terminal GPO1.

Symbol	Initial Value	Setting	Description
GPO1	0	0	GPO1 pin Low
		1	GPO1 pin High

GPO2 is a register that sets the output data of the terminal GPO2.

Symbol	Initial Value	Setting	Description
GPO2	0	0	GPO2 pin Low
		1	GPO2 pin High

GPO3 is a register that sets the output data of the terminal GPO3.

Symbol	Initial Value	Setting	Description
GPO3	0	0	GPO3 pin Low
		1	GPO3 pin High

ABOUT is a register that does the setting that outputs the AB_XBA signal of an internal signal to the output terminal of the GPO2.
In ANIME mode, when the current of the driver has changed from CH[RGB][n]A to CH[RGB][n]B, AB_XBA outputs H. L is output when having changed from CH[RGB][n]B to CH[RGB][n]A.
Please adjust the GPO2 register to 0 when you use this function.

Symbol	Initial Value	Setting	Description
ABOUT	0	0	GPO2 normal operation
		1	GPO2 output AB_XBA signal

7.9 Standby state

This IC is provided a stand-by circuit. When it is ON, the standby state is activated.
In the standby state, all internal circuits are turned OFF.
The standby state is activated by setting the XSTB register to "0".

"XSTB" is a register that sets ON/OFF of the stand-by circuit.

Symbol	Initial Value	Setting	Description
XSTB	0	0	Stand-by circuit ON (standby state)
		1	Stand-by circuit OFF (standard state)

7.10 Reset circuit

This IC performs three types of reset sequences: software reset, hardware reset and power-on reset.

7.10.1 Software reset

Software reset is executed when "1" is written in the RESET register.
This IC returns from reset state by setting the RESET register to "0".

"RESET" is a register that initializes the internal register.

Symbol	Initial Value	Setting	Description
RESET	0	1	Register initialization
		0	Active

7.10.2 Power-on reset

This IC is provided a power-on reset circuit that initializes the register.
When the power is turned on, the register is automatically initialized.

7.10.3 Hardware reset

This IC has XRESET pin which initializes I^2C I/F and internal register.
When XRESET pin is set to "L", internal register is initialized and IC shifts standby state.
While XRESET pin is set to "L", I^2C input can't be received.
XRESET pin is pulled-up with 3.5kΩ (TYP) internal register.
Set XRESET pin to "OPEN" when you don't use hard reset function.

XRESET pin is an input terminal that initializes I^2C I/F and register.

Pin Name	Setting	Description
XRESET	H	Active
	L	I^2C I/F and register initialization

7.11 I²C-Bus interface

This IC operates as a slave on the I²C-Bus. At this time, the SCL line functions as the I²C clock input, and the SDA line as the bi-directional serial data bus.

This IC is also assigned with the 7-bit slave address in compliance with the I²C bus standard.

Higher 6 bits of the slave address are fixed internally. Lower 1bit is assigned to XA0 pin. If XA0 pin is GND then the lower 1bit is "1", else if XA0 pin is VDD then the lower 1bit is "0".

The low-pass filters are installed in the digital lines of both SCL and SDA in order to reduce the influence of bus noise.

These filters assure the higher communication reliability of this IC even in an environment that is exposed to noise. However, it is recommended to use the proper layout design.

The general call address is not supported.

7.11.1 Description of basic operations

This IC is provided a register used to set various operations.

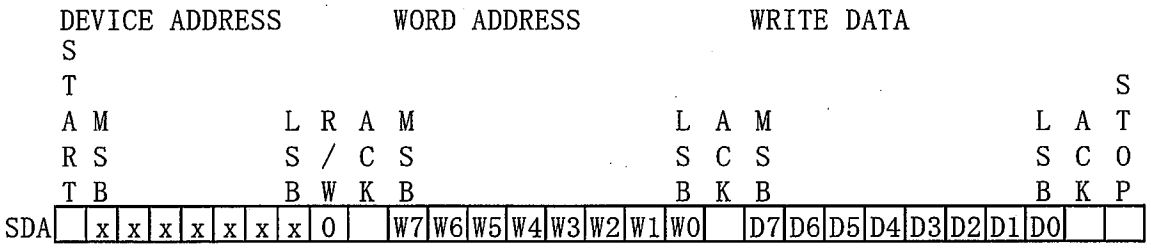
The register can be set with the I²C-Bus, and the pins used with the I²C-Bus are listed below

Pin Name	Description
SCL	I²C Clock
SDA	I²C Data Input/Output

7.11.2 Basic format

In this IC, 1 byte is composed of 8 bits. The first byte indicates the device address, the second byte indicates the word address, and the third byte indicates the write data.

I²C WRITE FORMAT



7.11.2.1 Device Address

The following matrixes show the slave address on the I²C-Bus.
A0 bit is assigned to negated XA0 port.

A6	A5	A4	A3
0	1	1	1

A2	A1	A0	W
0	1	!(XA0)	0

7.11.2.2 Address extension function

This IC can connect two device or less on same I2C-Bus. The least significant of slave address is assigned to XA0port. . If XA0 pin is GND then the least significant bit is “1”, else if XA0 pin is VDD then the least significant bit is “0”.

XA0 端子は I²C のスレーブアドレスの下位１ビットを設定する外部入力端子です。
XA0 port is the external input signal controlled the least significant of slave address.

Pin Name	Setting	Description
XA0	High	XA0=0 Device Address =74H
	Low	XA0=1 Device Address=76H

7.11.2.3 Word address

Five bits, W0, W1, W2, W3, W4 and W5, are used to select the address of the internal register.
W6 and W7 are the reservation bit for extension. These bits should be set to "0".

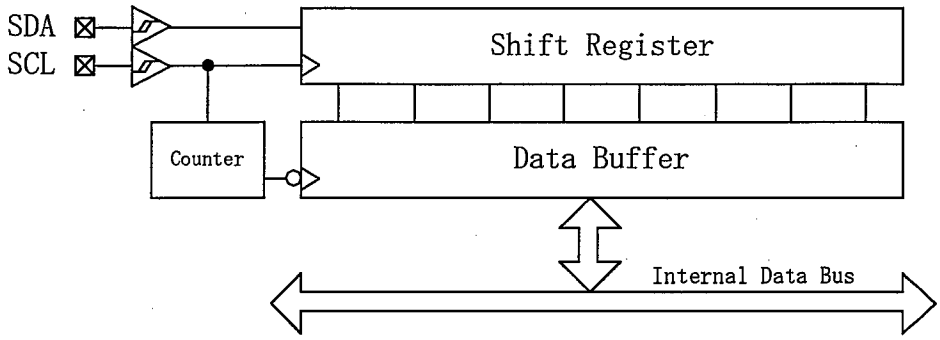
7.11.2.4 Write data

These data are written in the internal register.

7.11.2.5 Data write timing

The SDA data shifts on the rising edge of the SCL clock.

This data is transferred to the data buffer from the shift register at the falling edge of the eighth clock of SCL, and then written in the register.



7.11.3 Write format

The format written data in the register of this IC for the host is as follows. Address 00H is exclusively for output and cannot be written in.

START	DEVICE ADDRESS	0	ACK	WORD ADDRESS	ACK	WRITE DATA	ACK	STOP

7.11.4 Test register

This IC includes the registers for testing.

00H, 04H and 05H are registers for testing and banned writing.

7.11.5 Data output delay function

This IC is equipped timing delay circuit. Data output delay register "XDDELAY" changes the data output timing of ACK and READ DATA.

"XDDELAY" is a register that changes the data output timing of ACK and READ DATA.

Symbol	Initial Value	Setting	Description
XDDELAY	0	0	Delay circuit ON (300ns -1000ns)
		1	Delay circuit OFF

When you use I2C I/F by 3.4MHz (Hs-mode), set XDDELAY register to "1".

8. Register Map

Register

ADDRESS		SYMBOL	DATA								Initial Value
			D7	D6	D5	D4	D3	D2	D1	D0	
0	00H	TEST1									H'00
1	01H	START	RESET	XSTB		ABOUT	GPO3	GPO2	GPO1	GPO0	H'00
2	02H	LEDS	EXT_EN	EN_XEN	XDDELAY				DOSC[1]	DOSC[0]	H'00
3	03H	MODE		CYCLE[2]	CYCLE[1]	CYCLE[0]	BLINKHD	MODE[2]	MODE[1]	MODE[0]	H'00
4	04H	TEST2									H'00
5	05H	TEST3									H'00
6	06H	CP			SS[1]	SS[0]		OSC[2]	OSC[1]	OSC[0]	H'00
7	07H	CHR01A	CHR0A[3]	CHR0A[2]	CHR0A[1]	CHR0A[0]	CHR1A[3]	CHR1A[2]	CHR1A[1]	CHR1A[0]	H'00
8	08H	CHR23A	CHR2A[3]	CHR2A[2]	CHR2A[1]	CHR2A[0]	CHR3A[3]	CHR3A[2]	CHR3A[1]	CHR3A[0]	H'00
9	09H	CHR45A	CHR4A[3]	CHR4A[2]	CHR4A[1]	CHR4A[0]	CHR5A[3]	CHR5A[2]	CHR5A[1]	CHR5A[0]	H'00
10	0AH	CHG01A	CHG0A[3]	CHG0A[2]	CHG0A[1]	CHG0A[0]	CHG1A[3]	CHG1A[2]	CHG1A[1]	CHG1A[0]	H'00
11	0BH	CHG23A	CHG2A[3]	CHG2A[2]	CHG2A[1]	CHG2A[0]	CHG3A[3]	CHG3A[2]	CHG3A[1]	CHG3A[0]	H'00
12	0CH	CHG45A	CHG4A[3]	CHG4A[2]	CHG4A[1]	CHG4A[0]	CHG5A[3]	CHG5A[2]	CHG5A[1]	CHG5A[0]	H'00
13	0DH	CHB01A	CHB0A[3]	CHB0A[2]	CHB0A[1]	CHB0A[0]	CHB1A[3]	CHB1A[2]	CHB1A[1]	CHB1A[0]	H'00
14	0EH	CHB23A	CHB2A[3]	CHB2A[2]	CHB2A[1]	CHB2A[0]	CHB3A[3]	CHB3A[2]	CHB3A[1]	CHB3A[0]	H'00
15	0FH	CHB45A	CHB4A[3]	CHB4A[2]	CHB4A[1]	CHB4A[0]	CHB5A[3]	CHB5A[2]	CHB5A[1]	CHB5A[0]	H'00
16	10H										H'00
17	11H										H'00
18	12H										H'00
19	13H										H'00
20	14H										H'00
21	15H										H'00
22	16H										H'00
23	17H	CHR01B	CHR0B[3]	CHR0B[2]	CHR0B[1]	CHR0B[0]	CHR1B[3]	CHR1B[2]	CHR1B[1]	CHR1B[0]	H'00
24	18H	CHR23B	CHR2B[3]	CHR2B[2]	CHR2B[1]	CHR2B[0]	CHR3B[3]	CHR3B[2]	CHR3B[1]	CHR3B[0]	H'00
25	19H	CHR45B	CHR4B[3]	CHR4B[2]	CHR4B[1]	CHR4B[0]	CHR5B[3]	CHR5B[2]	CHR5B[1]	CHR5B[0]	H'00
26	1AH	CHG01B	CHG0B[3]	CHG0B[2]	CHG0B[1]	CHG0B[0]	CHG1B[3]	CHG1B[2]	CHG1B[1]	CHG1B[0]	H'00
27	1BH	CHG23B	CHG2B[3]	CHG2B[2]	CHG2B[1]	CHG2B[0]	CHG3B[3]	CHG3B[2]	CHG3B[1]	CHG3B[0]	H'00
28	1CH	CHG45B	CHG4B[3]	CHG4B[2]	CHG4B[1]	CHG4B[0]	CHG5B[3]	CHG5B[2]	CHG5B[1]	CHG5B[0]	H'00
29	1DH	CHB01B	CHB0B[3]	CHB0B[2]	CHB0B[1]	CHB0B[0]	CHB1B[3]	CHB1B[2]	CHB1B[1]	CHB1B[0]	H'00
30	1EH	CHB23B	CHB2B[3]	CHB2B[2]	CHB2B[1]	CHB2B[0]	CHB3B[3]	CHB3B[2]	CHB3B[1]	CHB3B[0]	H'00
31	1FH	CHB45B	CHB4B[3]	CHB4B[2]	CHB4B[1]	CHB4B[0]	CHB5B[3]	CHB5B[2]	CHB5B[1]	CHB5B[0]	H'00
32	20H										H'00
33	21H										H'00
34	22H										H'00
35	23H										H'00
36	24H										H'00
37	25H										H'00
38	26H										H'00
39	27H	CHR01C	CHR0C[3]	CHR0C[2]	CHR0C[1]	CHR0C[0]	CHR1C[3]	CHR1C[2]	CHR1C[1]	CHR1C[0]	H'00
40	28H	CHR23C	CHR2C[3]	CHR2C[2]	CHR2C[1]	CHR2C[0]	CHR3C[3]	CHR3C[2]	CHR3C[1]	CHR3C[0]	H'00
41	29H	CHR45C	CHR4C[3]	CHR4C[2]	CHR4C[1]	CHR4C[0]	CHR5C[3]	CHR5C[2]	CHR5C[1]	CHR5C[0]	H'00
42	2AH	CHG01C	CHG0C[3]	CHG0C[2]	CHG0C[1]	CHG0C[0]	CHG1C[3]	CHG1C[2]	CHG1C[1]	CHG1C[0]	H'00
43	2CH	CHG23C	CHG2C[3]	CHG2C[2]	CHG2C[1]	CHG2C[0]	CHG3C[3]	CHG3C[2]	CHG3C[1]	CHG3C[0]	H'00
44	2CH	CHG45C	CHG4C[3]	CHG4C[2]	CHG4C[1]	CHG4C[0]	CHG5C[3]	CHG5C[2]	CHG5C[1]	CHG5C[0]	H'00
45	2DH	CHB01C	CHB0C[3]	CHB0C[2]	CHB0C[1]	CHB0C[0]	CHB1C[3]	CHB1C[2]	CHB1C[1]	CHB1C[0]	H'00
46	2EH	CHB23C	CHB2C[3]	CHB2C[2]	CHB2C[1]	CHB2C[0]	CHB3C[3]	CHB3C[2]	CHB3C[1]	CHB3C[0]	H'00
47	2FH	CHB45C	CHB4C[3]	CHB4C[2]	CHB4C[1]	CHB4C[0]	CHB5C[3]	CHB5C[2]	CHB5C[1]	CHB5C[0]	H'00

Note 1: ☒ resistor is banned writing "1". Be sure to use "0".

9. Pin Function

9.1 VIN pin、VCC pin、VDD pin

VIN pin, VCC pin are power supply terminals.
The applicable voltage of VIN is from 3.0 to 4.5V.
The applicable voltage of VCC is lower than VIN (2.3 to 3.2V).
Apply the same voltage of VDD as the one on the Pull-Up side of the I^2C-Bus.

9.2 IREF pin

IREF pin sets the reference current of the internal circuit.
The resistance (13kΩ± 1%) should be connected between the IREF pin and GND pin

9.3 EN pin

EN pin is an enable input terminal for CH0~CH5 pins.
When this function is not used, this pin should be set to "L".

9.4 CH0 pin, CH1 pin, CH2 pin, CH3 pin, CH4 pin, CH5 pin

CH0, CH1, CH2, CH3, CH4 and CH5 pins are constant current driver terminals.
When these pin are not used, these pins should be connected to VCC.

9.5 ROUT pin, GOUT pin, BOUT pin

ROUT, GOUT, and BOUT pins are column driver terminals.
On standby, only ROUT is enabled.

9.6 GPO0 pin, GPO1 pin, GPO2 pin, GPO3 pin

GPO0, GPO1, GPO2, and GPO3 pins are general purpose output (GPO) terminals.
All pins output "High" or "Low" according to the value of I2C registers.

9.7 INT pin

When data is demanded from HOST, the "High" pulse is output.

9.8 SDA pin, SCL pin

SCL pin is the clock terminal of I2C interface. SDA pin is the data input terminal of I2C interface.
SDA pin has output open-drain transistor for ACK signal.

10. Cautions

- Connect the ground pins (CGND, GND, PGND) with the shortest distance and set pins same potential.
- It is recommended to install a capacitor between the power supply terminal and grounding terminal.
- Position a bypass capacitor between the power supply terminal and grounding pin close to the IC.
- Position a flying capacitor between the C1N-C1P pin and C2N-C2P pin close to the IC to reduce line resistance. To reduce the line resistance and ESR (serial resistance of flying capacitor) makes drop voltage small and conversion efficiency improvement when charge pump is boost-up.
- Position a smoothing capacitor between CPO and GND pin close to the IC to reduce line resistance. To reduce the line resistance and ESR (serial resistance of smoothing capacitor) makes drop voltage small and conversion efficiency improvement when charge pump is boost-up.
- Don't apply voltage CPO pin.
- Don't set input terminals (EN pin) floating.
- Supply input terminals (EN pin) with input voltage range specified electric characteristics.
- Don't supply voltage or current to output terminals (GPO0,GPO1,GPO2,GPO3,INT) from the outside of terminals.
- Use patterns as broad as and as short as possible for the power supply lines and grounding lines.
- In any case, use input voltage within the limits of maximum applied voltage.
- Position the IREF pin close to the IC to circumvent the effect of noise.
- Connect constant current driver terminal to VCC when LED is unconnected. Other constant current driver terminals should connect LED between ROUT, GOOT and BOUT terminals.
- Don't put in strong light against IC when you use this IC.
- It is recommended to reset IC after setting VCC to "High".
- Connect neither terminal RIN nor terminal GBIN excluding terminal VIN or terminal CPO.

11.Absolute Maximum Ratings

parameter	Symbol	定格値	Unit	備考
Power supply VIN	VIN	5.5	V	
Power supply VCC	VCC	5.5	V	VCC≦VIN
Power supply VDD	VDD	-0.3V～VCC+0.3	V	VDD≦VCC
Terminal voltage1	Vin1	-0.3V～VDD+0.3	V	input pin : EN,XA0, XRESET
Terminal voltage2	Vin2	-0.3V～VDD+0.3	V	input pin : SCL,SDA
CPO output current	ICPO	220	mA	Total drive current
Output current	ILED	35/ch	mA	Each drive pin current
Power dissipation	Pd	1660	mW	Ta≦25℃ Note 1
Derating ratio	ΔPd	16.6	mW/℃	Ta>25℃ Note 1
Operating temperature range	Topr	-20～85	℃	
Storage temperature range	Tstg	-55～125	℃	

Note 1: Free convection, on-board, compiled with SEMI42-996

12. Recommended Operating Condition

Parameter	Symbol	Value	Unit	Conditions
Power supply VIN	VIN	3.0～4.5	V	
Power supply VCC	VCC	2.3～3.2	V	
Power supply VDD	VDD	1.8～VCC	V	
Oscillating frequency	fOSC	660	kHz	RIREF=13kΩ
I^2C communication frequency	fCLK	400	kHz	

13.Electric Characteristics

See the Block Diagram unless otherwise specified.
VIN=3.6V, VCC=2.5V, VDD=1.8V, Ta=25℃, RIREF=13kΩ
The current direction is regarded positive when entering the IC and negative when exiting.

Current consumption

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
Stand-by supply current	ISS1	XSTB="0"	-	0	3	μA
VIN Supply current	IIN1	VIN=4.2V,CPO output: 1x mode CPO output: No load current	-	0.17	0.32	mA
VCC Supply current	ICC1	VCC=2.5V	-	0.7	1.5	mA
VDD Supply current	IVDD1	VDD=1.8V	-	0	3	μA

Voltage reference circuit

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
IREF Pin voltage	VREF	RIREF=13kΩ		480		mV

Constant current driver circuit.

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
Output current (CH0pin、CH1pin、CH2pin、CH3pin、CH4pin、CH5pin)	ICH(F)	NORMAL mode CH[RGB][n]A:0FH	23.3	25.9	28.5	mA
	ICH(C)	NORMAL mode CH[RGB][n]A:0CH	18.7	20.8	22.8	mA
	ICH(6)	NORMAL mode CH[RGB][n]A:06H	9.4	10.5	11.5	mA
	ICH(0)	NORMAL mode CH[RGB][n]A:00H	-	0. 00	0.01	mA
LED drive pin Constant current1	ΔLED1	Voltage of current output pin: 0.35V~1.3V NORMAL mode CH[RGB][n]A:06H	-	±1	±5	%
LED drive pin Constant current2	ΔLED2	Voltage of current output pin: 0.35V~1.3V NORMAL mode CH[RGB][n]A:0FH	-	±1	±5	%

Charge pump circuit

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
CPO output inpedance1	ZCPO1	VIN=4V, CP at 1x mode ZCPO1=(VIN-VCPO)/Iout		1.2		Ω
CPO output inpedance2	ZCPO2	VIN=3V, CP at 1.5x mode ZCPO2=(1.5×VIN-VCPO)/Iout		3.1		Ω
Oscillating frequency0	fOSC0cp	Address 06H:00H(Initial value)	500	660	820	kHz

SDA pin, SCL pin, XA0 pin, EN pin, XRESET pin

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
High level input voltage	VIH		0.7VDD	-	VDD	V
Low level input voltage	VIL		0	-	0.3VDD	V
High level input current	IIH		-1	-	1	μA
Low level input current	IIL		-1	-	1	μA
Hysteresis voltage	Vhys			0.05VDD		V
SDA output pin voltage	VOL	IOL=3mA	-	-	0.2VDD	V
Reset pulse width	PW_{RE}	XRESET of the period of "Low"	10			μs

GPO0 pin, GPO1 pin, GPO2 pin, GPO3 pin

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	Unit
High level output voltage	VOH	IOH= -1mA	0.8VDD	-	-	V
Low level output voltage	VOL	IOL= 1mA	-	-	0.2VDD	V

INT pin

Parameter	Symbol	Measure condition	MIN.	TYP.	MAX.	unit
High level output voltage	VOH	IOH= -1mA	0.8VDD	-	-	V
Low level output voltage	VOL	IOL= 1mA	-	-	0.2VDD	V

14. I²C-BUS Interface timing characteristics

All specified output timings are based on 20% and 80% of VDD.

Fs-mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCL clock frequency	fS_{CL}		0	-	400	kHz
Hold time(repeated) START condition	tHD;STA		600	-	-	ns
LOW period of the SCL clock	tLOW		1300	-	-	ns
HIGH period of the SCL clock	tHIGH		600	-	-	ns
Data set-up time	tSU;DAT		100	-	-	ns
Data hold time	tHD;DAT		0	-	-	ns
SCL and SDA rise time	tr	Note 1.	20+0.1Cb	-	-	ns
SCL and SDA fall time	tf	Note 1.	20+0.1Cb	-	-	ns
Capacitive load represented by each bus line	Cb		-	-	400	pF
Set-up time for STOP condition	tSU;STO		600	-	-	ns
Tolerable spike width on bus	tSP		-	-	50	ns
Bus free time between START and STOP condition	tBUF		1300	-	-	ns
Noise margin at the LOW level for each connected device (including hysteresis)	VnL		0.1×VDD	-	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	VnH		0.2×VDD	-	-	V

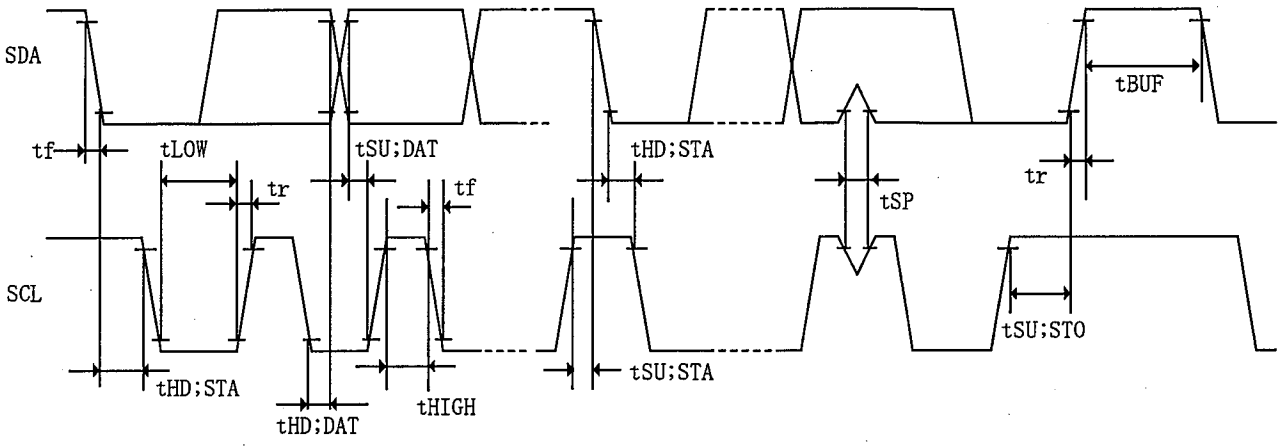
Hs-mode

SCLH clock frequency	fS_{CLH}		0	-	3.4	MHz
Set-up time(repeated) START condition	tSU;STA		160	-	-	ns
Hold time(repeated) START condition	tHD;STA		160	-	-	ns
LOW period of the SCLH clock	tLOW		160	-	-	ns
HIGH period of the SCLH clock	tHIGH		60	-	-	ns
Data set-up time	tSU;DAT		10	-	-	ns
Data hold time	tHD;DAT		20	-	70	ns
Rise time of the SCLH signal	trCL		10	-	-	ns
Rise time of the SCLH signal after the acknowledge bit	trCL1		10	-	-	ns
Fall time of the SCLH signal	tfCL		10	-	-	ns
Rise time of the SDAH signal	trDA		10	-	-	ns
Fall time of the SCLH signal	tfCL1		10	-	-	ns
Set-up time for STOP condition	tSU;STO		160	-	-	ns
Capacitive load for the SDAH and SCLH lines	Cb2		-	-	100	pF
Capacitive load for the SDAH and SCLH lines	Cb		-	-	400	pF
Tolerable spike width on bus	tSP		-	-	5	ns
Noise margin at the LOW level for each connected device (including hysteresis)	VnL		0.1×VDD	-	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	VnH		0.2×VDD	-	-	V

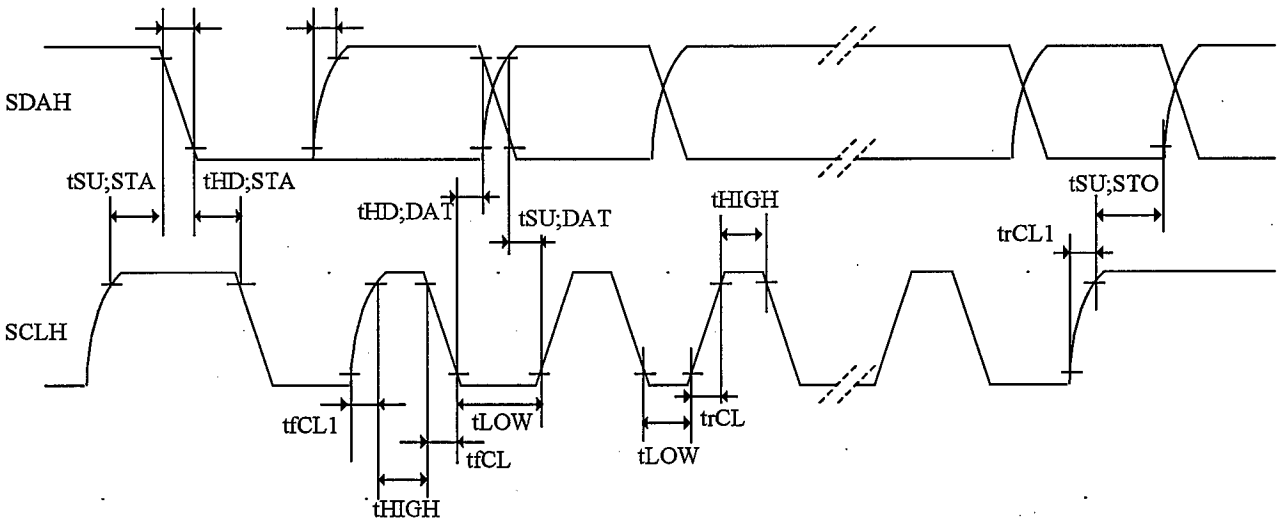
Note 1: Cb=100pF total capacitance of one bus line.

14.1 I²C-Bus timing diagram

14.1.1 I²C-Bus timing diagram (Fs-mode)



14.1.2 I²C-Bus timing diagram (Hs-mode)

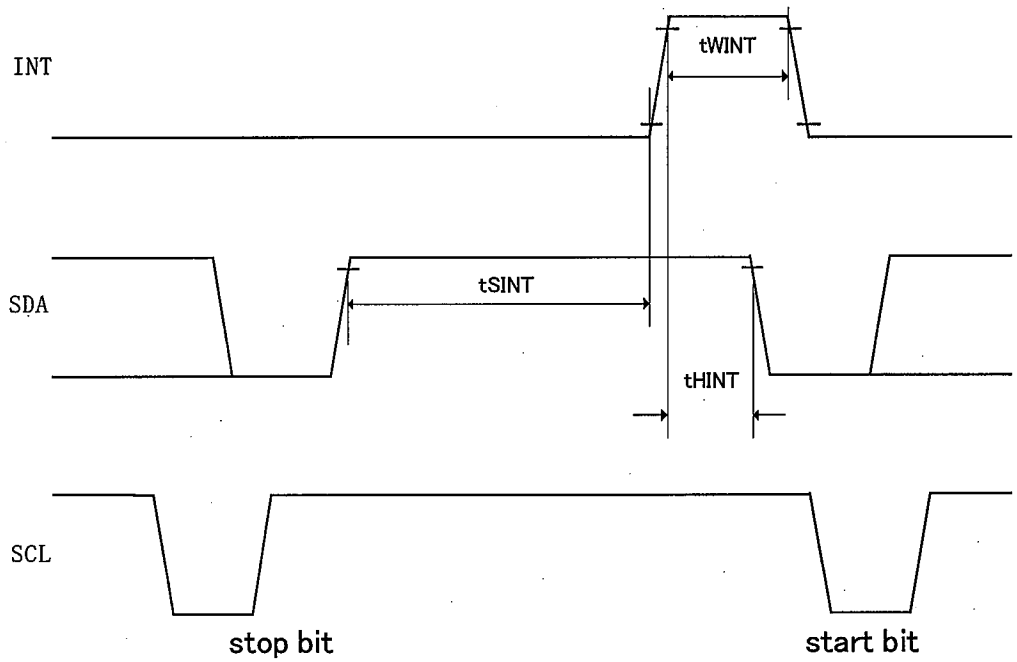


15.INT signal timing characteristics

All specified output timings are based on 20% and 80% of VDD

Parameter	Symbol	measure condition	MIN.	TYP.	MAX.	unit
INT siglnal output width	tWINT		10	-	-	ms
Setup time from I2C stop condition to rising edge.of INT signal.	tSINT		4	-	-	ms
Hold time from rising edge of INT signal to I2C start condition.	tHINT		0	-	-	ns

15.1 **INT signal timig chart**



16 Package and packing specification

Reference

[Applicability]

This specification applies to an IC package of the LEAD-FREE delivered as a standard specification.

1.Storage Conditions.

1-1.Storage conditions required before opening the dry packing.

- Normal temperature : 5～40℃
- Normal humidity : 80% (Relative humidity) max.
- Storage period : One year max.

*"Humidity" means "Relative humidity"

1-2.Storage conditions required after opening the dry packing.

In order to prevent moisture absorption after opening, ensure the following storage conditions apply:

(1) Storage conditions for one-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

(2) Storage conditions for two-time soldering. (Convection reflow*1, IR/Convection reflow.*1)

a. Storage conditions following opening and prior to performing the 1st reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after opening.

b. Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow.

- Temperature : 5～25℃
- Humidity : 60% max.
- Period : 96 hours max. after completion of the 1st reflow.

*1:Air or nitrogen environment.

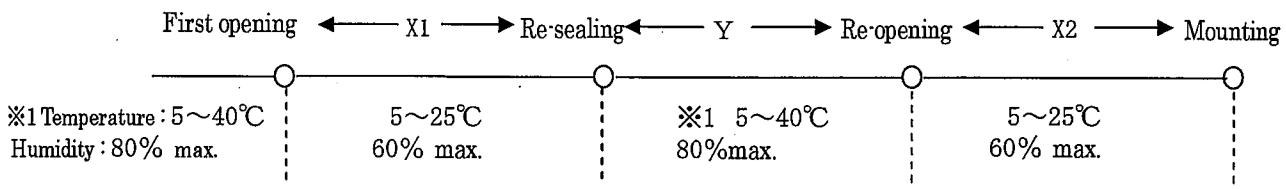
1-3.Temporary storage after opening.

To re-store the devices before soldering, do so only once and use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using heat-sealing.

The storage period, temperature and humidity must be as follows :

(1) Storage temperature and humidity.

※1 : External atmosphere temperature and humidity of the dry packing.



(2) Storage period.

- X1+X2 : Refer to Section 1-2(1) and (2)a , depending on the mounting method.
- Y : Two weeks max.

Reference

2. Baking Condition.

(1) Situations requiring baking before mounting.

- Storage conditions exceed the limits specified in Section 1-2 or 1-3.
- Humidity indicator in the desiccant was already red (pink) when opened.
  (Also for re-opening.)

(2) Recommended baking conditions.

- Baking temperature and period : 120+5/-0℃ for 3～4 hours.
- The above baking conditions apply since the embossed carrier tape are heat-resistant.

(3) Storage after baking.

- After baking, store the devices in the environment specified in Section 1-2 and mount immediately.

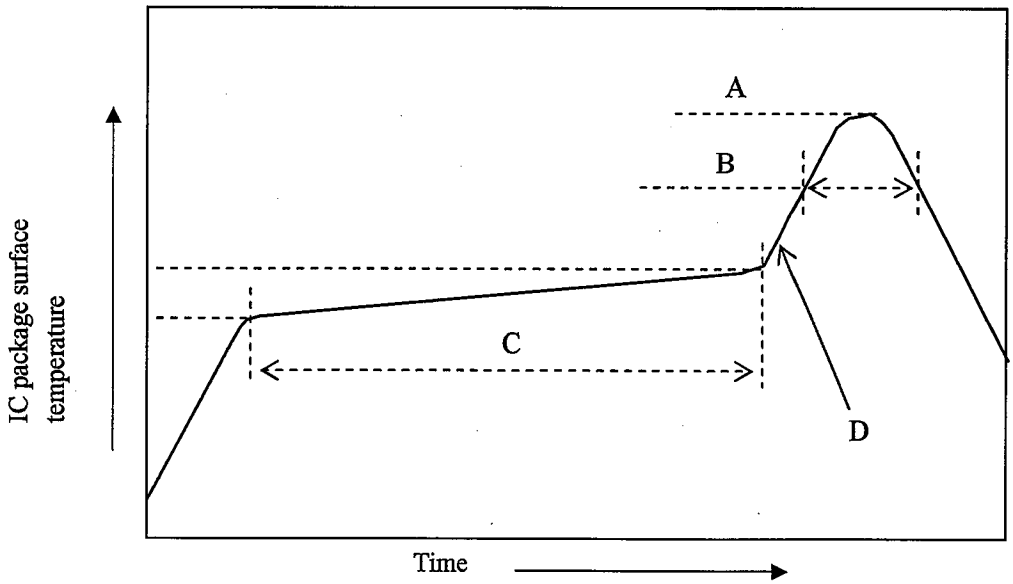
3. Surface mount conditions.

The following soldering conditions are recommended to ensure device quality.

3-1.Soldering.

(1) Convection reflow or IR/Convection reflow. (one-time soldering or two-time soldering in air or nitrogen environment)

- Temperature and period :
  - A) Peak temperature. 250℃ max.
  - B) Heating temperature. 40 to 60 seconds as 220℃
  - C) Preheat temperature. It is 150 to 200℃, and is 120±30 seconds
  - D) Temperature increase rate. It is 1 to 3℃/seconds
- Measuring point : IC package surface.
- Temperature profile :



3-2.Recommended heating condition for repair.

Pre heating : 100℃ or more within 90 sec. from room temperature to 90±30 sec.
Reflow heating : within ten sec. at a temperature of 250℃ to 260℃
(Please confirm not only melting solder of the repair area but also the back of the PCB.)

※Use of an "Under-fill"
Since the external terminals are arranged at intervals of 0.5mm, SHARP recommends use of appropriate "Under fill" to this product for high reliability.

Reference

4. Condition for removal of residual flux.
   (1) Washing method : dipping in the appropriate solvent and generating the circular flow (preferable)
   (2) Washing time : It depends on the solvent performance.
   (3) Solvent temperature : It depends on the solvent performance.

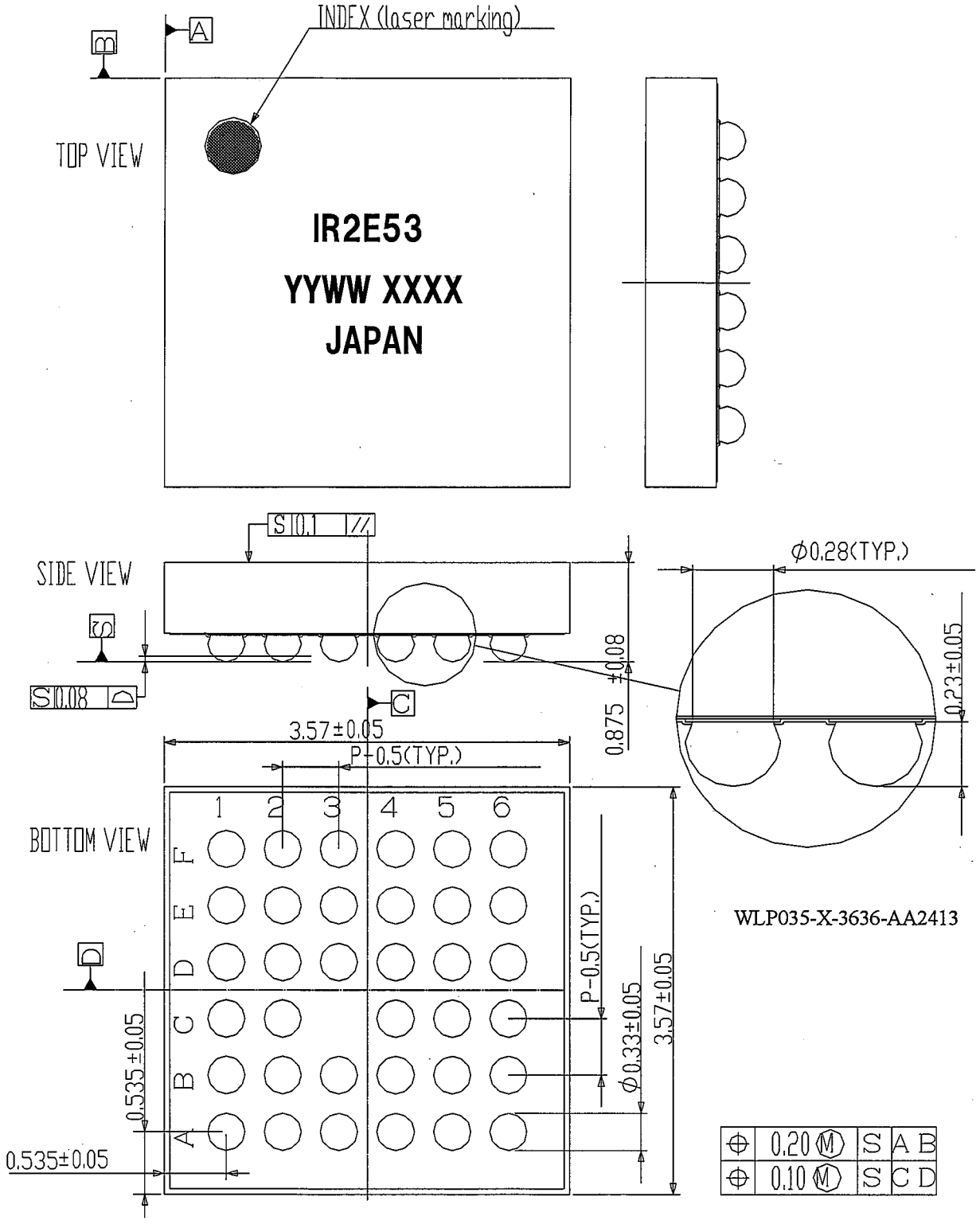
5. Package outline specification.
   5-1. Package outline.
   Refer to the attached drawing.
   (Body dimensions do not include burr of resin.)
   5-2. LEAD FINISH or BALL TYPE
   LEAD FREE TYPE (Sn-3Ag-0.5Cu) ※Use of an "Under-fill"
   5-3. Package weight.
   0.03g/pcs. About.

6. Markings.
   6-1.Marking details. (The information on the package should be given as follows.)
   (1) Product name : IR2E53
   (2) Date code : (Example) YYWW XXXX
   YY → Denotes the production year. (Last two digits of the year.)
   WW → Denotes the production week. (01・02・～・52・53)
   XXXX → Denotes the production ref. code.
   (3) "JAPAN" indicates the country of origin.

   6-2.Marking layout.
   The layout is shown in the attached drawing.
   (However, this layout does not specify the size of the marking character and marking position.)

Reference

(Note)It is those with an underline printing in a date code because of ~ LEAD FREE type.



NAME	WLP035-X-3636			BALL TYPE
DRAWING NO.	AA2413	UNIT	mm	Sn-3Ag-0.5Cu
NOTE	Body dimensions do not include burr of resin. ※Use of an "Under-fill": Since the external terminals are arranged at intervals of 0.5mm, SHARP recommends use of appropriate "Under fill" to this product for high reliability.			

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Reference

7.Packing specifications (Embossed carrier tape specifications)

This standard applies to the embossed carrier tape specifications for ICs supplied by SHARP CORPORATION. SHARP's embossed carrier tape specifications are generally based on those described in JIS C 0806 (Japanese Industrial Standard) and EIA481A.

7-1.Tape structure

The embossed carrier tape is made of conductive plastic. The embossed portions of the carrier tape are filled with IC packages and a top covering tape is used to enclose them.

7-2.Taping reel and embossed carrier tape size

For the taping reel and embossed carrier tape sizes, refer to the attached drawing.

7-3.IC package enclosure direction in embossed carrier tape

The IC package enclosure direction in the embossed portion relative to the direction in which the tape is pulled is indicated by an index mark on the package (indicating the No. 1 pin) shown in the attached drawing.

7-4.Missing IC packages in embossed carrier tape

The number of missing IC packages in the embossed carrier tape per reel should not exceed either 1 or 0.1 % of the total contained on the tape per reel, whichever is larger. There should never be more than two consecutive missing IC packages.

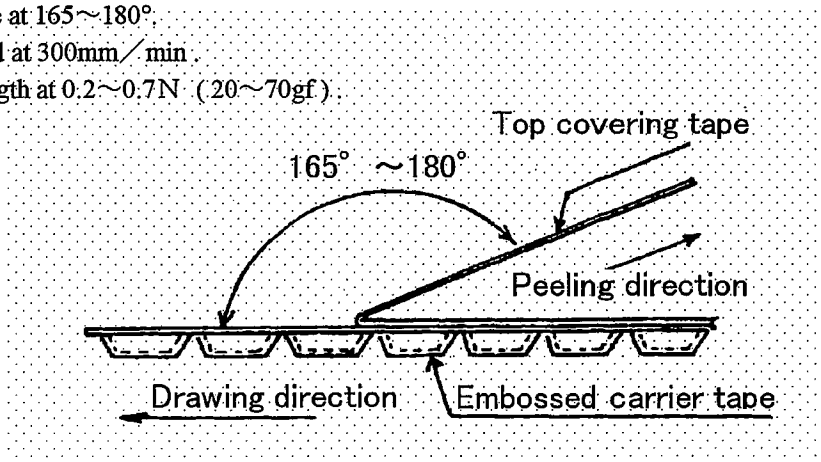
7-5.Tape joints

There is no joint in an embossed carrier tape.

7-6.Peeling strength of the top covering tape

Peeling strength must meet the following conditions.

(1) Peeling angle at 165~180°.
(2) Peeling speed at 300mm/min.
(3) Peeling strength at 0.2~0.7N (20~70gf).



7-7. Packing

(1) The top covering tape (leader side) at the leading edge of the embossed carrier tape, and the trailing edge of the embossed carrier tape, should both be held in place with paper adhesive tape at least 30 mm in length.
(2) The leading and trailing edges of the embossed carrier tape should be left empty (with embossed portions not filled with IC packages) in the attached drawing.
(3) The number of IC packages enclosed in the embossed carrier tape per reel should generally comply with the list given below.

Number of IC Packages/ Reel	Number of IC Packages/ Inner carton	Number of IC Packages/ Outer carton
2000 devices / Reel	2000 devices / Inner carton	10000 devices / Outer carton

Reference

7-8.Indications

The following should be indicated on the taping reel and the packing carton.

・Part Number (Product Name) ・Storage Quantity ・Packed Date

・Manufacture's Name (SHARP)

Note : The IC taping direction is indicated by " EL " suffixed to the part number .

EL : Equivalent to " L " of the JIS C 0806 standard..

7-9.Protection during transportation

The IC packages should have no deformation and deterioration of their electrical characteristics resulting from transportation.

8.Precautions for use.

(1) Please prevent a chemical and physical damage at the package handling.
Please do not put the stress which damages the terminal part and circuit formation side of external connection especially.

(2) When opening the packing, please prepare the antistatic work stand and a human body should also work under static-stopper state.
Moreover, when dealing with a package, please ground a human body, an equipment, a work stand, and equipment electrically not to occur a static electricity.

(3) When a package is mounted, it is required to use suitable assembly technology so that a electric, thermal and mechanical property can be maintained.

(4) Please use a device within one year of the date of delivery.

(5) As for chip off of device, width 0.2mm Max.Or length 1.0mm Max.Or depth 0.2mm Max. It does not exist.

9.Chemical substance information in the product.

Product Information Notification based on Chinese law, Management Methods for Controlling Pollution by Electronic Information Products.

Names and Contents of the Toxic and Hazardous Substances or Elements in the Product

Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (Cr(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)
○	○	○	○	○	○

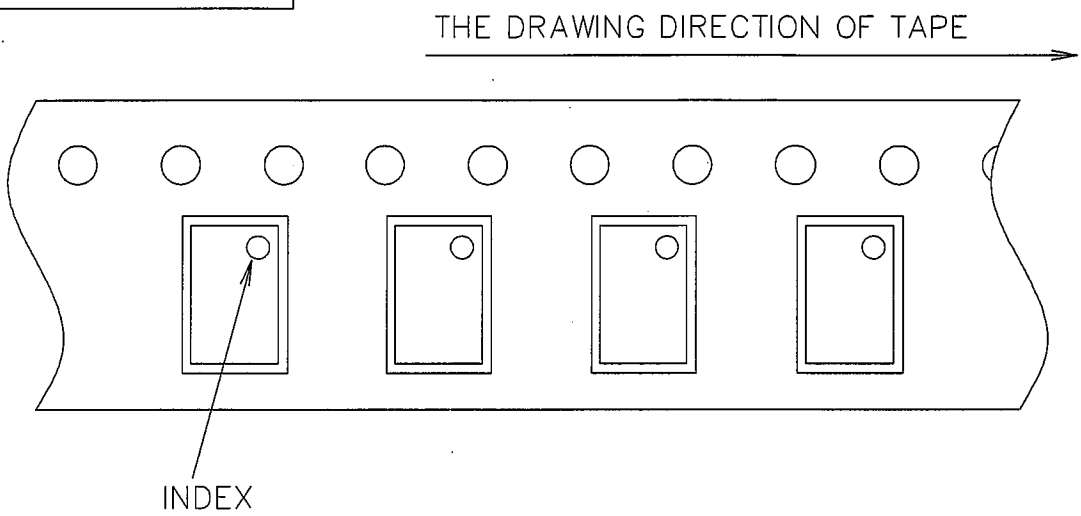
○ : indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.

× : indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006 standard.

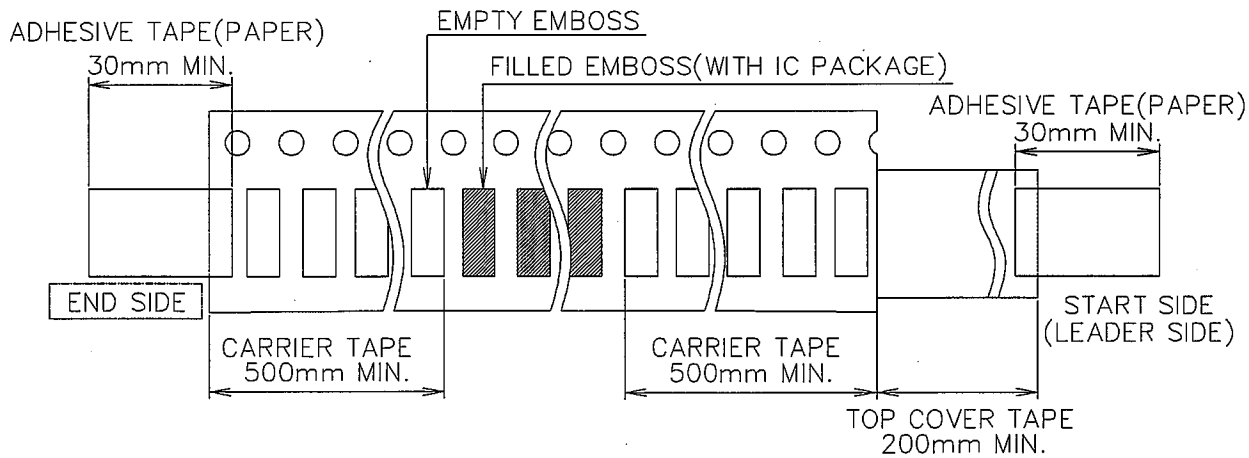
Reference

EMBOSS TAPING TYPE (EL)

IC TAPING DIRECTION



LEADER SIDE AND END SIDE OF TAPE



名称 NAME	Emboss taping type(EL)			備考 NOTE
DRAWING NO.	CV522	単位 UNIT	mm	

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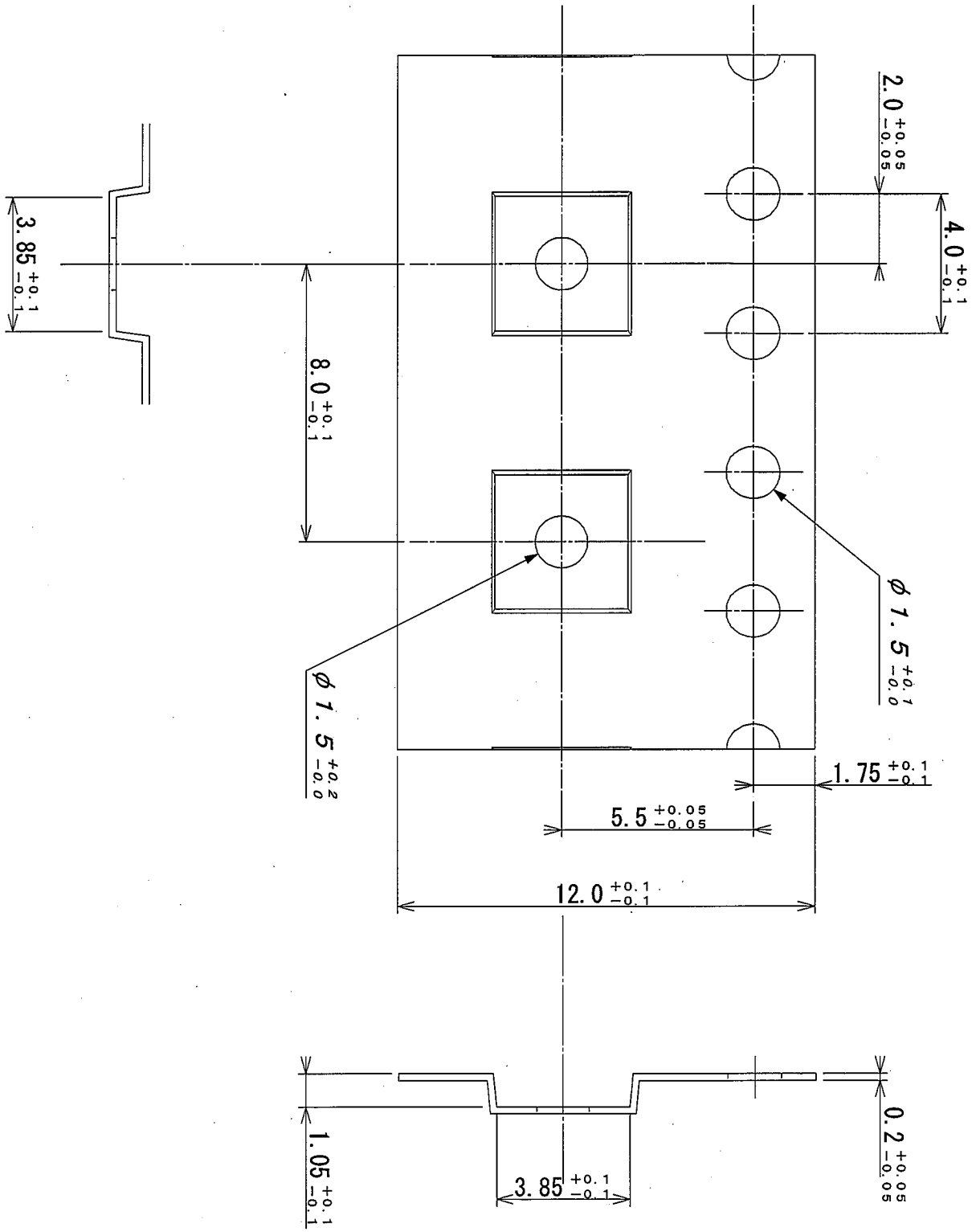
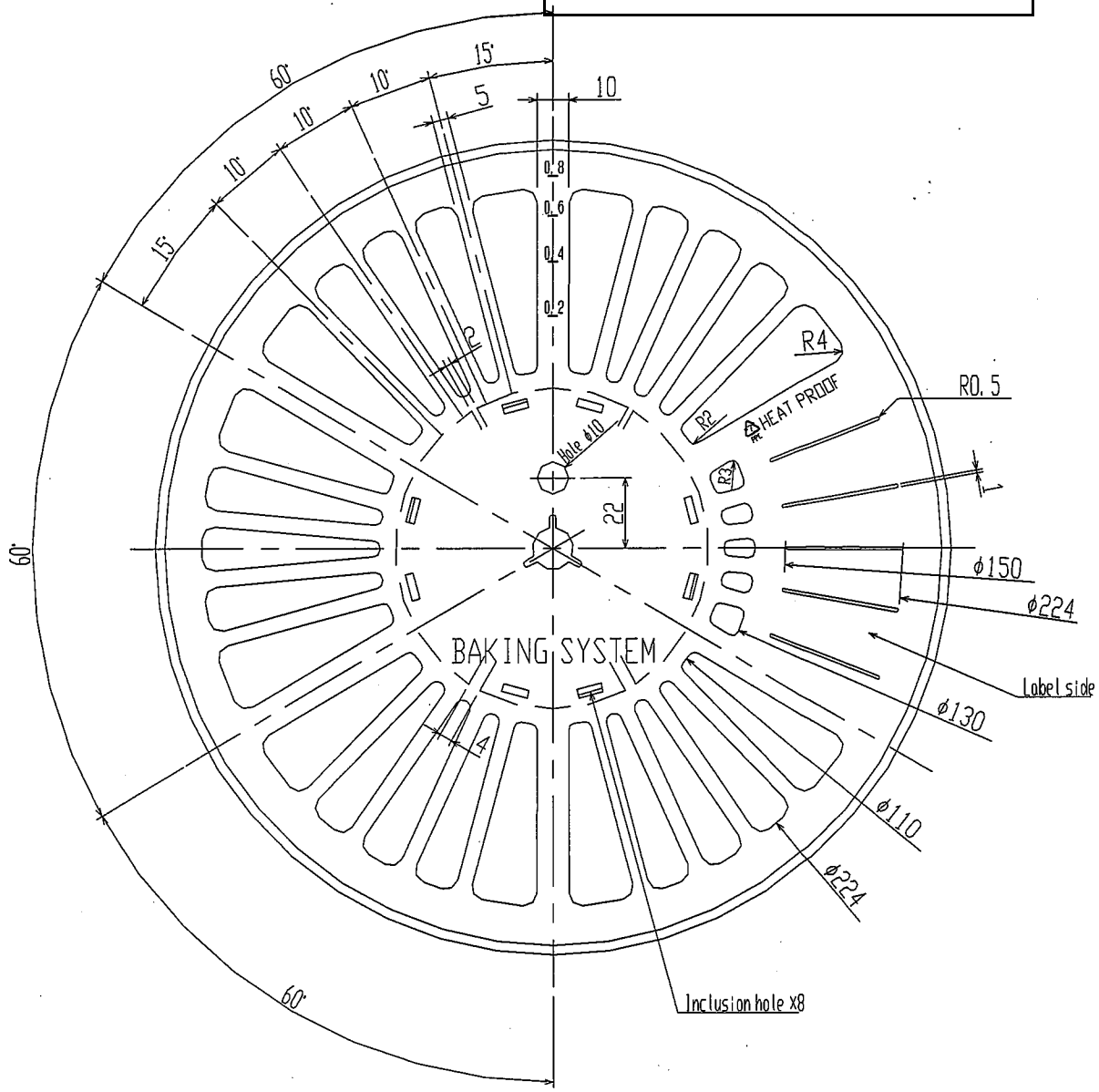
Reference

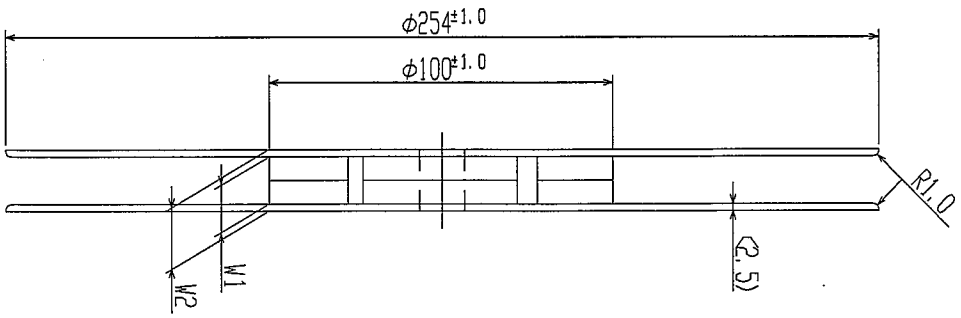


名称 NAME	SEC033-3636CPOM-RH	備考 NOTE
DRAWING NO. CV1020	単位 UNIT mm	

20070807

Reference



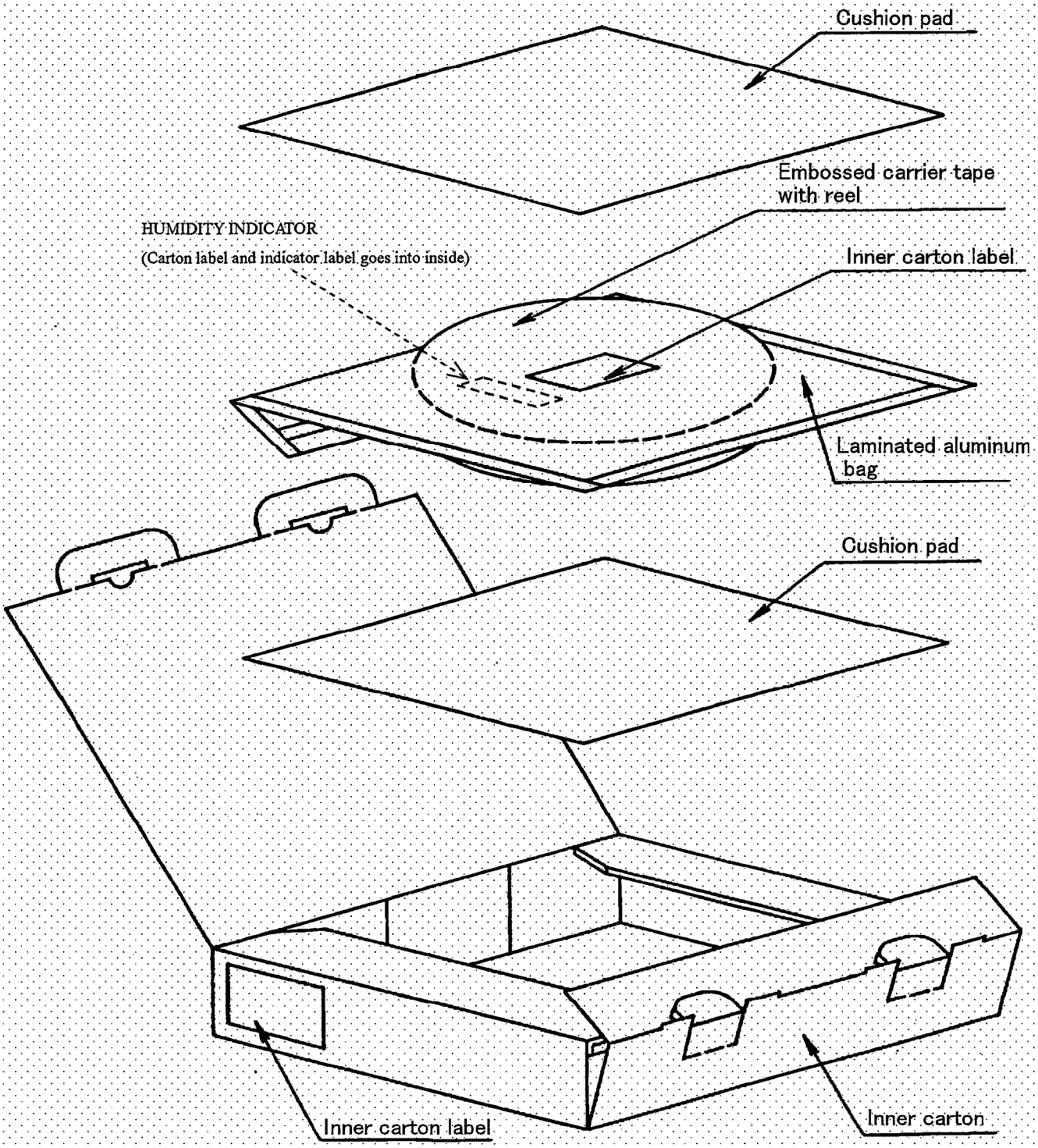


TAPE SIZE	W1	W2
12mm	13.5±1.0	18.5±1.0

名称 NAME	Reel for embossed carrier tape			備考 NOTE
DRAWING NO.	250	単位 UNIT	mm	

20070807

Reference

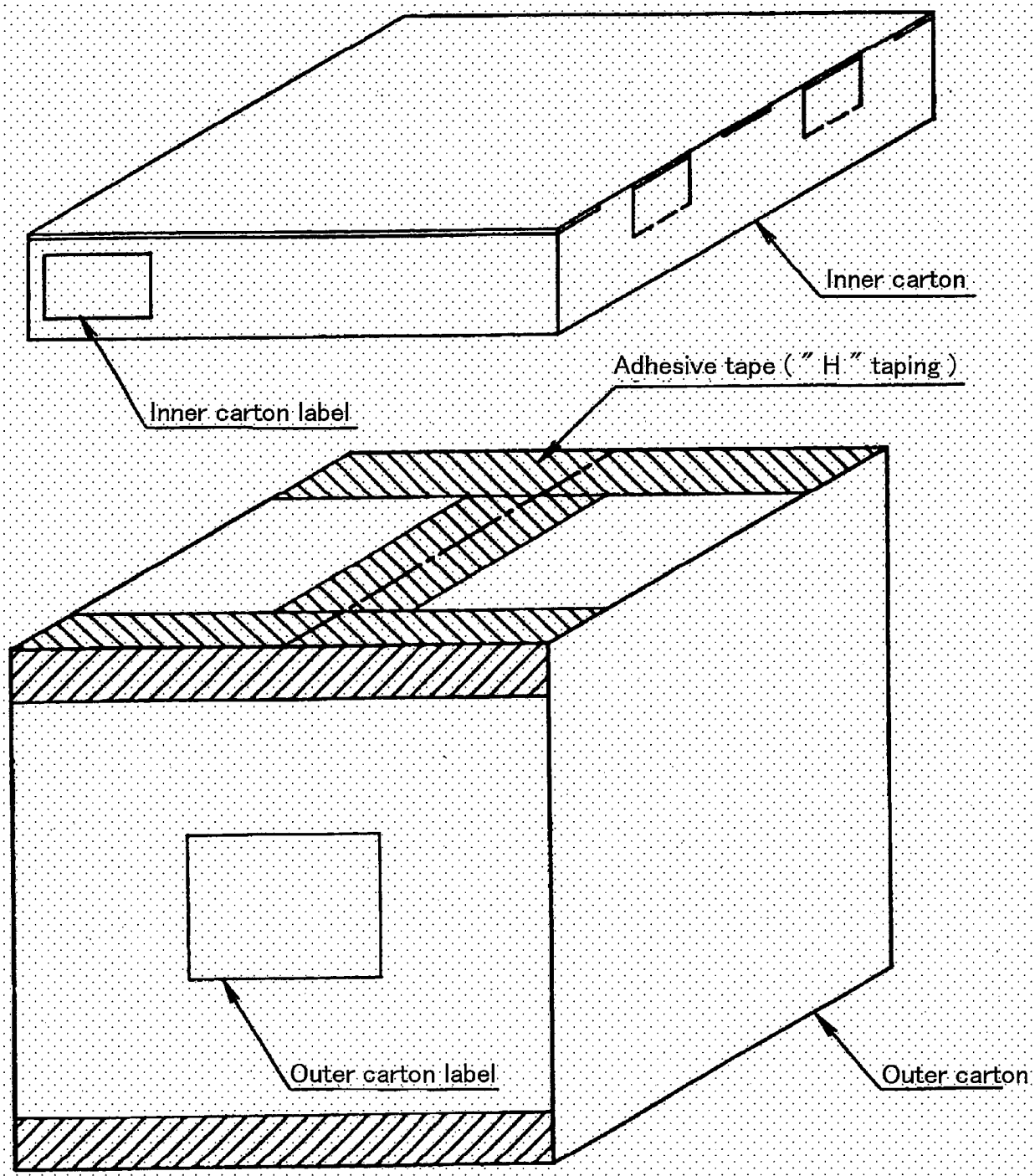


	L		W		H
Inner carton - Outer dimensions : :	345	×	345	×	55

名称 NAME	Packing specifications《1》		備考 NOTE
DRAWING NO.	CV428	単位 UNIT	mm

20070807

Reference



	L		W		H
Inner carton - Outer dimensions :	345	×	345	×	55
Outer carton - Outer dimensions :	365	×	315	×	385

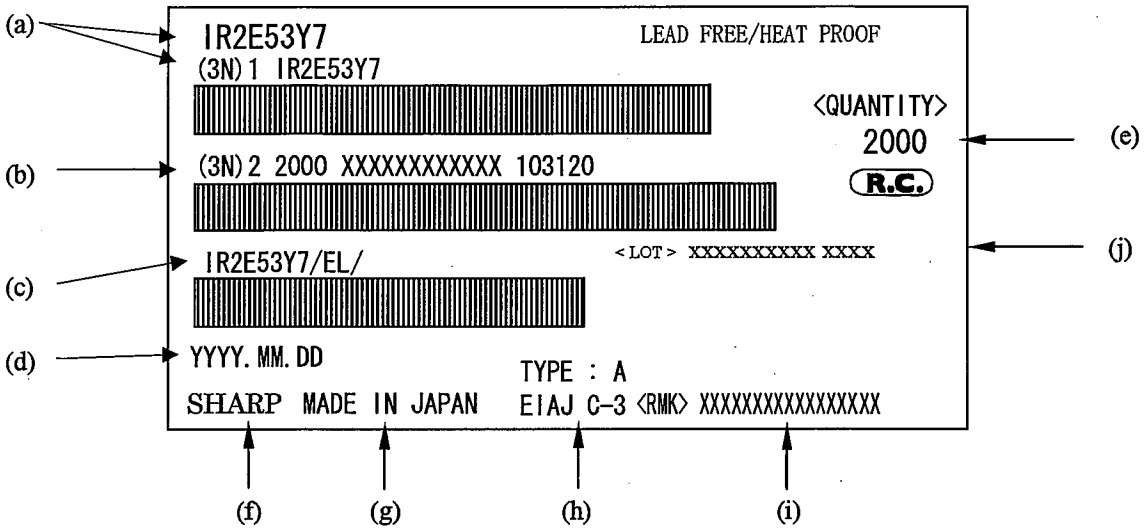
名称 NAME	Packing specifications 《2》		備考 出荷数量が端数の場合、本仕様と異なることがあります。 NOTE There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ426	単位 UNIT	mm

20070807

Reference

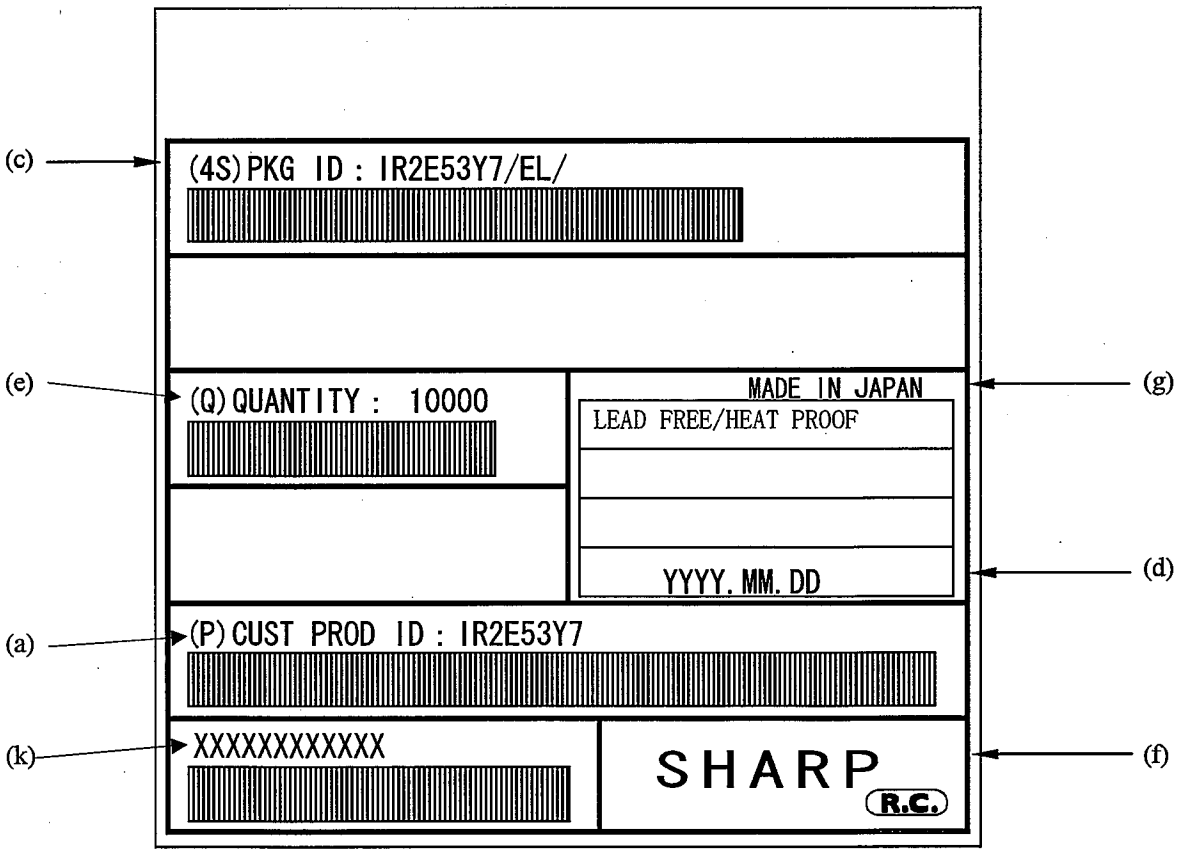
(Note) The << LEAD FREE >> display shows a lead free article.
"R.C." is Sharp's corporate logo indicating that the product is RoHS compliant.

Inner carton label



Outer carton label

(Former) EIAJ B Standard conforming



(a) Product name
(b) Quantity PD lot Company code
(c) Part No. (SHARP)
(d) Packed date
(e) Quantity
(f) "SHARP" Logo
(g) The country of origin
(h) Type name (Conformity standard)
(i) Sharp management No.
(j) Sharp control No.
(k) Shipment lot