TEXAS INSTRUMENTS

SN74LVC2GU04-Q1
SCES902 – SEPTEMBER 2019

SN74LVC2GU04-Q1 Dual Unbuffered Inverter

1 Features

- AEC-Q100 Qualified for automotive applications:
  - Device temperature grade 1: –40°C to +125°C, T_A
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Max t_{pd} of 3.7 ns at 3.3 V
- Low power consumption, 10-µA max I_{CC}
- ±24-mA Output drive at 3.3 V
- Typical V_{OLP} (output ground bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Can be used as a down translator to translate inputs from a max of 5.5 V down to the V_{CC} level
- Unbuffered outputs

2 Applications

- AV receivers
- Blu-ray players and home theaters
- DVD recorders and players
- Desktop or notebook PCs
- Digital radio or internet radio players
- Digital video cameras (DVC)
- Embedded PCs
- GPS: Personal navigation devices
- Mobile internet devices
- Network projector front-ends
- Portable media players
- Pro audio mixers
- Smoke detectors
- Solid-state drive (SSD): enterprise
- High-definition (HDTV)
- Tablets: enterprise
- Audio docks: portable
- DLP front projection systems
- DVR and DVS
- Digital picture frame (DPF)
- Digital still cameras

3 Description

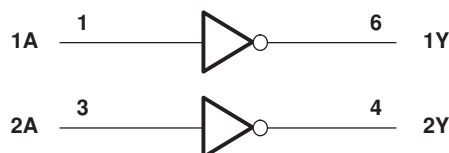This dual inverter is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2GU04-Q1 device contains two inverters with unbuffered outputs and performs the Boolean function $Y = \overline{A}$.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2GU04QDRYRQ1	SON (6)	1.45 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
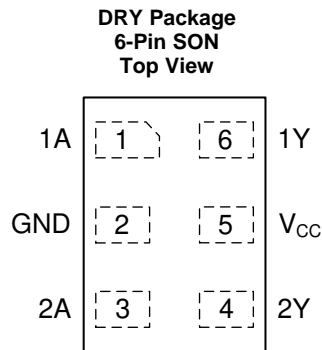
Logic Diagram (Positive Logic)

Table of Contents

4 Revision History

DATE	REVISION	NOTES
September 2019	*	Initial release.

5 Pin Configuration and Functions

DRY Package
6-Pin SON
Top View

```
1A │ 1    6 │ 1Y

GND │ 2    5 │ VCC

2A │ 3    4 │ 2Y
```

Pin Functions

PIN		I/O	DESCRIPTION
NAME	DRY Package[1]		
1A	1	I	Input
1Y	6	O	Output
2A	3	I	Input
2Y	4	O	Output
V_{CC}	5	—	Positive Supply
GND	2	—	Ground

(1) See Package drawing at the end of the data sheet for dimensions

6 Specifications

6.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		−0.5	6.5	V
V_I	Input voltage range[2]		−0.5	6.5	V
V_O	Voltage range applied to any output in the high or low state[2][3]		−0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
I_{OK}	Output clamp current	$V_O < 0$		−50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CC} or GND			±100	mA
T_A	Operating free-air temperature		−40	125	°C
T_J	Operating junction temperature			150	°C
T_{stg}	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

6.2 ESD Ratings

			MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	$I_O = -100$ µA	$0.75 \times V_{CC}$		V
V_{IL}	Low-level input voltage	$I_O = 100$ µA		$0.25 \times V_{CC}$	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.4 Thermal Information

THERMAL METRIC[1]		DRY (6 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	233.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	144.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	119.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	119.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
					MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
V_{OH}		V_{IL} = 0 V	I_{OH} = −100 µA	1.65 V to 5.5 V	V_{CC} − 0.1			V_{CC} − 0.1			V
			I_{OH} = −4 mA	1.65 V	1.2			1.2			
			I_{OH} = −8 mA	2.3 V	1.9			1.9			
			I_{OH} = −16 mA	3 V	2.4			2.4			
			I_{OH} = −24 mA		2.3			2.3			
			I_{OH} = −32 mA	4.5 V	3.8			3.8			
V_{OL}		V_{IH} = V_{CC}	I_{OL} = 100 µA	1.65 V to 5.5 V			0.1			0.1	V
			I_{OL} = 4 mA	1.65 V			0.45			0.45	
			I_{OL} = 8 mA	2.3 V			0.3			0.3	
			I_{OL} = 16 mA	3 V			0.4			0.4	
			I_{OL} = 24 mA				0.55			0.55	
			I_{OL} = 32 mA	4.5 V			0.55			0.55	
I_I	A inputs	V_I = 5.5 V or GND		0 to 5.5 V			±5			±5	µA
I_{CC}		V_I = 5.5 V or GND,	I_O = 0	1.65 V to 5.5 V			10			10	µA
C_I		V_I = V_{CC} or GND		3.3 V		7					pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

Product Folder Links: *SN74LVC2GU04-Q1*

6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C | | | | | | | | UNIT |
| | | | V_{CC} = 1.8 V ± 0.15 V | | V_{CC} = 2.5 V ± 0.2 V | | V_{CC} = 3.3 V ± 0.3 V | | V_{CC} = 5 V ± 0.5 V | | |
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.2	5.5	1	4	1.1	3.7	1	3	ns

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Parameter Measurement Information)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | –40°C to 125°C | | | | | | | | UNIT |
| | | | V_{CC} = 1.8 V ± 0.15 V | | V_{CC} = 2.5 V ± 0.2 V | | V_{CC} = 3.3 V ± 0.3 V | | V_{CC} = 5 V ± 0.5 V | | |
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	1.2	6.3	1	4.5	1.1	4.2	1	3.5	ns

6.8 Operating Characteristics

T_A = 25°C

| PARAMETER | TEST CONDITIONS | V_{CC} = 1.8 V | V_{CC} = 2.5 V | V_{CC} = 3.3 V | V_{CC} = 5 V | UNIT |
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	f = 10 MHz	7	7	8	23	pF

6.9 Typical Characteristic

Figure 1. t_{pd} vs V_{CC}

Product Folder Links: SN74LVC2GU04-Q1
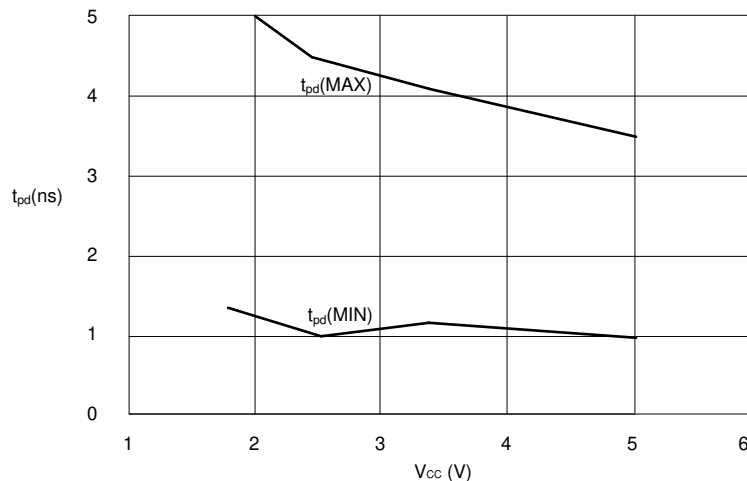
7 Parameter Measurement Information
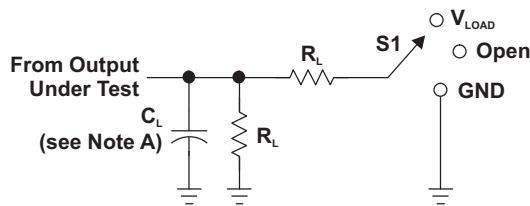
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	2 × V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	2 × V_{CC}	50 pF	500 Ω	0.3 V

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**
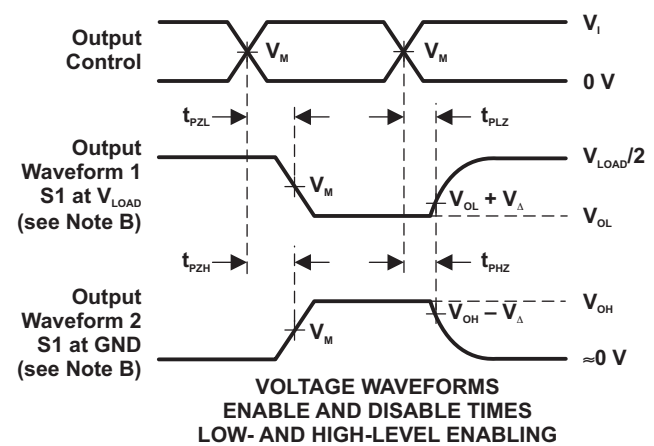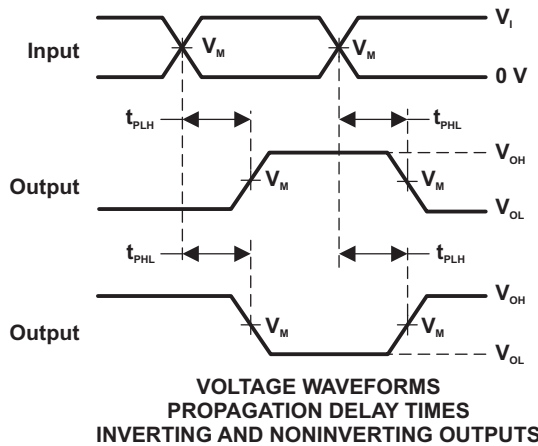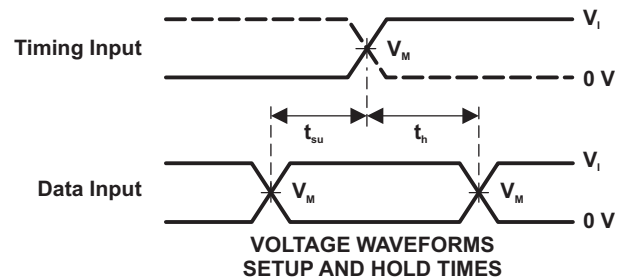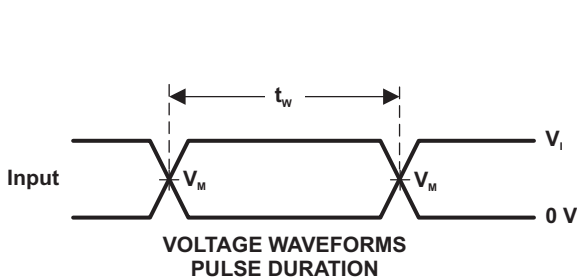
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.
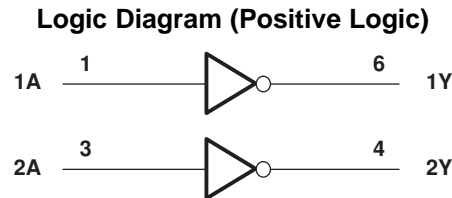
Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC2GU04-Q1 device contains two inverters with unbuffered outputs with a maximum sink current of 32 mA.

8.2 Functional Block Diagram

Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high-drive capability of this device creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst-case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Signals that are applied to the inputs need to have fast edge rates, as shown by $\Delta t/\Delta v$ in the *Recommended Operating Conditions*, to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

Feature Description (continued)

8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 3.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
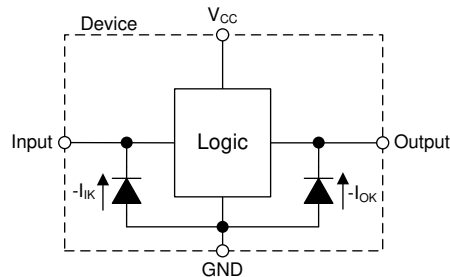
Figure 3. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.5 Unbuffered Logic

A standard CMOS logic function typically consists of at least three stages: the input inverter, the logic function, and the output inverter. Some devices have multiple stages at the input or output for various reasons. An unbuffered CMOS logic function eliminates the extra input and output stages; the device only contains the required logic function which is directly driven from the inputs and directly drives the outputs.

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. To learn more about how to use an unbuffered inverter in an oscillator circuit, see *Use of the CMOS Unbuffered Inverter in Oscillator Circuits*.

8.4 Device Functional Modes

Table 1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

Product Folder Links: *SN74LVC2GU04-Q1*

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. An example application circuit is shown in Figure 4. To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.

9.2 Typical Application
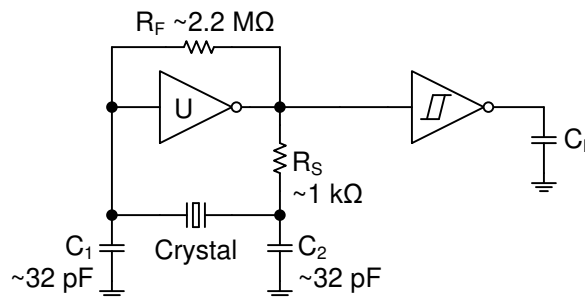
Figure 4. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.
 1. Recommended Input Conditions
   – Specified high and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
    – Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in *Recommended Operating Conditions* at any valid V_{CC}.
 2. Absolute Maximum Output Conditions
    – Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in *Absolute Maximum Ratings*.
    – Outputs must not be pulled above the voltage rated in the *Absolute Maximum Ratings*.

Product Folder Links: *SN74LVC2GU04-Q1*

Typical Application (continued)

9.2.3 Application Curve
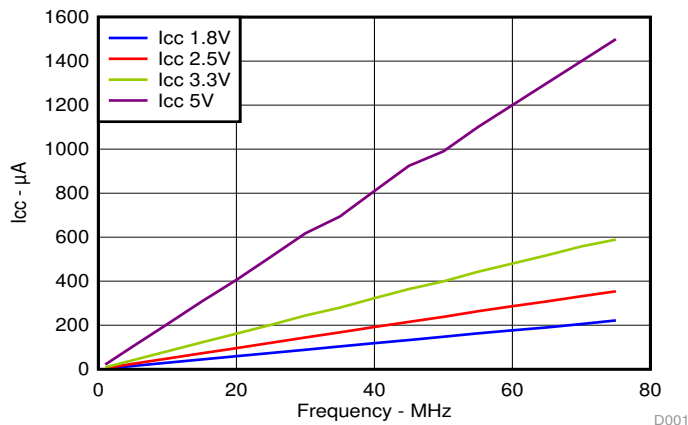
Figure 5. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions* table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

Product Folder Links: *SN74LVC2GU04-Q1*

11 Layout

11.1 Layout Guidelines

Even low data rate digital signals can contain high-frequency signal components due to fast edge rates. When a printed-circuit board (PCB) trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners.

An example layout is given in Figure 6 for the DRY (SON) package. This example layout includes a 0402 (metric) capacitor and uses the measurements found in the example board layout appended to this end of this datasheet. A via of diameter 0.1 mm (3.973 mil) is placed directly in the center of the device. This via can be used to trace out the center pin connection through another board layer, or it can be left out of the layout
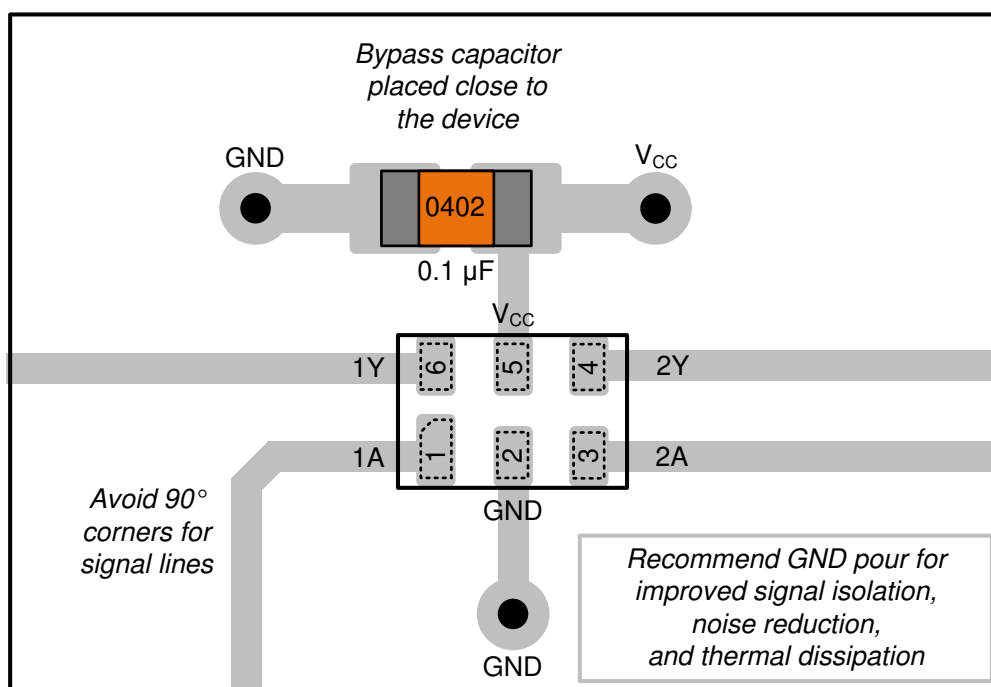
11.2 Layout Example

Figure 6. Layout example for DRY package

Product Folder Links: *SN74LVC2GU04-Q1*

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
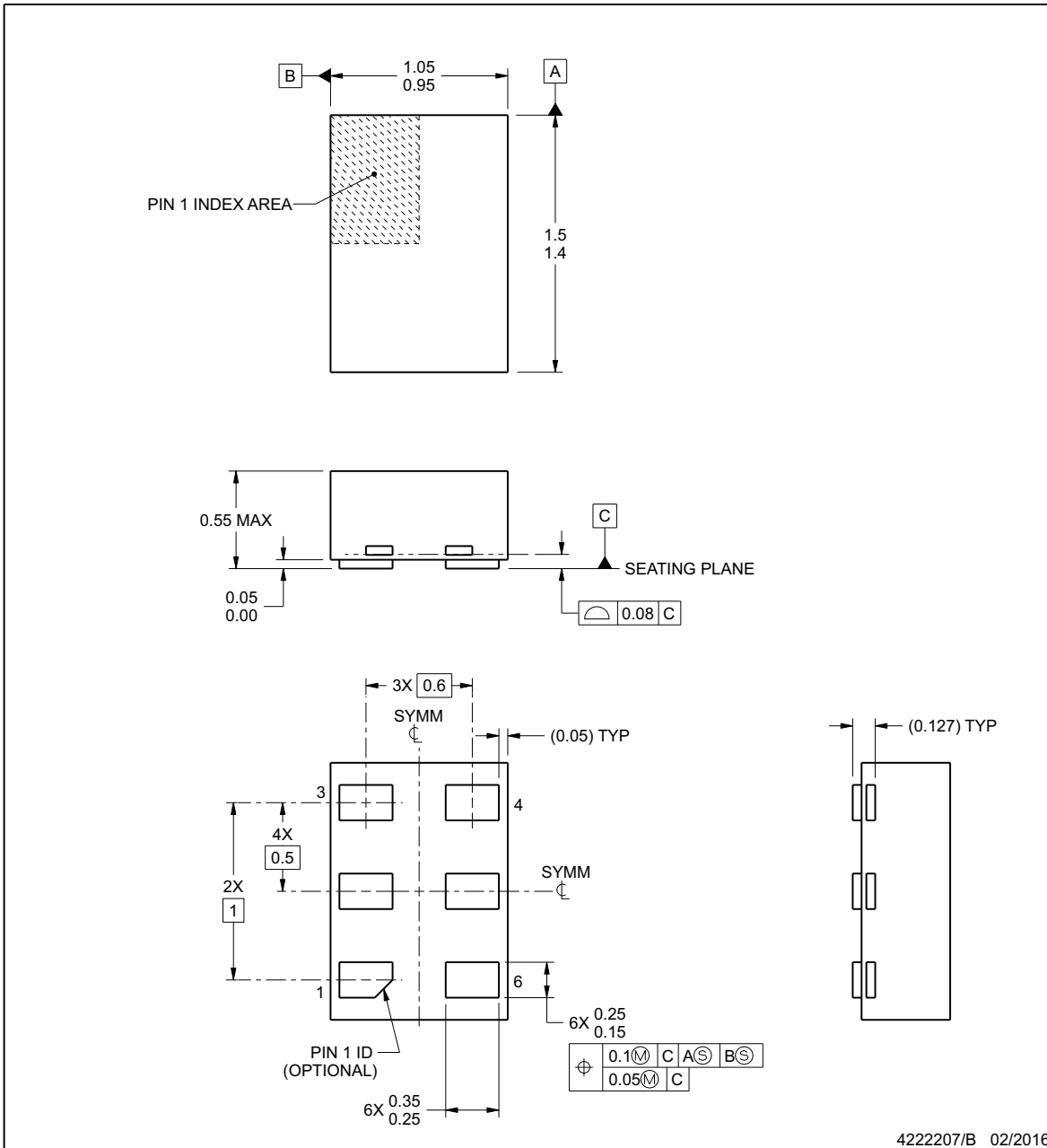
PACKAGE OUTLINE

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

B ← 1.05 / 0.95 → A

PIN 1 INDEX AREA

1.5 / 1.4

0.55 MAX

0.05 / 0.00

C

SEATING PLANE

⌒ 0.08 C

3X 0.6

SYMM ℄

(0.05) TYP

3   4

4X 0.5

2X 1

SYMM ℄

1   6

(0.127) TYP

6X 0.25 / 0.15

PIN 1 ID (OPTIONAL)

⊕ 0.1 Ⓜ C AⓈ BⓈ
0.05 Ⓜ C

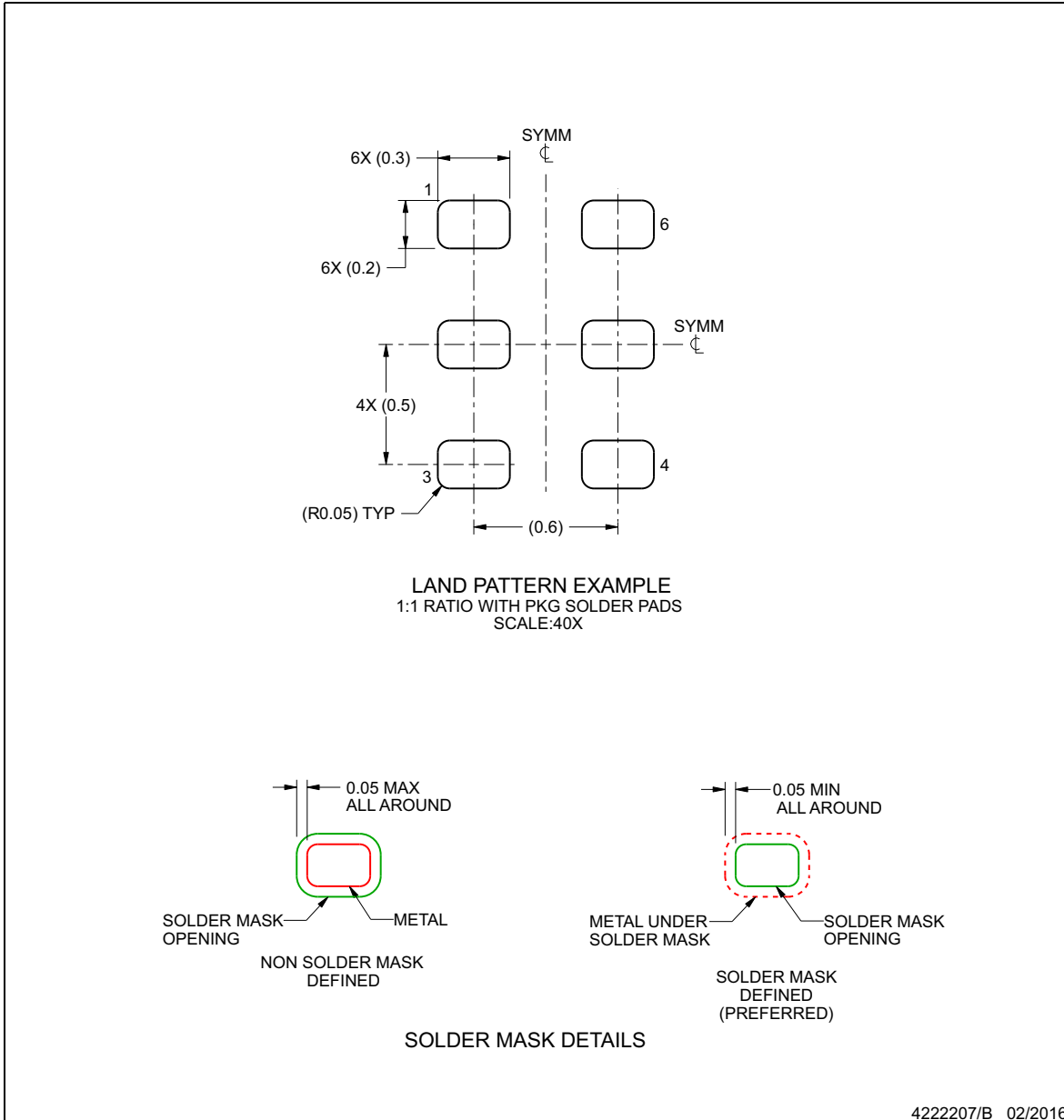6X 0.35 / 0.25

4222207/B   02/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

Product Folder Links: *SN74LVC2GU04-Q1*

EXAMPLE BOARD LAYOUT

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

SYMM

6X (0.3)

1

6X (0.2)

6

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

4222207/B   02/2016

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

Product Folder Links: *SN74LVC2GU04-Q1*
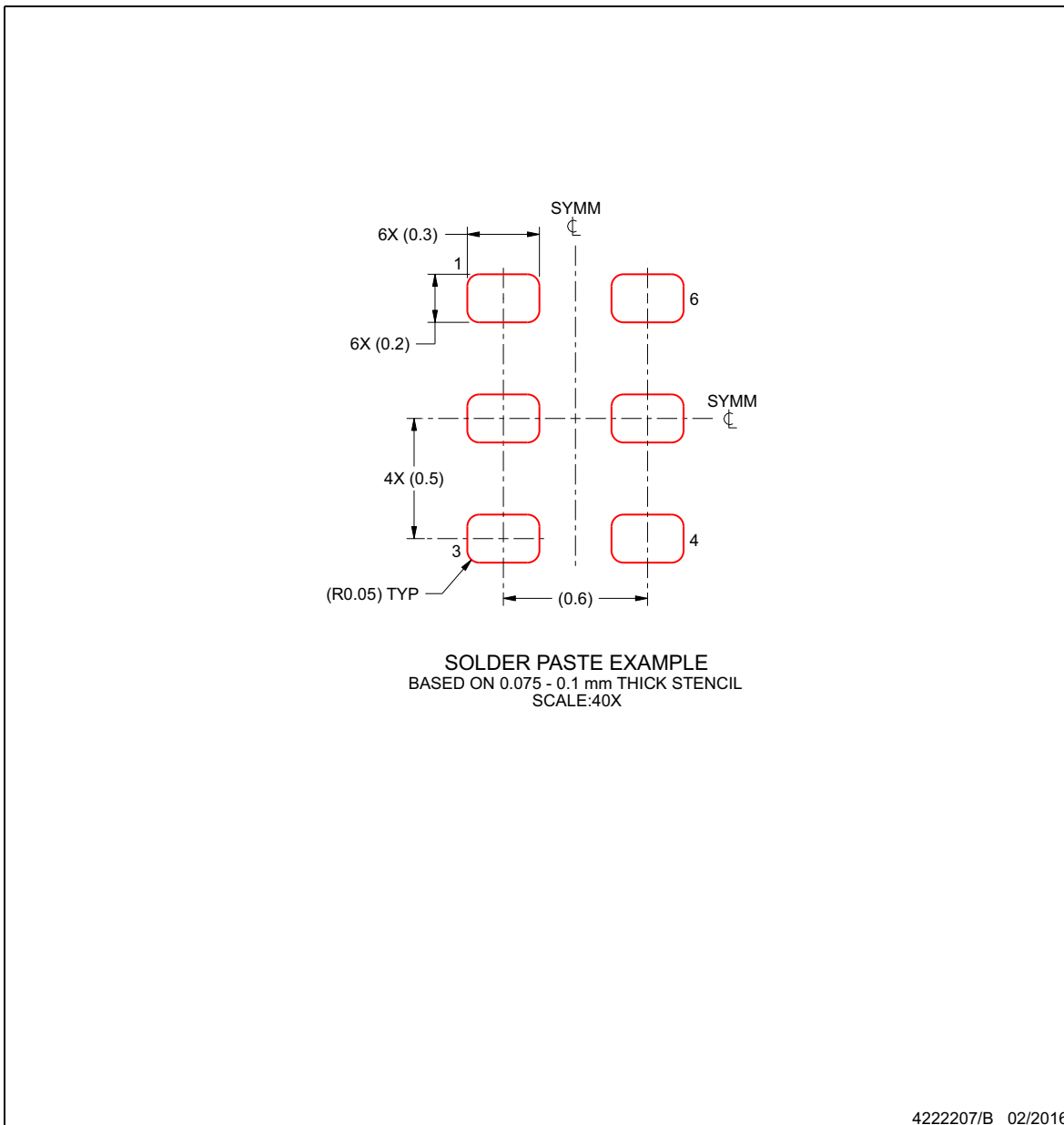
EXAMPLE STENCIL DESIGN

DRY0006B   USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B   02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Submit Documentation Feedback   17

Product Folder Links: *SN74LVC2GU04-Q1*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
1P2GU04QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	FZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC2GU04-Q1 :

● Catalog: SN74LVC2GU04

NOTE: Qualified Version Definitions:

    ● Catalog - TI's standard catalog product

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P2GU04QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

![Texas Instruments]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P2GU04QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

B | 1.05
0.95 | A

PIN 1 INDEX AREA

1.5
1.4

0.55 MAX

C

SEATING PLANE

0.05
0.00

| 0.08 | C |

3X 0.6

SYMM

(0.05) TYP

(0.127) TYP

3

4X
0.5

2X
1

SYMM

1

6

6X 0.25
0.15

PIN 1 ID
(OPTIONAL)

| ⊕ | 0.1 Ⓜ | C | AⓈ | BⓈ |
| | 0.05 Ⓜ | C | | |

6X 0.35
0.25

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM

6X (0.3)

1

6X (0.2)

SYMM

4X (0.5)

3

(R0.05) TYP

6

4

(0.6)

LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X

0.05 MAX
ALL AROUND

SOLDER MASK
OPENING

METAL

**NON SOLDER MASK
DEFINED**

0.05 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**SOLDER MASK
DEFINED
(PREFERRED)**

SOLDER MASK DETAILS

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NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

6X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)

SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

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