ADS1120-Q1 用于小型信号传感器的车用低功耗、低噪声、16 位模数转换器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 的下列结果：
  - 温度等级 1：-40°C 至 +125°C
  - 人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 充电器件模型 (CDM) ESD 分类等级 C4B
- 低流耗：
  占空比模式下低至 120μA（典型值）
- 宽电源电压：2.3V 至 5.5V
- 可编程增益：1V/V 至 128V/V
- 可编程数据速率：5SPS 至 2kSPS
- 16 位无噪声分辨率（20SPS 时）
- 采用单周期稳定数字滤波器，在 20SPS 时实现 50Hz 和 60Hz 同步抑制
- 两个差分输入或四个单端输入
- 双匹配可编程电流源：50μA 至 1.5mA
- 内部 2.048V 基准电压：漂移 5ppm/°C（典型值）
- 内部 2% 精准振荡器
- 内部温度传感器：精度 0.5°C（典型值）
- SPI™- 兼容接口（模式 1）

2 应用

- 温度传感器：
  - 热电偶
  - 电阻式温度检测器 (RTD)：
    2 线、3 线或 4 线制类型
- 桥式传感器：
  - 压力传感器
  - 应力计
- 电池电压测量

3 说明

ADS1120-Q1 是一款精密的 16 位模数转换器 (ADC)，所集成的多种特性能够降低系统成本并减少小型传感器信号测量应用中的组件数量。 这个器件具有通过灵活的输入复用器 (MUX) 实现的两个差分输入或四个单端输入，一个低噪声可编程增益放大器 (PGA)，两个可编程励磁电流源，一个电压基准，一个振荡器，一个低侧开关和一个精密温度传感器。

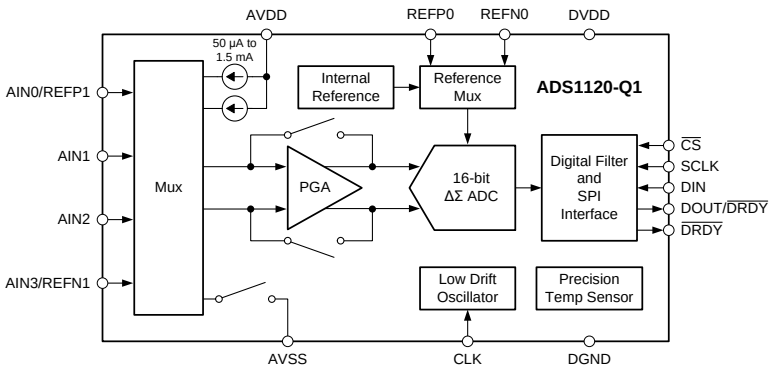
此器件能够以高达 2000 次/秒 (SPS) 采样数据速率执行转换，并且能够在单周期内稳定。 针对噪声环境中的工业应用，当采样频率为 20SPS 时，数字滤波器能够实现 50Hz 和 60Hz 同步抑制。 其内部 PGA 提供高达 128V/V 的增益。此 PGA 使得 ADS1120-Q1 非常适用于小传感器信号测量应用，例如电阻式温度检测器 (RTD)、热电偶、热敏电阻和桥式传感器。 该器件在使用 PGA 时支持测量伪差分或全差分信号。 此外，该器件还可配置为绕过内部 PGA，同时仍提供高输入阻抗和高达 4V/V 的增益，从而实现单端测量。

在禁用 PGA 后的占空比模式下运行功耗可低至 120μA。 通过模式 1 SPI 兼容接口建立与器件之间的通信。 ADS1120-Q1 采用薄型小外形尺寸 (TSSOP)-16 封装，额定工作温度范围为 -40°C 至 +125°C。

器件信息(1)

部件号	封装	封装尺寸（标称值）
ADS1120-Q1	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。



目录

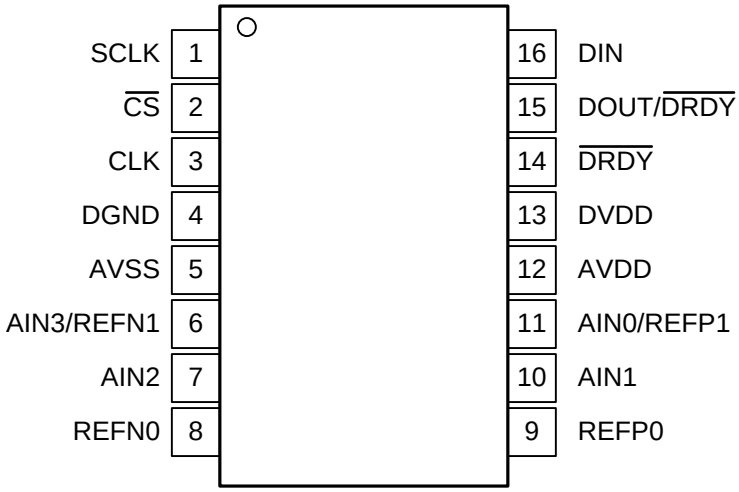
4 修订历史记录

Changes from Original (August 2013) to Revision A **Page**

- 已更改产品预览数据表 ... 1

5 Pin Configurations and Functions

PW Package
TSSOP-16
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	SCLK	Digital input	Serial clock input
2	$\overline{CS}$	Digital input	Chip select, active low. Connect to DGND if not used.
3	CLK	Digital input	External clock source pin. Connect to DGND if not used.
4	DGND	Digital	Digital ground
5	AVSS	Analog	Negative analog power supply
6	AIN3/REFN1	Analog input	Analog input 3, negative reference input 1. Internal low-side power switch connected between AIN3/REFN1 and AVSS. Leave unconnected or tie to AVDD if not used.
7	AIN2	Analog input	Analog input 2. Leave unconnected or tie to AVDD if not used.
8	REFN0	Analog input	Negative reference input 0. Leave unconnected or tie to AVDD if not used.
9	REFP0	Analog input	Positive reference input 0. Leave unconnected or tie to AVDD if not used.
10	AIN1	Analog input	Analog input 1. Leave unconnected or tie to AVDD if not used.
11	AIN0/REFP1	Analog input	Analog input 0, positive reference input 1. Leave unconnected or tie to AVDD if not used.
12	AVDD	Analog	Positive analog power supply
13	DVDD	Digital	Positive digital power supply
14	$\overline{DRDY}$	Digital output	Data ready, active low. Leave unconnected or tie to DVDD using a weak pull-up resistor if not used.
15	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready, active low
16	DIN	Digital input	Serial data input

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	7	V
DVDD to DGND	–0.3	7	V
AVSS to DGND	–2.8	0.3	V
Analog input voltage	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	DGND – 0.3	DVDD + 0.3	V
Input current, continuous, any terminal except power supply terminals	–10	10	mA
Junction temperature, T_J	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)	–750	750	V
			Other pins	–500	500	V

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Unipolar analog power supply	AVDD to AVSS	2.3		5.5	V
		AVSS to DGND	–0.1	0	0.1	V
	Bipolar analog power supply	AVDD to DGND	2.3	2.5	2.75	V
		AVSS to DGND	–2.75	–2.5	–2.3	V
	Digital power supply	DVDD to DGND	2.3		5.5	V
ANALOG INPUTS(1)						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} – V_{(AINN)}$(2)	$–V_{ref}$ / Gain		V_{ref} / Gain	V
$V_{(AINx)}$	Absolute input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	See the *Low-Noise PGA* section			
V_{CM}	Common-mode input voltage	PGA disabled, gain = 1 to 4	AVSS – 0.1		AVDD + 0.1	V
		PGA enabled, gain = 1 to 128	See the *Low-Noise PGA* section			
VOLTAGE REFERENCE INPUTS(3)						
V_{ref}	Differential reference input voltage	$V_{ref} = V_{(REFPx)} – V_{(REFNx)}$	0.75	2.5	AVDD	V
$V_{(REFNx)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFPx)}$ – 0.75	V
$V_{(REFPx)}$	Absolute positive reference voltage		$V_{(REFNx)}$ + 0.75		AVDD + 0.1	V
EXTERNAL CLOCK SOURCE						
$f_{(CLK)}$	External clock frequency		0.5	4.096	4.5	MHz
	Duty cycle		40%		60%	
DIGITAL INPUTS						
	Input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA. AINx denotes one of the four available analog inputs. *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case. See the *Bypassing the PGA* section for more information.
(2) Excluding the effects of offset and gain error. Limited to ±[(AVDD – AVSS) – 0.4 V] / Gain, when the PGA is enabled.
(3) REFPx and REFNx denote one of the two available differential reference input pairs.

6.4 Thermal Information

THERMAL METRIC(1)		TSSOP (PW) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.3	
ψ_{JT}	Junction-to-top characterization parameter	2.4	
ψ_{JB}	Junction-to-board characterization parameter	43.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{ref} = 2.5 V (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Absolute input current		See the *Typical Characteristics*			
	Differential input current		See the *Typical Characteristics*			
SYSTEM PERFORMANCE						
	Resolution (no missing codes)		16			Bits
DR	Data rate	Normal mode	20, 45, 90, 175, 330, 600, 1000			SPS
		Duty-cycle mode	5, 11.25, 22.5, 44, 82.5, 150, 250			SPS
		Turbo mode	40, 90, 180, 350, 660, 1200, 2000			SPS
	Noise (input-referred)		See the *Noise Performance* section			
INL	Integral nonlinearity	Gain = 1, V_{CM} = 0.5 AVDD, best fit(2)		8	20	ppm
		Gain = 2 to 128, V_{CM} = 0.5 AVDD, best fit		8		ppm
V_{IO}	Input offset voltage	PGA disabled, gain = 1 to 4, differential inputs		±4		µV
		Gain = 1 to 128, differential inputs		±4		µV
	Offset drift	PGA disabled, gain = 1 to 4		0.25		µV/°C
		Gain = 1 to 128		0.25		µV/°C
	Gain error	PGA disabled, gain = 1 to 4		±0.015%		
		Gain = 1 to 128, T_A = 25°C	–0.1%	±0.015%	0.1%	
	Gain drift	PGA disabled, gain = 1 to 4		1		ppm/°C
		Gain = 1 to 128(2)		1	5	ppm/°C
NMRR	Normal-mode rejection ratio(2)	50 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 10	105			dB
		60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 11	105			dB
		50 Hz or 60 Hz ±3%, DR = 20 SPS, external CLK, 50/60 bit = 01	90			dB
CMRR	Common-mode rejection ratio	At dc, gain = 1	90	105		dB
		$f_{(CM)}$ = 50 Hz, DR = 2000 SPS(2)	90	115		dB
		$f_{(CM)}$ = 60 Hz, DR = 2000 SPS(2)	90	115		dB
PSRR	Power-supply rejection ratio	AVDD at dc, V_{CM} = 0.5 AVDD, gain = 1	80	105		dB
		DVDD at dc, V_{CM} = 0.5 AVDD, gain = 1(2)	90	115		dB
INTERNAL VOLTAGE REFERENCE						
	Initial accuracy	T_A = 25°C	2.045	2.048	2.051	V
	Reference drift(2)			5	40	ppm/°C
	Long-term drift	1000 hours		110		ppm
VOLTAGE REFERENCE INPUTS						
	Reference input current	REFP0 = V_{ref}, REFN0 = AVSS		±10		nA
INTERNAL OSCILLATOR						
	Internal oscillator accuracy	Normal mode	–2%	±1%	2%	

(1) *PGA disabled* means the low-noise PGA is powered down and bypassed. Gains of 1, 2, and 4 are still possible in this case. See the *Bypassing the PGA* section for more information.
(2) Minimum and maximum values are ensured by design and characterization data.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 3.3 V, AVSS = 0 V, DVDD = 3.3 V, PGA enabled, DR = 20 SPS, and external V_{ref} = 2.5 V (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXCITATION CURRENT SOURCES (IDACs)						
	Current settings			50, 100, 250, 500, 1000, 1500		µA
	Compliance voltage	All current settings			AVDD – 0.9	V
	Accuracy	All current settings, each IDAC	–6%	±1%	6%	
	Current match	Between IDACs		±0.3%		
	Temperature drift	Each IDAC		50		ppm/°C
	Temperature drift matching	Between IDACs		10		ppm/°C
TEMPERATURE SENSOR						
	Temperature sensor resolution	Conversion resolution		14		Bits
		Temperature resolution		0.03125		°C
	Temperature sensor accuracy	T_A = 0°C to +75°C		±0.25		°C
		T_A = –40°C to +125°C		±0.5		°C
		Temperature sensor accuracy vs analog supply voltage		0.0625	0.25	°C/V
LOW-SIDE POWER SWITCH						
R_{ON}	On-resistance			3.5		Ω
	Current through switch				30	mA
DIGITAL INPUT/OUTPUT						
V_{IH}	High-level input voltage		0.7 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.3 DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 3 mA	0.8 DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA			0.2 DVDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = DGND	–10		10	µA
POWER-SUPPLY						
I_{AVDD}	Analog supply current(3)	Power-down mode		0.1	3	µA
		Duty-cycle mode, PGA disabled		65		µA
		Normal mode, PGA disabled		240		µA
		Normal mode, gain = 1 to 16		340	490	µA
		Normal mode, gain = 32		425		µA
		Normal mode, gain = 64, 128		510		µA
		Turbo mode, gain = 1 to 16		540		µA
I_{DVDD}	Digital supply current(3)	Power-down mode		0.3	5	µA
		Duty-cycle mode		55		µA
		Normal mode		75	110	µA
		Turbo mode		95		µA
P_D	Power dissipation(3)	Duty-cycle mode, PGA disabled		0.4		mW
		Normal mode, gain = 1 to 16		1.4		mW
		Turbo mode, gain = 1 to 16		2.1		mW

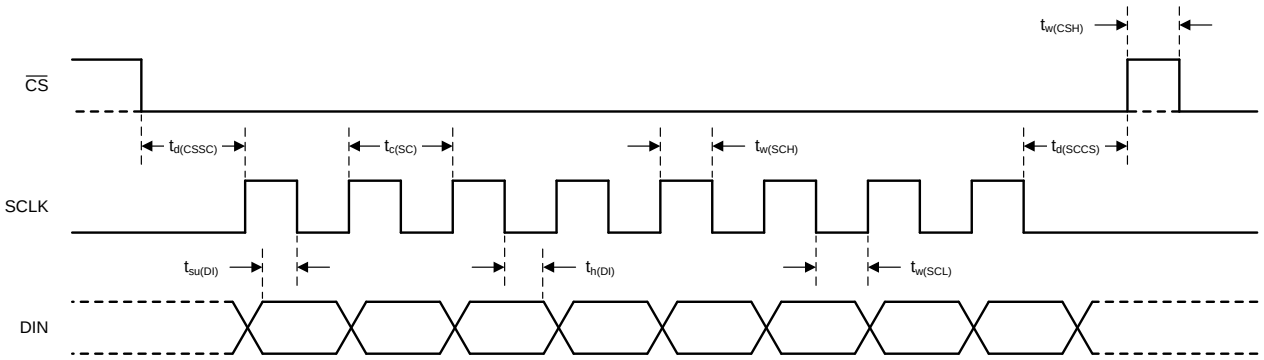
(3) Internal voltage reference selected, internal oscillator enabled, both IDACs turned off.

6.6 SPI Timing Requirements

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
$t_{d(CSSC)}$	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge	50		ns
$t_{d(SCCS)}$	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	25		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	50		ns
$t_{c(SC)}$	SCLK period(1)	150		ns
$t_{w(SCH)}$	Pulse duration, SCLK high(1)	60		ns
$t_{w(SCL)}$	Pulse duration, SCLK low(1)	60		ns
$t_{su(DI)}$	Setup time, DIN valid before SCLK falling edge	50		ns
$t_{h(DI)}$	Hold time, DIN valid after SCLK falling edge	25		ns

(1) If a complete command is not sent within 13955 · $t_{(MOD)}$ (normal mode, duty-cycle mode) or 27910 · $t_{(MOD)}$ (turbo mode), the serial interface resets and the next SCLK pulse starts a new communication cycle.
$t_{(MOD)}$ = 1 / $f_{(MOD)}$. Modulator frequency ($f_{(MOD)}$) is 256 kHz in normal and duty-cycle mode and 512 kHz in turbo mode, when using the internal oscillator or an external 4.096-MHz clock.



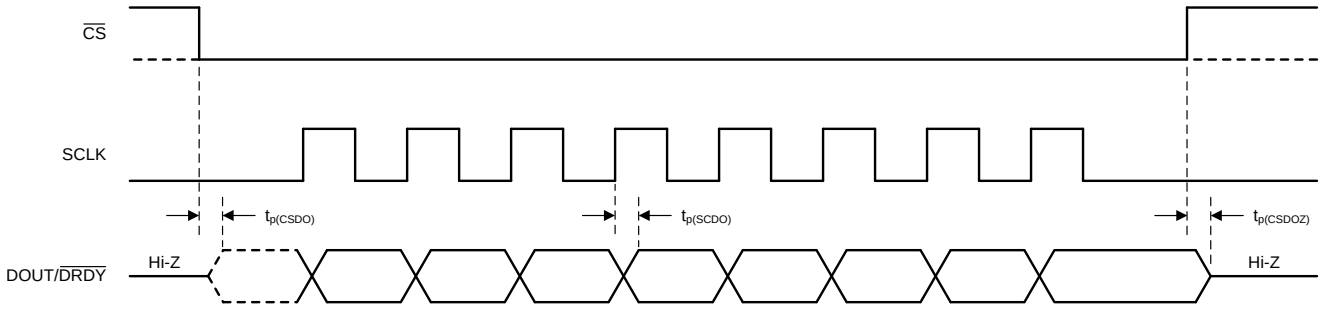
NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

Figure 1. Serial Interface Timing Requirements

6.7 SPI Switching Characteristics

over operating ambient temperature range, DVDD = 2.3 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 10 kΩ to DGND			50	ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 10 kΩ to DGND	0		50	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 10 kΩ to DGND			50	ns

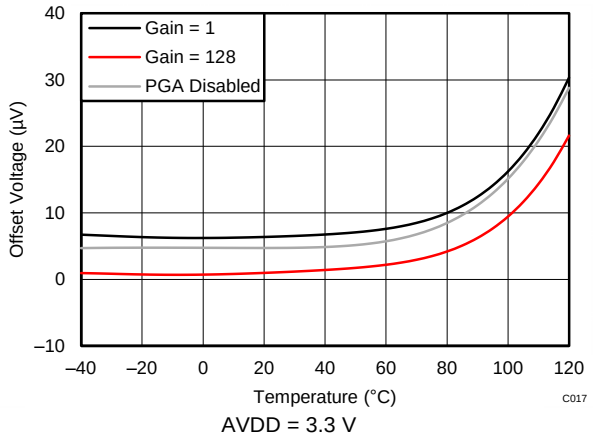


NOTE: Single-byte communication is shown. Actual communication may be multiple bytes.

Figure 2. Serial Interface Switching Characteristics

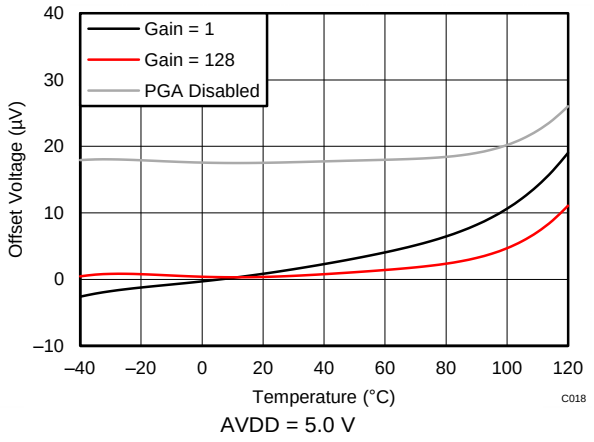
6.8 Typical Characteristics

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).



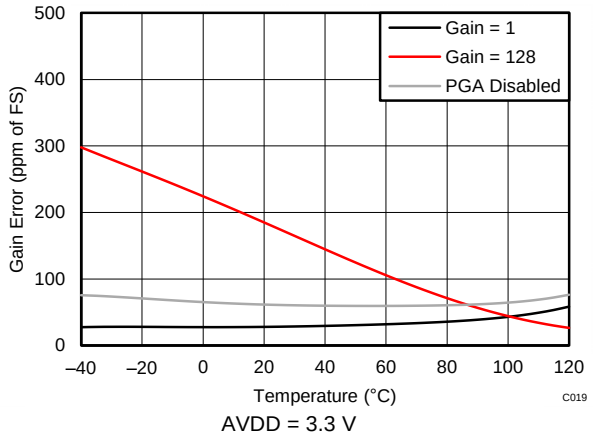
AVDD = 3.3 V

Figure 3. Input-Referred Offset Voltage vs Temperature



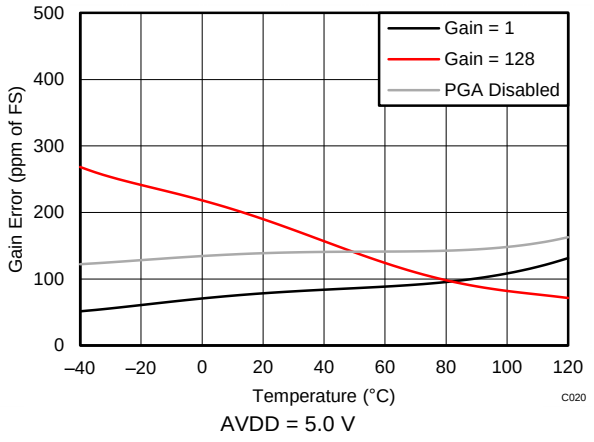
AVDD = 5.0 V

Figure 4. Input-Referred Offset Voltage vs Temperature



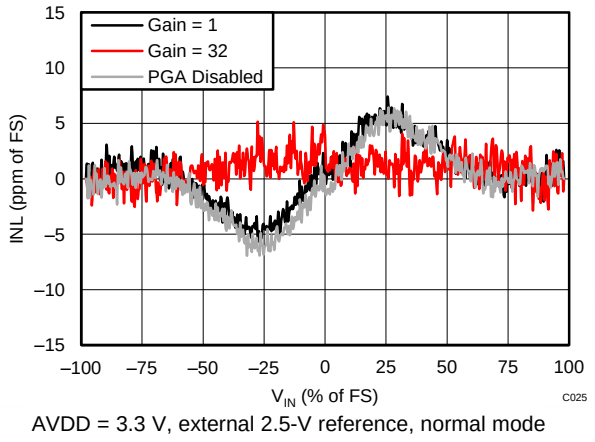
AVDD = 3.3 V

Figure 5. Gain Error vs Temperature



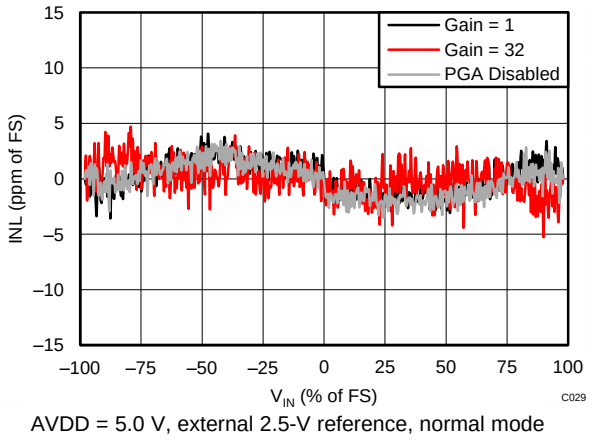
AVDD = 5.0 V

Figure 6. Gain Error vs Temperature



AVDD = 3.3 V, external 2.5-V reference, normal mode

Figure 7. Integral Nonlinearity vs Differential Input Signal

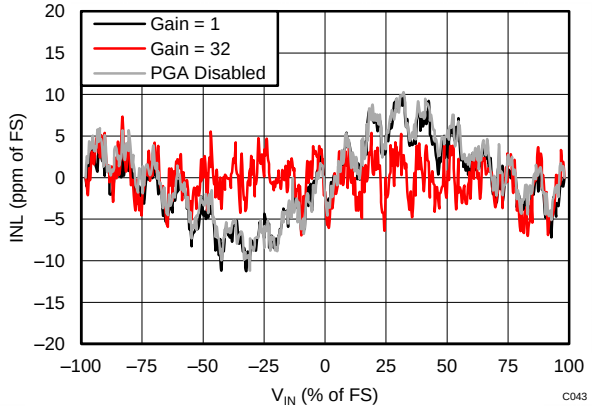


AVDD = 5.0 V, external 2.5-V reference, normal mode

Figure 8. Integral Nonlinearity vs Differential Input Signal

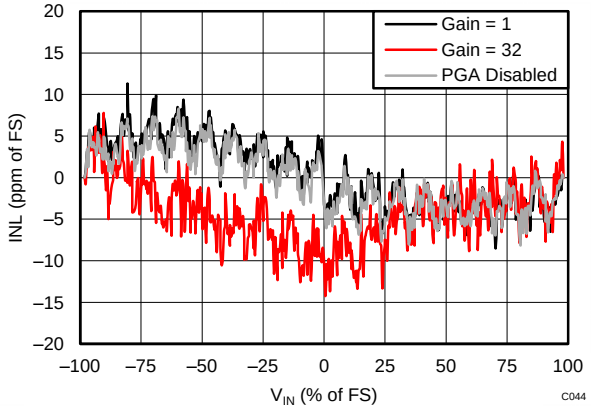
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).



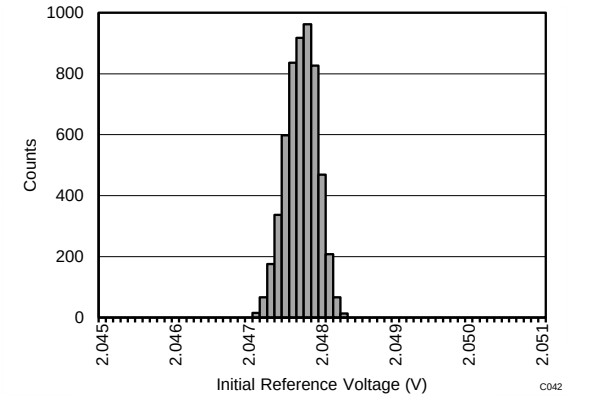
AVDD = 3.3 V, internal reference, normal mode

Figure 9. Integral Nonlinearity vs Differential Input Signal



AVDD = 5.0 V, internal reference, normal mode

Figure 10. Integral Nonlinearity vs Differential Input Signal



T_A = 25°C, data from 5490 devices

Figure 11. Internal Reference Voltage Histogram

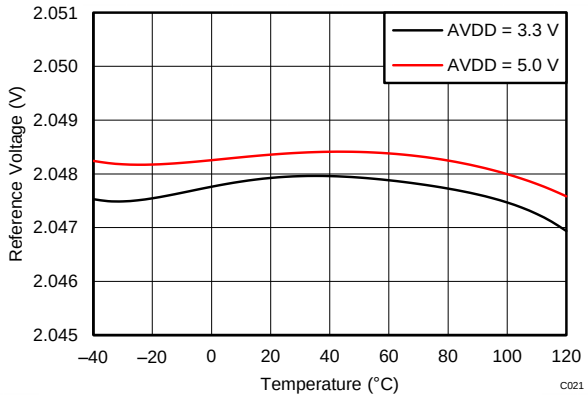
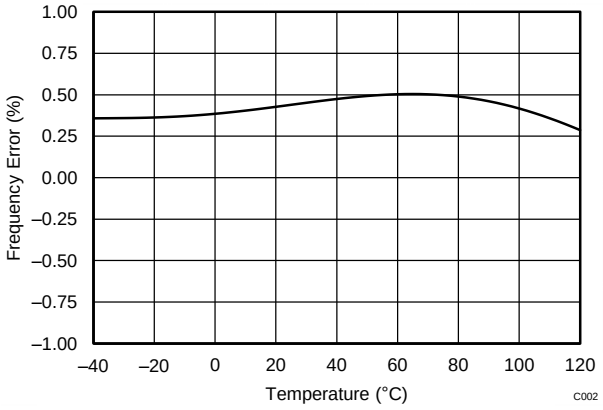


Figure 12. Internal Reference Voltage vs Temperature



DVDD = 3.3 V, normal mode

Figure 13. Internal Oscillator Accuracy vs Temperature

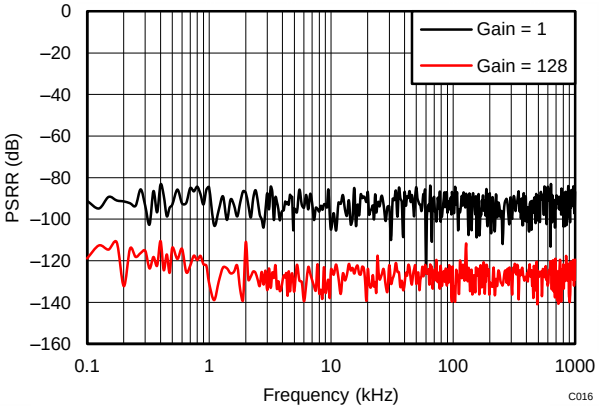
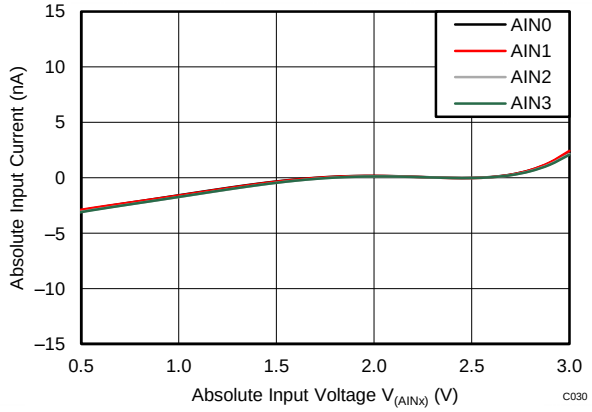


Figure 14. AVDD Power-Supply Rejection Ratio vs Frequency

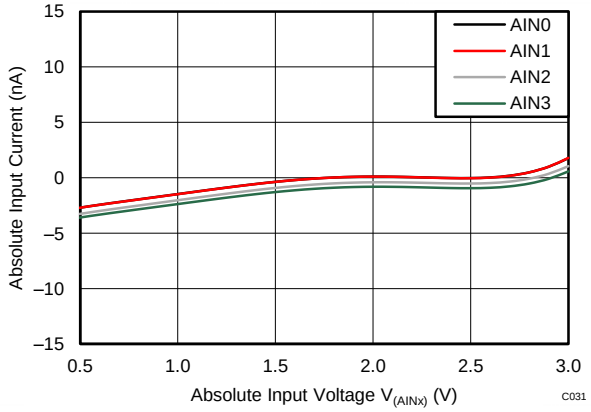
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).



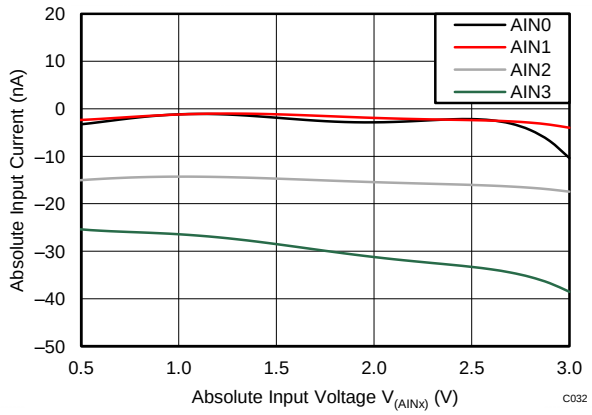
AVDD = 3.3 V, PGA enabled, T_A = –40°C

Figure 15. Absolute Input Current vs Absolute Input Voltage



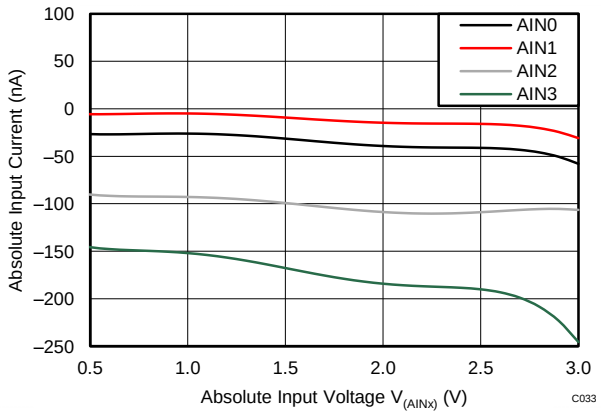
AVDD = 3.3 V, PGA enabled, T_A = 25°C

Figure 16. Absolute Input Current vs Absolute Input Voltage



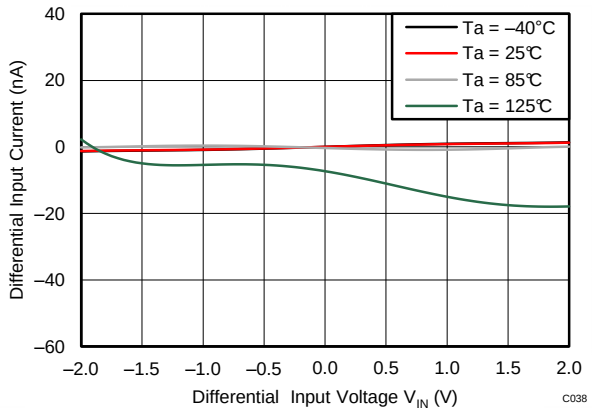
AVDD = 3.3 V, PGA enabled, T_A = 85°C

Figure 17. Absolute Input Current vs Absolute Input Voltage



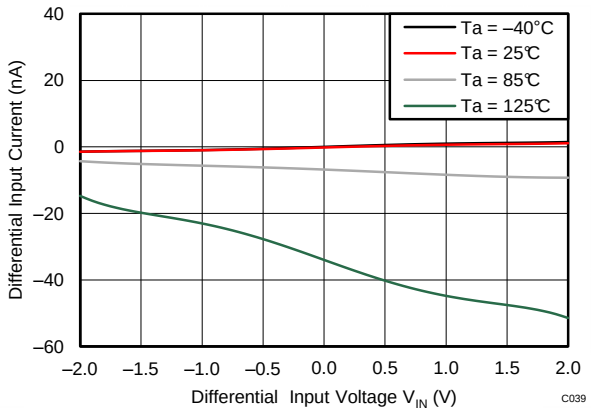
AVDD = 3.3 V, PGA enabled, T_A = 125°C

Figure 18. Absolute Input Current vs Absolute Input Voltage



AVDD = 3.3 V, PGA enabled, AIN_P = AIN0, AIN_N = AIN1

Figure 19. Differential Input Current vs Differential Input Voltage

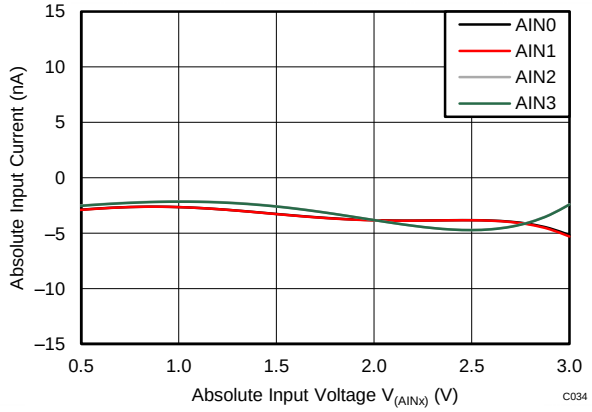


AVDD = 3.3 V, PGA enabled, AIN_P = AIN3, AIN_N = AIN2

Figure 20. Differential Input Current vs Differential Input Voltage

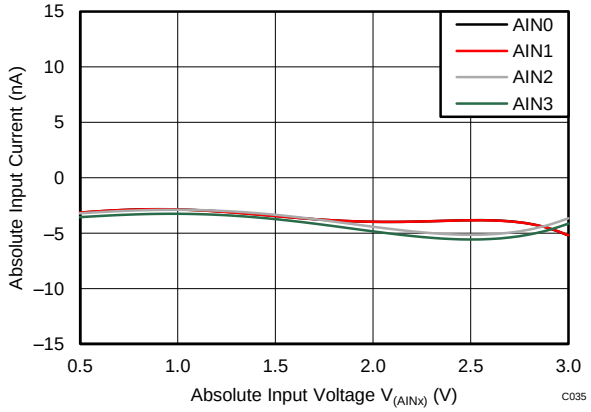
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).



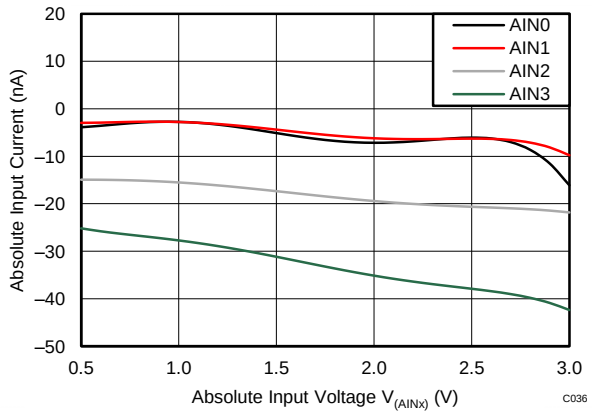
AVDD = 3.3 V, PGA disabled, T_A = –40°C

Figure 21. Absolute Input Current vs Absolute Input Voltage



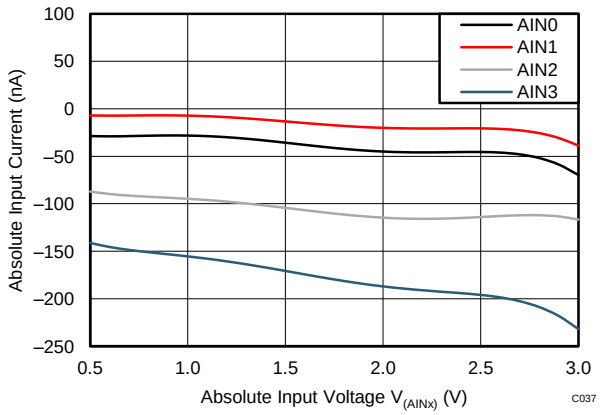
AVDD = 3.3 V, PGA disabled, T_A = 25°C

Figure 22. Absolute Input Current vs Absolute Input Voltage



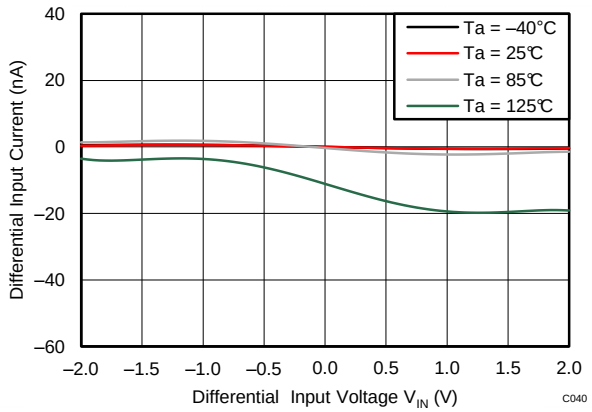
AVDD = 3.3 V, PGA disabled, T_A = 85°C

Figure 23. Absolute Input Current vs Absolute Input Voltage



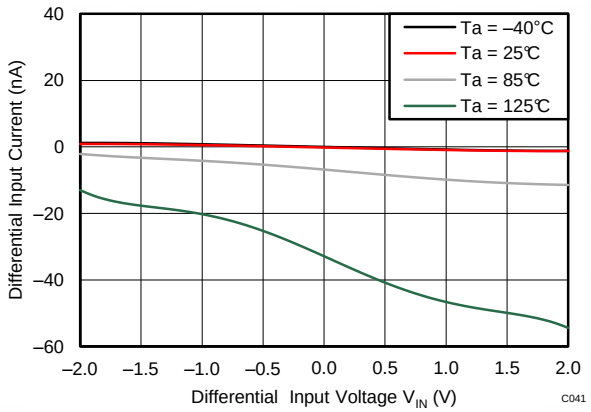
AVDD = 3.3 V, PGA disabled, T_A = 125°C

Figure 24. Absolute Input Current vs Absolute Input Voltage



AVDD = 3.3 V, PGA disabled, AIN_P = AIN0, AIN_N = AIN1

Figure 25. Differential Input Current vs Differential Input Voltage



AVDD = 3.3 V, PGA disabled, AIN_P = AIN3, AIN_N = AIN2

Figure 26. Differential Input Current vs Differential Input Voltage

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).

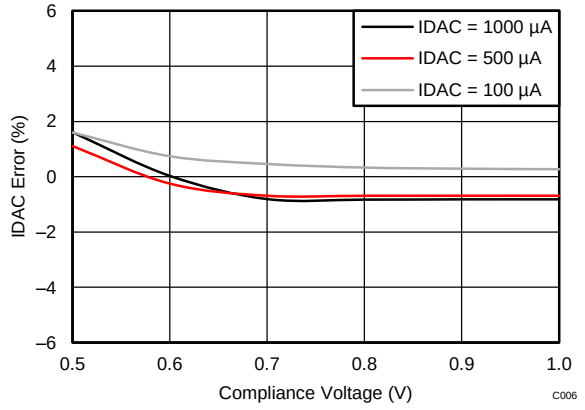


Figure 27. IDAC Accuracy vs Compliance Voltage

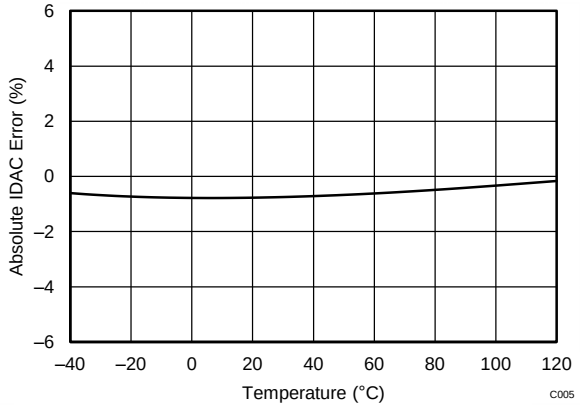


Figure 28. IDAC Accuracy vs Temperature

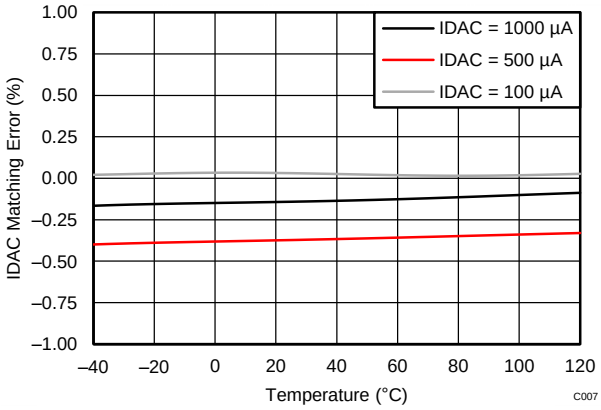
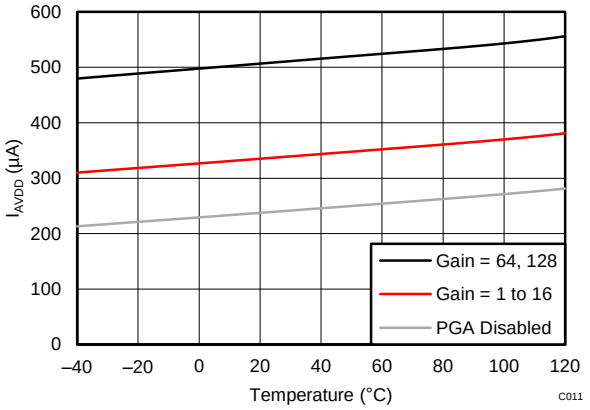
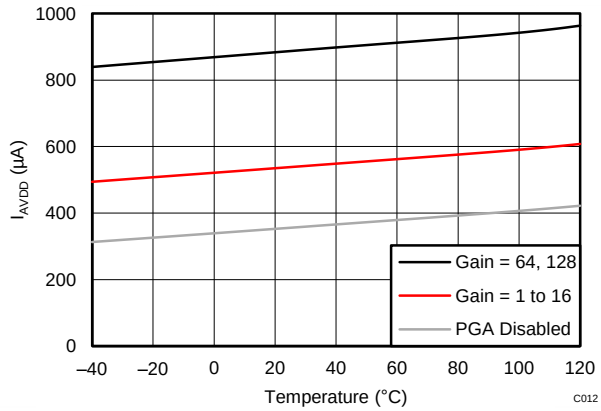


Figure 29. IDAC Matching vs Temperature



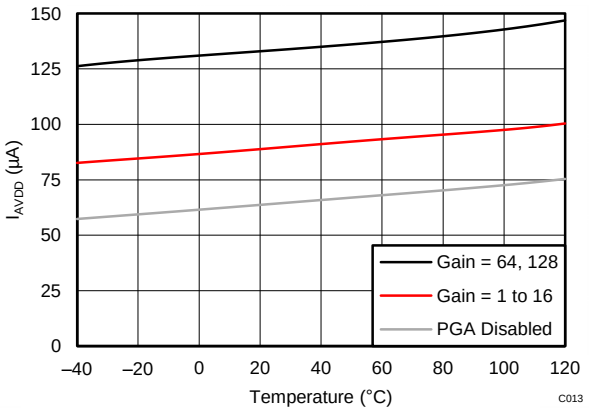
AVDD = 3.3 V, internal reference, normal mode

Figure 30. I_{AVDD} vs Temperature



AVDD = 3.3 V, internal reference, turbo mode

Figure 31. I_{AVDD} vs Temperature

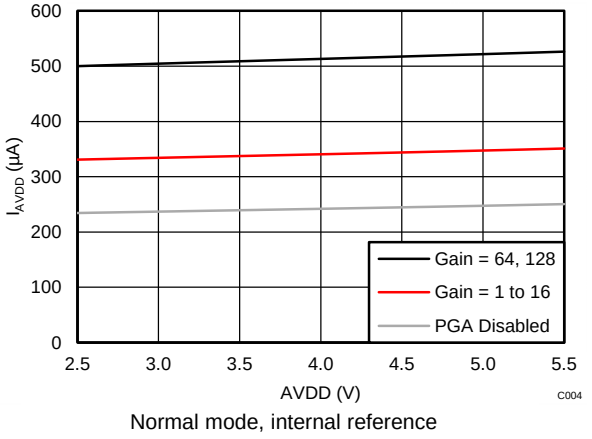


AVDD = 3.3 V, internal reference, duty-cycle mode

Figure 32. I_{AVDD} vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3.3 V, AVSS = 0 V, and PGA enabled using external V_{ref} = 2.5 V (unless otherwise noted).



Normal mode, internal reference

Figure 33. I_{AVDD} vs AVDD

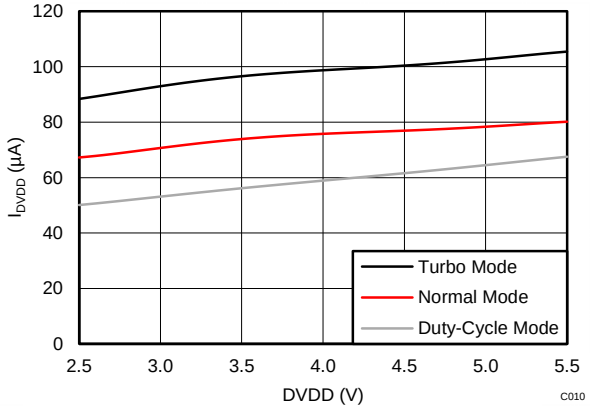
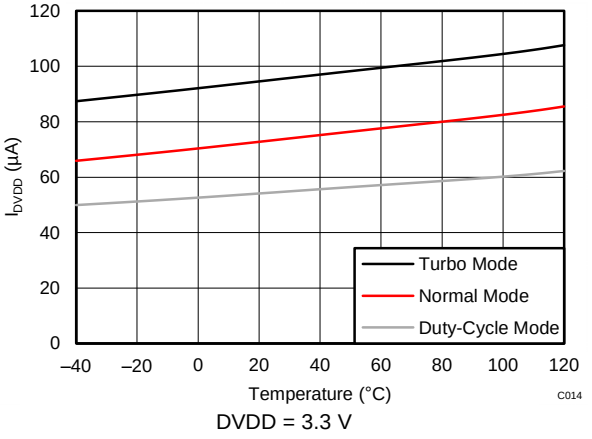


Figure 34. I_{DVDD} vs DVDD



DVDD = 3.3 V

Figure 35. I_{DVDD} vs Temperature

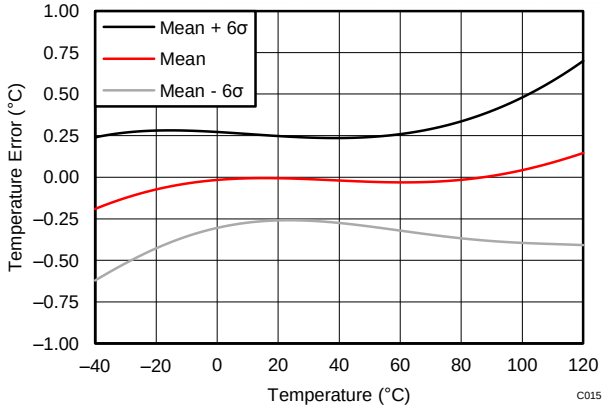


Figure 36. Internal Temperature Sensor Accuracy vs Temperature

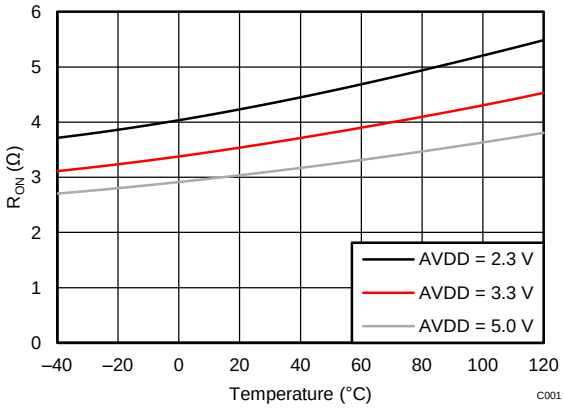


Figure 37. Low-Side Power Switch R_{ON} vs Temperature

7 Parameter Measurement Information

7.1 Noise Performance

Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are based on the principle of oversampling. The input signal of a ΔΣ ADC is sampled at a high frequency (modulator frequency) and subsequently filtered and decimated in the digital domain to yield a conversion result at the respective output data rate. The ratio between modulator frequency and output data rate is called *oversampling ratio* (OSR). By increasing the OSR, and thus reducing the output data rate, the noise performance of the ADC can be optimized. In other words, the input-referred noise drops when reducing the output data rate because more samples of the internal modulator are averaged to yield one conversion result. Increasing the gain also reduces the input-referred noise, which is particularly useful when measuring low-level signals.

Table 1 to Table 4 summarize the device noise performance. Data are representative of typical noise performance at T_A = 25°C using the internal 2.048-V reference. Data shown are the result of averaging readings from a single device over a time period of approximately 0.75 seconds and are measured with the inputs internally shorted together. Table 1 and Table 3 list the input-referred noise in units of μV_{RMS} for the conditions shown. Note that μV_{PP} values are shown in parenthesis. Table 2 and Table 4 list the corresponding data in effective number of bits (ENOB) calculated from μV_{RMS} values using Equation 1. Note that noise-free bits calculated from peak-to-peak noise values are shown in parenthesis.

The input-referred noise (Table 1 and Table 3) only changes marginally when using an external low-noise reference, such as the REF5020A-Q1. To calculate ENOB numbers and noise-free bits when using a reference voltage other than 2.048 V, use Equation 1 to Equation 3:

$$\text{ENOB} = \ln(\text{Full-Scale Range} / V_{RMS\text{-Noise}}) / \ln(2) \quad (1)$$

$$\text{Noise-Free Bits} = \ln(\text{Full-Scale Range} / V_{PP\text{-Noise}}) / \ln(2) \quad (2)$$

$$\text{Full-Scale Range} = 2 \cdot V_{ref} / \text{Gain} \quad (3)$$

Table 1. Noise in μV_{RMS} (μV_{PP}) at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (1.95)	0.98 (0.98)	0.49 (0.49)
45	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (1.95)	0.98 (0.98)	0.49 (0.51)
90	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)	7.81 (7.81)	3.91 (3.91)	1.95 (2.14)	0.98 (1.22)	0.49 (0.85)
175	62.50 (63.72)	31.25 (34.06)	15.63 (17.76)	7.81 (11.20)	3.91 (5.13)	1.95 (3.09)	0.98 (2.14)	0.49 (1.60)
330	62.50 (106.93)	31.25 (50.78)	15.63 (26.25)	7.81 (14.13)	3.91 (7.52)	1.95 (4.66)	0.98 (2.69)	0.49 (1.99)
600	62.50 (151.61)	31.25 (72.27)	15.63 (39.43)	7.81 (19.26)	3.91 (12.77)	1.95 (6.87)	0.98 (4.76)	0.55 (3.34)
1000	62.50 (227.29)	31.25 (122.68)	15.63 (58.53)	7.81 (31.52)	3.91 (18.08)	1.95 (10.71)	1.03 (6.52)	0.70 (4.01)
2000	62.50 (265.14)	31.25 (127.32)	15.63 (65.43)	7.81 (37.02)	3.91 (18.89)	1.95 (12.00)	1.13 (7.60)	0.82 (5.81)

Table 2. ENOB from RMS Noise (Noise-free Bits from Peak-to-Peak Noise) at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA ENABLED)							
	1	2	4	8	16	32	64	128
20	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)
45	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.49)
90	16 (16)	16 (16)	16 (16)	16 (16)	16 (16)	16 (15.87)	16 (15.67)	16 (15.20)
175	16 (15.97)	16 (15.88)	16 (15.82)	16 (15.48)	16 (15.61)	16 (15.34)	16 (14.87)	16 (14.29)
330	16 (15.23)	16 (15.30)	16 (15.25)	16 (15.15)	16 (15.05)	16 (14.74)	16 (14.54)	16 (13.97)
600	16 (14.72)	16 (14.79)	16 (14.66)	16 (14.70)	16 (14.29)	16 (14.18)	16 (13.72)	15.83 (13.23)
1000	16 (14.14)	16 (14.03)	16 (14.09)	16 (13.99)	16 (13.79)	16 (13.54)	15.92 (13.26)	15.49 (12.96)
2000	16 (13.92)	16 (13.97)	16 (13.93)	16 (13.76)	16 (13.73)	16 (13.38)	15.79 (13.04)	15.25 (12.43)

Table 3. Noise in μV_{RMS} (μV_{PP}) with PGA Disabled at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA DISABLED)		
	1	2	4
20	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
45	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
90	62.50 (62.50)	31.25 (31.25)	15.63 (15.63)
175	62.50 (65.92)	31.25 (35.40)	15.63 (18.92)
330	62.50 (94.24)	31.25 (50.17)	15.63 (28.75)
600	62.50 (138.67)	31.25 (78.13)	15.63 (39.79)
1000	62.50 (260.50)	31.25 (120.97)	15.63 (63.72)
2000	62.50 (250.98)	31.25 (131.35)	15.63 (68.18)

Table 4. ENOB from RMS Noise (Noise-free Bits from Peak-to-Peak Noise) with PGA Disabled at AVDD = 3.3 V, AVSS = 0 V, and Internal Reference = 2.048 V

DATA RATE (SPS)	GAIN (PGA DISABLED)		
	1	2	4
20	16 (16)	16 (16)	16 (16)
45	16 (16)	16 (16)	16 (16)
90	16 (16)	16 (16)	16 (16)
175	16 (15.92)	16 (15.82)	16 (15.72)
330	16 (15.41)	16 (15.32)	16 (15.12)
600	16 (14.85)	16 (14.68)	16 (14.65)
1000	16 (13.94)	16 (14.05)	16 (13.97)
2000	16 (13.99)	16 (13.93)	16 (13.87)

8 Detailed Description

8.1 Overview

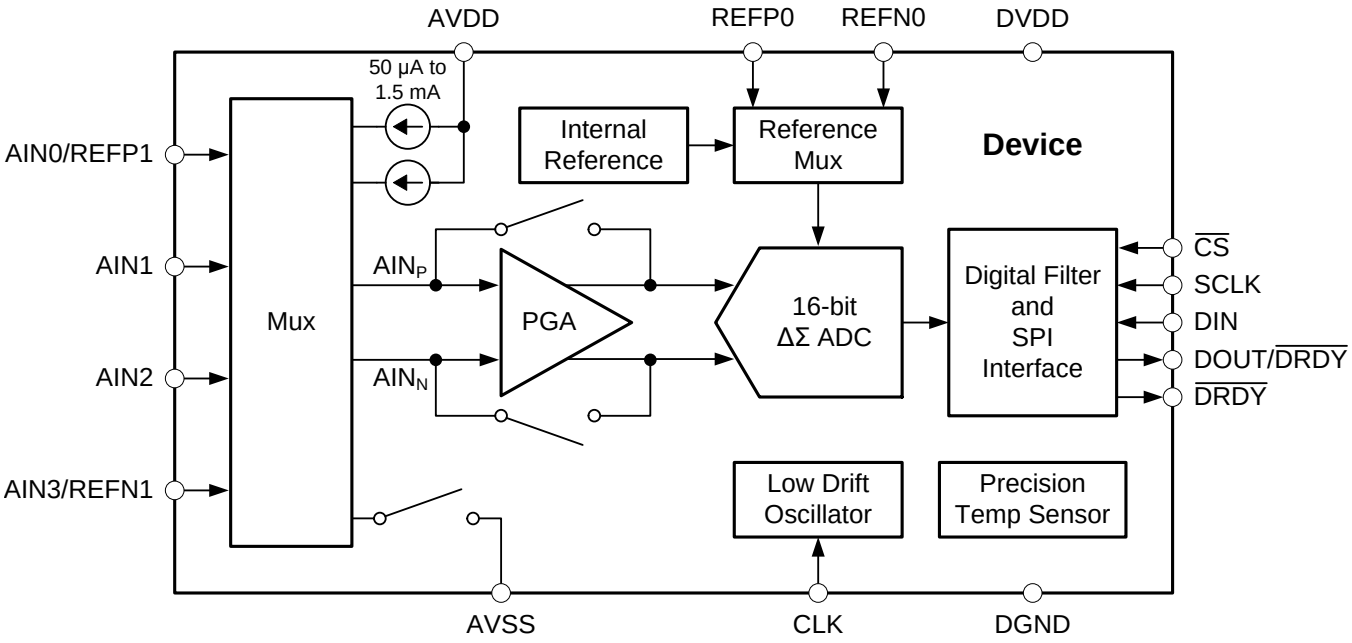
The ADS1120-Q1 is a small, low-power, 16-bit, ΔΣ ADC that offers many integrated features to reduce system cost and component count in applications measuring small sensor signals.

In addition to the ΔΣ ADC core and single-cycle settling digital filter, the device offers a low-noise, high input impedance, programmable gain amplifier (PGA), an internal voltage reference, and a clock oscillator. The device also integrates a highly linear and accurate temperature sensor as well as two matched programmable current sources (IDACs) for sensor excitation. All of these features are intended to reduce the required external circuitry in typical sensor applications and improve overall system performance. An additional low-side power switch eases the design of low-power bridge sensor applications. The device is fully configured through four registers and controlled by six commands through a mode 1 SPI-compatible interface. The *Functional Block Diagram* section shows the device functional block diagram.

The ADS1120-Q1 ADC measures a differential signal, V_{IN}, which is the difference in voltage between nodes AIN_P and AIN_N. The converter core consists of a differential, switched-capacitor, ΔΣ modulator followed by a digital filter. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage. This architecture results in a very strong attenuation of any common-mode signal.

The device has two available conversion modes: single-shot and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value in an internal data buffer. The device then enters a low-power state to save power. Single-shot mode is intended to provide significant power savings in systems that require only periodic conversions, or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. New data are available at the programmed data rate. Data can be read at any time without concern of data corruption and always reflect the most recently completed conversion.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Multiplexer

The device contains a very flexible input multiplexer, as shown in Figure 38. Either four single-ended signals, two differential signals, or a combination of two single-ended signals and one differential signal can be measured. The multiplexer is configured by four bits (MUX[3:0]) in the configuration register. When single-ended signals are measured, the negative ADC input (AIN_N) is internally connected to AVSS by a switch within the multiplexer. For system-monitoring purposes, the analog supply (AVDD – AVSS) / 4 or the currently-selected external reference voltage ($V_{(REFPx)} - V_{(REFNx)}$) / 4 can be selected as inputs to the ADC. The multiplexer also offers the possibility to route any of the two programmable current sources to any analog input (AINx) or to any dedicated reference pin (REFP0, REFN0).

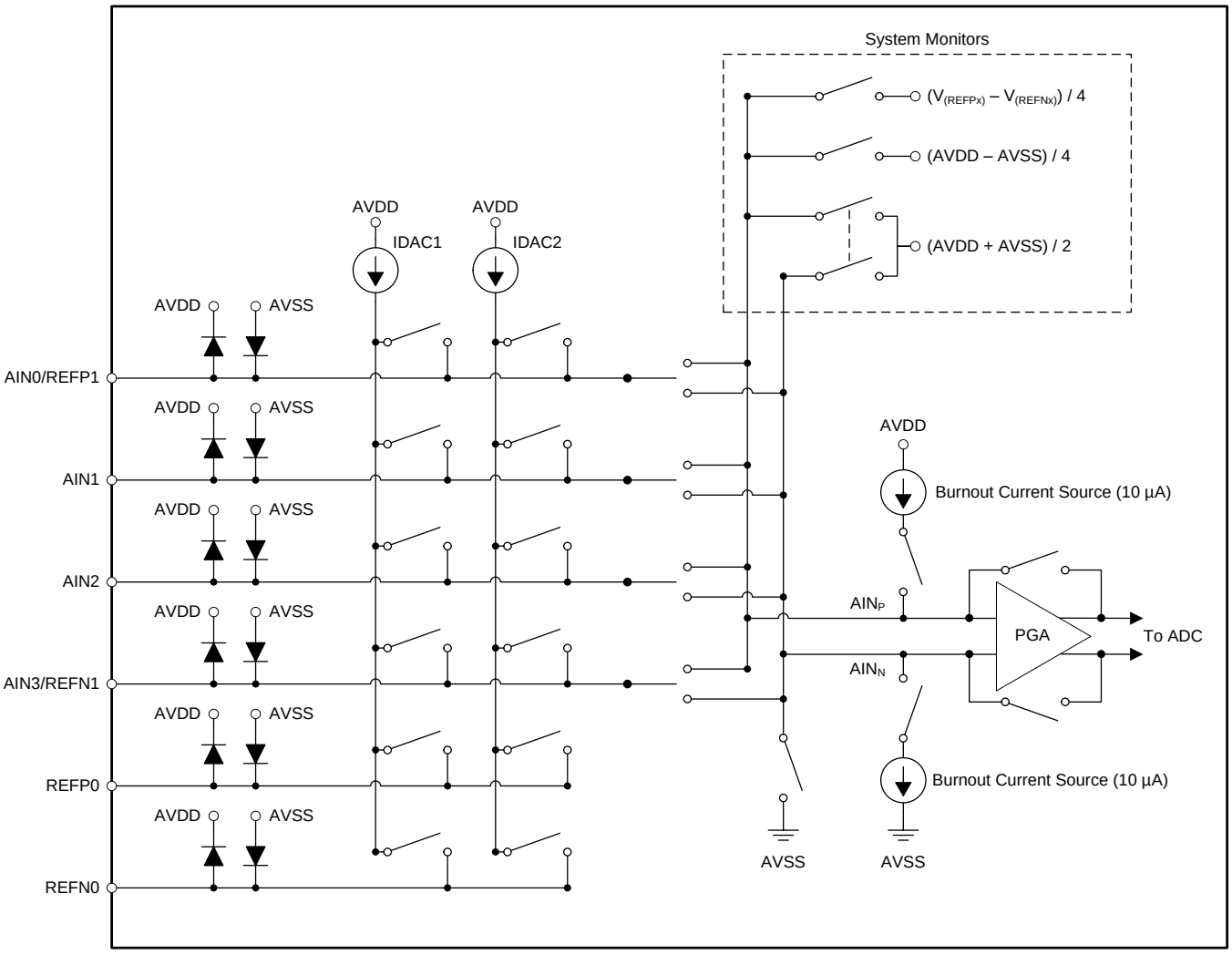


Figure 38. Analog Input Multiplexer

Electrostatic discharge (ESD) diodes to AVDD and AVSS protect the inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range provided by Equation 4:

$$AVSS - 0.3\ V < V_{(AINx)} < AVDD + 0.3\ V \quad (4)$$

If the voltages on the input pins have any potential to violate these conditions, external Schottky clamp diodes or series resistors may be required to limit the input current to safe values (see the *Absolute Maximum Ratings* table). Overdriving an unused input on the device may affect conversions taking place on other input pins. If any overdrive on unused inputs is possible, TI recommends clamping the signal with external Schottky diodes.

Feature Description (continued)

8.3.2 Low-Noise PGA

The device features a low-noise, low-drift, high input impedance, programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Three bits (GAIN[2:0]) in the configuration register are used to configure the gain. A simplified diagram of the PGA is shown in Figure 39. The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the PGA gain. The PGA input is equipped with an electromagnetic interference (EMI) filter.

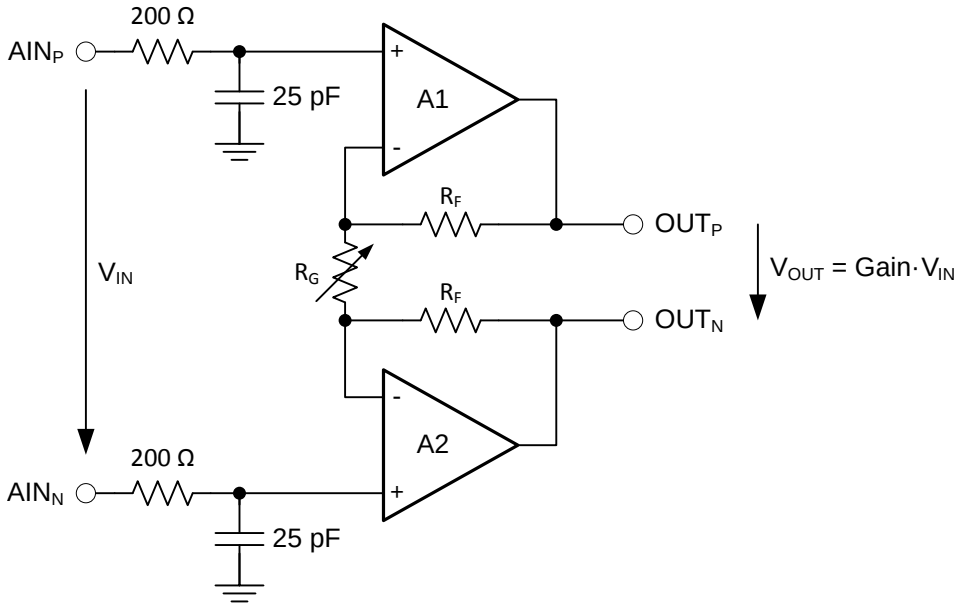


Figure 39. Simplified PGA Diagram

V_{IN} denotes the differential input voltage $V_{IN} = (V_{(AINP)} – V_{(AINN)})$. The gain of the PGA can be calculated with Equation 5:

$$\text{Gain} = 1 + 2 \cdot R_F / R_G \quad (5)$$

Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 6:

$$\text{FSR} = \pm V_{ref} / \text{Gain} \quad (6)$$

Table 5 shows the corresponding full-scale ranges when using the internal 2.048-V reference.

Table 5. PGA Full-Scale Range

GAIN SETTING	FSR
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

8.3.2.1 PGA Common-Mode Voltage Requirements

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section.

The outputs of both amplifiers (A1 and A2) in Figure 39 can not swing closer to the supplies (AVSS and AVDD) than 200 mV. If the outputs OUT_P and OUT_N are driven to within 200 mV of the supply rails, the amplifiers saturate and consequently become nonlinear. To prevent this nonlinear operating condition the output voltages must meet Equation 7:

$$AVSS + 0.2\ V \le V_{(OUTN)},\ V_{(OUTP)} \le AVDD - 0.2\ V \quad (7)$$

Translating the requirements of Equation 7 into requirements referred to the PGA inputs (AIN_P and AIN_N) is beneficial because there is no direct access to the outputs of the PGA. The PGA employs a symmetrical design, therefore the common-mode voltage at the output of the PGA can be assumed to be the same as the common-mode voltage of the input signal, as shown in Figure 40.

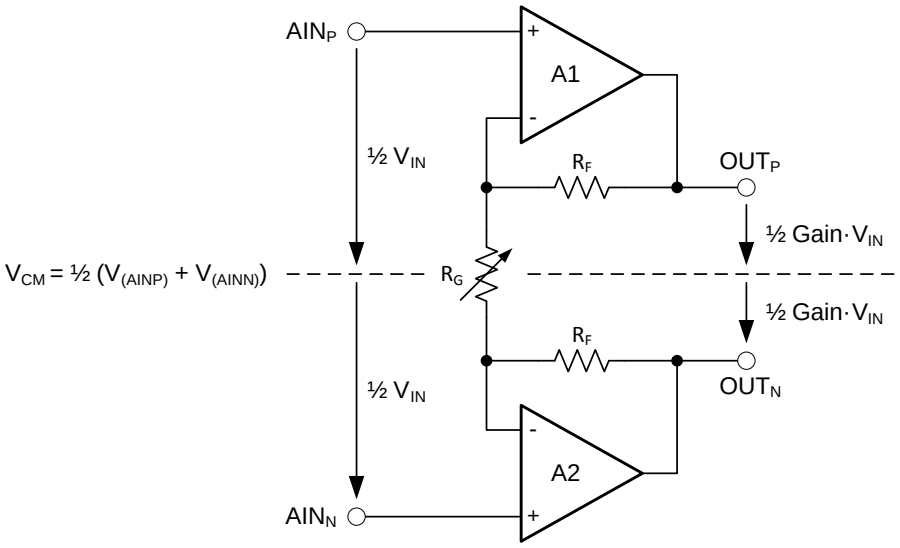


Figure 40. PGA Common-Mode Voltage

The common-mode voltage is calculated using Equation 8:

$$V_{CM} = ½\ (V_{(AINP)} + V_{(AINN)}) = ½\ (V_{(OUTP)} + V_{(OUTN)}) \quad (8)$$

The voltages at the PGA inputs (AIN_P and AIN_N) can be expressed as Equation 9 and Equation 10:

$$V_{(AINP)} = V_{CM} + ½\ V_{IN} \quad (9)$$

$$V_{(AINN)} = V_{CM} – ½\ V_{IN} \quad (10)$$

The output voltages ($V_{(OUTP)}$ and $V_{(OUTN)}$) can then be calculated as Equation 11 and Equation 12:

$$V_{(OUTP)} = V_{CM} + ½\ Gain \cdot V_{IN} \quad (11)$$

$$V_{(OUTN)} = V_{CM} – ½\ Gain \cdot V_{IN} \quad (12)$$

The requirements for the output voltages of amplifiers A1 and A2 (Equation 7) can now be translated into requirements for the input common-mode voltage range using Equation 11 and Equation 12, which are given in Equation 13 and Equation 14:

$$V_{CM\ (MIN)} \ge AVSS + 0.2\ V + ½\ Gain \cdot V_{IN\ (MAX)} \quad (13)$$

$$V_{CM\ (MAX)} \le AVDD – 0.2\ V – ½\ Gain \cdot V_{IN\ (MAX)} \quad (14)$$

In order to calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ($V_{IN\ (MAX)}$) that occurs in the application must be used. $V_{IN\ (MAX)}$ can be less than the maximum possible FS value.

In addition to Equation 13, the minimum V_{CM} must also meet Equation 15 because of the specific design implementation of the PGA.

$$V_{CM\ (MIN)} \ge AVSS + ¼\ (AVDD – AVSS) \quad (15)$$

Figure 41 and Figure 42 show a graphical representation of the common-mode voltage limits for AVDD = 3.3 V and AVSS = 0 V, with gain = 1 and gain = 16, respectively.

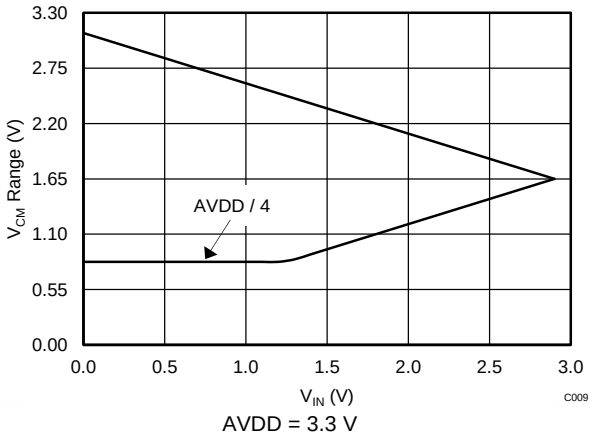


Figure 41. Common-Mode Voltage Limits (Gain = 1)

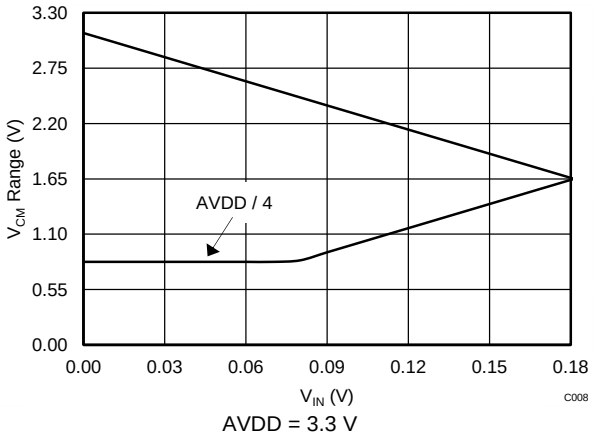


Figure 42. Common-Mode Voltage Limits (Gain = 16)

The following discussion explains how to apply Equation 13 through Equation 15 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference, V_{ref} = 2.5 V. The maximum possible differential input voltage $V_{IN} = (V_{(AINP)} – V_{(AINN)})$ that can be applied is then limited to the full-scale range of FSR = ±2.5 V / 16 = ±0.156 V. Consequently, Equation 13 through Equation 15 yield an allowed V_{CM} range of 1.45 V ≤ V_{CM} ≤ 1.85 V.

If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire full-scale range but is limited to $V_{IN\ (MAX)}$ = ±0.1 V, for example, then this reduced input signal amplitude relaxes the V_{CM} restriction to 1.0 V ≤ V_{CM} ≤ 2.3 V.

In the case of a fully-differential sensor signal, each input (AIN_P, AIN_N) can swing up to ±50 mV around the common-mode voltage $(V_{(AINP)} + V_{(AINN)}) / 2$, which must remain between the limits of 1.0 V and 2.3 V. The output of a symmetrical wheatstone bridge is an example of a fully-differential signal. Figure 43 shows a situation where the common-mode voltage of the input signal is at the lowest limit. $V_{(OUTN)}$ is exactly at 0.2 V in this case. Any further decrease in common-mode voltage (V_{CM}) or increase in differential input voltage (V_{IN}) drives $V_{(OUTN)}$ below 0.2 V and saturates amplifier A2.

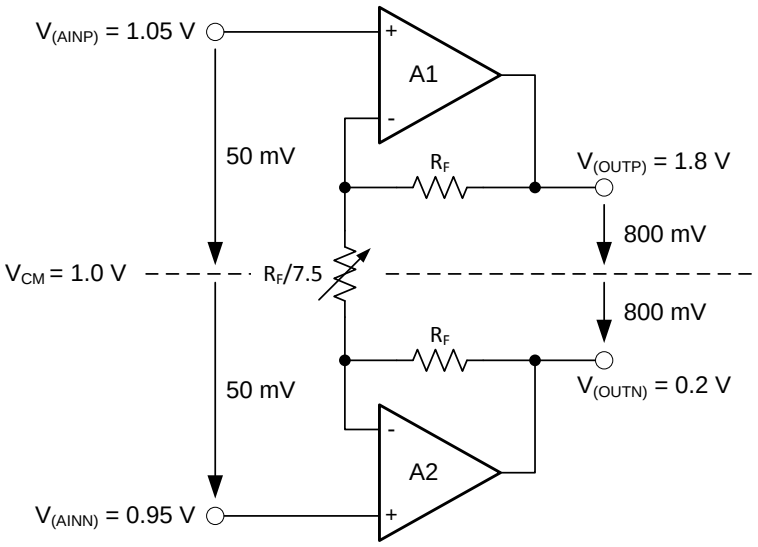


Figure 43. Example where V_{CM} is at Lowest Limit

In contrast, the signal of an RTD is of a pseudo-differential nature (if implemented as shown in the *RTD Measurement* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage between 0.95 V and 2.25 V. The positive input can then swing up to $V_{IN\ (MAX)}$ = 100 mV above the negative input. Note that in this case the common-mode voltage changes at the same time the voltage on the positive input changes. That is, while the input signal swings between 0 V ≤ V_{IN} ≤ $V_{IN\ (MAX)}$, the common-mode voltage swings between $V_{(AINN)}$ ≤ V_{CM} ≤ $V_{(AINN)}$ + ½ $V_{IN\ (MAX)}$. Satisfying the common-mode voltage requirements for the maximum input voltage $V_{IN\ (MAX)}$ ensures the requirements are met throughout the entire signal range.

Figure 44 and Figure 45 show examples of both fully-differential and pseudo-differential signals, respectively.

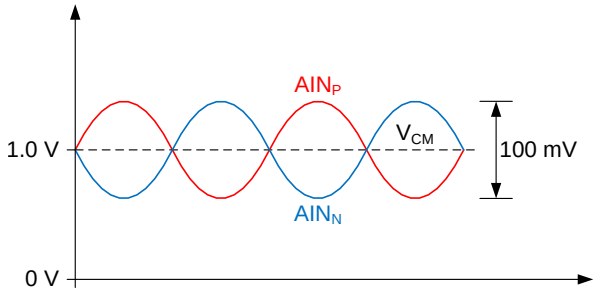


Figure 44. Fully-Differential Input Signal

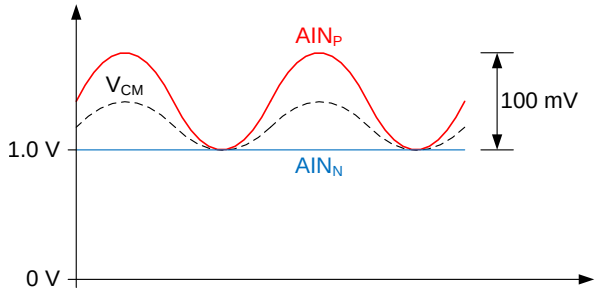


Figure 45. Pseudo-Differential Input Signal

NOTE

Remember, common-mode voltage requirements with PGA enabled (Equation 13 to Equation 15) are as follows:

- $V_{CM\ (MIN)}$ ≥ AVSS + ¼ (AVDD – AVSS)
- $V_{CM\ (MIN)}$ ≥ AVSS + 0.2 V + ½ Gain · $V_{IN\ (MAX)}$
- $V_{CM\ (MAX)}$ ≤ AVDD – 0.2 V – ½ Gain · $V_{IN\ (MAX)}$

8.3.2.2 Bypassing the PGA

At gains of 1, 2, and 4, the device can be configured to disable and bypass the low-noise PGA. Disabling the PGA lowers the overall power consumption and also removes the restrictions of Equation 13 through Equation 15 for the common-mode input voltage range, V_{CM}. The usable absolute and common-mode input voltage range is (AVSS – 0.1 V ≤ $V_{(AINx)}$, V_{CM} ≤ AVDD + 0.1 V) when the PGA is disabled. In order to measure single-ended signals that are referenced to AVSS (AIN_P = V_{IN}, AIN_N = AVSS), the PGA must be bypassed.

The PGA is disabled by setting the PGA_BYPASS bit in the configuration register. When the PGA is disabled, the device uses a buffered switched-capacitor stage to obtain gains 1, 2, and 4. An internal buffer in front of the switched-capacitor stage ensures that the effect on the input loading resulting from the capacitor charging and discharging is minimal. Refer to Figure 21 to Figure 26 for the typical values of absolute input currents (current flowing into or out of each input) and differential input currents (difference in absolute current between positive and negative input) when the PGA is disabled.

For signal sources with high output impedance, external buffering may still be necessary. Note that active buffers introduce noise and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

8.3.3 Modulator

A ΔΣ modulator is used in the ADS1120-Q1 to convert the analog input voltage into a pulse code modulated (PCM) data stream. The modulator runs at a modulator clock frequency of $f_{(MOD)} = f_{(CLK)} / 16$ in normal and duty-cycle mode and $f_{(MOD)} = f_{(CLK)} / 8$ in turbo mode, where $f_{(CLK)}$ is either provided by the internal oscillator or the external clock source. Table 6 shows the modulator frequency for each operating mode using either the internal oscillator or an external clock of 4.096 MHz.

Table 6. Modulator Clock Frequency for Different Operating Modes(1)

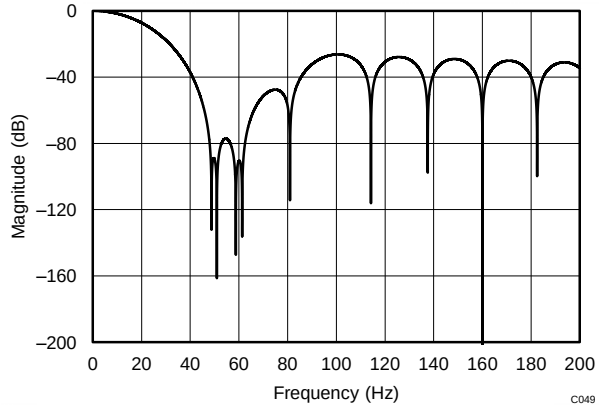
OPERATING MODE	$f_{(MOD)}$
Duty-cycle mode	256 kHz
Normal mode	256 kHz
Turbo mode	512 kHz

(1) Using the internal oscillator or an external 4.096-MHz clock.

8.3.4 Digital Filter

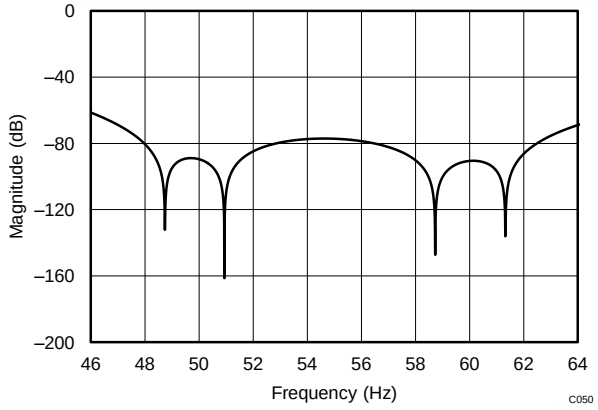
The device uses a linear-phase finite impulse response (FIR) digital filter that performs both filtering and decimation of the digital data stream coming from the modulator. The digital filter is automatically adjusted for the different data rates and always settles within a single cycle. At data rates of 5 SPS and 20 SPS, the filter can be configured to reject 50-Hz or 60-Hz line frequencies or to simultaneously reject 50 Hz and 60 Hz. Two bits (50/60[1:0]) in the configuration register are used to configure the filter accordingly. The frequency responses of the digital filter are shown in Figure 46 to Figure 59 for different output data rates using the internal oscillator or an external 4.096-MHz clock.

The filter notches and output data rate scale proportionally with the clock frequency. For example, a notch that appears at 20 Hz when using a 4.096-MHz clock appears at 10 Hz if a 2.048-MHz clock is used. Note that the internal oscillator can vary over temperature as specified in the *Electrical Characteristics* table. The data rate or conversion time, respectively, and filter notches consequently vary by the same amount. Consider using an external precision clock source if a digital filter notch at a specific frequency with a tighter tolerance is required.



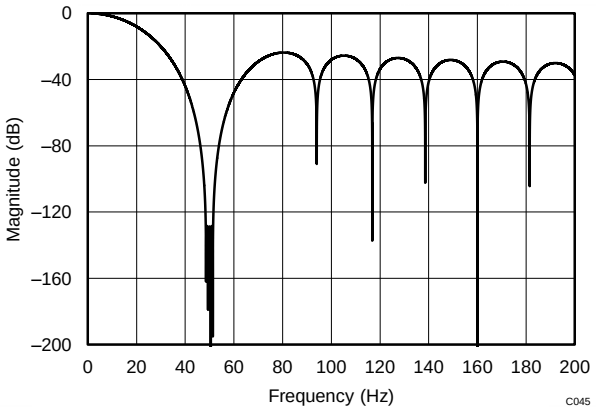
Simultaneous 50-Hz and 60-Hz Rejection, 50/60[1:0] = 01

Figure 46. Filter Response (DR = 20 SPS)



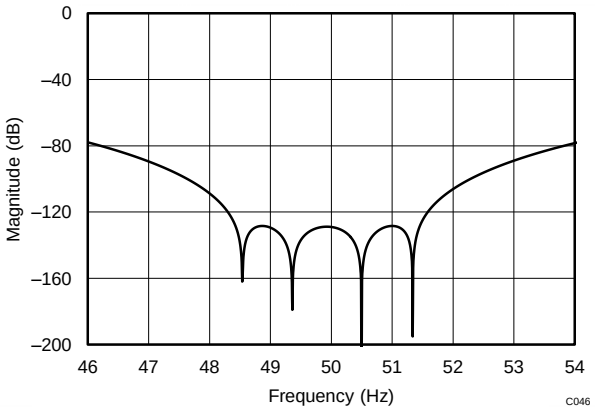
Simultaneous 50-Hz and 60-Hz Rejection, 50/60[1:0] = 01

Figure 47. Detailed View of Filter Response (DR = 20 SPS)



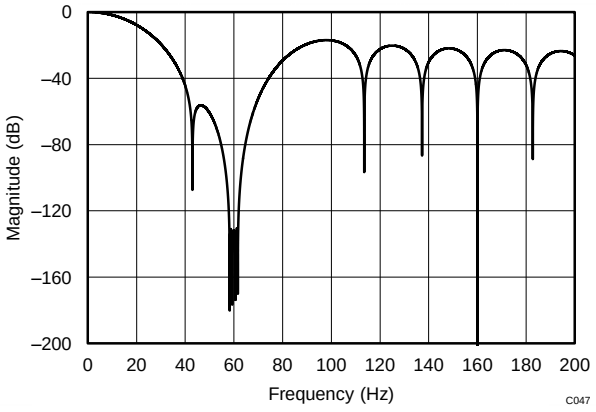
50-Hz Rejection Only, 50/60[1:0] = 10

Figure 48. Filter Response (DR = 20 SPS)



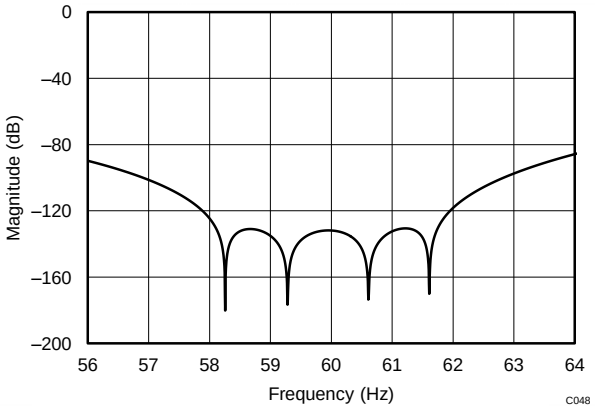
50-Hz Rejection Only, 50/60[1:0] = 10

Figure 49. Detailed View of Filter Response (DR = 20 SPS)



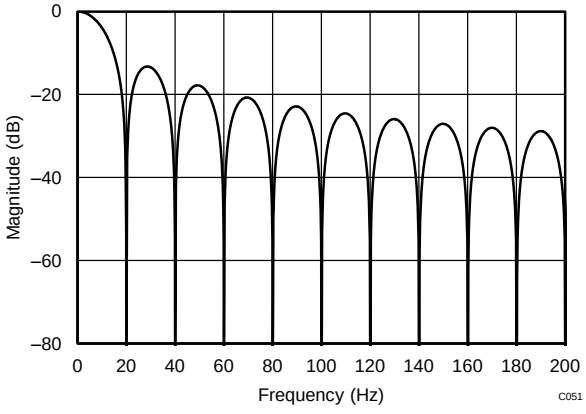
60-Hz Rejection Only, 50/60[1:0] = 11

Figure 50. Filter Response (DR = 20 SPS)



60-Hz Rejection Only, 50/60[1:0] = 11

Figure 51. Detailed View of Filter Response (DR = 20 SPS)



50/60[1:0] = 00

Figure 52. Filter Response (DR = 20 SPS)

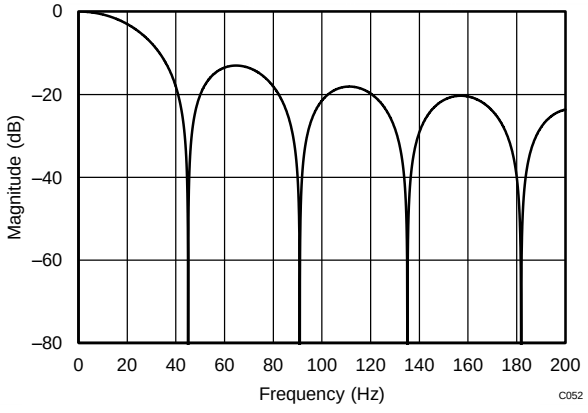


Figure 53. Filter Response (DR = 45 SPS)

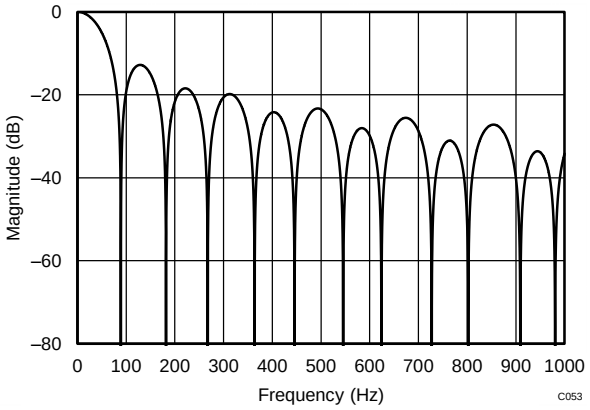


Figure 54. Filter Response (DR = 90 SPS)

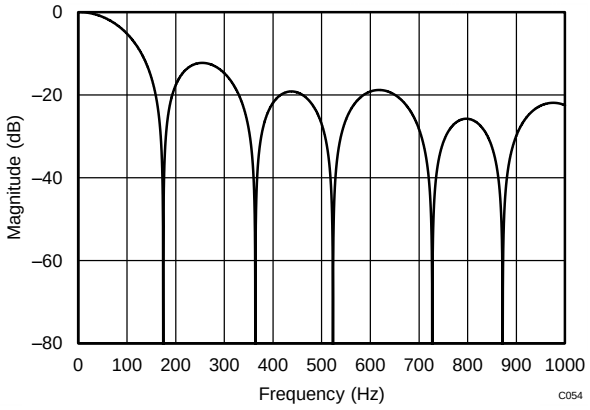


Figure 55. Filter Response (DR = 175 SPS)

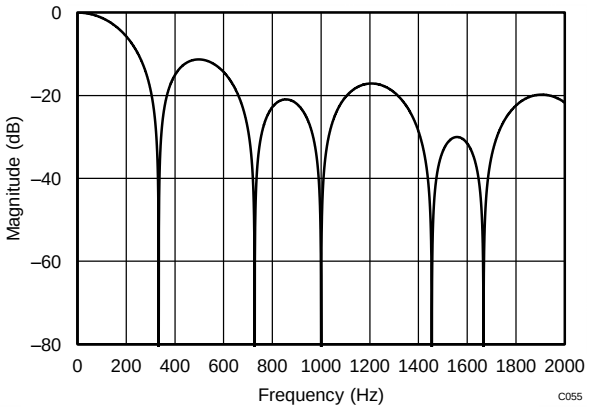


Figure 56. Filter Response (DR = 330 SPS)

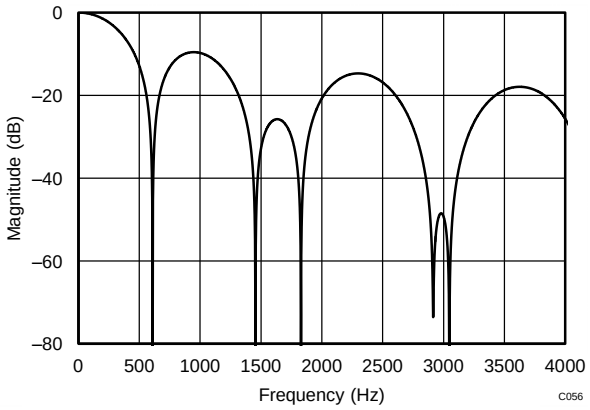


Figure 57. Filter Response (DR = 600 SPS)

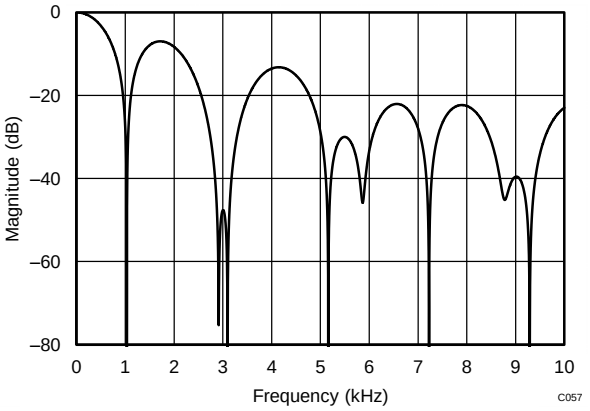


Figure 58. Filter Response (DR = 1 kSPS)

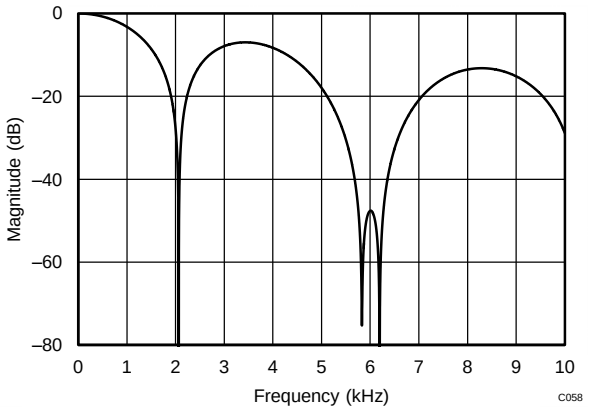


Figure 59. Filter Response (DR = 2 kSPS)

8.3.5 Output Data Rate

Table 7 shows the actual conversion times for each data rate setting. The values provided are in terms of $t_{(CLK)}$ cycles using an external clock with a clock frequency of $f_{(CLK)}$ = 4.096 MHz. The data rates scale proportionally in case an external clock with a frequency other than 4.096 MHz is used.

Continuous conversion mode data rates are timed from one $\overline{DRDY}$ falling edge to the next $\overline{DRDY}$ falling edge. The first conversion starts 210 · $t_{(CLK)}$ (normal mode, duty-cycle mode) or 114 · $t_{(CLK)}$ (turbo mode) after the last SCLK falling edge of the START/SYNC command.

Single-shot mode data rates are timed from the last SCLK falling edge of the START/SYNC command to the $\overline{DRDY}$ falling edge and rounded to the next $t_{(CLK)}$. In case the internal oscillator is used, an additional oscillator wake-up time of up to 50 µs (normal mode, duty-cycle mode) or 25 µs (turbo mode) must be added in single-shot mode. The internal oscillator starts to power up at the first SCLK rising edge of the START/SYNC command. If an SCLK frequency higher than 160 kHz (normal mode, duty-cycle mode) or 320 kHz (turbo mode) is used, the oscillator may not be fully powered up at the end of the START/SYNC command. The ADC then waits until the internal oscillator is fully powered up before starting a conversion.

Single-shot conversion times in duty-cycle mode are the same as in normal mode. See the *Duty-Cycle Mode* section for more details on duty-cycle mode operation.

Table 7. Conversion Times

NOMINAL DATA RATE (SPS)	–3-dB BANDWIDTH (Hz)	ACTUAL CONVERSION TIME ($t_{(CLK)}$)	
		CONTINUOUS CONVERSION MODE	SINGLE-SHOT MODE
Normal Mode			
20	13.1	204768	204850
45	20.0	91120	91218
90	39.6	46128	46226
175	77.8	23664	23762
330	150.1	12464	12562
600	279.0	6896	6994
1000	483.8	4144	4242
Duty-Cycle Mode			
5	13.1	823120	n/a
11.25	20.0	364560	n/a
22.5	39.6	184592	n/a
44	77.8	94736	n/a
82.5	150.1	49936	n/a
150	279.0	27664	n/a
250	483.8	16656	n/a
Turbo Mode			
40	26.2	102384	102434
90	39.9	45560	45618
180	79.2	23064	23122
350	155.6	11832	11890
660	300.3	6232	6290
1200	558.1	3448	3506
2000	967.6	2072	2130

Note that even though the conversion time at the 20-SPS setting is not exactly 1 / 20 Hz = 50 ms, this discrepancy does not affect the 50-Hz or 60-Hz rejection. To achieve the 50-Hz and 60-Hz rejection specified in the *Electrical Characteristics*, the external clock frequency must be 4.096 MHz. When using the internal oscillator, the conversion time and filter notches vary by the amount specified in the *Electrical Characteristics* table for oscillator accuracy.

8.3.6 Voltage Reference

The device offers an integrated low-drift, 2.048-V reference. For applications that require a different reference voltage value or a ratiometric measurement approach, the device offers two differential reference input pairs (REFP0, REFN0 and REFP1, REFN1). In addition, the analog supply (AVDD) can be used as a reference.

The reference source is selected by two bits (VREF[1:0]) in the configuration register. By default, the internal reference is selected. The internal voltage reference requires less than 25 µs to fully settle after power-up, when coming out of power-down mode, or when switching from an external reference source to the internal reference.

The differential reference inputs allow freedom in the reference common-mode voltage. REFP0 and REFN0 are dedicated reference inputs whereas REFP1 and REFN1 are shared with inputs AIN0 and AIN3, respectively. All reference inputs are internally buffered to increase input impedance. Therefore, additional reference buffers are usually not required when using an external reference. When used in ratiometric applications, the reference inputs do not load the external circuitry. Note that the analog supply current increases by approximately 75 µA when using an external reference because the reference buffers are enabled. In most cases the conversion result is directly proportional to the stability of the reference source. Any noise and drift of the source is reflected in the conversion result.

8.3.7 Clock Source

The device system clock can either be provided by the internal low-drift oscillator or by an external clock source on the CLK input. Connect the CLK pin to DGND before power-up or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator after two rising edges on the CLK pin are detected. The device then operates on the external clock. After the ADS1120-Q1 switches to the external clock, the device can only be switched back to the internal oscillator by cycling the power supplies or by sending a RESET command.

8.3.8 Excitation Current Sources

The device provides two matched programmable excitation current sources (IDACs) for RTD applications. The output current of the current sources can be programmed to 50 µA, 100 µA, 250 µA, 500 µA, 1000 µA, or 1500 µA using the respective bits (IDAC[2:0]) in the configuration register. Each current source can be connected to any of the analog inputs (AINx) as well as to any of the dedicated reference inputs (REFP0 and REFN0). Both current sources can also be connected to the same pin. Routing of the IDACs is configured by bits (I1MUX[2:0], I2MUX[2:0]) in the configuration register. Care must be taken not to exceed the compliance voltage of the IDACs. In other words, limit the voltage on the pin where the IDAC is routed to ≤ (AVDD – 0.9 V), otherwise the specified accuracy of the IDAC current is not met. For three-wire RTD applications, the matched current sources can be used to cancel errors caused by sensor lead resistance (see the *3-Wire RTD Measurement* section for more details).

The IDACs require up to 200 µs to start up after the IDAC current is programmed to the respective value using bits IDAC[2:0]. If configuration registers 2 and 3 are not written during the same WREG command, TI recommends to first set the IDAC current to the respective value using bits IDAC[2:0] and thereafter select the routing for each IDAC (I1MUX[2:0], I2MUX[2:0]).

In single-shot mode, the IDACs remain active between any two conversions if the IDAC[2:0] bits are set to a value other than 000. However, the IDACs are powered down whenever the POWERDOWN command is issued.

8.3.9 Low-Side Power Switch

A low-side power switch with low on-resistance connected between the analog input AIN3/REFN1 and AVSS is integrated in the device as well. This power switch can be used to reduce system power consumption in bridge sensor applications by powering down the bridge circuit between conversions. When the respective bit (PSW) in the configuration register is set, the switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued. Note that the switch stays closed between conversions in single-shot mode in case the PSW bit is set to 1. The switch can be opened at any time by setting the PSW bit to 0. By default, the switch is always open.

8.3.10 Sensor Detection

To help detect a possible sensor malfunction, the device provides internal 10-µA, burn-out current sources. When enabled by setting the respective bit (BCS) in the configuration register, one current source sources current to the positive analog input (AIN_P) currently selected while the other current source sinks current form the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading may also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading may indicate a shorted sensor. Note that the absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

Keep in mind that ADC readings of a functional sensor may be corrupted when the burn-out current sources are enabled. TI recommends disabling the burn-out current sources when preforming the precision measurement, and only enabling them to test for sensor fault conditions.

8.3.11 System Monitor

The device provides some means for monitoring the analog power supply and the external voltage reference. To select a monitoring voltage, the internal multiplexer (MUX[3:0]) must be configured accordingly in the configuration register. The device automatically bypasses the PGA and sets the gain to 1, irrespective of the configuration register settings while the monitoring feature is used. Note that the system monitor function only provides a coarse result and is not meant to be a precision measurement.

When measuring the analog power supply (MUX[3:0] = 1101), the resulting conversion is approximately (AVDD – AVSS) / 4. The device uses the internal 2.048-V reference for the measurement regardless of what reference source is selected in the configuration register (VREF[1:0]).

When monitoring one of the two possible external reference voltage sources (MUX[3:0] = 1100), the result is approximately ($V_{(REFPx)} – V_{(REFNx)}$) / 4. REFPx and REFNx denote the external reference input pair selected in the configuration register (VREF[1:0]). The device automatically uses the internal reference for the measurement.

8.3.12 Offset Calibration

The internal multiplexer offers the option to short both PGA inputs (AIN_P and AIN_N) to mid-supply (AVDD + AVSS) / 2. This option can be used to measure and calibrate the device offset voltage by storing the result of the shorted input voltage reading in a microcontroller and consequently subtracting the result from each following reading. TI recommends taking multiple readings with the inputs shorted and averaging the result to reduce the effect of noise.

8.3.13 Power Supplies

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels. The power supplies can be sequenced in any order but in no case can any analog or digital inputs exceed the respective analog or digital power-supply voltage limits.

8.3.14 Temperature Sensor

The ADS1120-Q1 offers an integrated precision temperature sensor. The temperature sensor mode is enabled by setting bit TS = 1 in the configuration register. When in temperature sensor mode, the settings of configuration register 0 have no effect and the device uses the internal reference for measurement, regardless of the selected voltage reference source. Temperature data are represented as a 14-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 14 bits are used to indicate the temperature measurement result. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format, as shown in Table 8.

Table 8. 14-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0.03125	00 0000 0000 0001	0001
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–55	11 1001 0010 0000	3920

8.3.14.1 Converting from Temperature to Digital Codes

8.3.14.1.1 For Positive Temperatures (for Example, 50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit, left-justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.03125°C per count) = 1600 = 0640h = 00 0110 0100 0000

8.3.14.1.2 For Negative Temperatures (for Example, –25°C):

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.03125°C per count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

8.3.14.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all bits. Then, multiply the result by –0.03125°C.

Example: The device reads back 0960h: 0960h has an MSB = 0.

0960h · 0.03125°C = 2400 · 0.03125°C = 75°C

Example: The device reads back 3CE0h: 3CE0h has an MSB = 1.

Complement the result: 3CE0h → 0320h

0320h · 0.03125°C = 800 · 0.03125°C = –25°C

8.4 Device Functional Modes

8.4.1 Power-Up and Reset

When the device powers up, a reset is performed. The reset process takes approximately 50 µs. After this power-up reset time, all internal circuitry (including the voltage reference) are stable and communication with the device is possible. As part of the reset process, the device sets all bits in the configuration registers to the respective default settings. By default, the device is set to single-shot mode. After power-up, the device performs a single conversion using the default register settings and then enters a low-power state. When the conversion is complete, the $\overline{DRDY}$ pin transitions from high to low. The high-to-low transition of the $\overline{DRDY}$ pin can be used to signal that the ADS1120-Q1 is operational and ready to use. The power-up behavior is intended to prevent systems with tight power-supply requirements from encountering a current surge during power-up.

8.4.2 Conversion Modes

The device can be operated in one of two conversion modes that can be selected by the CM bit in the configuration register. These conversion modes are single-shot and continuous conversion mode.

8.4.2.1 Single-Shot Mode

In single-shot mode, the device only performs a conversion when a START/SYNC command is issued. The device consequently performs one single conversion and returns to a low-power state afterwards. The internal oscillator and all analog circuitry (except for the excitation current sources) are turned off while the device waits in this low-power state until the next conversion is started. In addition, every write access to any configuration register also starts a new conversion. Writing to any configuration register while a conversion is ongoing functions as a new START/SYNC command that stops the current conversion and restarts a single new conversion. Each conversion is fully settled (assuming the analog input signal settles to its final value before the conversion starts) because the device digital filter settles within a single cycle.

8.4.2.2 Continuous Conversion Mode

In continuous conversion mode, the device continuously performs conversions. When a conversion completes, the device places the result in the output buffer and immediately begins another conversion.

In order to start continuous conversion mode, the CM bit must be set to 1 followed by a START/SYNC command. The first conversion starts $210 \cdot t_{(CLK)}$ (normal mode, duty-cycle mode) or $114 \cdot t_{(CLK)}$ (turbo mode) after the last SCLK falling edge of the START/SYNC command. Writing to any configuration register during an ongoing conversion restarts the current conversion. TI recommends always sending a START/SYNC command immediately after the CM bit is set to 1.

Device Functional Modes (continued)

8.4.3 Operating Modes

In addition to the different conversion modes, the device can also be operated in different operating modes that can be selected to trade-off power consumption, noise performance, and output data rate. These modes are: normal mode, duty-cycle mode, turbo mode, and power-down mode.

8.4.3.1 Normal Mode

Normal mode is the default mode of operation after power-up. In this mode, the internal modulator of the ΔΣ ADC runs at a modulator clock frequency of $f_{(MOD)} = f_{(CLK)} / 16$, where the system clock ($f_{(CLK)}$) is either provided by the internal oscillator or the external clock source. The modulator frequency is 256 kHz when using the internal oscillator. Normal mode offers output data rate options ranging from 20 SPS to 1 kSPS with the internal oscillator. The data rate is selected by the DR[2:0] bits in the configuration register. In case an external clock source with a clock frequency other than 4.096 MHz is used, the data rates scale accordingly. For example, using an external clock with $f_{(CLK)}$ = 2.048 MHz yields data rates ranging from 10 SPS to 500 SPS.

8.4.3.2 Duty-Cycle Mode

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the device supports an automatic duty-cycle mode that can yield significant power savings by periodically entering a low-power state between conversions. In principle, the device runs in normal mode with a duty cycle of 25%. This functionality means the device performs one conversion in the same manner as when running in normal mode but then automatically enters a low power-state for three consecutive conversion cycles. The noise performance in duty-cycle mode is therefore comparable to the noise performance in normal mode at four times the data rate. Data rates in duty-cycle mode range from 5 SPS to 250 SPS with the internal oscillator.

8.4.3.3 Turbo Mode

Applications that require higher data rates up to 2 kSPS can operate the device in turbo mode. In this mode, the internal modulator runs at a higher frequency of $f_{(MOD)} = f_{(CLK)} / 8$. $f_{(MOD)}$ equals 512 kHz when the internal oscillator or an external 4.096-MHz clock is used. Note that the device power consumption increases because the modulator runs at a higher frequency. Running the ADS1120-Q1 in turbo mode at a comparable output data rate as in normal mode yields better noise performance. For example, the input-referred noise at 90 SPS in turbo mode is lower than the input-referred noise at 90 SPS in normal mode.

8.4.3.4 Power-Down Mode

When the POWERDOWN command is issued, the device enters power-down mode after completing the current conversion. In this mode, all analog circuitry (including the voltage reference and both IDACs) are powered down, the low-side power switch is opened, and the device typically only uses 400 nA of current. While in power-down mode, the device holds the configuration register settings and responds to commands, but does not perform any data conversions.

Issuing a START/SYNC command wakes up the device and either starts a single conversion or starts continuous conversion mode, depending on the conversion mode selected by the CM bit. Note that writing to any configuration register wakes up the device as well, but only starts a single conversion regardless of the selected conversion mode (CM).

8.5 Programming

8.5.1 Serial Interface

The SPI-compatible serial interface of the device is used to read conversion data, read and write the device configuration registers, and control device operation. Only SPI mode 1 (CPOL = 0, CPHA = 1) is supported. The interface consists of five control lines ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$) but can be used with only four or even three control signals as well. The dedicated data-ready signal ($\overline{DRDY}$) can be configured to be shared with DOUT/$\overline{DRDY}$. If the serial bus is not shared with any other device, $\overline{CS}$ can be tied low permanently so that only signals SCLK, DIN, and DOUT/$\overline{DRDY}$ are required to communicate with the device.

8.5.1.1 Chip Select ($\overline{CS}$)

Chip select ($\overline{CS}$) is an active-low input that selects the device for SPI communication. This feature is useful when multiple devices share the same serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state; as such, DOUT/$\overline{DRDY}$ cannot indicate when data are ready. In situations where multiple devices are present on the bus, the dedicated $\overline{DRDY}$ pin can provide an uninterrupted monitor of the conversion status. If the serial bus is not shared with another peripheral, $\overline{CS}$ can be tied low.

8.5.1.2 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data into and out of the device on the DIN and DOUT/$\overline{DRDY}$ pins, respectively. Even though the input has hysteresis, TI recommends keeping the SCLK signal as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

8.5.1.3 Data Ready ($\overline{DRDY}$)

$\overline{DRDY}$ indicates when a new conversion result is ready for retrieval. When $\overline{DRDY}$ falls low, new conversion data are ready. $\overline{DRDY}$ transitions back high on the next SCLK rising edge. When no data are read during continuous conversion mode, $\overline{DRDY}$ remains low but pulses high for a duration of $2 \cdot t_{(MOD)}$ prior to the next $\overline{DRDY}$ falling edge. The $\overline{DRDY}$ pin is always actively driven, even when $\overline{CS}$ is high.

8.5.1.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data (commands and register data) to the device. The device latches data on DIN on the SCLK falling edge. The device never drives the DIN pin.

8.5.1.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)

DOUT/$\overline{DRDY}$ serves a dual-purpose function. This pin is used with SCLK to read conversion and register data from the device. Data on DOUT/$\overline{DRDY}$ are shifted out on the SCLK rising edge. DOUT/$\overline{DRDY}$ goes to a high-impedance state when $\overline{CS}$ is high.

In addition, the DOUT/$\overline{DRDY}$ pin can also be configured as a data-ready indicator by setting the DRDYM bit high in the configuration register. DOUT/$\overline{DRDY}$ then transitions low at the same time that the $\overline{DRDY}$ pin goes low to indicate new conversion data are available. Both signals can be used to detect if new data are ready. However, because DOUT/$\overline{DRDY}$ is disabled when $\overline{CS}$ is high, the recommended method of monitoring the end of a conversion when multiple devices are present on the SPI bus is to use the dedicated $\overline{DRDY}$ pin.

8.5.1.6 SPI Timeout

The ADS1120-Q1 offers an SPI timeout feature that can be used to recover communication when a serial interface transmission is interrupted. This feature is especially useful in applications where $\overline{CS}$ is permanently tied low and not used to frame a communication sequence. Whenever a complete command is not sent within $13955 \cdot t_{(MOD)}$ (normal mode, duty-cycle mode) or $27910 \cdot t_{(MOD)}$ (turbo mode), the serial interface resets and the next SCLK pulse starts a new communication cycle.

Programming (continued)

8.5.2 Data Format

The device provides 16 bits of data in binary twos complement format. The size of one code (LSB) is calculated using Equation 16.

$$1\ \text{LSB} = (2 \cdot V_{ref} / \text{Gain}) / 2^{16} = \text{FS} / 2^{15} \quad (16)$$

A positive full-scale input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{ref} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{ref} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale.

Table 9 summarizes the ideal output codes for different input signals.

Table 9. Ideal Output Code versus Input Signal

INPUT SIGNAL $V_{IN} = (V_{(AINP)} - V_{(AINN)})$	IDEAL OUTPUT CODE(1)
≥ +FS ($2^{15} - 1$) / 2^{15}	7FFFh
+FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

Mapping of the analog input signal to the output codes is shown in Figure 60.

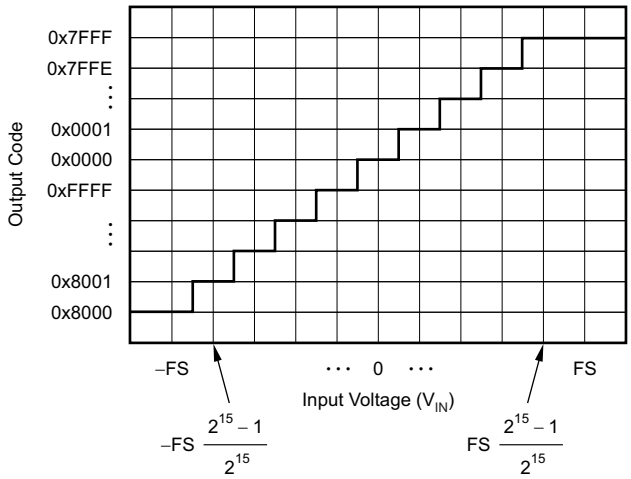


Figure 60. Code Transition Diagram

8.5.3 Commands

The device offers six different commands to control device operation, as shown in Table 10. Four commands are stand-alone instructions (RESET, START/SYNC, POWERDOWN, and RDATA). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction.

Table 10. Command Definitions

COMMAND	DESCRIPTION	COMMAND BYTE (1)
RESET	Reset the device	0000 011x
START/SYNC	Start or restart conversions	0000 100x
POWERDOWN	Enter power-down mode	0000 001x
RDATA	Read data by command	0001 xxxx
RREG	Read *nn* registers starting at address *rr*	0010 *rrnn*
WREG	Write *nn* registers starting at address *rr*	0100 *rrnn*

(1) Operands: rr = configuration register (00 to 11), nn = number of bytes – 1 (00 to 11), and x = don't care.

8.5.3.1 RESET (0000 011x)

Resets the device to the default values. Wait at least (50 µs + 32 · $t_{(CLK)}$) after the RESET command is sent before sending any other command.

8.5.3.2 START/SYNC (0000 100x)

In single-shot mode, the START/SYNC command is used to start a single conversion, or (when sent during an ongoing conversion) to reset the digital filter, and then restarts a single new conversion. When the device is set to continuous conversion mode, the START/SYNC command must be issued one time to start converting continuously. Sending the START/SYNC command while converting in continuous conversion mode resets the digital filter and restarts continuous conversions.

8.5.3.3 POWERDOWN (0000 001x)

The POWERDOWN command places the device into power-down mode. This command shuts down all internal analog components, opens the low-side switch, turns off both IDACs, but holds all register values. In case the POWERDOWN command is issued while a conversion is ongoing, the conversion completes before the ADS1120-Q1 enters power-down mode. As soon as a START/SYNC command is issued, all analog components return to their previous states.

8.5.3.4 RDATA (0001 xxxx)

The RDATA command loads the output shift register with the most recent conversion result. This command can be used when DOUT/$\overline{\text{DRDY}}$ or $\overline{\text{DRDY}}$ are not monitored to indicate that a new conversion result is available. If a conversion finishes in the middle of the RDATA command byte, the state of the $\overline{\text{DRDY}}$ pin at the end of the read operation signals whether the old or the new result is loaded. If the old result is loaded, $\overline{\text{DRDY}}$ stays low, indicating that the new result is not read out. The new conversion result loads when $\overline{\text{DRDY}}$ is high.

8.5.3.5 RREG (0010 rrnn)

The RREG command reads the number of bytes specified by *nn* (number of bytes to be read – 1) from the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked out after the RREG command byte. For example, the command to read three bytes (nn = 10) starting at configuration register 1 (rr = 01) is 0010 0110.

8.5.3.6 WREG (0100 rrnn)

The WREG command writes the number of bytes specified by *nn* (number of bytes to be written – 1) to the device configuration register, starting at register address rr. The command is completed after nn + 1 bytes are clocked in after the WREG command byte. For example, the command to write two bytes (nn = 01) starting at configuration register 0 (rr = 00) is 0100 0001. The configuration registers are updated on the last SCLK falling edge.

8.5.4 Reading Data

Output pins $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ (if the DRDYM bit is set high in the configuration register) transition low when new data are ready for retrieval. The conversion data are written to an internal data buffer. Data can be read directly from this buffer on DOUT/$\overline{DRDY}$ when $\overline{DRDY}$ falls low without concern of data corruption. An RDATA command does not have to be sent. Data are shifted out on the SCLK rising edges, MSB first, and consist of two bytes of data.

Figure 61 to Figure 63 show the timing diagrams for reading conversion data in continuous conversion mode and single-shot mode when not using the RDATA command.

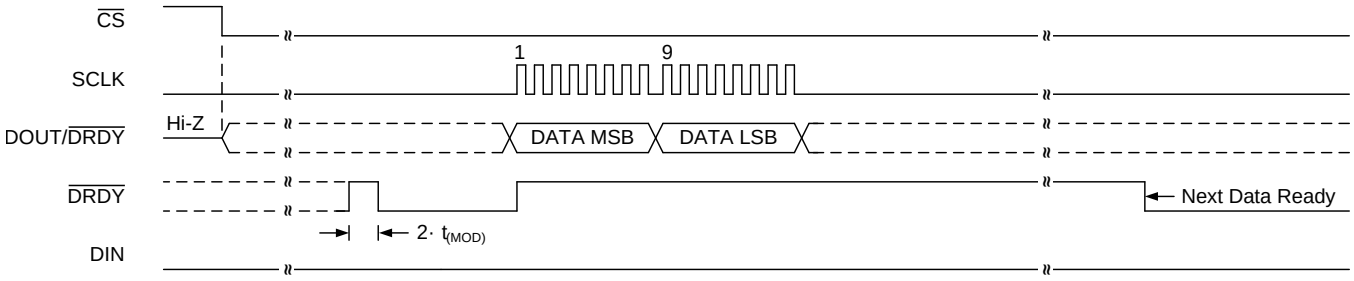


Figure 61. Continuous Conversion Mode (DRDYM = 0)

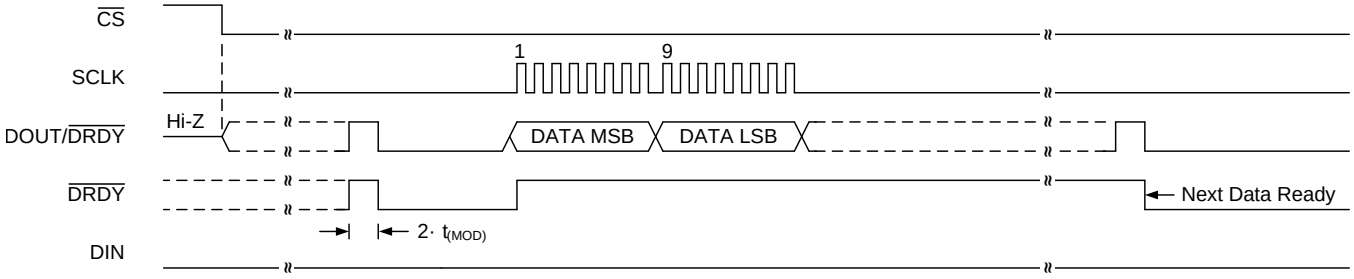


Figure 62. Continuous Conversion Mode (DRDYM = 1)

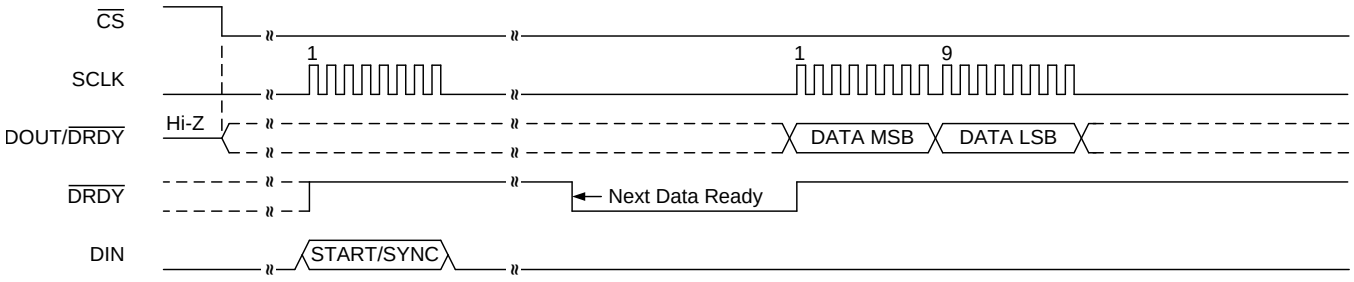


Figure 63. Single-Shot Mode (DRDYM = 0)

Data can also by read at any time without synchronizing to the $\overline{DRDY}$ signal using the RDATA command. When an RDATA command is issued, the conversion result currently stored in the data buffer is shifted out on DOUT/$\overline{DRDY}$ on the following SCLK rising edges. Data can be read continuously with the RDATA command as an alternative to monitoring $\overline{DRDY}$ or DOUT/$\overline{DRDY}$. The $\overline{DRDY}$ pin can be polled after the LSB is clocked out to determine if a new conversion result was loaded. If a new conversion completes during the read operation but data from the previous conversion are read, then $\overline{DRDY}$ is low. Otherwise, if the most recent result is read, $\overline{DRDY}$ is high. Figure 64 and Figure 65 illustrate the behavior for both cases.

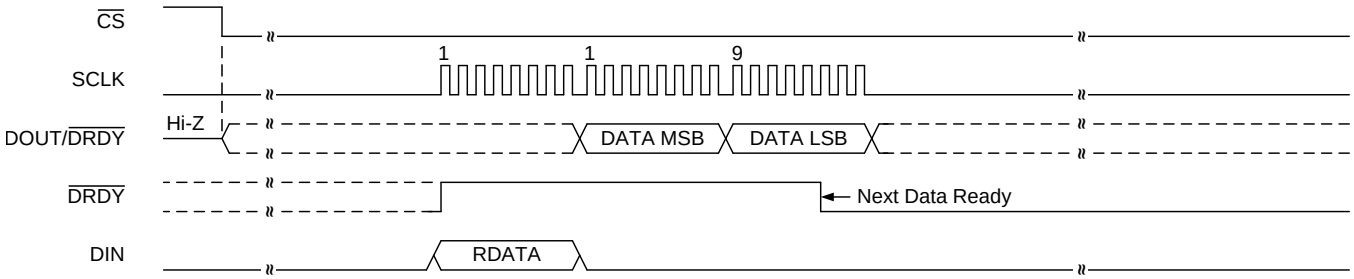


Figure 64. State of DRDY when a New Conversion Finishes During an RDATA Command

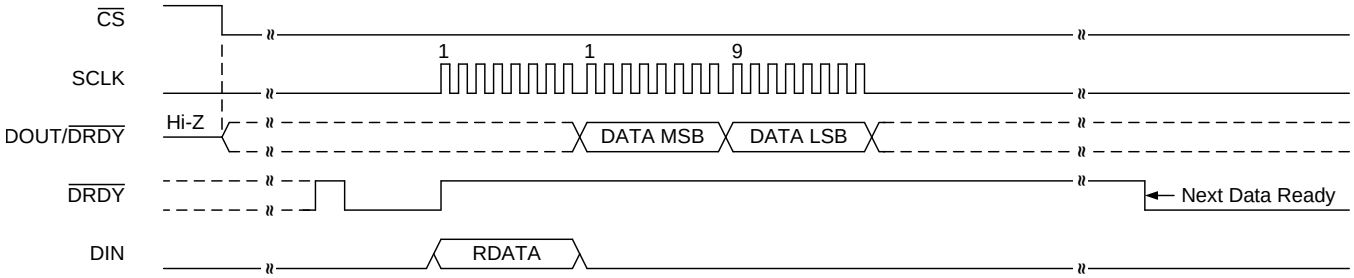


Figure 65. State of DRDY when the Most Recent Conversion Result is Read During an RDATA Command

8.5.5 Sending Commands

The device serial interface is capable of full-duplex operation while reading conversion data when not using the RDATA command. Full-duplex operation means commands are decoded at the same time that conversion data are read. Commands can be sent on any 8-bit data boundary during a data read operation. When a RREG or RDATA command is recognized, the current data read operation is aborted and the conversion data are corrupted, unless the command is sent while the last byte of the conversion result is retrieved. The device starts to output the requested data on DOUT/DRDY at the first SCLK rising edge after the command byte. To read data without interruption, keep DIN low while clocking out data.

A WREG command can be sent without corrupting an ongoing read operation. Figure 66 shows an example for sending a WREG command to write two configuration registers while reading conversion data in continuous conversion mode. After the command is clocked in (after the 32nd SCLK falling edge), the device resets the digital filter and starts converting with the new register settings. The WREG command can be sent on any of the 8-bit boundaries.

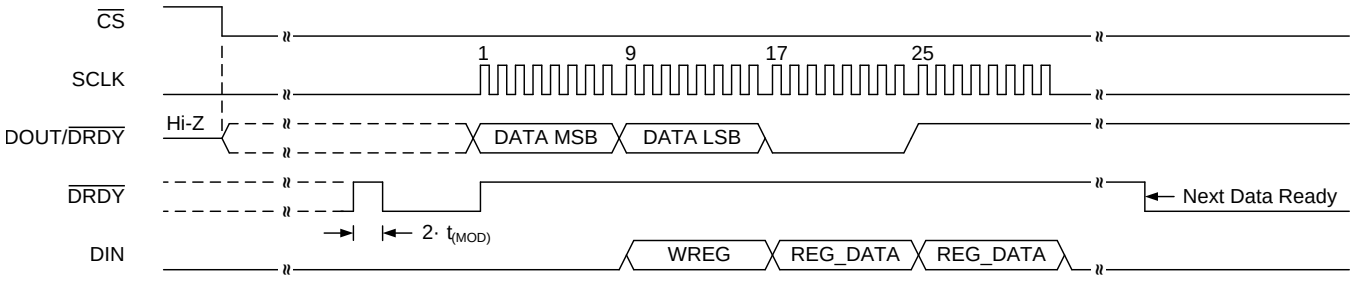


Figure 66. Example of Reading Data while Simultaneously Sending a WREG Command

Note that the serial interface does not decode commands while an RDATA or RREG command is executed. That is, all 16 bits of the conversion result must be read after the RDATA command is issued and all requested registers must be read after a RREG command is sent before a new command can be issued.

8.5.6 Interfacing with Multiple Devices

When connecting multiple ADS1120-Q1 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) line for each SPI-enabled device. When $\overline{\text{CS}}$ transitions high for the respective device, DOUT/$\overline{\text{DRDY}}$ enters a 3-state mode. Therefore, DOUT/$\overline{\text{DRDY}}$ cannot be used to indicate when new data are available if $\overline{\text{CS}}$ is high, regardless of the DRDYM bit setting in the configuration register. Only the dedicated $\overline{\text{DRDY}}$ pin indicates that new data are available, because the $\overline{\text{DRDY}}$ pin is actively driven even when $\overline{\text{CS}}$ is high.

In some cases the $\overline{\text{DRDY}}$ pin cannot be interfaced to the microcontroller. This scenario can occur if there are insufficient GPIO channels available on the microcontroller or if the serial interface must be galvanically isolated and thus the amount of channels must be limited. Therefore, in order to evaluate when a new conversion of one of the devices is ready, the microcontroller can periodically drop $\overline{\text{CS}}$ to the respective device and poll the state of the DOUT/$\overline{\text{DRDY}}$ pin. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low, provided that the DRDYM bit is configured to 1. If the DOUT/$\overline{\text{DRDY}}$ line drives low, when $\overline{\text{CS}}$ is taken low, new data are currently available. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available. This procedure requires that DOUT/$\overline{\text{DRDY}}$ is high after reading each conversion result and before taking $\overline{\text{CS}}$ high. To make sure DOUT/$\overline{\text{DRDY}}$ is taken high, send 16 additional SCLKs with DIN held low after each data read operation. DOUT/$\overline{\text{DRDY}}$ reads low during the first eight SCLKs after the conversion result is read, and reads high during the following eight SCLKs, as shown in Figure 67. Alternatively, valid data can be retrieved from the device at any time without concern of data corruption by using the RDATA command.

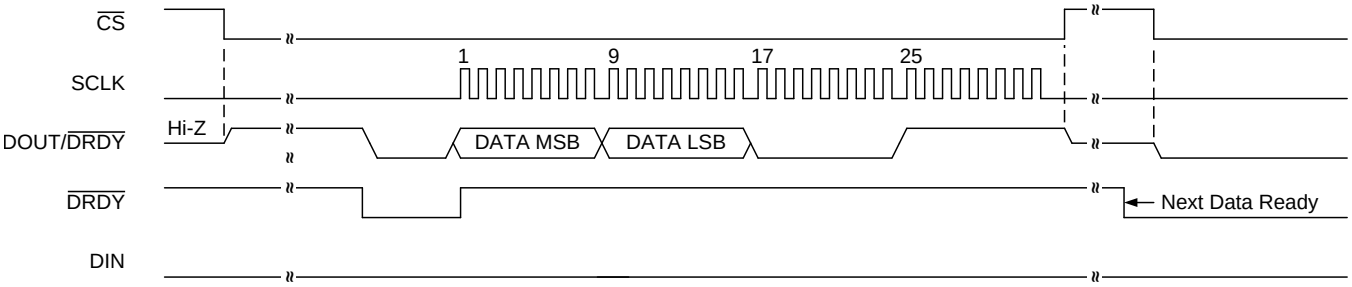


Figure 67. Example of Taking DOUT/$\overline{\text{DRDY}}$ High After Reading a Conversion Result

8.6 Register Map

8.6.1 Configuration Registers

The device has four 8-bit configuration registers that are accessible through the serial interface using the RREG and WREG commands. The configuration registers control how the device operates and can be changed at any time without causing data corruption. After power-up or reset, all registers are set to the default values (which are all 0). All registers retain their values during power-down mode. Table 11 shows the register map of the configuration registers.

Table 11. Configuration Register Map

REGISTER (Hex)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	MUX[3:0]				GAIN[2:0]			PGA_BYPASS
01h	DR[2:0]			MODE[1:0]		CM	TS	BCS
02h	VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
03h	I1MUX[2:0]			I2MUX[2:0]			DRDYM	RESERVED

8.6.1.1 Configuration Register 0 (offset = 00h) [reset = 00h]

Figure 68. Configuration Register 0

7	6	5	4	3	2	1	0
MUX[3:0]				GAIN[2:0]			PGA_BYPASS
R/W-0h				R/W-0h			R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 12. Configuration Register 0 Field Descriptions

Bit	Field	Type	Reset	Description
7:4	MUX[3:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. For settings where AIN_N = AVSS, the PGA must be disabled (PGA_BYPASS = 1) and only gains 1, 2, and 4 can be used. 0000 : AIN_P = AIN0, AIN_N = AIN1 (default) 0001 : AIN_P = AIN0, AIN_N = AIN2 0010 : AIN_P = AIN0, AIN_N = AIN3 0011 : AIN_P = AIN1, AIN_N = AIN2 0100 : AIN_P = AIN1, AIN_N = AIN3 0101 : AIN_P = AIN2, AIN_N = AIN3 0110 : AIN_P = AIN1, AIN_N = AIN0 0111 : AIN_P = AIN3, AIN_N = AIN2 1000 : AIN_P = AIN0, AIN_N = AVSS 1001 : AIN_P = AIN1, AIN_N = AVSS 1010 : AIN_P = AIN2, AIN_N = AVSS 1011 : AIN_P = AIN3, AIN_N = AVSS 1100 : $(V_{(REFPx)} – V_{(REFNx)})$ / 4 monitor (PGA bypassed) 1101 : (AVDD – AVSS) / 4 monitor (PGA bypassed) 1110 : AIN_P and AIN_N shorted to (AVDD + AVSS) / 2 1111 : Not used
3:1	GAIN[2:0]	R/W	0h	**Gain configuration** These bits configure the device gain. Gains 1, 2, and 4 can be used without the PGA. In this case, gain is obtained by a switched-capacitor structure. 000 : Gain = 1 (default) 001 : Gain = 2 010 : Gain = 4 011 : Gain = 8 100 : Gain = 16 101 : Gain = 32 110 : Gain = 64 111 : Gain = 128
0	PGA_BYPASS	R/W	0h	**Disables and bypasses the internal low-noise PGA** Disabling the PGA reduces overall power consumption and allows the common-mode voltage range (V_{CM}) to span from AVSS – 0.1 V to AVDD + 0.1 V. The PGA can only be disabled for gains 1, 2, and 4. The PGA is always enabled for gain settings 8 to 128, regardless of the PGA_BYPASS setting. 0 : PGA enabled (default) 1 : PGA disabled and bypassed

8.6.1.2 Configuration Register 1 (offset = 01h) [reset = 00h]

Figure 69. Configuration Register 1

7	6	5	4	3	2	1	0
DR[2:0]			MODE[1:0]		CM	TS	BCS
R/W-0h			R/W-0h		R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 13. Configuration Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	DR[2:0]	R/W	0h	**Data rate** These bits control the data rate setting depending on the selected operating mode. Table 14 lists the bit settings for normal, duty-cycle, and turbo mode.
4:3	MODE[1:0]	R/W	0h	**Operating mode** These bits control the operating mode the device operates in. 00 : Normal mode (256-kHz modulator clock, default) 01 : Duty-cycle mode (internal duty cycle of 1:4) 10 : Turbo mode (512-kHz modulator clock) 11 : Not used
2	CM	R/W	0h	**Conversion mode** This bit sets the conversion mode for the device. 0 : Single-shot mode (default) 1 : Continuous conversion mode
1	TS	R/W	0h	**Temperature sensor mode** This bit enables the internal temperature sensor and puts the device in temperature sensor mode. The settings of configuration register 0 have no effect and the device uses the internal reference for measurement when temperature sensor mode is enabled. 0 : Disables temperature sensor (default) 1 : Enables temperature sensor
0	BCS	R/W	0h	**Burn-out current sources** This bit controls the 10-µA, burn-out current sources. The burn-out current sources can be used to detect sensor faults such as wire breaks and shorted sensors. 0 : Current sources off (default) 1 : Current sources on

Table 14. DR Bit Settings(1)

NORMAL MODE	DUTY-CYCLE MODE	TURBO MODE
000 = 20 SPS	000 = 5 SPS	000 = 40 SPS
001 = 45 SPS	001 = 11.25 SPS	001 = 90 SPS
010 = 90 SPS	010 = 22.5 SPS	010 = 180 SPS
011 = 175 SPS	011 = 44 SPS	011 = 350 SPS
100 = 330 SPS	100 = 82.5 SPS	100 = 660 SPS
101 = 600 SPS	101 = 150 SPS	101 = 1200 SPS
110 = 1000 SPS	110 = 250 SPS	110 = 2000 SPS
111 = Not used	111 = Not used	111 = Not used

(1) Data rates provided are calculated using the internal oscillator or an external 4.096-MHz clock. The data rates scale proportionally with the external clock frequency when an external clock other than 4.096 MHz is used.

8.6.1.3 Configuration Register 2 (offset = 02h) [reset = 00h]

Figure 70. Configuration Register 2

7	6	5	4	3	2	1	0
VREF[1:0]		50/60[1:0]		PSW	IDAC[2:0]		
R/W-0h		R/W-0h		R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. Configuration Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7:6	VREF[1:0]	R/W	0h	**Voltage reference selection** These bits select the voltage reference source that is used for the conversion. 00 : Internal 2.048-V reference selected (default) 01 : External reference selected using dedicated REFP0 and REFN0 inputs 10 : External reference selected using AIN0/REFP1 and AIN3/REFN1 inputs 11 : Analog supply (AVDD – AVSS) used as reference
5:4	50/60[1:0]	R/W	0h	**FIR filter configuration** These bits configure the filter coefficients for the internal FIR filter. These bits only affect the 20-SPS setting in normal mode and 5-SPS setting in duty-cycle mode. 00 : No 50-Hz or 60-Hz rejection (default) 01 : Simultaneous 50-Hz and 60-Hz rejection 10 : 50-Hz rejection only 11 : 60-Hz rejection only
3	PSW	R/W	0h	**Low-side power switch configuration** This bit configures the behavior of the low-side switch connected between AIN3/REFN1 and AVSS. 0 : Switch is always open (default) 1 : Switch automatically closes when the START/SYNC command is sent and opens when the POWERDOWN command is issued
2:0	IDAC[2:0]	R/W	0h	**IDAC current setting** These bits set the current for both IDAC1 and IDAC2 excitation current sources. 000 : Off (default) 001 : Not used 010 : 50 µA 011 : 100 µA 100 : 250 µA 101 : 500 µA 110 : 1000 µA 111 : 1500 µA

8.6.1.4 Configuration Register 3 (offset = 03h) [reset = 00h]

Figure 71. Configuration Register 3

7	6	5	4	3	2	1	0
I1MUX[2:0]			I2MUX[2:0]			DRDYM	RESERVED
R/W-0h			R/W-0h			R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. Configuration Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7:5	I1MUX[2:0]	R/W	0h	**IDAC1 routing configuration** These bits select the channel where IDAC1 is routed to. 000 : IDAC1 disabled (default) 001 : IDAC1 connected to AIN0/REFP1 010 : IDAC1 connected to AIN1 011 : IDAC1 connected to AIN2 100 : IDAC1 connected to AIN3/REFN1 101 : IDAC1 connected to REFP0 110 : IDAC1 connected to REFN0 111 : Not used
4:2	I2MUX[2:0]	R/W	0h	**IDAC2 routing configuration** These bits select the channel where IDAC2 is routed to. 000 : IDAC2 disabled (default) 001 : IDAC2 connected to AIN0/REFP1 010 : IDAC2 connected to AIN1 011 : IDAC2 connected to AIN2 100 : IDAC2 connected to AIN3/REFN1 101 : IDAC2 connected to REFP0 110 : IDAC2 connected to REFN0 111 : Not used
1	DRDYM	R/W	0h	**$\overline{\text{DRDY}}$ mode** This bit controls the behavior of the DOUT/$\overline{\text{DRDY}}$ pin when new data are ready. 0 : Only the dedicated $\overline{\text{DRDY}}$ pin is used to indicate when data are ready (default) 1 : Data ready is indicated simultaneously on DOUT/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$
0	RESERVED	R/W	0h	**Reserved** Always write 0

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS1120-Q1 is a precision, 16-bit, ΔΣ ADC that offers many integrated features to ease the measurement of the most common sensor types including various types of temperature and bridge sensors. Primary considerations when designing an application with the ADS1120-Q1 include analog input filtering, establishing an appropriate external reference for ratiometric measurements, and setting the common-mode input voltage for the internal PGA. Connecting and configuring the serial interface appropriately is another concern. These considerations are discussed in the following sections.

9.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1120-Q1 are shown in Figure 72.

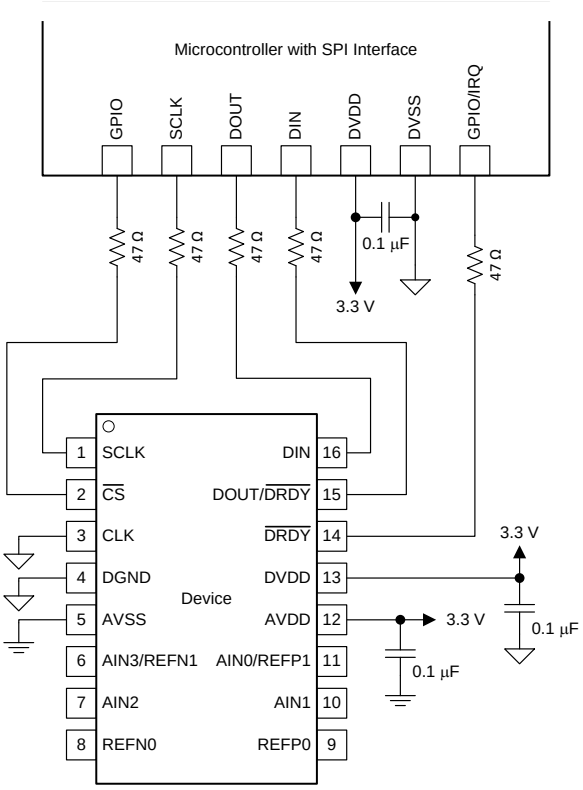


Figure 72. Serial Interface Connections

Most microcontroller SPI peripherals can operate with the ADS1120-Q1. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the *SPI Timing Requirements* section.

TI recommends placing 47-Ω resistors in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, and $\overline{DRDY}$). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Application Information (continued)

9.1.2 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is sampled at the modulator frequency $f_{(MOD)}$ and not at the output data rate. The filter response of the digital filter repeats at multiples of the sampling frequency ($f_{(MOD)}$), as shown in Figure 73. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

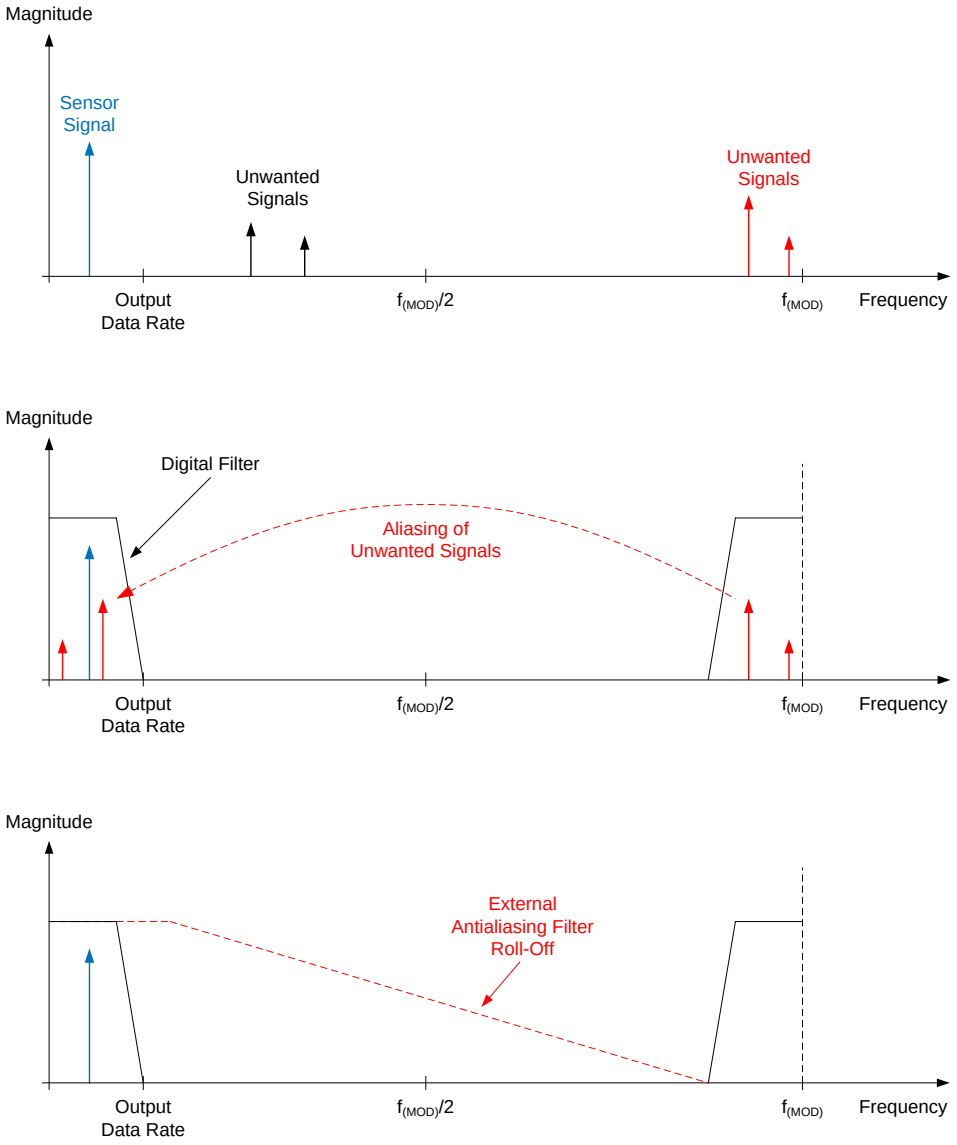


Figure 73. Effect of Aliasing

Application Information (continued)

Many sensor signals are inherently bandlimited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1120-Q1 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10x higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter as shown in Figure 39. The cutoff frequency of this filter is approximately 31.8 MHz, which helps reject high-frequency interferences.

9.1.3 External Reference and Ratiometric Measurements

The full-scale range of the ADS1120-Q1 is defined by the reference voltage and the PGA gain (FSR = $\pm V_{ref}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system needs. An external reference must be used if V_{IN} > 2.048 V. For example, an external 5-V reference and an AVDD = 5 V are required in order to measure a single-ended signal that can swing between 0 V and 5 V.

The reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. Because current noise and drift are common to both the sensor measurement and the reference, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element and the value of the reference resistor. The value of the excitation current source itself is not part of the ADC transfer function.

9.1.4 Establishing a Proper Common-Mode Input Voltage

The ADS1120-Q1 can be used to measure various types of input signal configurations: single-ended, pseudo-differential, and fully-differential signals (which can be either unipolar or bipolar). However, configuring the device properly for the respective signal type is important.

Signals where the negative analog input is fixed and referenced to analog ground ($V_{(AINN)}$ = 0 V) are commonly called *single-ended signals*. The common-mode voltage of a single-ended signal consequently varies between 0 V and V_{IN} / 2. If the PGA is disabled and bypassed, the common-mode input voltage of the ADS1120-Q1 can be as low as 100 mV below AVSS and as large as 100 mV above AVDD. Therefore, the PGA_BYPASS bit must be set in order to measure single-ended signals when a unipolar analog supply is used (AVSS = 0 V). Gains of 1, 2, and 4 are still possible in this configuration. Measuring a 0-mA to 20-mA or 4-mA to 20-mA signal across a load resistor of 100 Ω referenced to GND is a typical example. The ADS1120-Q1 can directly measure the signal across the load resistor using a unipolar supply, the internal 2.048-V reference, and gain = 1 when the PGA is bypassed.

If gains larger than 4 are needed to measure a single-ended signal, the PGA must be enabled. In this case, a bipolar supply is required for the ADS1120-Q1 to meet the common-mode voltage requirement of the PGA.

Signals where the negative analog input (AIN_N) is fixed at a voltage other the 0 V are referred to as *pseudo-differential signals*. The common-mode voltage of a pseudo-differential signal varies between $V_{(AINN)}$ and $V_{(AINN)}$ + V_{IN} / 2.

Application Information (continued)

Fully-differential signals in contrast are defined as signals having a constant common-mode voltage where the positive and negative analog inputs swing 180° out-of-phase but have the same amplitude.

The ADS1120-Q1 can measure pseudo-differential and fully-differential signals both with the PGA enabled or bypassed. However, the PGA must be enabled in order to use gains greater than 4. The common-mode voltage of the input signal must meet the input-common mode voltage restrictions of the PGA (as explained in the *PGA Common-Mode Voltage Requirements* section) when the PGA is enabled. Setting the common-mode voltage at or near (AVSS + AVDD) / 2 in most cases satisfies the PGA common-mode voltage requirements.

Signals where both the positive and negative inputs are always ≥ 0 V are called *unipolar signals*. These signals can in general be measured with the ADS1120-Q1 using a unipolar analog supply (AVSS = 0 V). As mentioned previously, the PGA must be bypassed in order to measure single-ended, unipolar signals when using a unipolar supply.

A signal is called *bipolar* when either the positive or negative input can swing below 0 V. A bipolar analog supply (such as AVDD = 2.5 V, AVSS = –2.5 V) is required in order to measure bipolar signals with the ADS1120-Q1. A typical application task is measuring a single-ended, bipolar ±10 V signal where AIN_N is fixed at 0 V while AIN_P swings between –10 V and 10 V. The ADS1120-Q1 cannot directly measure this signal because the 10 V exceeds the analog power-supply limits. However, one possible solution is to use a bipolar analog supply (AVDD = 2.5 V, AVSS = –2.5 V), gain = 1, and a resistor divider in front of the ADS1120-Q1. The resistor divider must divide the voltage down to ≤ ±2.048 V to be able to measure it using the internal 2.048-V reference.

Application Information (continued)

9.1.5 Pseudo Code Example

The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC in order to take subsequent readings from the ADS1120-Q1 in continuous conversion mode. The dedicated $\overline{DRDY}$ pin is used to indicate availability of new conversion data. The default configuration register settings are changed to gain = 16, continuous conversion mode, and simultaneous 50-Hz and 60-Hz rejection.

```
Power-up;
Delay to allow power supplies to settle and power-up reset to complete; minimum of 50 µs;
Configure the SPI interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA = 1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt input;
Set CS to the device low;
Delay for a minimum of td(CSSC);
Send the RESET command (06h) to make sure the device is properly reset after power-up;
Delay for a minimum of 50 µs + 32 · t(CLK);
Write the respective register configuration with the WREG command (43h, 08h, 04h, 10h, and 00h);
As an optional sanity check, read back all configuration registers with the RREG command (23h);
Send the START/SYNC command (08h) to start converting in continuous conversion mode;
Delay for a minimum of td(SCCS);
Clear CS to high (resets the serial interface);
Loop
    {
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of td(CSSC);
    Send 16 SCLK rising edges to read out conversion data on DOUT/DRDY;
    Delay for for a minimum of td(SCCS);
    Clear CS to high;
    }
Take CS low;
Delay for a minimum of td(CSSC);
Send the POWERDOWN command (02h) to stop conversions and put the device in power-down mode;
Delay for a minimum of td(SCCS);
Clear CS to high;
```

TI recommends running an offset calibration before performing any measurements or when changing the gain of the PGA. The internal offset of the device can, for example, be measured by shorting the inputs to mid-supply (MUX[3:1] = 1110). The microcontroller then takes multiple readings from the device with the inputs shorted and stores the average value in the microcontroller memory. When measuring the sensor signal, the microcontroller then subtracts the stored offset value from each device reading to obtain an offset compensated result. Note that the offset can be either positive or negative in value.

9.2 Typical Application

9.2.1 K-Type Thermocouple Measurement (–200°C to +1250°C)

Figure 74 shows the basic connections of a thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouple itself, the only external circuitry required are two biasing resistors, a simple low-pass, antialiasing filter, and the power-supply decoupling capacitors.

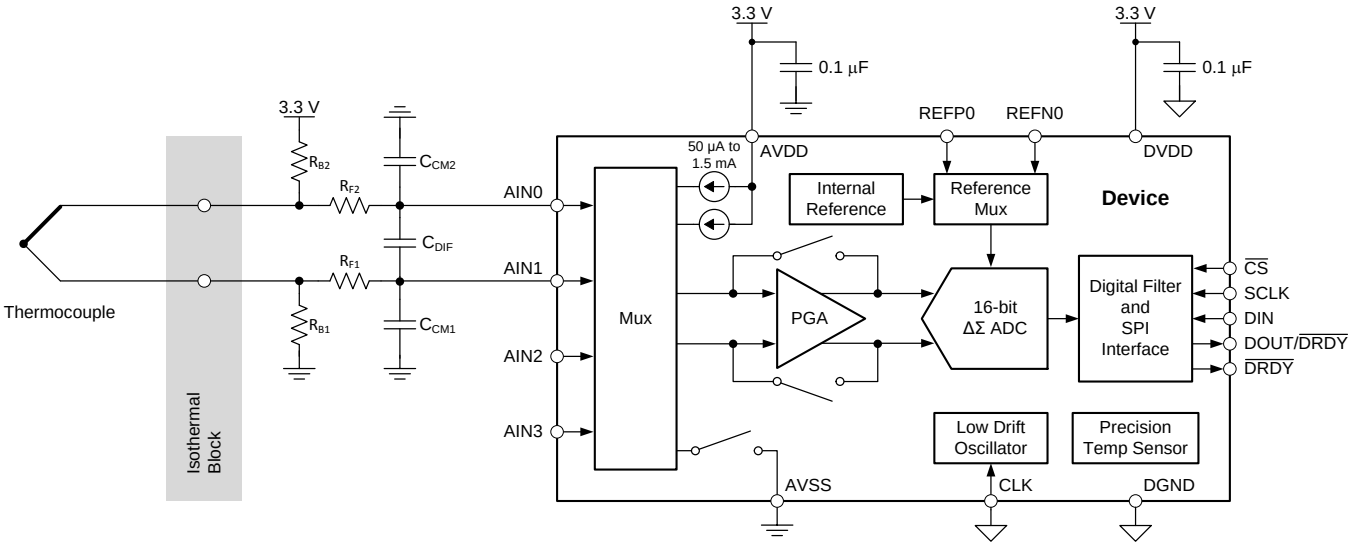


Figure 74. Thermocouple Measurement

9.2.1.1 Design Requirements

Table 17. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Reference voltage	Internal 2.048-V reference
Update rate	≥10 readings per second
Thermocouple type	K
Temperature measurement range	–200°C to +1250°C
Measurement accuracy at T_A = 25°C(1)	±0.5°C

(1) Not accounting for error of the thermocouple and cold-junction temperature measurement; offset calibration at $T_{(TC)} = T_{(CJ)}$ = 25°C; no gain calibration.

9.2.1.2 Detailed Design Procedure

The biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple to within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, either a bipolar supply (for example, AVDD = 2.5 V and AVSS = –2.5 V) must be used for the device to meet the common-mode voltage requirement of the PGA, or the PGA must be bypassed. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

In addition to biasing the thermocouple, R_{B1} and R_{B2} are also useful for detecting an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs (AIN0 and AIN1) to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

Although the device digital filter attenuates high-frequency components of noise, TI recommends providing a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{F1}, R_{F2}, and the differential capacitor C_{DIF} offers a cutoff frequency that is calculated using Equation 17.

$$f_C = 1 / [2\pi \cdot (R_{F1} + R_{F2}) \cdot C_{DIF}] \quad (17)$$

Two common-mode filter capacitors (C_{M1} and C_{M2}) are also added to offer attenuation of high-frequency, common-mode noise components. TI recommends that the differential capacitor C_{DIF} be at least an order of magnitude (10x) larger than the common-mode capacitors (C_{M1} and C_{M2}) because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The filter resistors R_{F1} and R_{F2} also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels if an overvoltage on the inputs occur. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. TI recommends limiting the filter resistor values to below 1 kΩ.

The filter component values used in this design are: $R_{F1} = R_{F2} = 1$ kΩ, $C_{DIF} = 100$ nF, and $C_{CM1} = C_{CM2} = 10$ nF.

The highest measurement resolution is achieved when matching the largest potential input signal to the FSR of the ADC by choosing the highest possible gain. From the design requirement, the maximum thermocouple voltage occurs at $T_{(TC)} = 1250$°C and is $V_{(TC)} = 50.644$ mV as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature of $T_{(CJ)} = 0$°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at $T_{(TC)} = 1250$°C produces an output voltage of $V_{(TC)} = 50.644$ mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of $T_{(CJ)} = –40$°C. The maximum gain that can be applied when using the internal 2.048-V reference is then calculated as (2.048 V / 52.171 mV) = 39.3. The next smaller PGA gain setting the device offers is 32.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. To measure the internal temperature of the ADS1120-Q1, the device must be set to internal temperature sensor mode by setting the TS bit to 1 in the configuration register. For best performance, careful board layout is critical to achieve good thermal conductivity between the cold junction and the device package.

However, the device does not perform automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to internal temperature sensor mode (TS = 1) to acquire the temperature of the cold junction. An algorithm similar to the following must be implemented on the microcontroller to compensate for the cold-junction temperature:

1. Measure the thermocouple voltage, $V_{(TC)}$, between AIN0 and AIN1.
2. Measure the temperature of the cold junction, $T_{(CJ)}$, using the temperature sensor mode of the ADS1120-Q1.
3. Convert the cold-junction temperature into an equivalent thermoelectric voltage, $V_{(CJ)}$, using the tables or equations provided by NIST.
4. Add $V_{(TC)}$ and $V_{(CJ)}$ and translate the summation back into a thermocouple temperature using the NIST tables or equations again.

In some applications, the integrated temperature sensor of the ADS1120-Q1 cannot be used (for example, if the accuracy is not high enough or if the device cannot be placed close enough to the cold junction). The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor, RTD, or an analog temperature sensor.

The device is capable of 16-bit, noise-free resolution using a gain of 32, the internal 2.048-V reference, and a data rate of 20 SPS (see Table 1 and Table 2). Accordingly the device is able to resolve signals as small as one LSB. The LSB size is calculated using Equation 18:

$$1 \text{ LSB} = (2 \cdot V_{ref} / \text{Gain}) / 2^{16} = (2 \cdot 2.048 \text{ V} / 32) / 2^{16} = 1.953 \text{ µV} \quad (18)$$

To get an approximation of the achievable temperature resolution per ADC code, the LSB size is divided by the average sensitivity of a K-type thermocouple (41 µV/°C), as shown in Equation 19.

$$\text{Temperature Resolution per Code} = 1.953 \text{ µV} / 41 \text{ µV/°C} = 0.05\text{°C} \quad (19)$$

The register settings for this design are shown in Table 18.

Table 18. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	0Ah	AIN_P = AIN0, AIN_N = AIN1, gain = 32, PGA enabled
01h	04h	DR = 20 SPS, normal mode, continuous conversion mode
02h	10h	Internal voltage reference, simultaneous 50-Hz and 60-Hz rejection
03h	00h	No IDACs used

9.2.1.3 Application Curves

Figure 75 and Figure 76 show the measurement results. The measurements are taken at $T_A = T_{(CJ)} = 25°C$. A system offset calibration is performed at $T_{(TC)} = 25°C$, which translates to a $V_{(TC)} = 0$ V when $T_{(CJ)} = 25°C$. No gain calibration is implemented. The data in Figure 75 are taken using a precision voltage source as the input signal instead of a thermocouple. The respective temperature measurement error in Figure 76 is calculated from the data in Figure 75 using the NIST tables.

The design meets the required temperature measurement accuracy given in Table 17. Note that the measurement error shown in Figure 76 does not include the error of the thermocouple itself and the measurement error of the cold-junction temperature. Those two error sources are in general larger than 0.2°C and therefore, in many cases, dominate the overall system measurement accuracy.

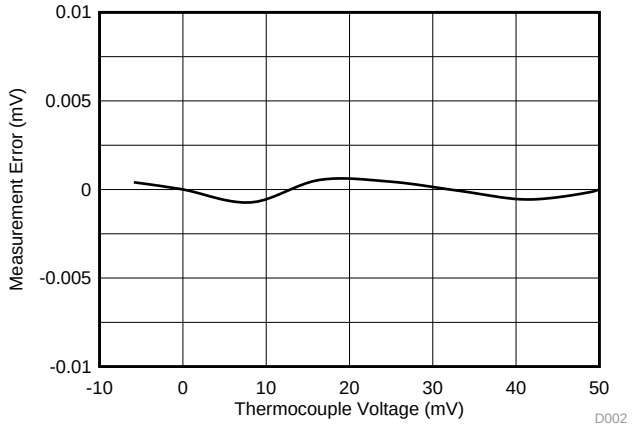


Figure 75. Voltage Measurement Error vs $V_{(TC)}$

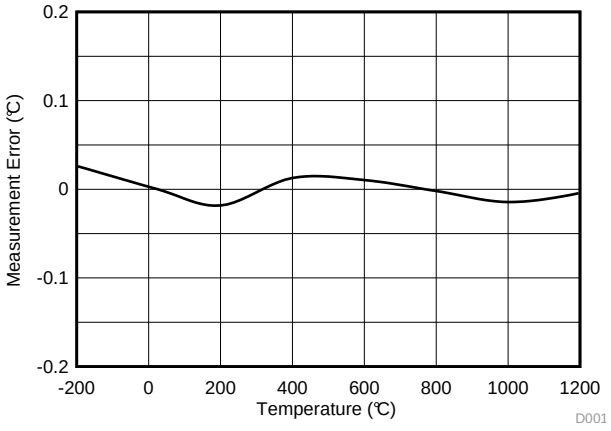


Figure 76. Temperature Measurement Error vs $T_{(TC)}$

9.2.2 3-Wire RTD Measurement (–200°C to +850°C)

The ADS1120-Q1 integrates all necessary features (such as dual-matched programmable current sources, buffered reference inputs, and a PGA) to ease the implementation of ratiometric 2-, 3-, and 4-wire RTD measurements. Figure 77 shows a typical implementation of a ratiometric 3-wire RTD measurement using the excitation current sources integrated in the device to excite the RTD as well as to implement automatic RTD lead-resistance compensation.

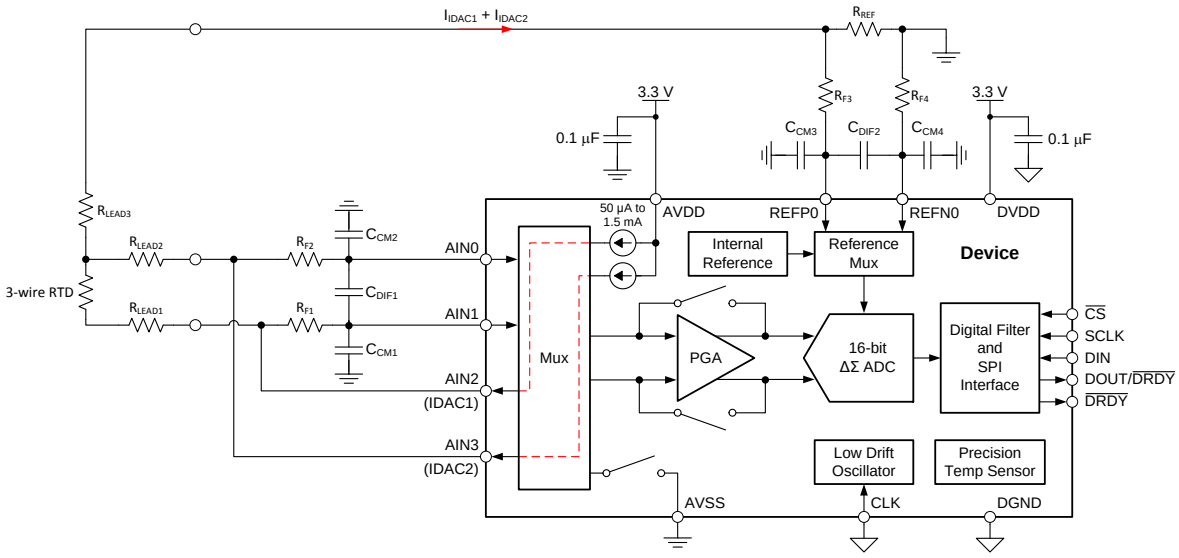


Figure 77. 3-Wire RTD Measurement

9.2.2.1 Design Requirements

Table 19. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Update rate	20 readings per second
RTD type	3-wire Pt100
Maximum RTD lead resistance	15 Ω
RTD excitation current	500 µA
Temperature measurement range	–200°C to +850°C
Measurement accuracy at T_A = 25°C (1)	±0.2°C

(1) Not accounting for error of RTD; offset calibration is performed with R_{RTD} = 100 Ω; no gain calibration.

9.2.2.2 Detailed Design Procedure

The circuit in Figure 77 employs a ratiometric measurement approach. In other words, the sensor signal (that is, the voltage across the RTD in this case) and the reference voltage for the ADC are derived from the same excitation source. Therefore, errors resulting from temperature drift or noise of the excitation source cancel out because these errors are common to both the sensor signal and the reference.

In order to implement a ratiometric 3-wire RTD measurement using the device, IDAC1 is routed to one of the leads of the RTD and IDAC2 is routed to the second RTD lead. Both currents have the same value, which is programmable by the IDAC[2:0] bits in the configuration register. The design of the device ensures that both IDAC values are closely matched, even across temperature. The sum of both currents flows through a precision, low-drift reference resistor, R_{REF}. The voltage, V_{ref}, generated across the reference resistor (as shown in Equation 20) is used as the ADC reference voltage. Equation 20 reduces to Equation 21 because $I_{IDAC1} = I_{IDAC2}$.

$$V_{ref} = (I_{IDAC1} + I_{IDAC2}) \cdot R_{REF} \quad (20)$$

$$V_{ref} = 2 \cdot I_{IDAC1} \cdot R_{REF} \quad (21)$$

To simplify the following discussion, the individual lead resistance values of the RTD (R_{LEADx}) are set to zero. Only IDAC1 excites the RTD to produce a voltage (V_{RTD}) proportional to the temperature-dependable RTD value and the IDAC1 value, as shown in Equation 22.

$$V_{RTD} = R_{RTD\ (at\ temperature)} \cdot I_{IDAC1} \quad (22)$$

The device internally amplifies the voltage across the RTD using the PGA and compares the resulting voltage against the reference voltage to produce a digital output code proportional to Equation 23 through Equation 25:

$$Code \propto V_{RTD} \cdot Gain / V_{ref} \quad (23)$$

$$Code \propto (R_{RTD\ (at\ temperature)} \cdot I_{IDAC1} \cdot Gain) / (2 \cdot I_{IDAC1} \cdot R_{REF}) \quad (24)$$

$$Code \propto (R_{RTD\ (at\ temperature)} \cdot Gain) / (2 \cdot R_{REF}) \quad (25)$$

As can be seen from Equation 25, the output code only depends on the value of the RTD, the PGA gain, and the reference resistor (R_{REF}), but not on the IDAC1 value. The absolute accuracy and temperature drift of the excitation current therefore does not matter. However, because the value of the reference resistor directly affects the measurement result, choosing a reference resistor with a very low temperature coefficient is important to limit errors introduced by the temperature drift of R_{REF}.

The second IDAC2 is used to compensate for errors introduced by the voltage drop across the lead resistance of the RTD. All three leads of a 3-wire RTD typically have the same length and, thus, the same lead resistance. Also, IDAC1 and IDAC2 have the same value. Taking the lead resistance into account, the differential voltage (V_{IN}) across the ADC inputs, AIN0 and AIN1, is calculated using Equation 26:

$$V_{IN} = I_{IDAC1} \cdot (R_{RTD} + R_{LEAD1}) - I_{IDAC2} \cdot R_{LEAD2} \quad (26)$$

When $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$, Equation 26 reduces to Equation 27:

$$V_{IN} = I_{IDAC1} \cdot R_{RTD} \quad (27)$$

In other words, the measurement error resulting from the voltage drop across the RTD lead resistance is compensated, as long as the lead resistance values and the IDAC values are well matched.

A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs, as well as on the reference inputs (R_{F3}, R_{F4}, C_{DIF2}, C_{CM3}, and C_{CM4}). The same guidelines for designing the input filter apply as described in the *Thermocouple Measurement* section. For best performance, TI recommends matching the corner frequencies of the input and reference filter. More detailed information on matching the input and reference filter can be found in application report *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248* (SBAA201).

The reference resistor R_{REF} not only serves to generate the reference voltage for the device, but also sets the common-mode voltage of the RTD to within the specified common-mode voltage range of the PGA.

When designing the circuit, care must also be taken to meet the compliance voltage requirement of the IDACs. The IDACs require that the maximum voltage drop developed across the current path to AVSS be equal or less than AVDD – 0.9 V in order to operate accurately. This requirement means that Equation 28 must be met at all times.

$$AVSS + I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD}) + (I_{IDAC1} + I_{IDAC2}) \cdot (R_{LEAD3} + R_{REF}) \leq AVDD - 0.9\ V \quad (28)$$

The device also offers the possibility to route the IDACs to the same inputs used for measurement. If the filter resistor values R_{F1} and R_{F2} are small enough and well matched, IDAC1 can be routed to AIN1 and IDAC2 to AIN0 in Figure 77. In this manner, even two 3-wire RTDs sharing the same reference resistor can be measured with a single device.

This design example discusses the implementation of a 3-wire Pt100 measurement to be used to measure temperatures ranging from –200°C to +850°C as stated in Table 19. The excitation current for the Pt100 is chosen as I_{IDAC1} = 500 µA, which means a combined current of 1 mA is flowing through the reference resistor, R_{REF}. As mentioned previously, besides creating the reference voltage for the ADS1120-Q1, the voltage across R_{REF} also sets the common-mode voltage for the RTD measurement. In general, choose the largest reference voltage possible while still maintaining the compliance voltage of the IDACs as well as meeting the common-mode voltage requirement of the PGA. TI recommends setting the common-mode voltage at or near half the analog supply (in this case 3.3 V / 2 = 1.65 V), which in most cases satisfies the common-mode voltage requirements of the PGA. The value for R_{REF} is then calculated by Equation 29:

$$R_{REF} = V_{ref} / (I_{IDAC1} + I_{IDAC2}) = 1.65\ V / 1\ mA = 1.65\ k\Omega \quad (29)$$

The stability of R_{REF} is critical to achieve good measurement accuracy over temperature and time. Choosing a reference resistor with a temperature coefficient of ±10 ppm/°C or better is advisable. If a 1.65 kΩ value is not readily available, another value near 1.65 kΩ (such as 1.62 kΩ or 1.69 kΩ) can certainly be used as well.

As a last step, the PGA gain must be selected in order to match the maximum input signal to the FSR of the ADC. The resistance of a Pt100 increases with temperature. Therefore, the maximum voltage to be measured ($V_{IN\ (MAX)}$) occurs at the positive temperature extreme. At 850°C, a Pt100 has an equivalent resistance of approximately 391 Ω as per the NIST tables. The voltage across the Pt100 equates to Equation 30:

$$V_{IN\ (MAX)} = V_{RTD\ (at\ 850°C)} = R_{RTD\ (at\ 850°C)} \cdot I_{IDAC1} = 391\ \Omega \cdot 500\ \mu A = 195.5\ mV \quad (30)$$

The maximum gain that can be applied when using a 1.65-V reference is then calculated as (1.65 V / 195.5 mV) = 8.4. The next smaller PGA gain setting available in the ADS1120-Q1 is 8. At a gain of 8, the ADS1120-Q1 offers a FSR value as described in Equation 31:

$$FSR = \pm V_{ref} / Gain = \pm 1.65\ V / 8 = \pm 206.25\ mV \quad (31)$$

This range allows for margin with respect to initial accuracy and drift of the IDACs and reference resistor.

After selecting the values for the IDACs, R_{REF}, and PGA gain, make sure to double check that the settings meet the common-mode voltage requirements of the PGA and the compliance voltage of the IDACs. To determine the true common-mode voltage at the ADC inputs (AIN0 and AIN1) the lead resistance must be taken into account as well.

The smallest common-mode voltage occurs at the lowest measurement temperature (–200°C) with R_{LEADx} = 0 Ω and is calculated using Equation 32 and Equation 33.

$$V_{CM\ (MIN)} = V_{ref} + (I_{IDAC1} + I_{IDAC2}) \cdot R_{LEAD3} + I_{IDAC2} \cdot R_{LEAD2} + ½\ I_{IDAC1} \cdot R_{RTD\ (at\ –200°C)} \quad (32)$$

$$V_{CM\ (MIN)} = 1.65\ V + ½\ 500\ \mu A \cdot 18.52\ \Omega = 1.655\ V \quad (33)$$

Actually, assuming $V_{CM\ (MIN)} = V_{ref}$ is a sufficient approximation.

$V_{CM\ (MIN)}$ must meet two requirements: Equation 15 requires $V_{CM\ (MIN)}$ to be larger than AVDD / 4 = 3.3 V / 4 = 0.825 V and Equation 13 requires $V_{CM\ (MIN)}$ to meet Equation 34:

$$V_{CM\ (MIN)} \geq AVSS + 0.2\ V + ½\ Gain \cdot V_{IN\ (MAX)} = 0\ V + 0.2\ V + (½ \cdot 8 \cdot 195.5\ mV) = 982\ mV \quad (34)$$

Both restrictions are satisfied in this design with a $V_{CM\ (MIN)}$ = 1.65 V.

The largest common-mode voltage occurs at the highest measurement temperature (850°C) and is calculated using Equation 35 and Equation 36.

$$V_{CM\ (MAX)} = V_{ref} + (I_{IDAC1} + I_{IDAC2}) \cdot R_{LEAD3} + I_{IDAC2} \cdot R_{LEAD2} + ½\ I_{IDAC1} \cdot R_{RTD\ (at\ 850°C)} \quad (35)$$

$$V_{CM\ (MAX)} = 1.65\ V + 1\ mA \cdot 15\ \Omega + 500\ \mu A \cdot 15\ \Omega + ½\ 500\ \mu A \cdot 391\ \Omega = 1.77\ V \quad (36)$$

$V_{CM\ (MAX)}$ does meet the requirement given by Equation 14, which in this design equates to Equation 37:

$$V_{CM\ (MAX)} \leq AVDD – 0.2\ V – ½\ Gain \cdot V_{IN\ (MAX)} = 3.3\ V – 0.2\ V – (½ \cdot 8 \cdot 195.5\ mV) = 2.318\ V \quad (37)$$

Finally, the maximum voltage that can occur on input AIN1 must be calculated to determine if the compliance voltage (AVDD – 0.9 V = 3.3 V – 0.9 V = 2.4 V) of IDAC1 is met. Note that the voltage on input AIN0 is smaller than the one on input AIN1. Equation 38 and Equation 39 show that the voltage on AIN1 is less than 2.4 V, even when taking the worst-case lead resistance into account.

$$V_{AIN1\ (MAX)} = V_{ref} + (I_{IDAC1} + I_{IDAC2}) \cdot R_{LEAD3} + I_{IDAC1} \cdot (R_{RTD\ (at\ 850°C)} + R_{LEAD1}) \quad (38)$$

$$V_{AIN1\ (MAX)} = 1.65\ V + 1\ mA \cdot 15\ \Omega + 500\ \mu A \cdot (391\ \Omega + 15\ \Omega) = 1.868\ V \quad (39)$$

The register settings for this design are shown in Table 20.

Table 20. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	66h	AIN_P = AIN1, AIN_N = AIN0, gain = 8, PGA enabled
01h	04h	DR = 20 SPS, normal mode, continuous conversion mode
02h	55h	External reference (REFP0, REFN0), simultaneous 50-Hz and 60-Hz rejection, IDAC = 500 µA
03h	70h	IDAC1 = AIN2, IDAC2 = AIN3

9.2.2.2.1 Design Variations for 2-Wire and 4-Wire RTD Measurements

Implementing a 2- or 4-wire RTD measurement is very similar to the 3-wire RTD measurement illustrated in Figure 77, except that only one IDAC is required.

Figure 78 shows a typical circuit implementation of a 2-wire RTD measurement. The main difference compared to a 3-wire RTD measurement is with respect to the lead resistance compensation. The voltage drop across the lead resistors, R_{LEAD1} and R_{LEAD2}, in this configuration is directly part of the measurement (as shown in Equation 40) because there is no means to compensate the lead resistance by use of the second current source. Any compensation must be done by calibration.

$$V_{IN} = I_{IDAC1} \cdot (R_{LEAD1} + R_{RTD} + R_{LEAD2}) \quad (40)$$

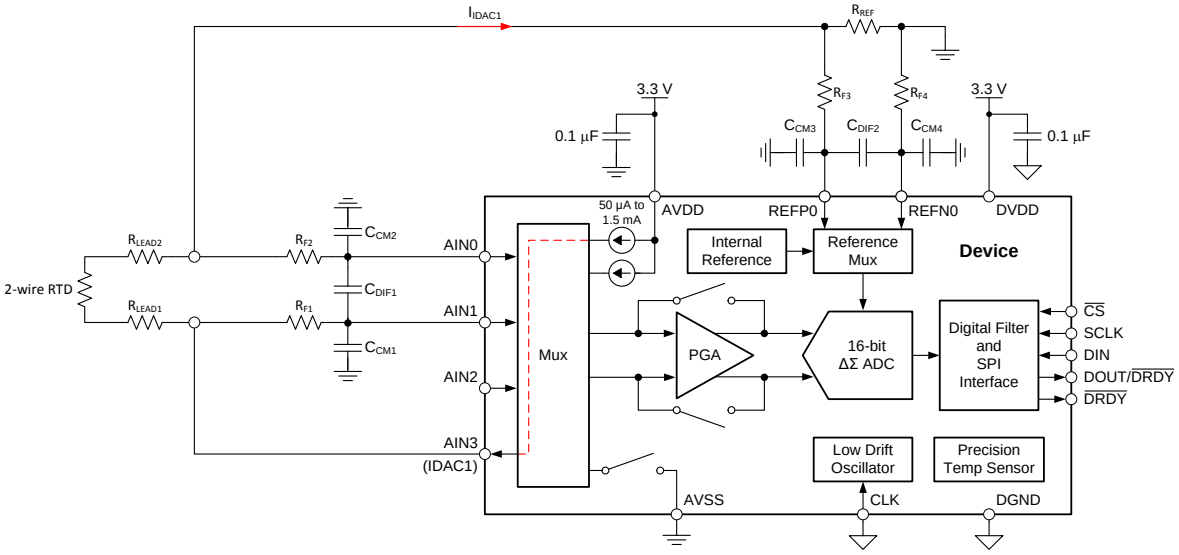


Figure 78. 2-Wire RTD Measurement

Figure 79 shows a typical circuit implementation of a 4-wire RTD measurement. Similar to the 2-wire RTD measurement, only one IDAC is required for exciting and measuring a 4-wire RTD in a ratiometric manner. The main benefit of using a 4-wire RTD is that the ADC inputs are connected to the RTD in the form of a Kelvin connection. Apart from the input leakage currents of the ADC, there is no current flow through the lead resistors R_{LEAD2} and R_{LEAD3} and therefore no voltage drop is created across them. The voltage at the ADC inputs consequently equals the voltage across the RTD and the lead resistance is of no concern.

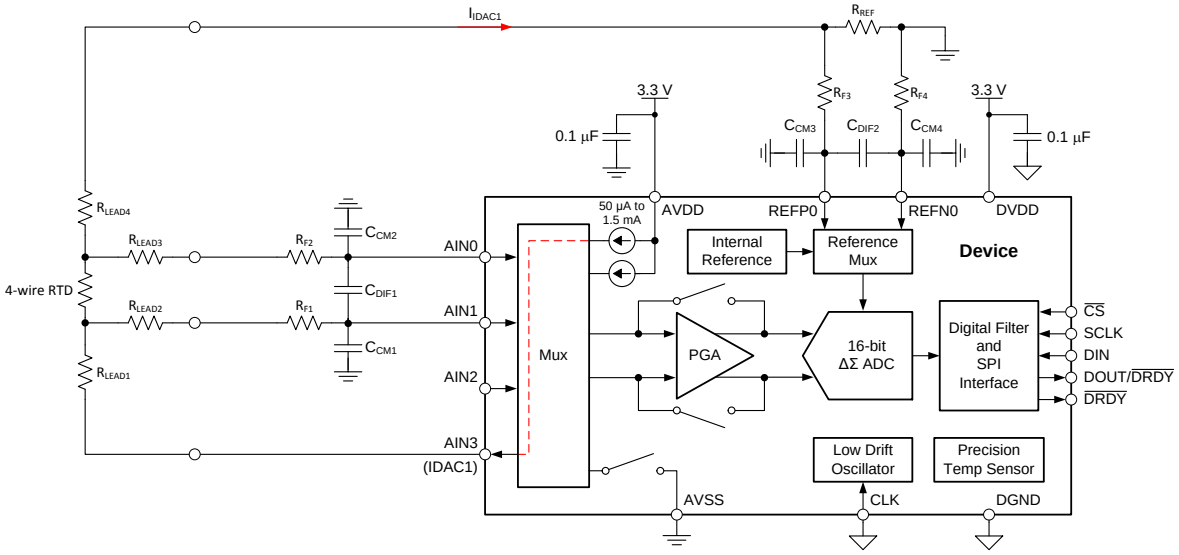


Figure 79. 4-Wire RTD Measurement

Note that because only one IDAC is used and flows through the reference resistor, R_{REF}, the transfer function of a 2- and 4-wire RTD measurement differs compared to the one of a 3-wire RTD measurement by a factor of 2, as shown in Equation 41.

$$\text{Code} \propto (R_{RTD\ (at\ Temperature)} \cdot \text{Gain}) / R_{REF} \quad (41)$$

In addition, the common-mode and reference voltage is reduced compared to the 3-wire RTD configuration. Therefore, some further modifications may be required in case the 3-wire RTD design is used to measure 2- and 4-wire RTDs as well. If the decreased common-mode voltage does not meet the $V_{CM\ (MIN)}$ requirements of the PGA anymore, either increase the value of R_{REF} by switching in a larger resistor or, alternatively, increase the excitation current while decreasing the gain at the same time.

9.2.2.3 Application Curves

Figure 80 and Figure 81 show the measurement results. The measurements are taken at T_A = 25°C. A system offset calibration is performed using a reference resistor of 100 Ω. No gain calibration is implemented. The data in Figure 80 are taken using precision resistors instead of a 3-wire Pt100. The respective temperature measurement error in Figure 81 is calculated from the data in Figure 80 using the NIST tables.

The design meets the required temperature measurement accuracy given in Table 19. Note that the measurement error shown in Figure 81 does not include the error of the RTD itself.

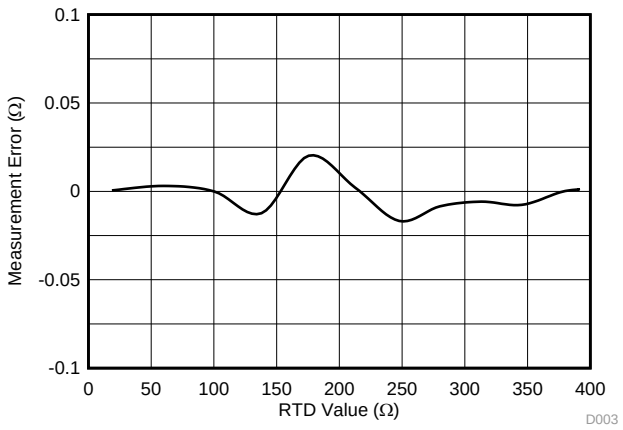


Figure 80. Resistance Measurement Error vs R_{RTD}

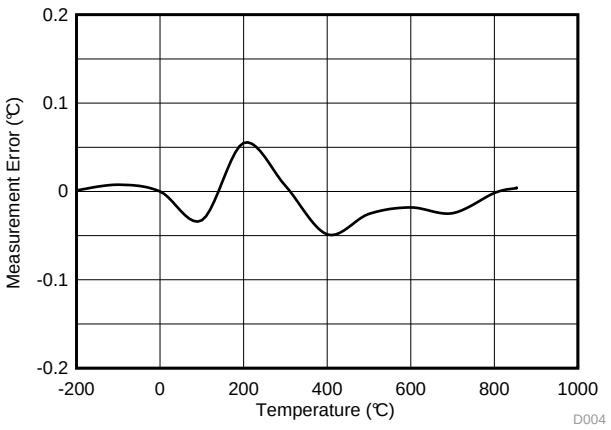


Figure 81. Temperature Measurement Error vs $T_{(RTD)}$

9.2.3 Bridge Measurement

The device offers several features to ease the implementation of ratiometric bridge measurements (such as a PGA with gains up to 128, buffered, differential reference inputs, and a low-side power switch).

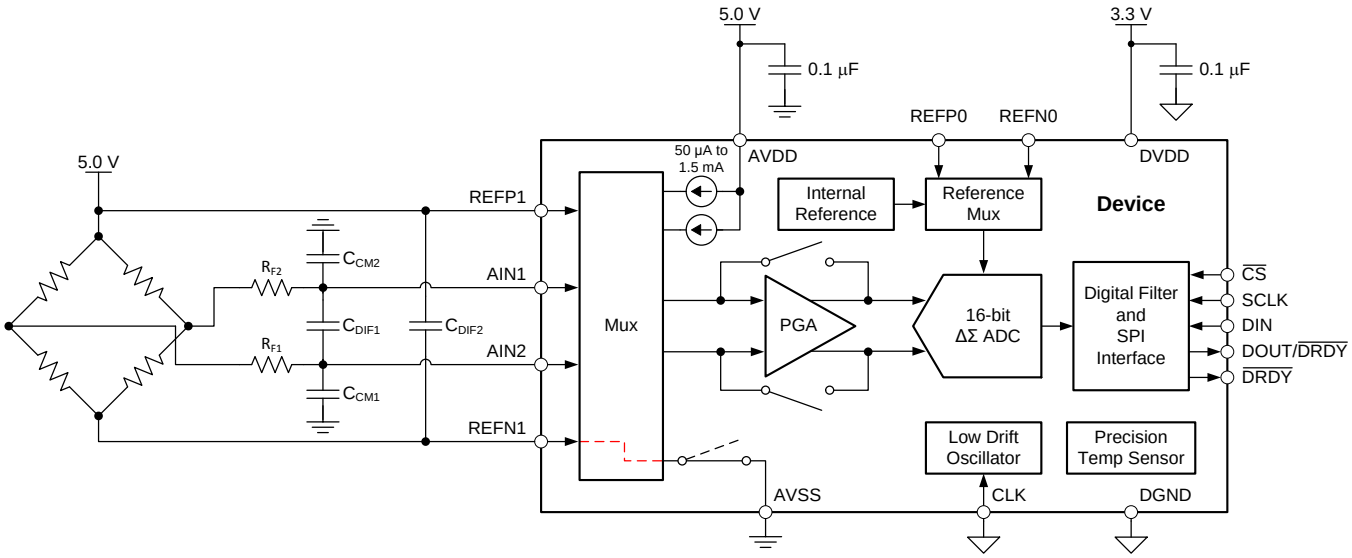


Figure 82. Bridge Measurement

9.2.3.1 Design Requirements

Table 21. Design Requirements

DESIGN PARAMETER	VALUE
Analog supply voltage	5.0 V
Digital supply voltage	3.3 V
Load cell type	4-wire load cell
Load cell sensitivity	2 mV/V
Excitation voltage	5 V
Noise-free counts	8000

9.2.3.2 Detailed Design Procedure

To implement a ratiometric bridge measurement, the bridge excitation voltage is simultaneously used as the reference voltage for the ADC; see Figure 82. With this configuration, any drift in excitation voltage also shows up on the reference voltage, consequently canceling out drift error. Either of the two device reference input pairs can be connected to the bridge excitation voltage. However, only the negative reference input (REFN1) can be internally routed to a low-side power switch. By connecting the low side of the bridge to REFN1, the device can automatically power-down the bridge by opening the low-side power switch. When the PSW bit in the configuration register is set to 1, the device opens the switch every time a POWERDOWN command is issued and closes the switch again when a START/SYNC command is sent.

The PGA offers gains up to 128, which helps amplify the small differential bridge output signal to make optimal use of the ADC full-scale range. Using a symmetrical bridge with the excitation voltage equal to the supply voltage of the device ensures that the output signal of the bridge meets the common-mode voltage requirement of the PGA.

Note that the maximum input voltage of ADS1120-Q1 is limited to $V_{IN\ (MAX)}$ = ±[(AVDD – AVSS) – 0.4 V] / Gain, which means the entire full-scale range, FSR = ±(AVDD – AVSS) / Gain, cannot be used in this configuration. This limitation is a result of the output drive capability of the PGA amplifiers (A1 and A2); see Figure 39. The output of each amplifier must stay 200 mV away from the rails (AVDD and AVSS), otherwise the PGA becomes nonlinear. Consequently, the maximum output swing of the PGA is limited to V_{OUT} = ±[(AVDD – AVSS) – 0.4 V].

Using a 2-mV/V load cell with a 5-V excitation yields a maximum differential output voltage of $V_{IN\ (MAX)}$ = ±10 mV, which meets Equation 42 when using a gain of 128.

$$V_{IN\ (MAX)} \leq \pm[(AVDD - AVSS) - 0.4\ V] / Gain = \pm(5\ V - 0.4\ V) / 128 = \pm 36\ mV \quad (42)$$

A first-order differential and common-mode RC filter (R_{F1}, R_{F2}, C_{DIF1}, C_{CM1}, and C_{CM2}) is placed on the ADC inputs. The reference has an additional capacitor C_{DIF2} to limit reference noise. Care must be taken to maintain a limited amount of filtering or the measurement will no longer be ratiometric.

The device is capable of 16-bit, noise-free resolution using a gain of 128 at 20 SPS for the specified reference voltage. Accordingly the device is able to resolve signals as small as one LSB. The LSB size is calculated using Equation 43:

$$1\ LSB = (2 \cdot V_{ref} / Gain) / 2^{16} = (2 \cdot 5.0\ V / 128) / 2^{16} = 1.192\ \mu V \quad (43)$$

To find the total number of counts available for the bridge measurement, the maximum output voltage is divided by the LSB value. Dividing 10 mV by 1.192 µV equates to 8389 total counts available, which meets the design parameter of 8000 counts.

The register settings for this design are shown in Table 22.

Table 22. Register Settings

REGISTER	SETTING	DESCRIPTION
00h	3Eh	AIN_P = AIN1, AIN_N = AIN2, gain = 128, PGA enabled
01h	04h	DR = 20 SPS, normal mode, continuous conversion mode
02h	98h	External reference (REFP1, REFN1), simultaneous 50-Hz and 60-Hz rejection, PSW = 1
03h	00h	No IDACs used

10 Power-Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels.

10.1 Power-Supply Sequencing

The power supplies can be sequenced in any order but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage limits. Wait approximately 50 µs after all power supplies are stabilized before communicating with the device to allow the power-up reset process to complete.

10.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply) and DVDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 83 and Figure 84. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. TI recommends connecting analog and digital ground together as close to the device as possible.

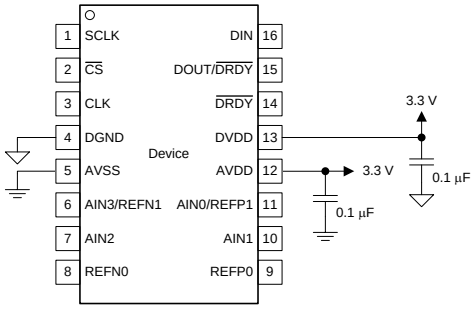


Figure 83. Unipolar Analog Power Supply

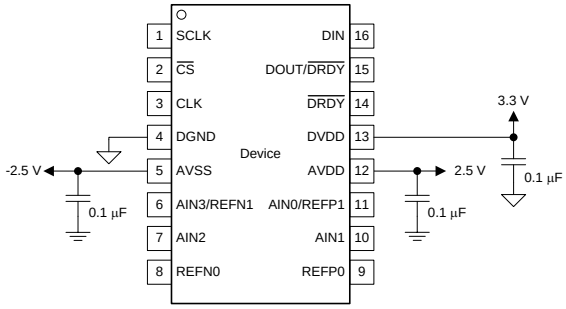


Figure 84. Bipolar Analog Power Supply

11 Layout

11.1 Layout Guidelines

TI recommends employing best design practices when laying out a printed circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 85. Although Figure 85 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

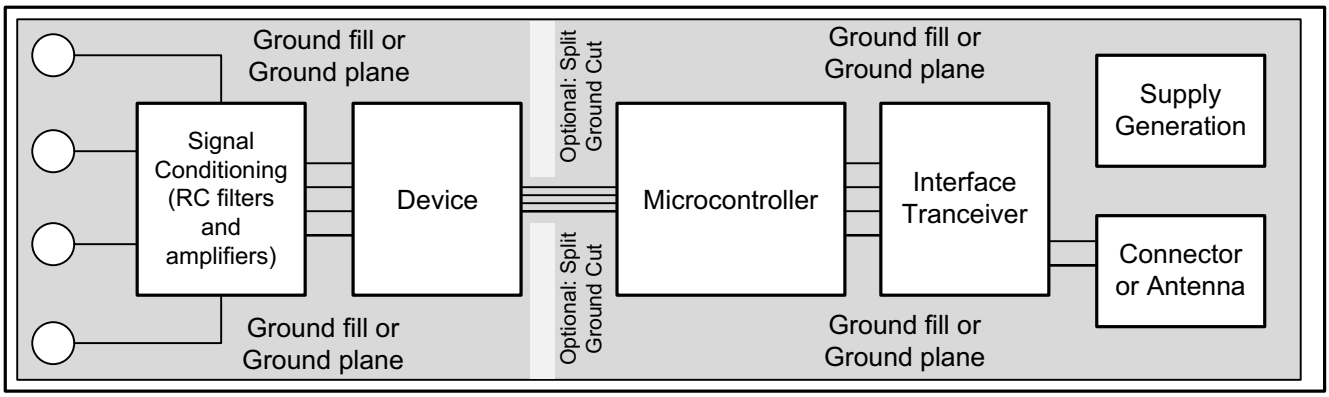


Figure 85. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Supply pins must be bypassed to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. If AVSS is connected to a negative supply, then connect an additional bypass capacitor from AVSS to AGND as well. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements are AIN0, AIN1 and AIN2, AIN3. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

11.2 Layout Example

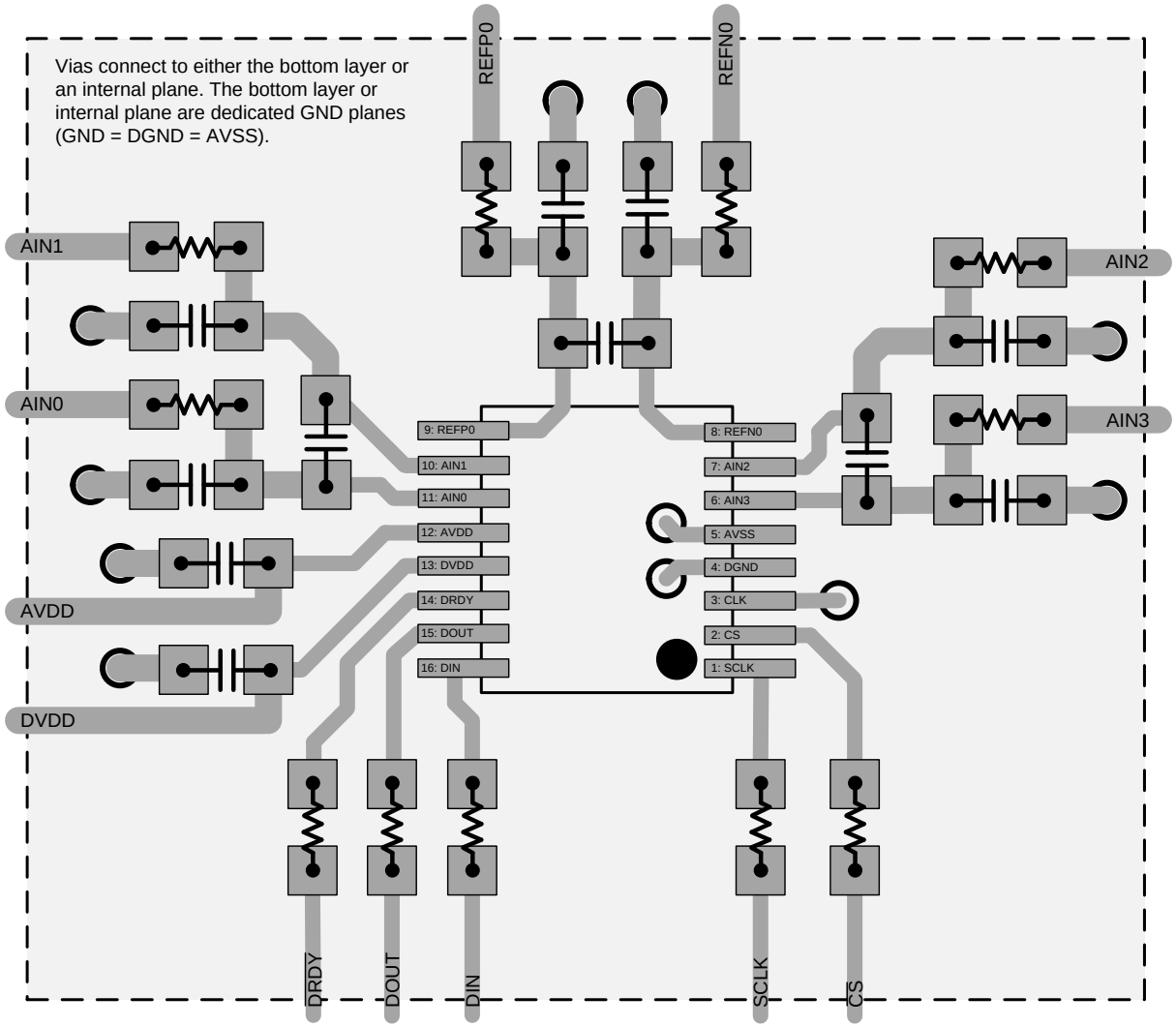


Figure 86. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

REF5020A-Q1 数据表，SBOS456

*《采用 ADS1148 和 ADS1248 进行 RTD 比率测量和滤波》*应用报告，SBAA201

12.2 商标

SPI is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1120QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	A1120Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

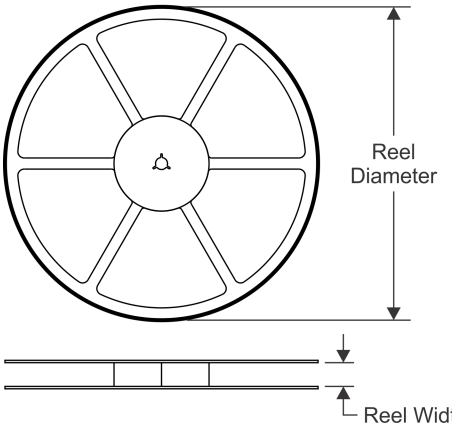
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

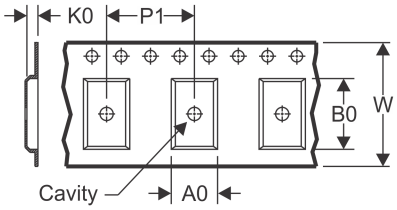
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

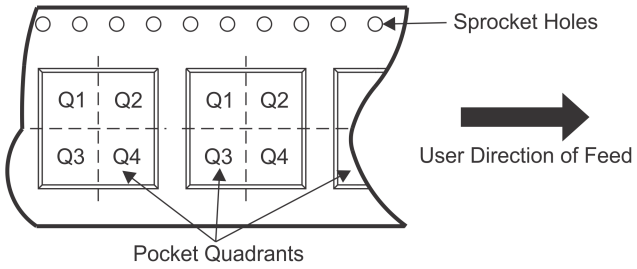


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

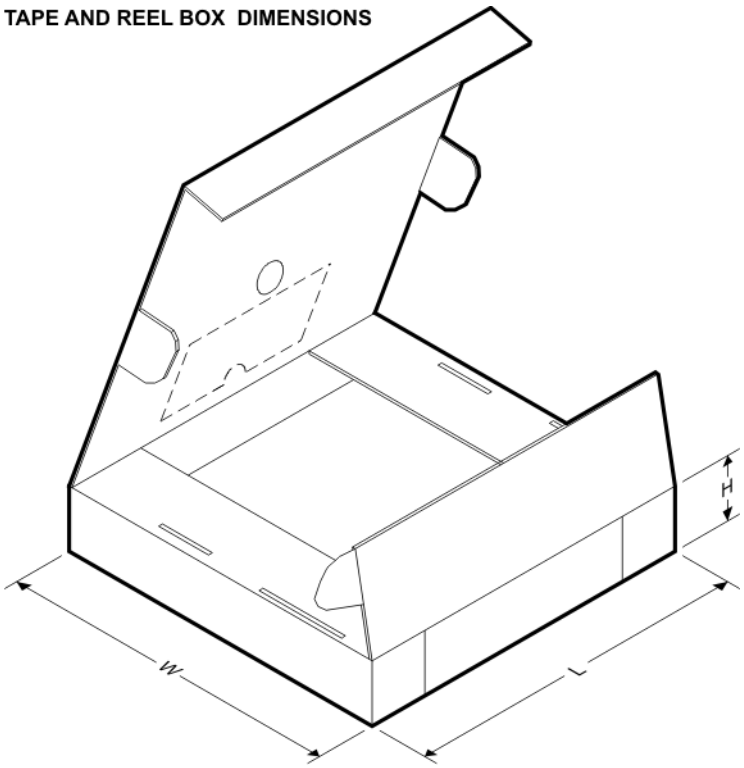
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1120QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

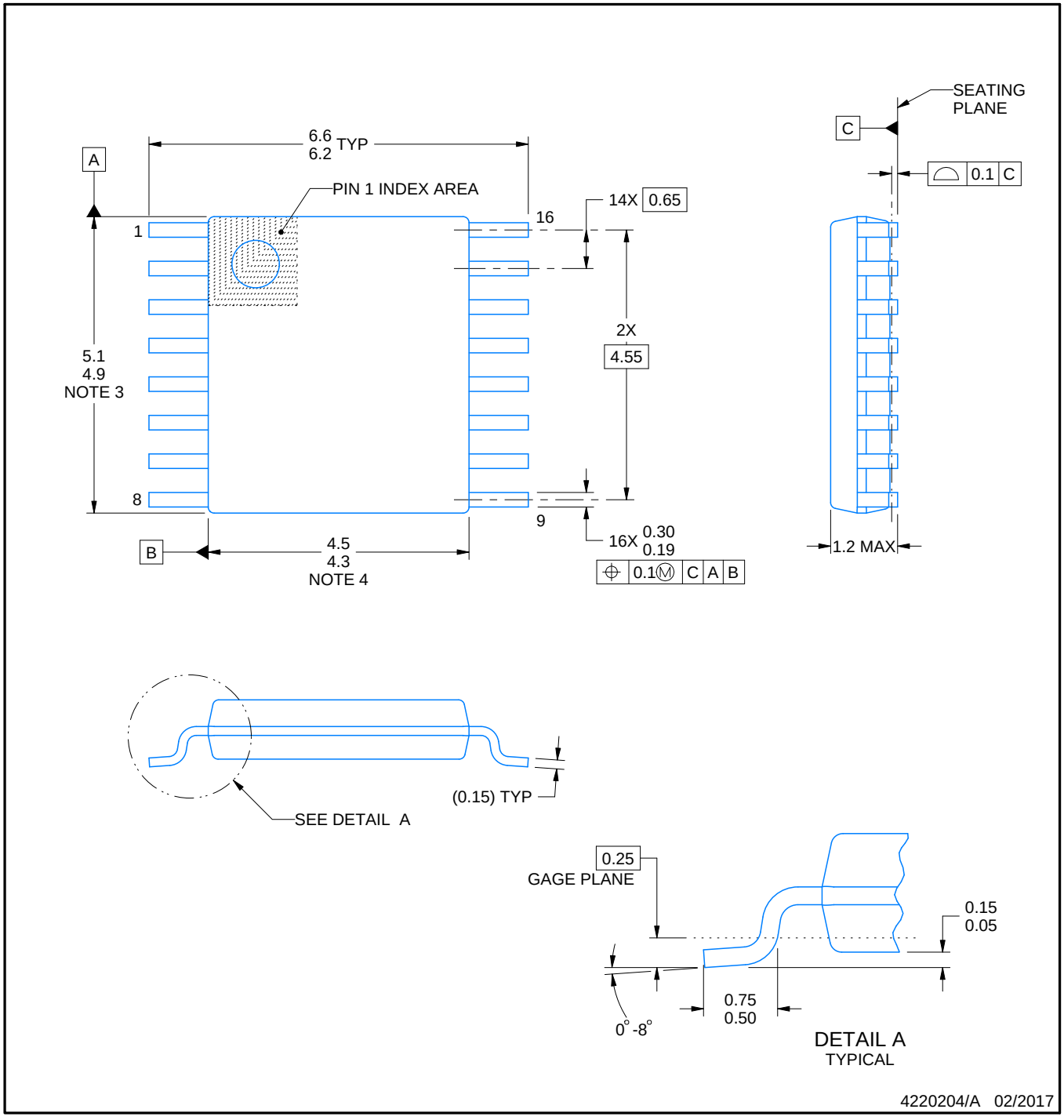
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1120QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

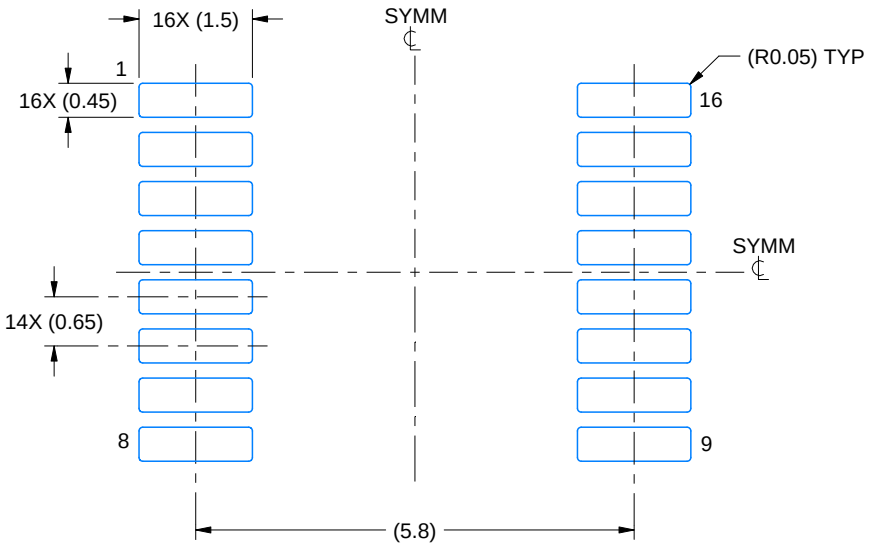
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

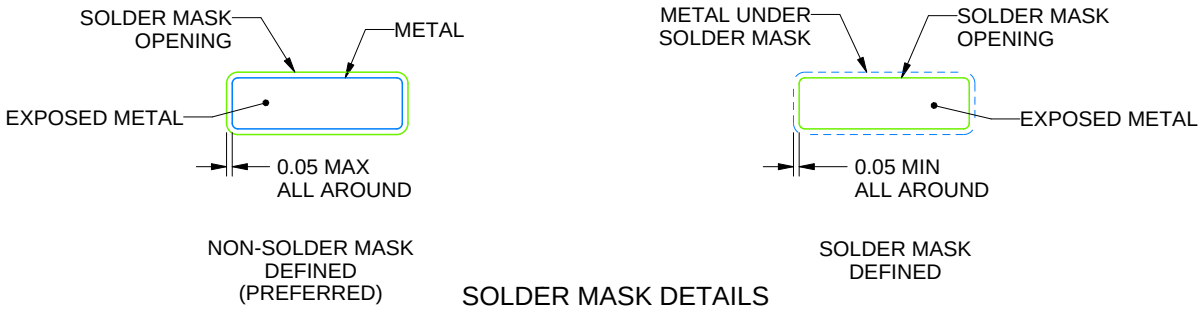


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

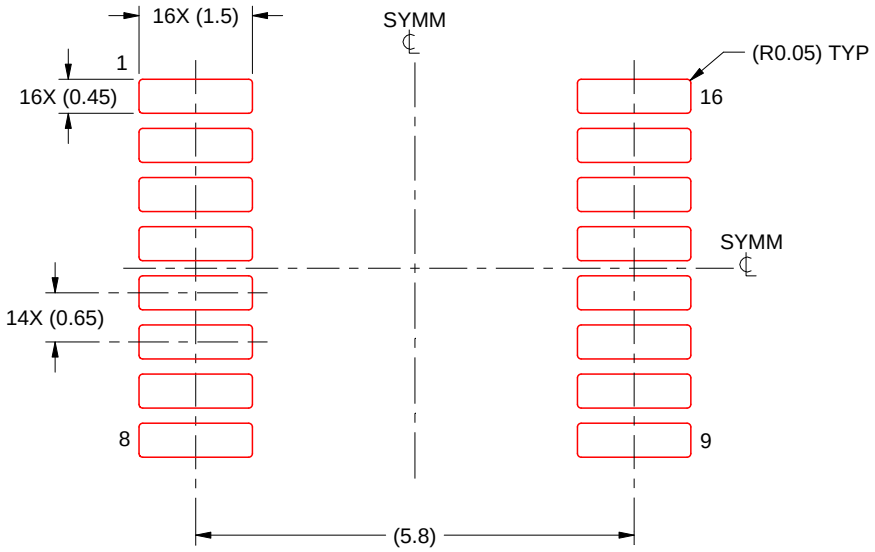


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265