

# 具备 PowerPath、USB BC1.2 检测和 USB On-the-Go (OTG) 升压式的 BQ25886 独立式 2 节电池、2A 升压模式电池充电器

## 1 特性

- 高效的 2A、1.5MHz 开关模式升压充电器
  - 在 5V 适配器、7.6V 电池、充电电流为 1A 下的充电效率为 93.4%
  - 针对 USB 输入和 2 节锂离子电池进行了优化
- 单个输入，支持 USB 输入适配器
  - 支持 4.3V 至 6.2V 的输入电压范围，绝对最大输入电压额定值为 20V
  - 输入电流限制（500mA 至 3.3A），支持 USB2.0、USB3.0 标准适配器
  - 集成式 USB D+/D- 自动检测 USB SDP、CDP、DCP 以及非标准适配器
- 独立功能，具有 PowerPath 管理功能
  - 采用 17mΩ 电池放电 MOSFET，具有较高的电池放电效率
  - 窄 VDC (NVDC) PowerPath 管理
    - 无需电池或深度放电的电池即可瞬时启动
    - 电池充电模式下实现理想的二极管运行
  - 通过 VSET 引脚可调的充电电压支持 8.2V、8.4V、8.7V 和 8.8V
  - 通过 ICHGSET 引脚可调的充电电流支持 100 至 2200mA
  - 通过 ILIM 引脚可调的输入电流限制
- 输入电流优化器 (ICO)，无需过载适配器即可最大限度地提高输入功率
- 高集成度包括所有 MOSFET、电流检测和环路补偿
- 高精度
  - ±0.5% 充电电压调节
  - ±5% 充电电流调节
  - ±7.5% 输入电流调节
- 安全
  - 在充电下的电池温度检测
  - 热调节和热关断

## 2 应用

- 无线扬声器
- 智能扬声器
- EPOS 打印机
- 便携式 POS
- IP 网络摄像头

## 3 说明

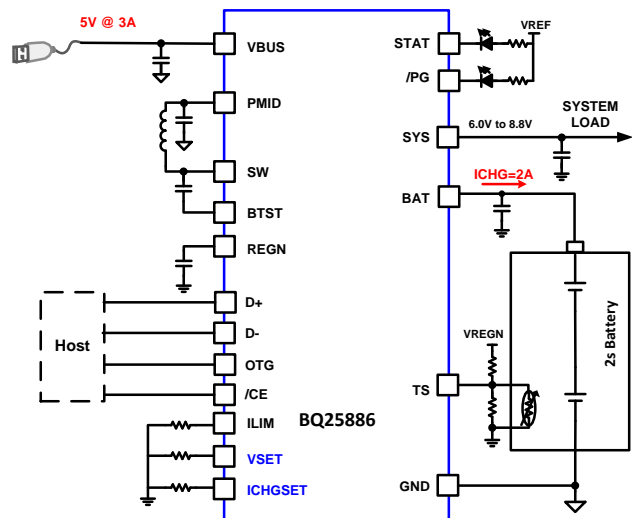
BQ25886 是一款高度集成的 2A 升压式开关模式电池充电管理以及能实现即时通电并提供精确终端控制的系统 PowerPath 管理器件，适用于 2 节 (2s) 锂离子和锂聚合物电池。BQ25886 是具有 PowerPath 和 OTG 功能的独立解决方案。

### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
BQ25886	VQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

### 简化原理图



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### Changes from Original (March 2019) to Revision A

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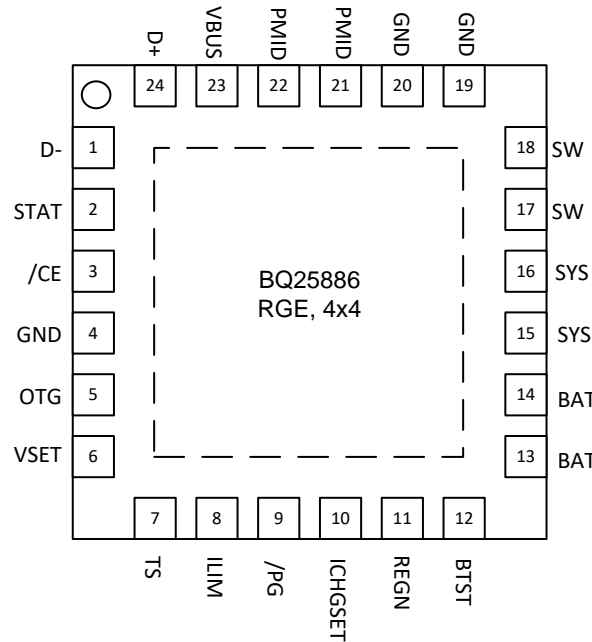
## 5 Device Comparison Table

**Table 1. Device Comparison**

<b>PART NUMBER</b>	<b>BQ25882</b>	<b>BQ25883</b>	<b>BQ25886</b>	<b>BQ25887</b>
VBUS Operating Range	3.9 to 6.2 V	3.9 to 6.2 V	4.3 to 6.2 V	3.9 to 6.2 V
USB Detection	D+/D-	D+/D-	D+/D-	PSEL
PowerPath	Yes	Yes	Yes	No
Cell Balancing	No	No	No	Yes
OTG	Up to 2 A	Up to 2 A	Up to 2 A	No OTG
16 bit ADC	Yes	Yes	No	Yes
Control Interface	I2C	I2C	Standalone	I2C
Status Pin	/PG	STAT, /PG	STAT, /PG	STAT, /PG
Package	2.1x2.1 WCSP-25	4x4 QFN-24	4x4 QFN-24	4x4 QFN-24

## 6 Pin Configuration and Functions

RGE Package (Standalone)  
24-Pin VQFN  
Top View



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D+	24	AIO	<b>Positive USB data line</b> – D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
D–	1	AIO	<b>Negative USB data line</b> – D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
STAT	2	DO	<b>Open drain charge status indicator</b> – Connect to the pull-up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault occurs, the STAT pin blinks at 1Hz.
$\overline{\text{CE}}$	3	DI	<b>Active Low Charge Enable Pin</b> – Battery charging is enabled when $\overline{\text{CE}}$ pin is LOW. $\overline{\text{CE}}$ pin is internally pulled low with 900k-Ω resistor.
OTG	5	DI	<b>OTG</b> – USB On-The-Go Enable input. Pull high to enable OTG function. Pull low to disable OTG function.
VSET	6	AI	<b>Battery Charge Voltage Limit</b> – VSET pin sets battery charge voltage. Program battery regulation voltage with a resistor pull-down from VSET to GND as follows: $R_{\text{VSET}} < 18\text{k}\Omega$ (short to GND) = 8.2 V $R_{\text{VSET}} = 39\text{k}\Omega$ ( $\pm 10\%$ ) = 8.8 V $R_{\text{VSET}} = 75\text{k}\Omega$ ( $\pm 10\%$ ) = 8.7 V $R_{\text{VSET}} > 150\text{k}\Omega$ (floating) = 8.4 V
TS	7	AI	<b>Temperature Qualification Voltage</b> – Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. Recommend 103AT-2 thermistor.
ILIM	8	AI	<b>Input Current Limit (IINDPM)</b> – ILIM pin sets the maximum input current and can be used to monitor input current. IINDPM loop regulates ILIM pin voltage at 0.8V. When ILIM pin is less than 0.8V, the input current can be calculated by $I_{\text{IN}} = K_{\text{ILIM}} \times V_{\text{ILIM}} / (R_{\text{ILIM}} \times 0.8\text{V})$ . A resistor connected from ILIM pin to ground sets the input current limit as maximum ( $I_{\text{INMAX}} = K_{\text{ILIM}} / R_{\text{ILIM}}$ ). When ILIM pin is short to GND, the input current limit is set to maximum by ILIM. Input current limit less than 500mA is not supported on ILIM pin. Do not float this pin.

**Pin Functions (continued)**

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{PG}$	9	DO	<b>Open drain active low power good indicator</b> – Connect to the pull up rail via 10-k $\Omega$ resistor. LOW indicates a good input source if the input voltage is within VVBUS_OP (3.9 V), and can provide more than IPOORSRC (30 mA).
ICHGSET	10	AI	<b>Charge Current Limit</b> – A resistor from ICHGSET to GND is used to program the charge current. The acceptable programming range on ICHGSET pin is 30mA (114 $\Omega$ ) – 2.2A (8k $\Omega$ ). Pre-charge and termination current is 1/10 of the fast charge current. The minimum pre-charge current is clamped at 30mA (typ). Minimum termination current is clamped at 10mA (typ). ICHGSET short to GND clamps charge current to minimum setting 30mA (typ). Floating ICHGSET disables charge.
REGN	11	P	<b>Gate Drive Supply</b> – Bias supply for internal MOSFETs driver and IC. Bypass REGN to GND with a 4.7- $\mu$ F ceramic capacitor. REGN current limit is 50 mA.
BTST	12	P	<b>PWM High-side Driver Supply</b> – Internally, BTST is connected to the cathode of the boot-strap diode. Connect a 47nF bootstrap capacitor from SW to BTST.
BAT	13, 14	P	<b>Battery Power Connection</b> – Connect minimum recommended 10- $\mu$ F capacitance after derating closely to the BAT pin and GND.
SYS	15, 16	P	<b>System Connection</b> – The internal BATFET is connected between SYS and BAT. When the battery falls below the minimum system voltage, the switch-mode converter keeps SYS above the minimum system voltage. Connect a 2x22- $\mu$ F capacitance after derating closely to the SYS pin and PGND.
SW	17, 18	P	<b>Inductor Connection</b> – Connect to the switched side of the external inductor.
GND	19, 20, 4	–	<b>Ground Return</b>
PMID	21, 22	P	<b>Blocking MOSFET Connection</b> – The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF. At least 1-uF is recommended at VBUS with the remainder at PMID. Typical value for PMID is 10 uF.
VBUS	23	P	<b>Input Supply</b> – VBUS is connected to the external DC supply. Bypass VBUS to GND with at least 1- $\mu$ F ceramic capacitor, placed as close to the IC as possible.
NC	1	–	<b>No Connect</b> – Leave these pins floating or tie to ground.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage Range (with respect to GND unless otherwise specified)	V <sub>BUS</sub> (converter not switching)	-0.3	20	V
	P <sub>MID</sub> (converter not switching)	-0.3	8.5	V
	BAT, SYS (converter not switching)	-0.3	12	V
	SW	-0.3 <sup>(2)</sup>	13	V
	BTST	-0.3	19	V
	REGN, STAT, /PG, TS	-0.3	6	V
	ILIM	-0.3	5	V
	BTST to SW	-0.3	6	V
D+, D-, ICHGSET, VSET, /CE	-0.3	6	V	
Output Sink Current	STAT, /PG		6	mA
Junction Temperature, T <sub>J</sub>		-40	150	°C
Storage temperature, T <sub>stg</sub>		-40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) -2V for 50ns

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>VBUS</sub>	Input Voltage	4.3		6.2	V
I <sub>VBUS</sub>	Average input current (VBUS)			3.3	A
I <sub>BAT</sub>	Average charge current (IBAT)			2.2	A
I <sub>BAT_RMS</sub>	RMS discharging current with internal MOSFET			5	A
I <sub>BAT_PK</sub>	Peak discharging current with internal MOSFET			9 (up to 1us)	A
V <sub>BAT</sub>	Battery Voltage			9.2 <sup>(1)</sup>	V
T <sub>A</sub>	Operating free-air temperature range	-40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on SW pin. A tight layout minimizes switching noise.

## 7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC <sup>(1)</sup>		BQ25886	
		RGE (VQFN)	
		24-PIN	
			UNIT
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (EVM <sup>(2)</sup> )	18	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (JEDEC <sup>(1)</sup> )	32.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	10.7	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	10.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, [SPRA953](#).

(2) Measured on 35μm thick copper, 4-layer board

## 7.5 Electrical Characteristics

V<sub>VBUS\_UVLO\_RISING</sub> < V<sub>VBUS</sub> < V<sub>VBUS\_OV</sub>, T<sub>J</sub> = -40°C to +125°C, and T<sub>J</sub> = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>QUIESCENT CURRENTS</b>						
I <sub>BAT</sub>	Battery discharge current (BAT)	VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T <sub>J</sub> = 25°C, ADC Disabled		12	14	μA
		VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T <sub>J</sub> < 85°C, ADC Disabled		12	20	μA
I <sub>VBUS_HIZ</sub>	Input supply current (VBUS) in HIZ	VBUS = 5 V, High-Z Mode, no battery, 25°C		30	48	μA
		VBUS = 5 V, High-Z Mode, no battery, <85°C		30	55.2	μA
I <sub>VBUS</sub>	Input supply current (VBUS)	VBUS = 5 V, V <sub>BAT</sub> = 7.6 V, converter not switching		1.5	3	mA
		VBUS = 5 V, V <sub>BAT</sub> = 7.6 V, converter switching, I <sub>SYS</sub> = 0A		3		mA
<b>VBUS/VBAT POWER UP</b>						
V <sub>VBUS_OP</sub>	VBUS operating range		4.3		6.2	V
V <sub>VBUS_UVLO_RISING</sub>	VBUS rising, no battery	VBUS rising		3.3	3.68	V
V <sub>VBUS_OV</sub>	VBUS over-voltage rising threshold	VBUS rising		6.2	6.6	V
	VBUS over-voltage falling threshold	VBUS falling		5.9	6.4	V
V <sub>POORSRC_FALLING</sub>	Bad adapter detection threshold	VBUS falling below V <sub>POORSRC_FALLING</sub>		3.7		V
I <sub>POORSRC</sub>	Bad adapter detection current source			15		mA
<b>POWER-PATH</b>						
V <sub>SYS</sub>	Typical System Regulation Voltage	ISYS = 0A, VBAT = 8.80 V > SYS_MIN, Charge Disabled		100		mV
		ISYS = 0A, VBAT < SYS_MIN, Charge Disabled		200		mV
V <sub>SYS_MIN</sub>	System Regulation Voltage	VBAT < SYS_MIN, Charge Disabled	6.2	6.4		V
<b>BATTERY CHARGER</b>						
V <sub>REG_ACC</sub>	Charge voltage	RVSET < 18 kΩ, VREG = 8.20 V, T <sub>J</sub> = -40°C - 85°C	8.159	8.2	8.241	V
V <sub>REG_ACC</sub>	Charge voltage	RVSET = 39 kΩ (±10%), VREG = 8.80 V, T <sub>J</sub> = -40°C - 85°C	8.756	8.8	8.844	V
V <sub>REG_ACC</sub>	Charge voltage	RVSET = 75 kΩ (±10%), VREG = 8.70 V, T <sub>J</sub> = -40°C - 85°C	8.656	8.7	8.744	V
V <sub>REG_ACC</sub>	Charge voltage	RSET > 150kΩ, VREG = 8.40 V, T <sub>J</sub> = -40°C to 85°C	8.358	8.4	8.442	V

### Electrical Characteristics (continued)

$V_{VBUS\_UVLO\_RISING} < V_{VBUS} < V_{VBUS\_OV}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$K_{ICHGSET}$	Charge current regulation setting ratio	$ICHG = R_{ICHGSET}/K_{ICHGSET}$ . $ICHG = 1000$ mA		3810		$\Omega/A$
$I_{CHG\_RANGE}$	Charge current regulation range		30		2200	mA
$I_{CHG\_ACC}$	Fast Charge current regulation accuracy	$ICHG = 1000$ mA, $VBAT = 6.2$ V or $7.6$ V, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	-7.5		7.5	%
$I_{CHG\_ACC}$	Fast Charge current regulation accuracy	$ICHG = 500$ mA, $VBAT = 6.2$ V or $7.6$ V, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	-15		15	%
$I_{CHG\_ACC}$	Fast Charge current regulation accuracy	$ICHG = 250$ mA, $VBAT = 6.2$ V or $7.6$ V, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	-25		25	%
$I_{PRECHG\_RANGE}$	Precharge current range		30		800	mA
$I_{PRECHG\_ACC}$	Precharge current accuracy	$VBAT = 5.2$ V, $IPRECHG = 200$ mA, $T_J = 25^{\circ}\text{C}$	170		237	mA
		$VBAT = 5.2$ V, $IPRECHG = 200$ mA, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	150		245	mA
$I_{TERM\_RANGE}$	Termination current range		10		800	mA
$I_{TERM\_ACC}$	Termination current accuracy	$ICHG = 1.5$ A, $ITERM = 150$ mA, $T_J = 25^{\circ}\text{C}$	143		159	mA
$I_{TERM\_ACC}$		$ICHG = 1.5$ A, $ITERM = 150$ mA, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	120		180	mA
$I_{TERM\_ACC}$		$ICHG = 1.5$ A, $ITERM = 50$ mA, $T_J = 25^{\circ}\text{C}$	42		60	mA
$I_{TERM\_ACC}$		$ICHG = 1.5$ A, $ITERM = 50$ mA, $T_J = 0^{\circ}\text{C}$ to $85^{\circ}\text{C}$	18		75	mA
$V_{BAT\_SHORT\_RISING}$	Short Battery Voltage rising threshold to start pre-charging	$VBAT$ rising	4.1	4.4	4.7	V
$V_{BAT\_SHORT\_FALLING}$	Short Battery Voltage falling threshold to stop pre-charging	$VBAT$ falling	3.7	4	4.3	V
$I_{BAT\_SHORT}$	Low Battery Voltage trickle charging current	$VBAT < 4.4$ V		100		mA
$V_{BAT\_LOWV\_RISING}$	$VBAT$ LOWV Rising threshold to start fast-charging	$VBAT$ rising, $VBATLOWV = 6.0$ V	5.7	6	6.3	V
$V_{BAT\_LOWV\_FALLING}$	$VBAT$ LOWV Falling threshold to stop fast-charging	$VBAT$ falling, $VBATLOWV = 6.0$ V	5.3	5.6	5.9	V
$V_{RECHG}$	Recharge threshold below $V_{REG}$	$VBAT$ falling		200		mV
$R_{ON\_QHS}$ (Q2)	High-side switching MOSFET on-resistance between SW and SYS (Q2)	$T_J = 25^{\circ}\text{C}$		32	35	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$		32	47	$\text{m}\Omega$
$R_{ON\_QLS}$ (Q3)	Low-side switching MOSFET on-resistance between SW and GND (Q3)	$T_J = 25^{\circ}\text{C}$		42	46	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$		42	63	$\text{m}\Omega$
$R_{ON\_QBAT}$ (Q4)	MOSFET on-resistance between SYS and BAT (Q4)	$T_J = 25^{\circ}\text{C}$		18	19	$\text{m}\Omega$
$R_{ON\_QBAT}$ (Q4)	MOSFET on-resistance between SYS and BAT (Q4)	$T_J = -40^{\circ}\text{C}$ - $85^{\circ}\text{C}$		18	23	$\text{m}\Omega$
$I_{BAT\_DISCHG}$	BAT Discharge current source	$VBAT = 8$ V, $EN\_BAT\_DISCHG = 1$	8	11.5	16	mA
<b>INPUT VOLTAGE / CURRENT REGULATION</b>						
$V_{INDPM}$	Input voltage regulation range		4.171	4.3	4.429	V
$K_{ILIM}$	$I_{INMAX} = K_{ILIM}/R_{ILIM}$	Input Current regulation by ILIM pin		1110		$A \times \Omega$
$I_{INDPM}$	Input current regulation limit, $I_{INMAX} = K_{ILIM}/R_{ILIM}$	Input Current regulation by ILIM pin = 0.5A	457	505	553	mA
		Input Current regulation by ILIM pin = 0.9A	839	909	980	mA
		Input Current regulation by ILIM pin = 1.5A	1413	1518	1624	mA
$R_{ON\_QBLK}$ (Q1)	Blocking MOSFET on-resistance between $VBUS$ and $PMID$ (QBLK)	$T_J = 25^{\circ}\text{C}$		33	37	$\text{m}\Omega$
		$T_J = -40^{\circ}\text{C}$ to $125^{\circ}\text{C}$		33	51	$\text{m}\Omega$



## Electrical Characteristics (continued)

 $V_{VBUS\_UVLO\_RISING} < V_{VBUS} < V_{VBUS\_OV}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>D + /D- DETECTION</b>						
$V_{D+D\_600MVSRC}$	D+/D- Voltage Source (600 mV)		500	600	700	mV
$I_{D+\_10UASRC}$	D+ Current Source (10 $\mu\text{A}$ )		7	10	14	$\mu\text{A}$
$I_{D+D\_100UASNK}$	D+/D- Current Sink (100 $\mu\text{A}$ )		50	100	150	$\mu\text{A}$
$V_{D+D\_0P325}$	D+/D- Comparator Threshold for Secondary Detection		250		400	mV
$R_{D\_19K}$	D- Resistor to Ground (19 k $\Omega$ )		14.25		24.8	k $\Omega$
$V_{D+\_0P8}$	D+ Comparator Threshold for Data Contact Detection				800	mV
$V_{D+D\_1P2}$	D+/D- Threshold for Non-standard adapter		1.05		1.35	V
$V_{D+D\_2P0}$	D+/D- Comparator Threshold for Non-standard adapter		1.85		2.15	V
$V_{D+D\_2P8}$	D+/D- Threshold for Non-standard adapter		2.55		2.85	V
$I_{D+D\_LKG}$	D+/D- Leakage Current	HiZ	-1		1	$\mu\text{A}$
<b>BATTERY OVER-VOLTAGE PROTECTION</b>						
$V_{BAT\_OVP\_RISING}$	Battery over-voltage rising threshold	VBAT rising, as percentage of VREG	102.5	104	105	%
$V_{BAT\_OVP\_FALLING}$	Battery over-voltage falling threshold	VBAT falling, as percentage of VREG	101	102	103.3	%
<b>THERMAL REGULATION AND THERMAL SHUTDOWN</b>						
$T_{REG}$	Junction temperature regulation accuracy	$T_{REG} = 120^{\circ}\text{C}$		120		$^{\circ}\text{C}$
$T_{SHUT\_RISING}$	Thermal Shutdown Rising threshold	Temperature Increasing		150		$^{\circ}\text{C}$
	Thermal Shutdown Falling threshold	Temperature Decreasing		120		$^{\circ}\text{C}$
<b>JEITA THERMISTOR COMPARATOR (BOOST MODE)</b>						
$V_{T1}$	TS pin voltage rising. T1 (0 $^{\circ}\text{C}$ ) threshold, Charge suspended below this temperature.	As Percentage to REGN	72.75	73.25	73.75	%
$V_{T1\_HYS}$	TS pin voltage falling. Charge re-enabled to ICHG/2 and VREG above this temperature	As Percentage to REGN		1.3		%
$V_{T2}$	TS pin voltage rising. T2 (10 $^{\circ}\text{C}$ ) threshold, charge set to ICHG/2 and VREG below this temperature	As Percentage to REGN	67.75	68.25	68.75	%
$V_{T2\_HYS}$	TS pin voltage falling. Charge set to ICHG and VREG above this temperature	As Percentage to REGN		1.2		%
$V_{T3}$	TS pin voltage falling. T3 (45 $^{\circ}\text{C}$ ) threshold, charge set to ICHG and 8.1 V above this temperature.	As Percentage to REGN	44.25	44.75	45.25	%
$V_{T3\_HYS}$	TS pin voltage rising. Charge set to ICHG and VREG below this temperature	As Percentage to REGN		1		%
$V_{T5}$	TS pin voltage falling. T5 (60 $^{\circ}\text{C}$ ) threshold, charge suspended above this temperature.	As Percentage to REGN	33.875	34.375	34.875	%
$V_{T5\_HYS}$	TS pin voltage rising. Charge set to ICHG and 8.1 V below this temperature	As Percentage to REGN		1.35		%
<b>COLD/HOT THERMISTOR COMPARATOR (OTG BUCK MODE)</b>						
$V_{BCOLD0}$	Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to REGN (Approx. – 10 $^{\circ}\text{C}$ w/ 103AT)	76.5	77	77.5	%
$V_{BCOLD0\_HYS}$	Cold Temperature Threshold, TS pin Voltage Falling Threshold	As Percentage to REGN		1		%

## Electrical Characteristics (continued)

 $V_{\text{VBUS\_UVLO\_RISING}} < V_{\text{VBUS}} < V_{\text{VBUS\_OV}}$ ,  $T_J = -40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ , and  $T_J = 25^{\circ}\text{C}$  for typical values (unless otherwise noted)

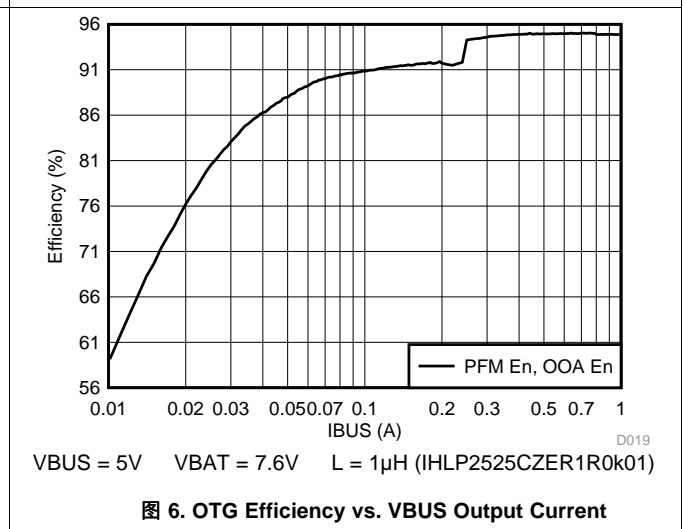
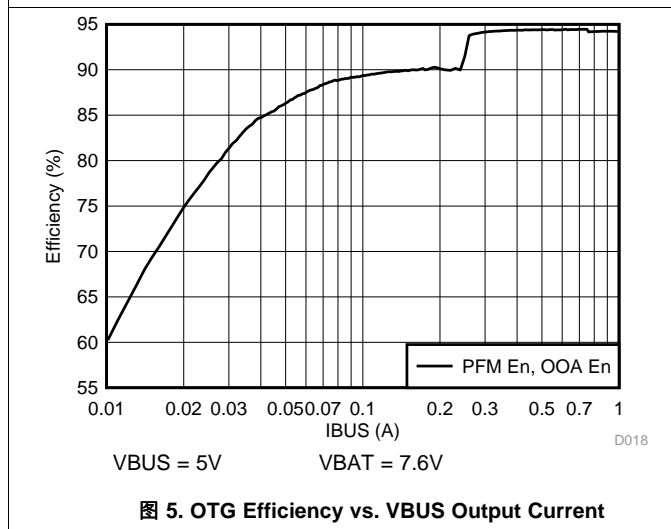
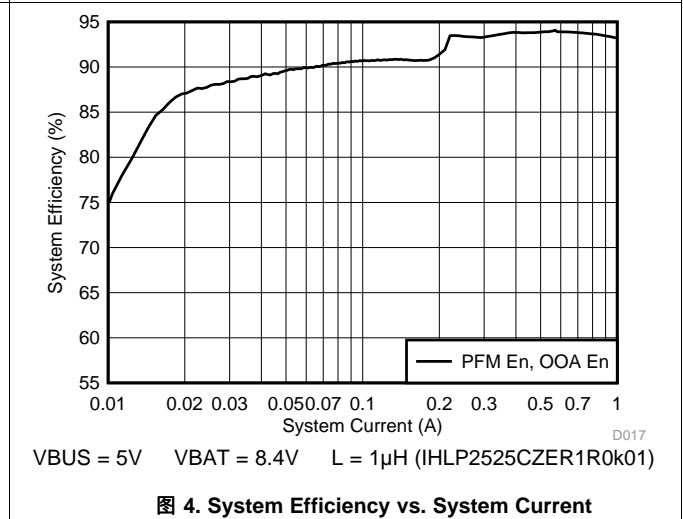
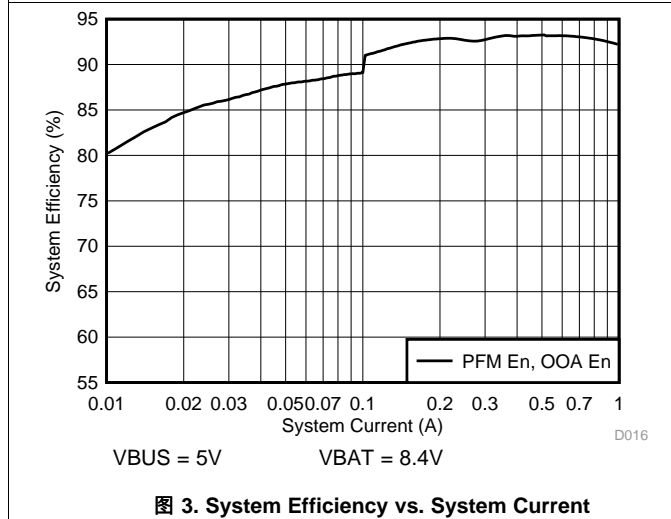
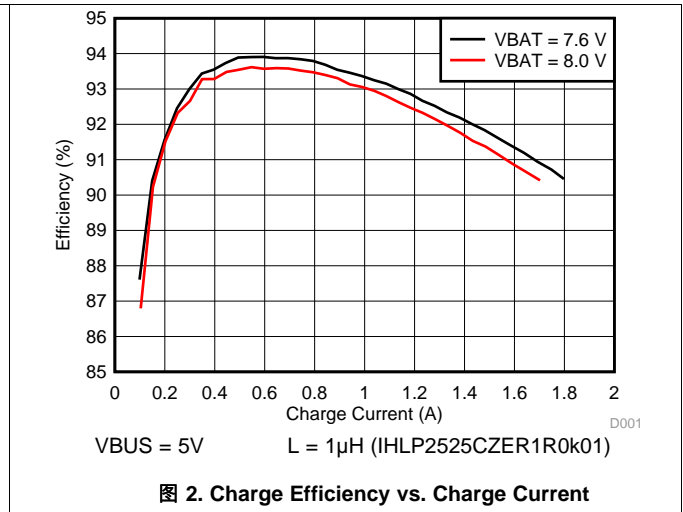
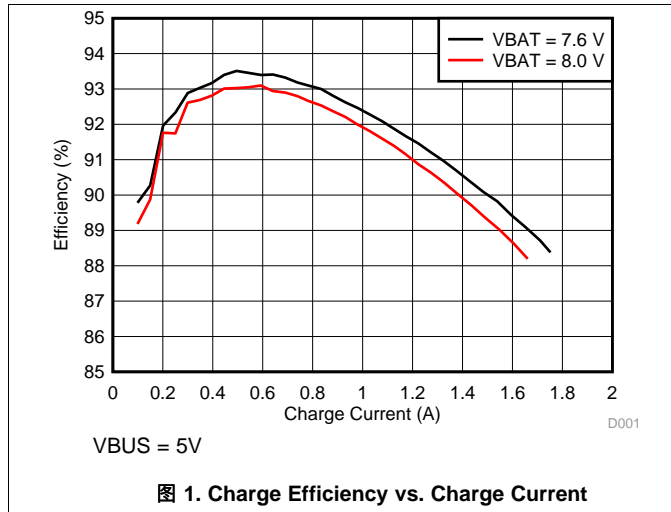
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{BHOT1}}$	Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to REGN (Approx. 60°C w/ 103AT)	33.875	34.375	34.875	%
$V_{\text{BHOT1\_HYS}}$	Hot Temperature Threshold, TS pin Voltage rising Threshold	As Percentage to REGN		3		%
<b>BOOST MODE CONVERTER</b>						
$F_{\text{SW}}$	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
<b>OTG BUCK MODE CONVERTER</b>						
$V_{\text{OTG\_ACC}}$	OTG Buck mode voltage regulation accuracy	$I_{\text{VBUS}} = 0\text{A}$ , $\text{OTG\_VLIM} = 5.1\text{V}$	4.947	5.1	5.253	V
$V_{\text{OTG\_ACC}}$	OTG Buck mode voltage regulation accuracy	$I_{\text{VBUS}} = 0\text{A}$ , $\text{OTG\_VLIM} = 5.1\text{V}$	-3		3	%
$I_{\text{OTG\_ACC}}$	OTG Buck mode current regulation accuracy	$\text{OTG\_ILIM} = 2\text{A}$	-15	-7.5	0	%
$V_{\text{OTG\_OVP}}$	OTG Buck mode over-voltage threshold		5.8	6		V
<b>REGN LDO</b>						
$V_{\text{REGN}}$	REGN LDO output voltage	$V_{\text{VBUS}} = 5\text{V}$ , $I_{\text{REGN}} = 20\text{mA}$	4.7	4.8	5.15	V
$I_{\text{REGN}}$	REGN LDO current limit	$V_{\text{VBUS}} = 5\text{V}$ , $V_{\text{REGN}} = 3.8\text{V}$	50			mA
<b>LOGIC I/O PIN (/CE)</b>						
$V_{\text{IH\_CEZ}}$	Input high threshold level, /CE		1.3			V
$V_{\text{IL\_CEZ}}$	Input low threshold level, /CE				0.4	V
$I_{\text{IN\_BIAS\_CEZ}}$	High level leakage current, /CE	Pull-up rail 1.8 V			2.5	µA
<b>LOGIC O PIN (/INT, /PG, STAT)</b>						
$V_{\text{OL}}$	Output low threshold level	Sink current = 5 mA			0.4	V
$I_{\text{OUT\_BIAS}}$	High level leakage current	Pull-up rail 1.8 V			1	µA

## 7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
<b>VBUS/BAT POWER UP</b>						
$t_{\text{VBUS\_OV}}$	VBUS OVP reaction time	VBUS rising above $V_{\text{BUS\_OV}}$ threshold to converter turn off		200		ns
$t_{\text{POORSRC}}$	Bad adapter detection duration			30		ms
<b>BATTERY CHARGER</b>						
$t_{\text{TERM\_DGL}}$	Deglitch time for charge termination	Charge current falling below $I_{\text{TERM}}$		250		ms
$t_{\text{RECGH\_DGL}}$	Deglitch time for recharge threshold	BAT voltage falling below $V_{\text{RECHG}} = 100\text{mV}$		250		ms
$t_{\text{BAT\_OVP\_DGL}}$	Deglitch time for battery over-voltage to disable charge			1		µs
$t_{\text{SAFETY}}$	Charge Safety Timer Accuracy	$\text{CHG\_TIMER} = 12\text{hours}$	10.8	12	13.2	hr
<b>DIGITAL CLOCK AND WATCHDOG TIMER</b>						
$f_{\text{LPDIG}}$	Digital low power clock	REGN LDO disabled	18	30	45	kHz
$f_{\text{DIG}}$	Digital clock	REGN LDO enabled	1.35	1.5	1.65	MHz

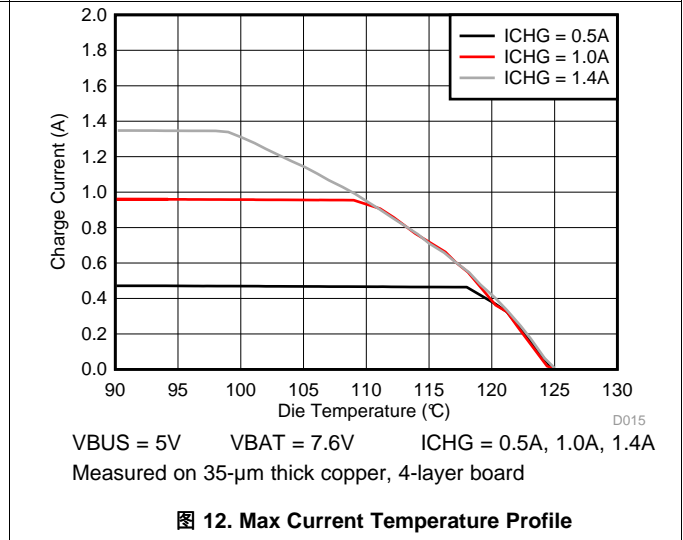
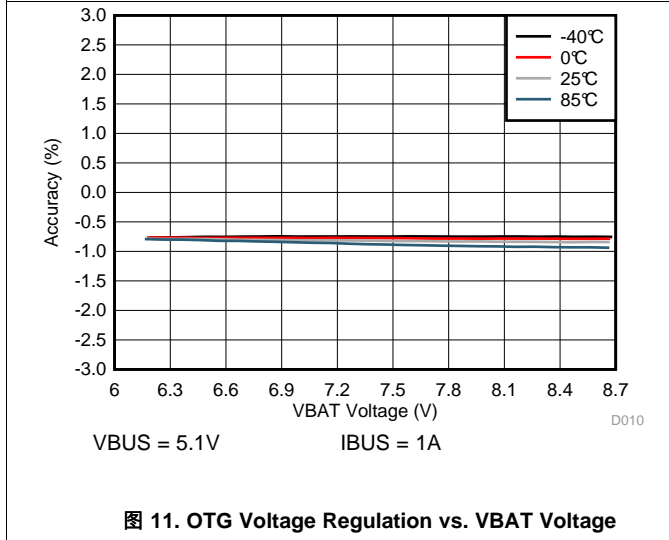
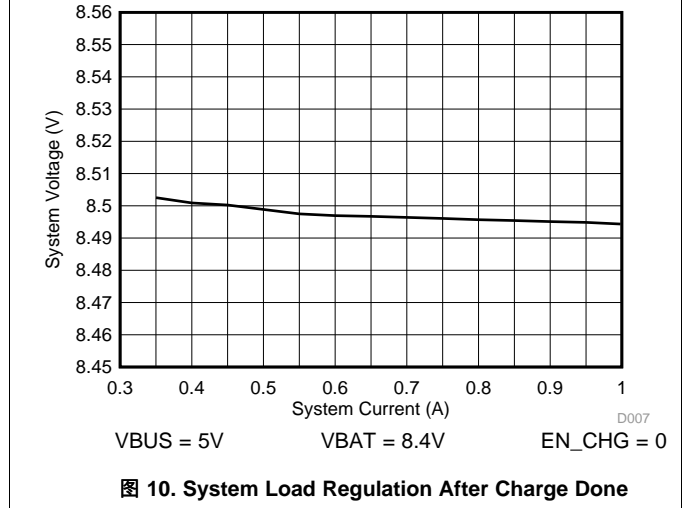
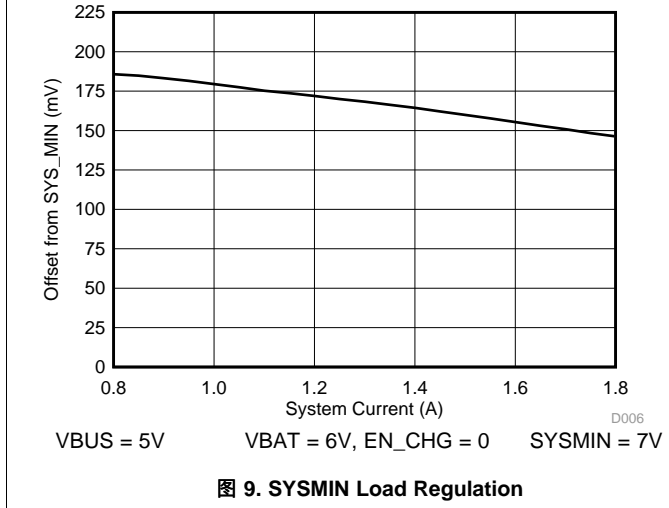
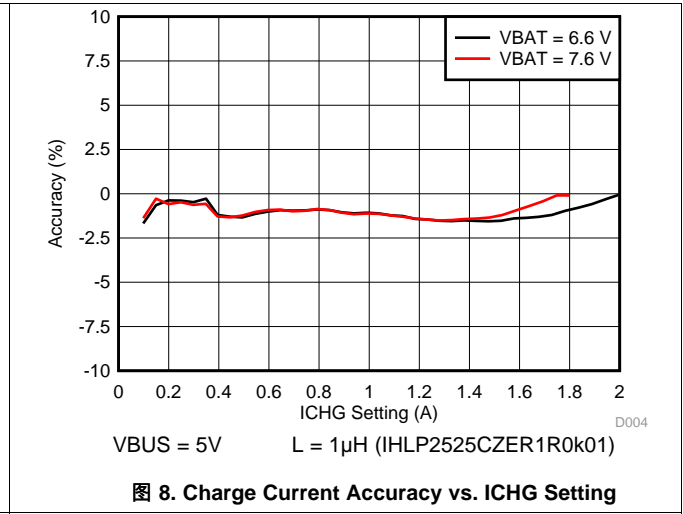
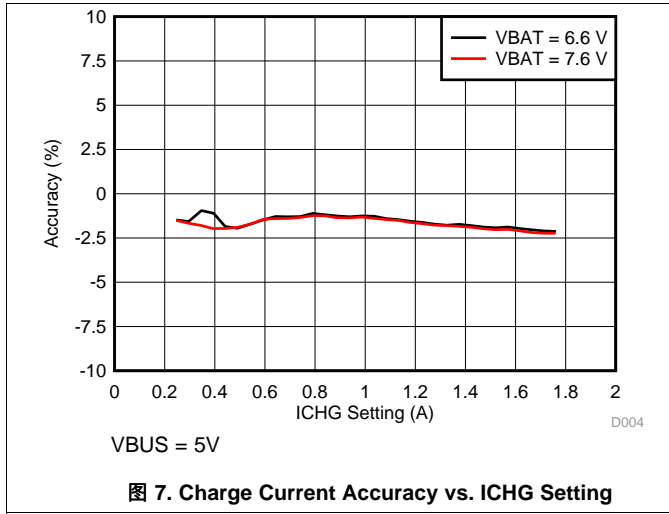
### 7.7 Typical Characteristics

$C_{VBUS} = 1\mu\text{F}$ ,  $C_{PMID} = 10\mu\text{F}$ ,  $C_{SYS} = 44\mu\text{F}$ ,  $C_{BAT} = 10\mu\text{F}$ ,  $L = 1\mu\text{H}$  (DFE252012F-1R0) (unless otherwise specified)



Typical Characteristics (接下页)

$C_{VBUS} = 1\mu F$ ,  $C_{PMID} = 10\mu F$ ,  $C_{SYS} = 44\mu F$ ,  $C_{BAT} = 10\mu F$ ,  $L = 1\mu H$  (DFE252012F-1R0) (unless otherwise specified)

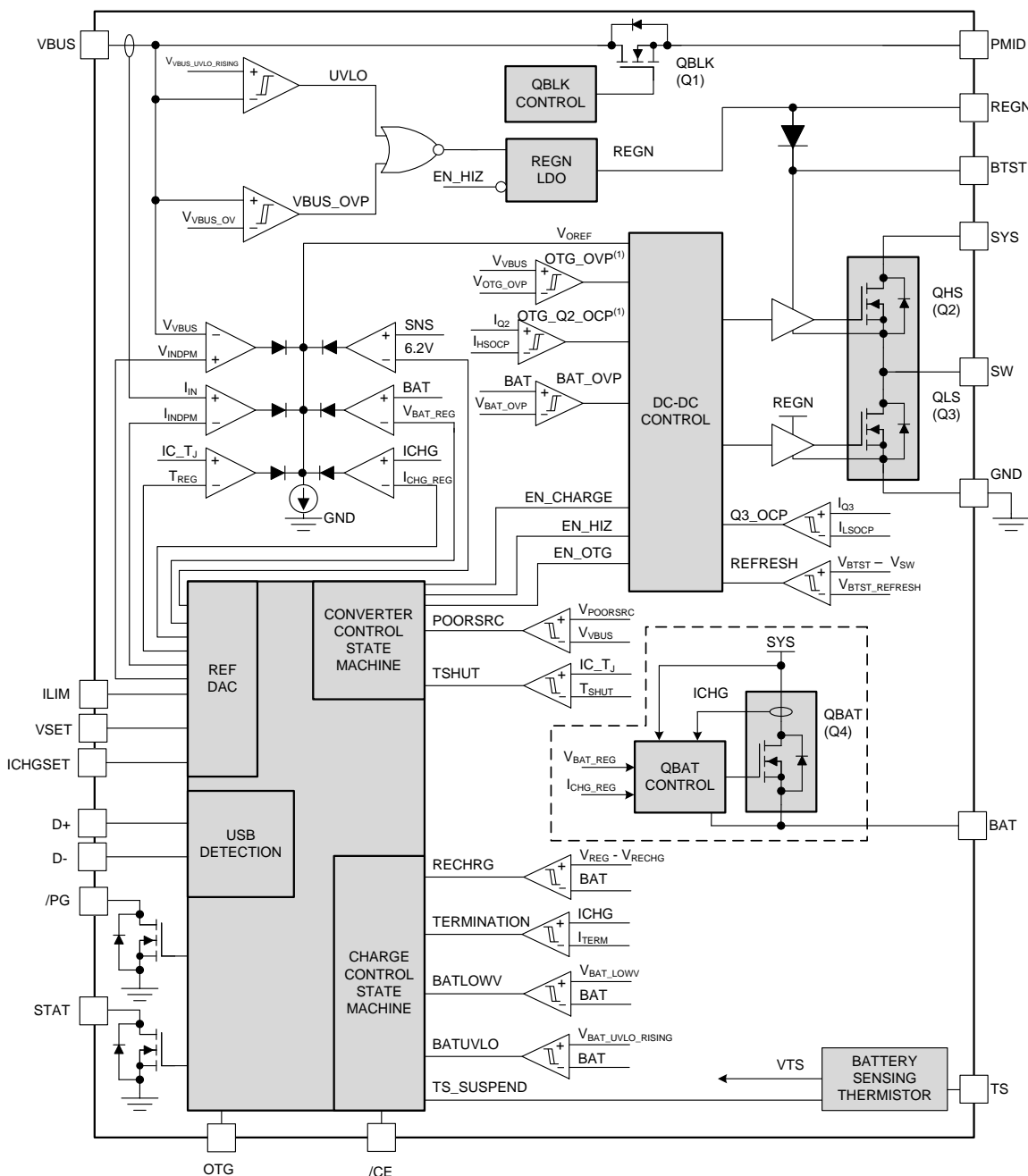


## 8 Detailed Description

### 8.1 Overview

The BQ25886 device is a highly integrated 2-A switch-mode battery charger for 2s Li-Ion and Li-polymer battery. It integrates the input blocking FET (Q1, QBLK), high-side switching FET (Q2, QHS), low-side switching FET (Q3, QLS), and battery FET (Q4, QBAT). The device also integrates the boot-strap diode for high-side gate drive.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Device Power-On-Reset

The internal bias circuits are powered from either VBAT or VBUS when it rises above  $V_{VBUS\_UVLO\_RISING}$  or  $V_{BAT\_UVLO\_RISING}$ . When VBUS rises above  $V_{VBUS\_UVLO\_RISING}$  or BAT rises above  $V_{BAT\_UVLO\_RISING}$ , the BATFET driver is active.

### 8.3.2 Device Power Up from Battery without Input Source

If only the battery is present and the voltage is above UVLO threshold ( $V_{BAT\_UVLO\_RISING}$ ), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low  $R_{DS(ON)}$  of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

### 8.3.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the boost converter is started. The power up sequence from input source is as listed:

1. Poor Source Qualification
2. Input Source Type Detection based on D+/D- to set default Input Current Limit (IINDPM) and input source type
3. Power Up REGN LDO
4. Converter Power-up

#### 8.3.3.1 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the boost converter.

1. VBUS voltage below  $V_{VBUS\_OVP}$
2. VBUS voltage above  $V_{POORSRC}$  when pulling  $I_{POORSRC}$  (typical 15mA)

If  $V_{VBUS\_OVP}$  is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (condition 2 above), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device goes to HIZ mode. The battery powers up the system when the device is in HIZ. On BQ25886, adapter re-plug-in is required to restart device operation. If the fault is not removed, the part will enter HIZ mode again after the 7 consecutive failures.

#### 8.3.3.2 Input Source Type Detection

After input source is qualified, the charger device runs input source type detection.

The BQ25886 sets input current limit through D+/D- pin. After input source type detection, /PG pin is pulled LOW. The charger input current is always limited by the lower of ILIM pin or input source detection (500mA or 900mA), Input Current Optimizer (ICO) setting if a DCP is detected.

##### 8.3.3.2.1 D+/D- Detection Sets Input Current Limit

The BQ25886 contains a D+/D- based input source detection to program the input current limit. The D+/D- detection has three major steps: Data Contact Detect (DCD), Primary Detection, and Secondary Detection.

Feature Description (接下页)

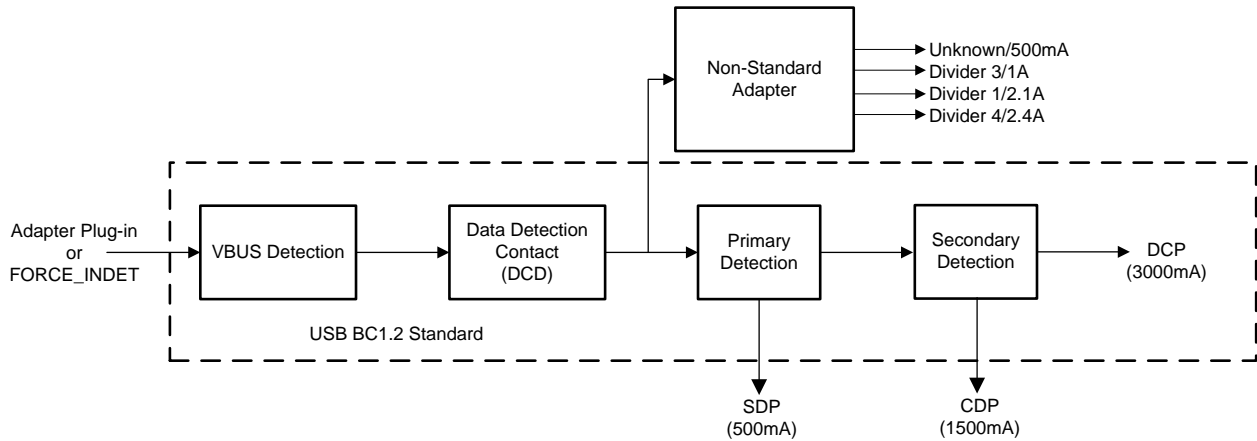


图 13. D+/D- Detection Flow

表 2. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D- THRESHOLD	INPUT CURRENT LIMIT
Divider 1	$V_{D+}$ within $V_{2P8\_VTH}$	$V_{D-}$ within $V_{2P0\_VTH}$	2.1 A
Divider 3	$V_{D+}$ within $V_{2P0\_VTH}$	$V_{D-}$ within $V_{2P8\_VTH}$	1 A
Divider 4	$V_{D+}$ within $V_{2P8\_VTH}$	$V_{D-}$ within $V_{2P8\_VTH}$	2.4 A

表 3. Input Current Limit Setting from D+/D- Detection

D+/D- DETECTION	INPUT CURRENT LIMIT (IINDPM)
USB SDP (USB500)	500 mA
USB CDP	1.5 A
USB DCP	3.0 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Unknown 5V Adapter	500 mA

8.3.3.3 Power Up REGN Regulator (LDO)

The REGN LDO supplies internal bias circuits as well as the QHS and QLS gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT and PG can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above  $V_{VBUS\_UVLO\_RISING}$  in boost mode or VBUS below  $V_{VBUS\_UVLO\_RISING}$  in buck mode
2. Poor Source Qualification detects a valid input source
3. Input Source Type Detection completes and sets appropriate input current limit
4. After 220-ms delay is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than  $I_{VBUS\_HIZ}$  from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

### 8.3.3.4 Converter Power Up

After the input current limit is set, the  $\overline{\text{PG}}$  pin is pulled LOW, and the converter is enabled, allowing the QHS and QLS to start switching. Before charging begins, the battery discharge source (IBAT\_DISCHG) is enabled automatically to detect the presence of battery. BATFET stays on to charge the battery. The device provides soft-start when system rail is ramped up.

As a battery charger, the device deploys a highly efficient 1.5-MHz boost switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device switches to PFM (Pulse Frequency Modulation) control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

### 8.3.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of a power source without staying in VINDPM to avoid input source overload.

On BQ25886, ICO starts automatically when DCP type of input source is detected. When other input source types are detected, ICO is disabled. The actual input current limit used by the Dynamic Power Management circuitry is limited by the lower value of current limit identified by the ICO algorithm or the current limit set by the ILIM pin. When the algorithm is enabled, it runs continuously to adjust input current limit of Dynamic Power Management (IINDPM) using ICO algorithm. When optimal input current is identified, the input current limit set by ICO will not be changed until the algorithm is forced to run by the following event:

1. A new input source is plugged-in
2. VINDPM is entered
3. VBUS\_OVP event

**表 4. Input Current Optimizer Automatic Operation**

DEVICE	INPUT SOURCE	INPUT CURRENT LIMIT (IINDPM)	AUTOMATIC START ICO ALGORITHM
BQ25886 (D+/D-)	USB SDP (USB500)	500 mA	Disable
	USB CDP	1.5 A	Disable
	USB DCP	3.0 A	Enable
	Divider 3	1 A	Disable
	Divider 1	2.1 A	Disable
	Divider 4	2.4 A	Disable
	Unknown 5V Adapter	500 mA	Disable

### 8.3.5 Buck Mode Operation from Battery (OTG)

The device supports buck converter operation to deliver power from the battery to other portable devices through USB port. The buck mode output current rating meets the USB On-The-Go 500-mA output requirement. The maximum output is 2.0 A. The buck operation is enabled when the following conditions are valid:

1. BAT above  $V_{\text{OTG\_BAT}}$
2. VBUS less than  $V_{\text{VBUS\_PRESENT}}$
3. Buck mode operation is enabled (OTG pin is pulled high)
4. Voltage at TS (thermistor) pin is within range BHOT and BCOLD
5. After 30-ms delay from buck mode enable



### 8.3.6 PowerPath Management

The device accommodates a wide range of input sources from USB, to wall adapter, to power bank. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

#### 8.3.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. Even with a fully depleted battery, the system is regulated above the minimum system voltage (fixed 6.2 V (typ)).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the the BATFET's drain to source voltage drop.

When the battery charging is disabled and VBAT is above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage.

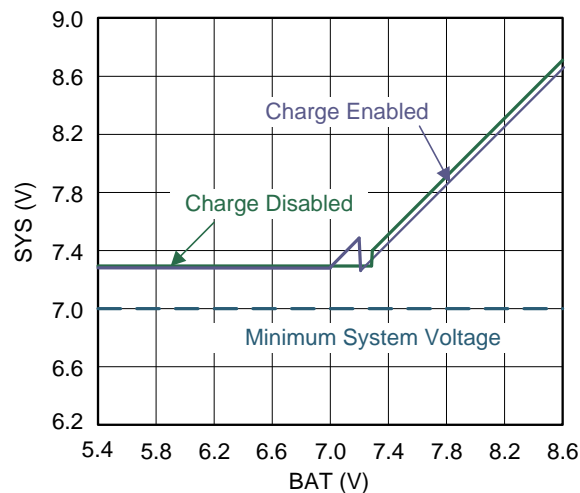


图 14. System Voltage vs. Battery Voltage

#### 8.3.6.2 Dynamic Power Management

To meet the maximum current limit in the USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. As the charger's system load plus charge current increases with constant input voltage, the charger's input current must increase. If this current exceeds the charger's preset input current limit or causes the input source voltage to droop near the input voltage limit (VINDPM fixed at 4.3 V typical), the device then reduces the charge current until the input current is regulated to the input current limit or the input voltage is regulated to the VINDPM threshold. Note that if the D+/D- algorithm detected a DCP port and VINDPM triggered, the ICO algorithm lowers the input current limit.

If the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the Supplement Mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

The figure shows the DPM response with 5-V/3-A adapter, 6.4-V battery, 1.5-A charge current and 6.8 V minimum system voltage setting.

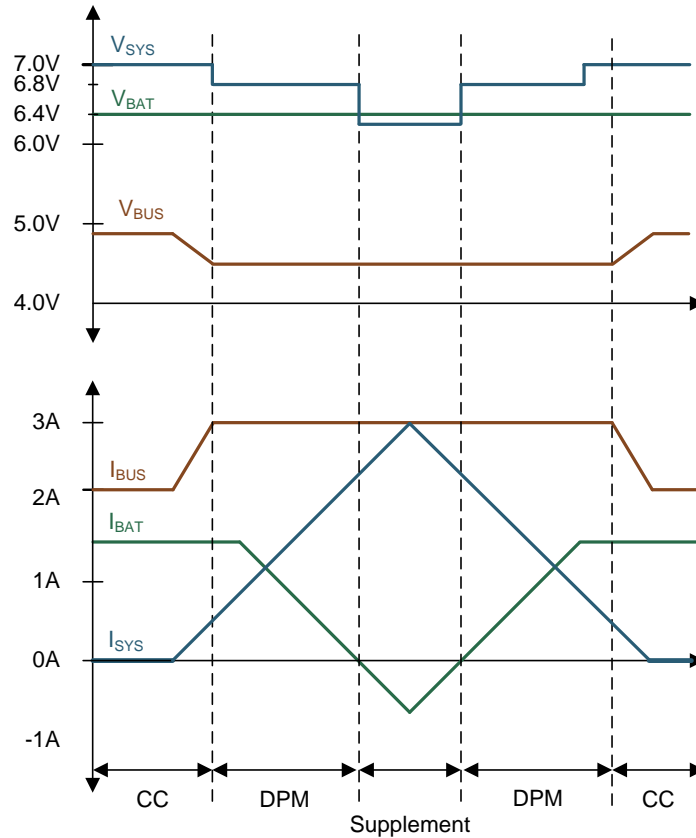


图 15. DPM Response

### 8.3.6.3 Supplement Mode

When the voltage falls below the battery voltage, the BATFET turns on.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce  $R_{DS(on)}$  until the BATFET is in full conduction. At this point onwards, the BATFET  $V_{DS}$  linearly increases with discharge current. The figure shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold ( $V_{BAT\_UVLO\_RISING}$ ).

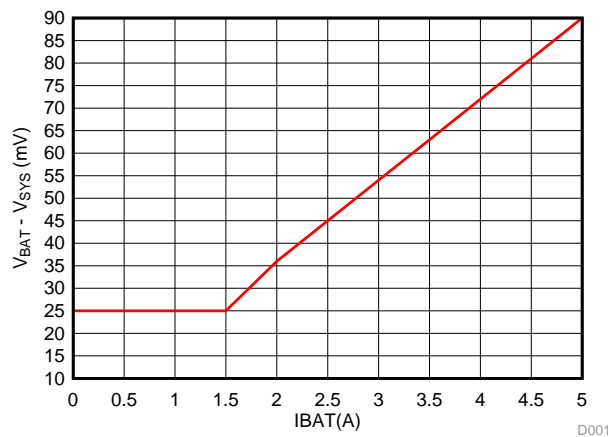


图 16. BATFET I-V Curve

### 8.3.7 Battery Charging Management

The BQ25886 charges 2-cell Li-Ion battery with up to 2.2-A charge current for high capacity battery. The low  $R_{DS(ON)}$  BATFET improves charging efficiency and minimize the voltage drop during discharging.

#### 8.3.7.1 Autonomous Charging Cycle

When battery charging is enabled ( $\overline{CE}$  pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in [表 5](#) below.

**表 5. Charging Parameter Default Settings**

DEFAULT MODE	BQ25886
Charging Voltage	Set by VSET
Charging Current	Set by ICHGSET
Pre-Charge Current	1/10 of ICHG
Termination Current	1/10 of ICHG
Temperature Profile	JEITA
Safety Timer	12 hours

A new charge cycle starts when the following conditions are valid:

1. Converter starts
2. No thermistor fault on TS
3. No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold fixed at 200 mV for BQ25886), the device automatically starts a new charging cycle. After the charge is done, toggle  $\overline{CE}$  pin can initiate a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). If no battery is connected, the STAT pin blinks as capacitance connected at BAT charges, discharges, then recharges.

#### 8.3.7.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off timer charging. At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in the [Charging Safety Timer](#) section.

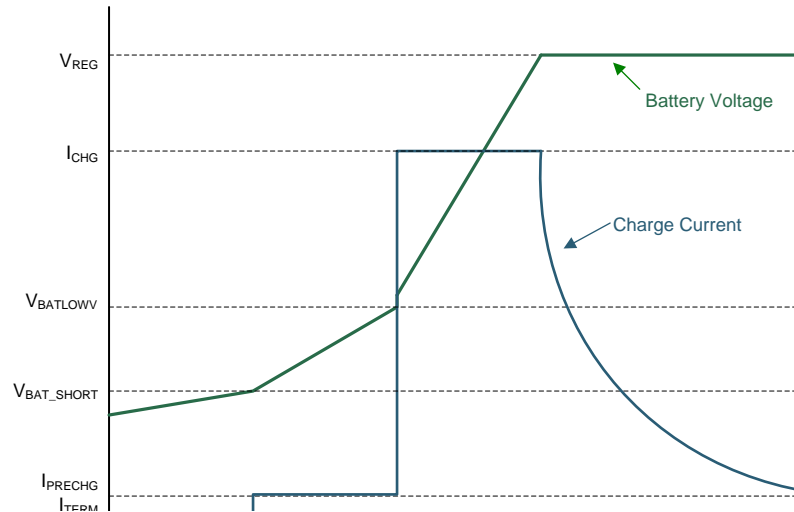


图 17. Battery Charging Profile

### 8.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the STAT pin goes HIGH. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. On the BQ25886, termination threshold is 1/10 of the fast charge current setting.

### 8.3.7.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

#### 8.3.7.4.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V / cell.

On the BQ25886, at cool temperature (T1-T2), the charge current is reduced to 20% of the fast charge current,  $I_{CHG}$ . At warm temperature (T3 - T5), the charge voltage is set to 8.0 V. Whenever the charger detects "warm" or "cool" temperature, termination is automatically disabled.

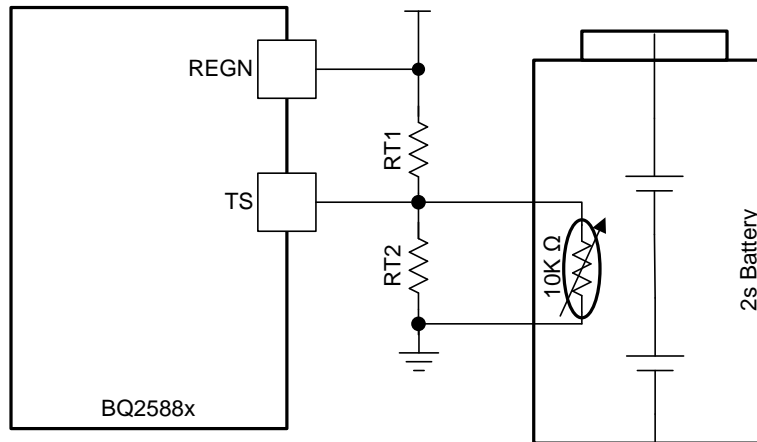


图 18. TS Resistor Network

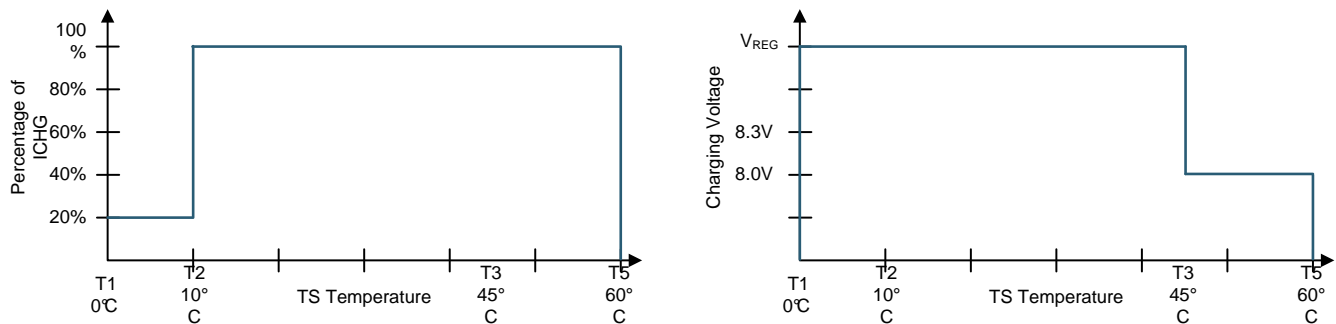


图 19. TS Charging Values

Assuming a 103AT NTC (Negative Temperature Coefficient) thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left( \frac{1}{V_{T5}} - \frac{1}{V_{T1}} \right)}{R_{NTC,T1} \times \left( \frac{1}{V_{T1}} - 1 \right) - R_{NTC,T5} \times \left( \frac{1}{V_{T5}} - 1 \right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

$$R_{NTC,T1} = 27.28 \text{ k}\Omega$$

$$R_{NTC,T5} = 3.02 \text{ k}\Omega$$

$$RT1 = 5.24 \text{ k}\Omega$$

$$RT2 = 30.31 \text{ k}\Omega$$

### 8.3.7.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the setting. For example, if the charger is in input current regulation throughout the whole charging cycle, and the safety timer is set to 12 hours, then the timer will expire in 24 hours.

During faults which disable charging, or supplement mode, timer is suspended. Once the fault goes away, safety timer resumes. If the charging cycle is stopped and started again, the timer gets reset.

The safety timer is reset for the following events:

1. Charging cycle stop and restart (toggle  $\overline{CE}$  pin, or charged battery falls below recharge threshold).
2. BAT voltage changes from pre-charge to fast-charge or vice versa.

The precharge safety timer (fixed 2hr counter that runs when  $V_{BAT} < V_{BAT\_LOWV}$ ), follows the same rules as the fast-charge safety timer in terms of getting suspended, reset, and counting at half-rate.

### 8.3.8 Status Outputs

#### 8.3.8.1 Power Good Indicator ( $\overline{PG}$ )

The open drain  $\overline{PG}$  pin goes low to indicate a good input source when:

1. VBUS above  $V_{VBUS\_UVLO\_RISING}$
2. VBUS below  $V_{VBUS\_OV}$  threshold
3. VBUS above  $V_{POORSRC}$  (typ. 3.7 V) when  $I_{POORSRC}$  (typ. 30 mA) current is applied (not a poor source)
4. Input Source Type Detection is completed

#### 8.3.8.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

表 6. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including trickle charge, pre-charge, fast-charge, recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault or battery over-voltage) OTG Buck Mode suspend (due to TS fault)	Blinking at 1Hz

### 8.3.9 Input Current Limit on ILIM Pin

For safe operation, the BQ2588x has an additional hardware pin on ILIM to limit maximum input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM pin setting and current limit set by D+/D- detection. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (refer to [Dynamic Power Management](#) section).

The ILIM pin can also be used to monitor input current. The voltage on ILIM pin is proportional to the input current. ILIM can be used to monitor input current with the following relationship:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (4)$$

For example, if ILIM pin is set with 820-Ω resistor, and the ILIM voltage 0.5V, the actual input current is 0.795 A to 0.973 A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V.

### 8.3.10 Voltage and Current Monitoring

The device closely monitors the input voltage, as well as internal FET currents for safe boost and buck mode operation.

### **8.3.10.1 Voltage and Current Monitoring in Boost Mode**

#### **8.3.10.1.1 Input Over-Voltage Protection**

The valid input voltage range for boost mode operation is  $V_{VBUS\_OP}$ . If VBUS voltage exceeds  $V_{VBUS\_OV}$ , the device stops switching immediately to protect the power FETs. The device automatically starts switching again when the over-voltage condition goes away.

#### **8.3.10.1.2 Input Under-Voltage Protection**

The valid input voltage range for boost mode operation is  $V_{VBUS\_OP}$ . If VBUS voltage falls below  $V_{POOR\_SRC}$  during operation, the device stops switching. The device automatically attempts to restart switching when the under-voltage condition goes away.

#### **8.3.10.1.3 System Over-Voltage Protection**

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above system regulation voltage. Upon SYSOVP, converter stops immediately to clamp the overshoot.

#### **8.3.10.1.4 System Over-Current Protection**

The charger device continually monitors and compares VBUS to VSYS to protect against a system short-circuit event. In the event that VSYS drops to within 250 mV of VBUS during operation, a short circuit event is flagged and the converter stops switching. The device attempts to recover from this condition automatically.

### **8.3.10.2 Voltage and Current Monitoring in OTG Buck Mode**

The device closely monitors the VBUS voltage, as well as RBFET (Q1, QBLK) and LSFET (Q3, QLS) current to ensure safe buck mode operation.

#### **8.3.10.2.1 VBUS Over-voltage Protection**

When the VBUS voltage rises above regulation target and exceeds  $V_{OTG\_OVP}$ , the device enters over-voltage protection which stops switching, and exits buck mode.

#### **8.3.10.2.2 VBUS Over-Current Protection**

The device monitors output current to provide output short protection. The OTG buck mode has built-in constant current regulation to allow OTG to adapt to various types of loads. If short circuit is detected on VBUS, the OTG turns off and retries 7 times. If the retries are not successful, OTG is disabled.

### **8.3.11 Thermal Regulation and Thermal Shutdown**

#### **8.3.11.1 Thermal Protection in Boost Mode**

The device monitors internal junction temperature,  $T_J$ , to avoid overheating and limits the IC surface temperature in boost mode. When the internal junction temperature exceeds the thermal regulation limit (120°C), the device reduces charge current.

During thermal regulation, the actual charging current is usually below the programmed value. Therefore, termination is disabled, and the safety timer runs at half the clock rate.

Additionally, the device has thermal shutdown to turn off the converter when IC surface temperature exceeds  $T_{SHUT}$ . The converter turns back on when IC temperature is below  $T_{SHUT\_HYS}$ .

#### **8.3.11.2 Thermal Protection in OTG Buck Mode**

The BQ2588x monitors the internal junction temperature to provide thermal shutdown during OTG buck mode.

### **8.3.12 Battery Protection**

#### **8.3.12.1 Battery Over-Voltage Protection (BATOVP)**

The battery over-voltage limit is clamped at 4% above the battery regulation voltage while charging. When battery over-voltage occurs, the charger device immediately disables charge.

## 8.4 Device Functional Modes

The BQ25886 is a standalone device and therefore does not include any functional modes for I<sup>2</sup>C operations.





## Typical Application (接下页)

### 9.2.1 Design Requirements

For this design example, use the parameters shown in 表 7 below.

表 7. Design Parameters

PARAMETER	VALUE
VBUS voltage range	4.3 V to 6.2 V
Input current limit (ILIM)	2.4 A
Fast charge current limit (ICHGSET)	1.5 A
Minimum System Voltage	6.2 V
Battery Regulation Voltage (VSET)	8.4 V

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Inductor Selection

The device has 1.5-MHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current should be higher than the input current ( $I_{IN}$ ) plus half the ripple current ( $I_{RIPPLE}$ ):

$$I_{SAT} \geq I_{IN} + \frac{I_{RIPPLE}}{2} \quad (5)$$

The inductor ripple current ( $I_{RIPPLE}$ ) depends on input voltage ( $V_{VBUS}$ ), duty cycle ( $D = V_{BAT}/V_{BUS}$ ), switching frequency ( $f_{SW}$ ) and inductance ( $L$ ):

$$I_{RIPPLE} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times f_{SW} \times L} \quad (6)$$

The maximum inductor ripple current happens in the vicinity of  $D = 0.5$ . Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

#### 9.2.2.2 Input (VBUS / PMID) Capacitor

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current occurs when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current  $I_{PMID}$  occurs where the duty cycle is closest to 50% and can be estimated by

$$I_{PMID} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (7)$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for up to 5-V input voltage. A minimum 10- $\mu$ F capacitor is suggested for up to 3.3-A input current. Keep in mind, long impedance cable would cause significant voltage drop with higher inrush current. For optimal performance, 44- $\mu$ F cap on PMID is recommended. In addition, a minimum 1- $\mu$ F capacitor is suggested at VBUS pin.

#### 9.2.2.3 Output (VSYS) Capacitor

The SYS capacitor is the boost converter output capacitor and should also have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current  $I_{COUT}$  is given:

$$I_{CSYS, rms} = I_{OUT} \times \sqrt{\frac{D}{1-D}} \quad (8)$$

The output capacitor voltage ripple is a function of the boost output current ( $I_{OUT}$ ), and can be calculated as follows:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{SYS}} \quad (9)$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for SYS decoupling capacitor and should be placed close to the SYS and GND pins of the IC. Voltage rating of the capacitor must be higher than normal output voltage level. 16-V rating or higher capacitor is preferred. Minimum 44- $\mu$ F capacitor is suggested for up to 2.2-A boost converter output current.

#### 9.2.2.4 ILIM resistor

The ILIM resistor sets the maximum input current limit and can be used to monitor input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (10)$$

Using maximum input current limit 900mA as an example. The KLIM is 1110. If the maximum input current limit cannot exceed 900mA, then IINMAX used in the calculation should be 819.9mA as regulation accuracy at 900mA (typ) setting is around +/-8.9%. Resistor accuracy should also be taken into consideration when setting input current limit. When ILIM pin is short to GND, the input current limit is set to maximum by ILIM. Input current limit less than 500mA is not supported on ILIM pin. Do not float this pin.

#### 9.2.2.5 ICHGSET resistor

A resistor from ICHGSET to GND is used to program the charge current. Pre-charge and termination current is 1/10 of the fast charge current. The minimum pre-charge current is clamped at 30mA (typ). Minimum termination current is clamped at 10mA (typ). ICHGSET short to GND clamps charge current to minimum setting 30mA (typ). Floating ICHGSET disables charge. RICHGSET can be calculated as:

$$I_{CHGSET} = \frac{R_{ICHGSET}}{K_{ICHGSET}} \quad (11)$$

### 9.2.3 Application Curves

$C_{VBUS} = 1 \mu\text{F}$ ,  $C_{PMID} = 10 \mu\text{F}$ ,  $C_{BAT} = 10 \mu\text{F}$ ,  $C_{SYS} = 44 \mu\text{F}$ ,  $L = \text{DFE252012F-1R0}$  ( $1 \mu\text{H}$ ) (unless otherwise specified)

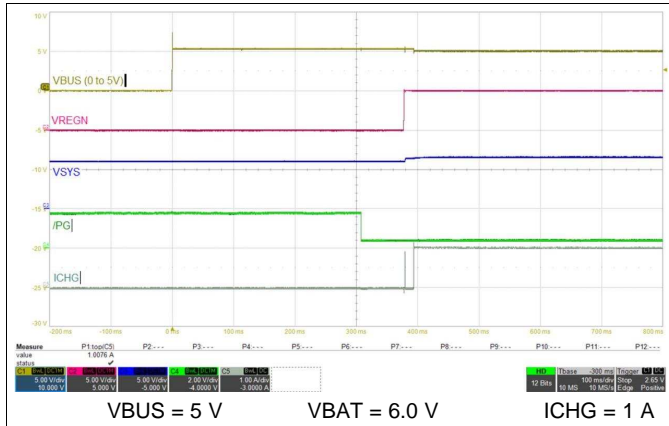


图 21. Adapter Power Up with Charge Enabled

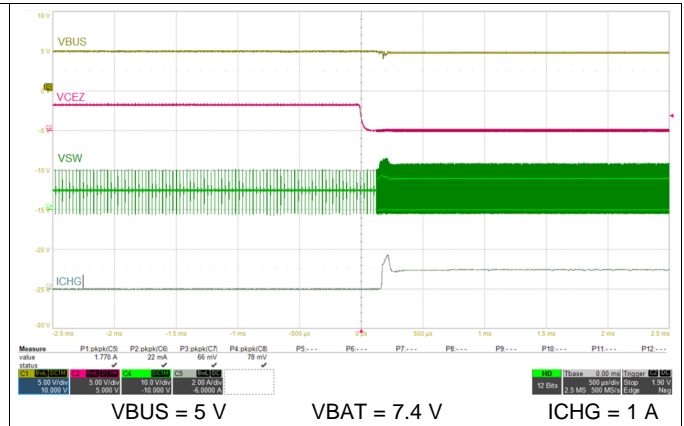


图 22. Charge Enable

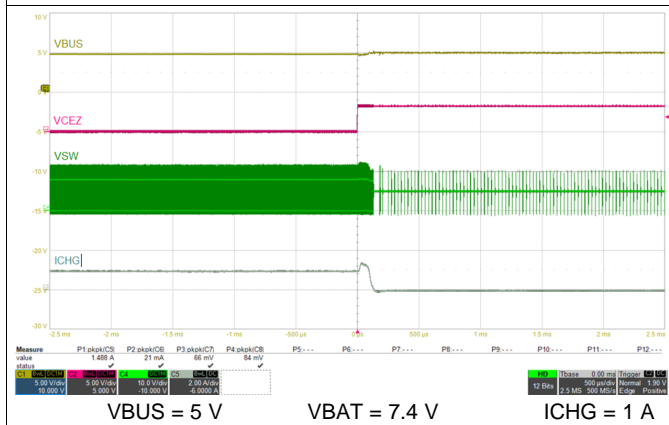


图 23. Charge Disabled

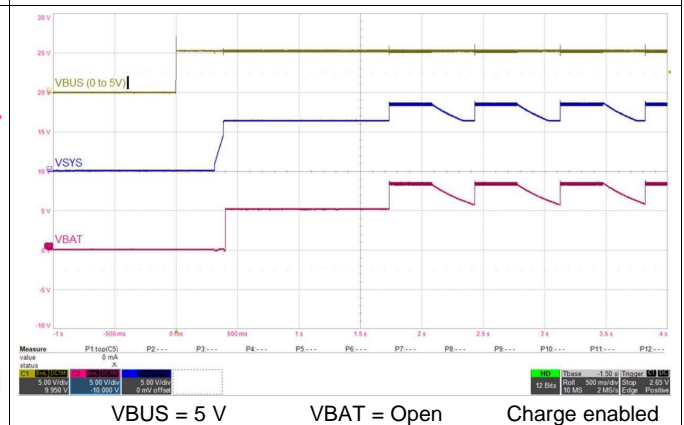


图 24. Adapter Plug-in with No Battery

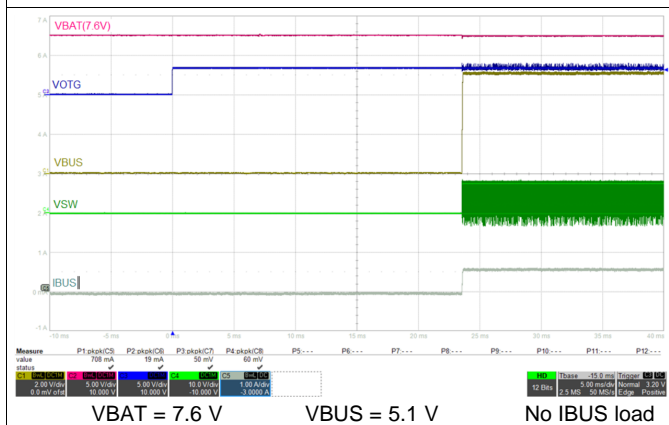


图 25. Buck Mode (OTG) Startup

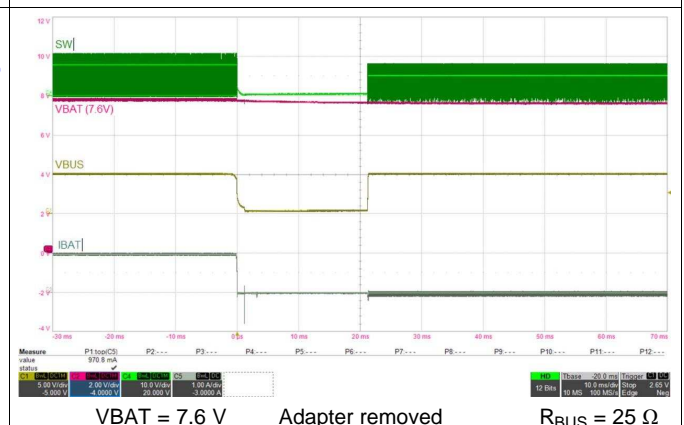


图 26. Buck Mode Startup After Adapter Removal

$C_{VBUS} = 1 \mu\text{F}$ ,  $C_{PMID} = 10 \mu\text{F}$ ,  $C_{BAT} = 10 \mu\text{F}$ ,  $C_{SYS} = 44 \mu\text{F}$ ,  $L = \text{DFE252012F-1R0}$  (1  $\mu\text{H}$ ) (unless otherwise specified)

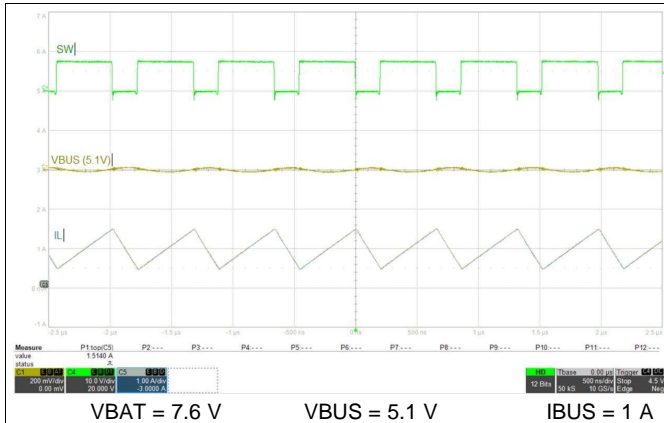


图 27. Buck Mode (OTG) PWM Switching

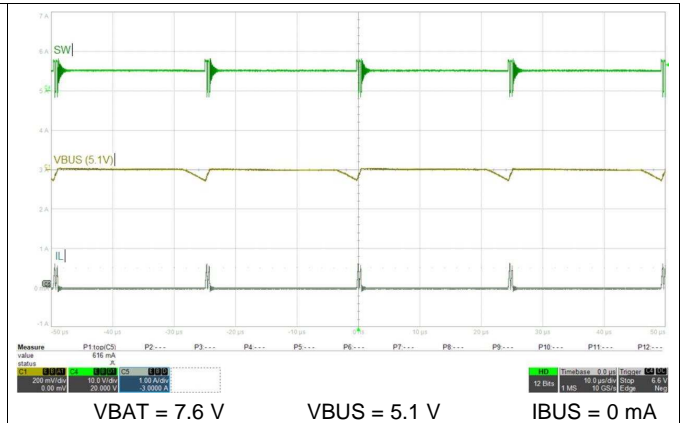


图 28. Buck Mode (OTG) PFM Switching

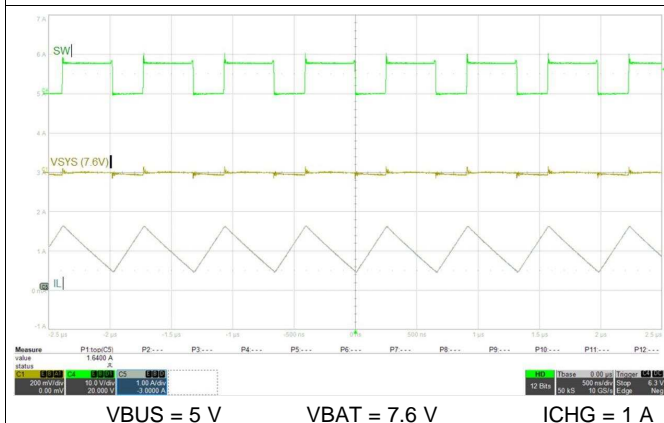


图 29. Boost Mode PWM Switching

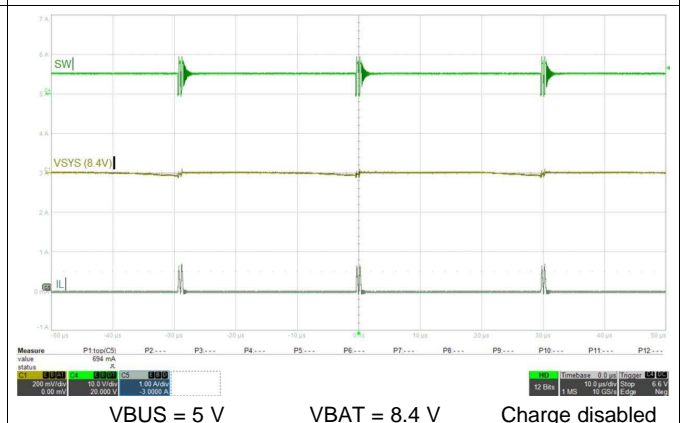


图 30. Boost Mode PFM Switching

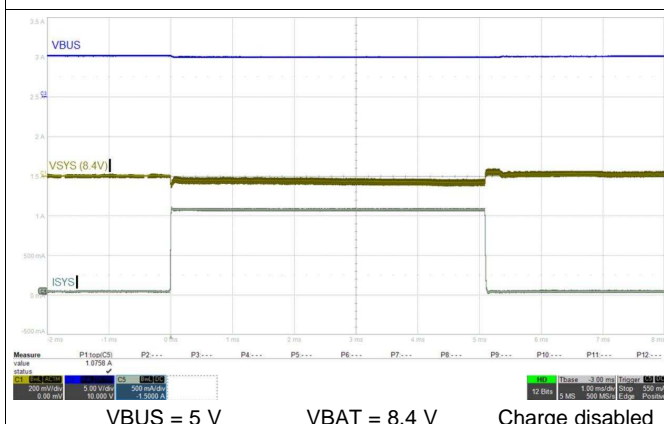


图 31. System Load Transient Response

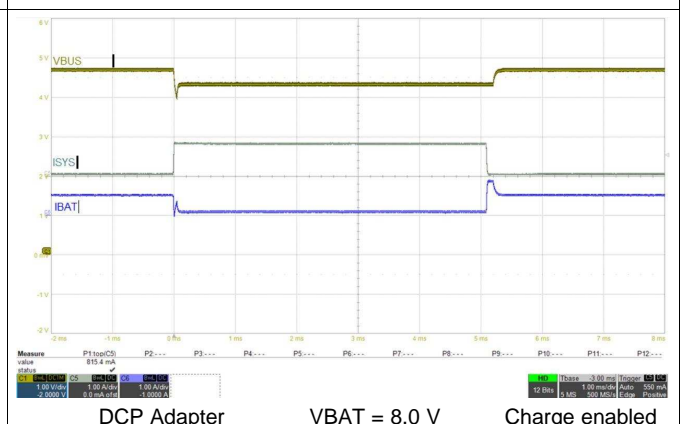
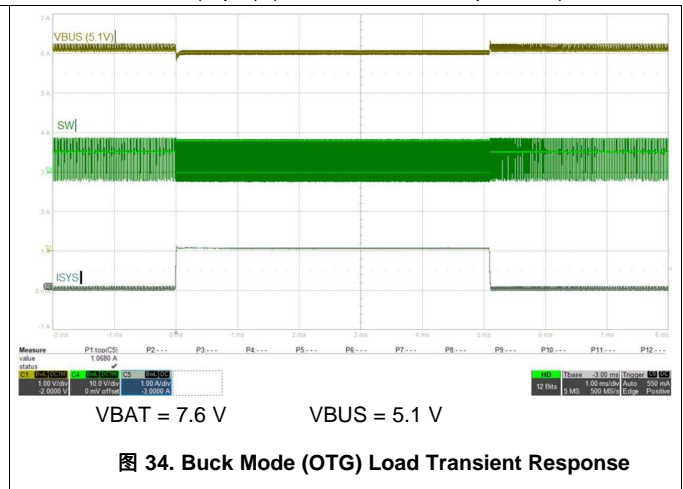
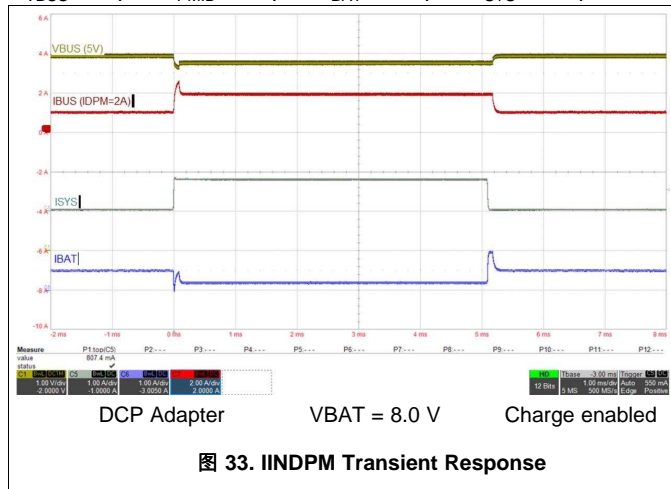


图 32. VINDPM Transient Response

$C_{VBUS} = 1 \mu\text{F}$ ,  $C_{PMID} = 10 \mu\text{F}$ ,  $C_{BAT} = 10 \mu\text{F}$ ,  $C_{SYS} = 44 \mu\text{F}$ ,  $L = \text{DFE252012F-1R0}$  (1  $\mu\text{H}$ ) (unless otherwise specified)



## 10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9-V and 6.2-V input with at least 500-mA current rating connected to VBUS or a 2-cell Li-Ion battery with voltage > VBAT\_UVLO connected to BAT. The source current rating needs to be at least 3-A in order for the boost converter of the charger to provide maximum output power to SYS.

## 11 Layout

### 11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Put SYS output capacitor as close to SYS and GND pins as possible. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place PMID input capacitor as close as possible to PMID pins and PGND pins and use shortest copper trace connection or GND plane.
3. Place inductor input terminal to SW pins as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the input current. Minimize parasitic capacitance from this area to any other trace or plane.
4. Decoupling capacitors should be placed on the same side of and next to the IC and make trace connection as short as possible.
5. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0- $\Omega$  resistor to tie analog ground to power ground.
6. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
7. Via size and number should be enough for a given current path.

Refer to the EVM design and the [Layout Example](#) below for the recommended component placement with trace and via locations.







## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 第三方产品免责声明

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### 12.2 文档支持

#### 12.2.1 相关文档

请参阅如下相关文档：

- [《BQ2588x 升压电池充电器评估模块用户指南》](#)

### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.7 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

### 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25886RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886	<a href="#">Samples</a>
BQ25886RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25886RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25886RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25886RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ25886RGET	VQFN	RGE	24	250	210.0	185.0	35.0

## GENERIC PACKAGE VIEW

RGE 24

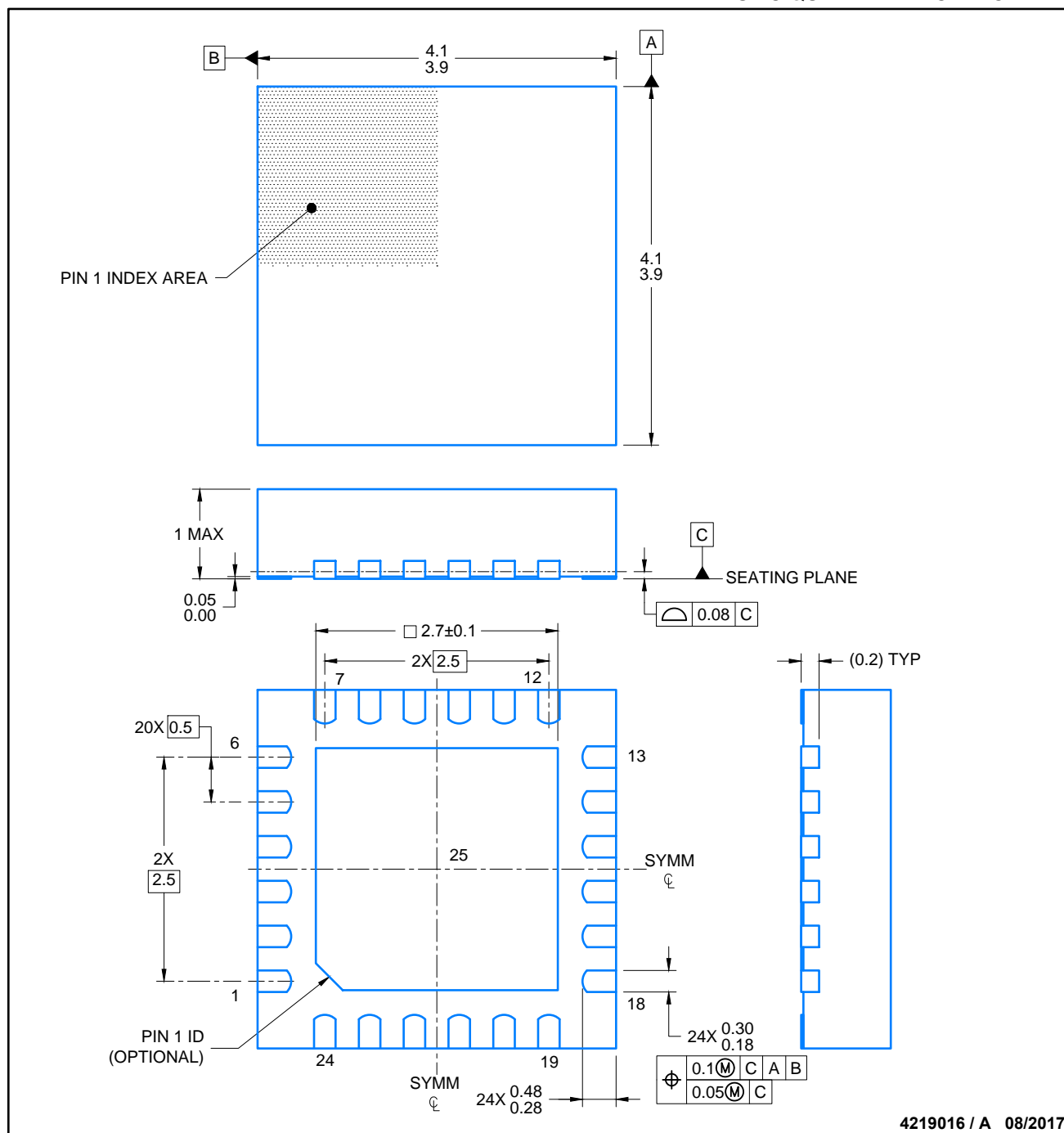
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

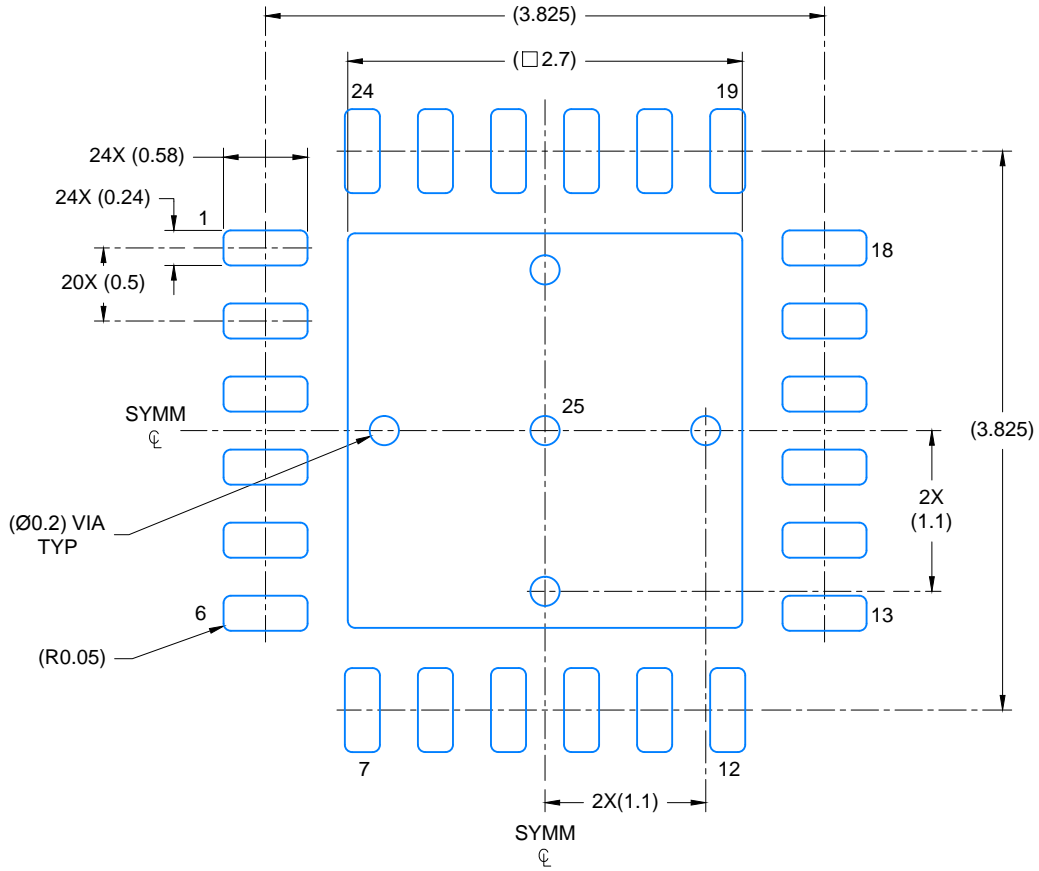
4204104/H



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.





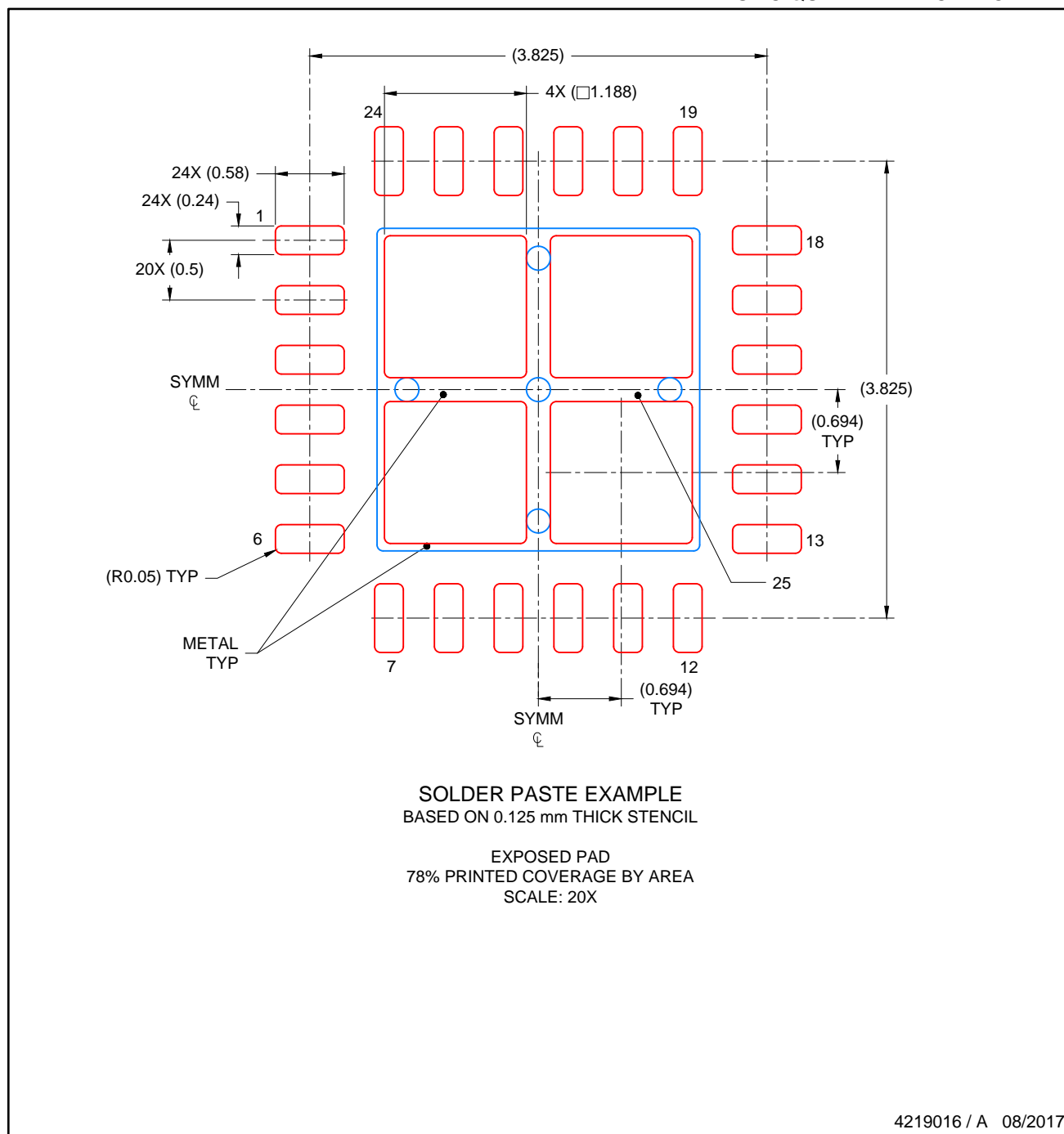
LAND PATTERN EXAMPLE  
SCALE: 20X



4219016 / A 08/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

## 重要声明和免责声明

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