CDx4HC243、CDx4HCT243 具有三态输出的高速 CMOS 逻辑四路总线收发器

1 特性

- 当 V_{CC} = 5V、C_L = 15pF、T_A = 25ºC 时，传播延迟典型值（A 到 B，B 到 A）为 7ns
- 三态输出
- 缓冲输入
- 扇出（在温度范围内）
  - 标准输出：10 个 LSTTL 负载
  - 总线驱动器输出：15 个 LSTTL 负载
- 宽工作温度范围：-55ºC 至 125ºC
- 平衡的传播延迟及转换时间
- 与 LSTTL 逻辑 IC 相比，功耗显著降低
- HC 类型
  - 2 V 至 6 V 工作电压
  - 高抗噪性：当 V_{CC} = 5V 时，N_{IL} = 30%，N_{IH} = V_{CC} 的 30%
- HCT 类型
  - 工作电压为 4.5 V 至 5.5 V
  - 直接 LSTTL 输入逻辑兼容性，V_{IL} = 0.8V（最大值），V_{IH} = 2V（最小值）
  - CMOS 输入兼容性，当电压为 V_{OL}、V_{OH} 时，I_I ≤ 1µA

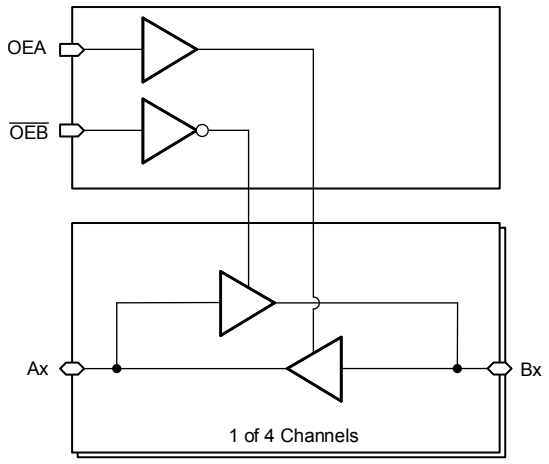
2 说明

CDx4HC243 和 CDx4HCT243 是具有三态输出的四路总线收发器。OEA 和 $\overline{OEB}$ 输入可通过器件来控制高阻抗状态和通信方向。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
CD54HC243F	CDIP (14)	19.55mm × 6.71mm
CD74HC243E	PDIP (14)	19.31mm × 6.35mm
CD74HC243M	SOIC (14)	8.65mm × 3.90mm
CD74HCT243E	PDIP (14)	19.31mm × 6.35mm
CD74HCT243M	SOIC (14)	8.65mm × 3.90mm

(1) 如需了解所有封装，请参阅数据表末尾的可订购产品附录。



功能方框图

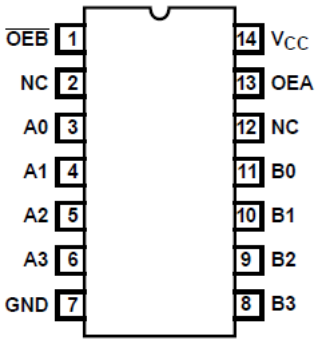
Table of Contents

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (October 2003) to Revision E (March 2022)	Page
• 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映现代数据表标准	1

4 Pin Configuration and Functions



J, N, or D Package
14-Pin CDIP, PDIP, or SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_{OK}	Output diode current	For V_C < -0.5V or V_O > V_{CC} + 0.5V		±20	mA
I_O	Drian Current, per output	For -0.5V < V_O < V_{CC} + 0.5V		±35	mA
I_O	Output source or sink current per output pin	For V_O > -0.5V or V_O < V_{CC} + 0.5V		±25	mA
	Continuous current through V_{CC} or GND			±70	mA
T_{stg}	Storage temperature range		-65	150	°C
T_J	Junction temperature			150	°C
	Lead temperature (Soldering 10s)(SOIC - Lead Tips Only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input rise and fall time	V_{CC} = 2V		1000	ns
		V_{CC} = 4.5V		500	
		V_{CC} = 6V		400	
T_A	Temperature Range		-55	125	°C

5.3 Thermal Information

THERMAL METRIC		N (PDIP) 14 PINS	D (SOIC) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	80	86	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS[1]	V_{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High-level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V_{IL}	Low-level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	
			6			1.8		1.8		1.8	
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		
		I_{OH} = – 7.8mA	6	5.48			5.34		5.2		
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	
		I_{OL} = 20 μA	6			0.1		0.1		0.1	
	Low-level output voltage TTL	I_{OL} = 6mA	4.5			0.26		0.33		0.4	
		I_{OL} = 7.8mA	6			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply Current	V_{CC} or GND	6			8		80		160	μA
I_{OZ}	Three-state leakage current	V_{IL} or V_{IH}	6			±0.5		±0.5		±10	μA
HCT TYPES											
V_{IH}	High-level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low-level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High-level output voltage CMOS loads	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High-level output voltage TTL loads	I_{OH} = – 6mA	4.5	3.98			3.84		3.7		
V_{OL}	Low-level output voltage CMOS loads	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low-level output voltage TTL loads	I_{OL} = 6mA	4.5			0.26		0.33		0.4	
I_I	Input leakage current	V_{CC} to GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_{CC} or GND	5.5			8		80		160	μA
ΔI_{CC} [2] [3]	Additional supply current per input pin	One of An or Bn	4.5 to 5.5		100	396		495		539	μA
		One of OEA or $\overline{OEB}$	4.5 to 5.5		100	216		270		294	
I_{OZ}	Three-state leakage current	V_{IL} or V_{IH}	5.5			±0.5		±5		±10	μA

(1) V_I = V_{IH} or V_{IL}, unless otherwise noted.
(2) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(3) Inputs held at V_{CC} – 2.1.

5.5 Switching Characteristics

Input t_t = 6ns. Unless otherwise specified, C_L = 50pF

PARAMETER		V_{CC} (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	Propagation delay data to outputs	2		90	115	135	ns
		4.5	7(1)	18	23	27	
		6		15	20	23	
t_{PZL}, t_{PZH}	Output high-Z, to high level to low level	2		150	190	225	ns
		4.5	12(1)	30	38	45	
		6		26	33	38	
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	2		150	190	225	ns
		4.5	12(1)	30	38	45	
		6		26	33	38	
t_t	Output transition times	2		60	75	90	ns
		4.5		12	15	18	
		6		10	13	15	
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} (2) (3)	Power dissipation capacitance	5	80				pF
HCT TYPES							
t_{pd}	Propagation delay data to outputs	4.5	9(1)	22	28	33	ns
t_{PZH}, t_{PLZ}	Output high-Z to high level to low level	4.5	14(1)	34	43	51	ns
t_{PHZ}, t_{PLZ}	Output high level, output low level to high-Z	4.5	14(1)	35	44	53	ns
t_t	Output transition times	4.5		12	15	18	ns
C_i	Input capacitance			10	10	10	pF
C_O	Three-state output capacitance			20	20	20	pF
C_{pd} (2) (3)	Power dissipation capacitance	5	91				pF

(1) Typical value tested at 5V, C_L = 15pF.
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}{}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

6 Parameter Measurement Information

t_{PD} is the maximum between t_{PLH} and t_{PHL}

t_t is the maximum between t_{TLH} and t_{THL}

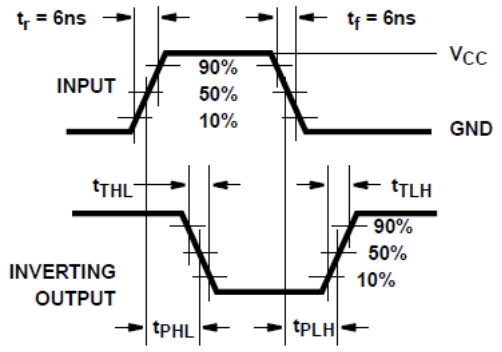


图 6-1. HC and HCT transition times and propagation delay times, combination logic

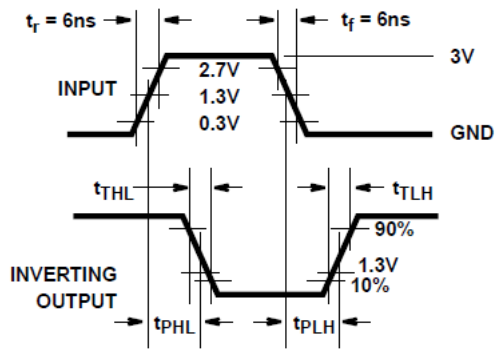


图 6-2. HCT transition times and tpopationg delay times, combination logic

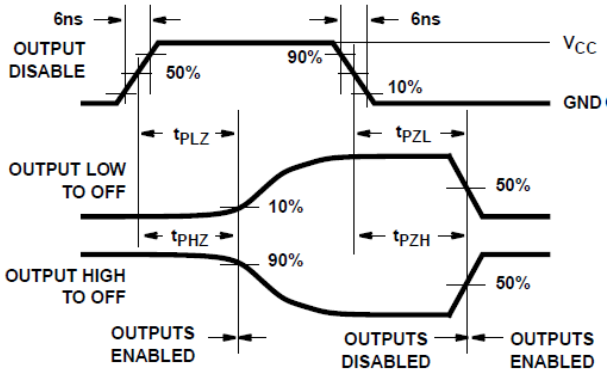


图 6-3. HC three-state propagation delay waveform

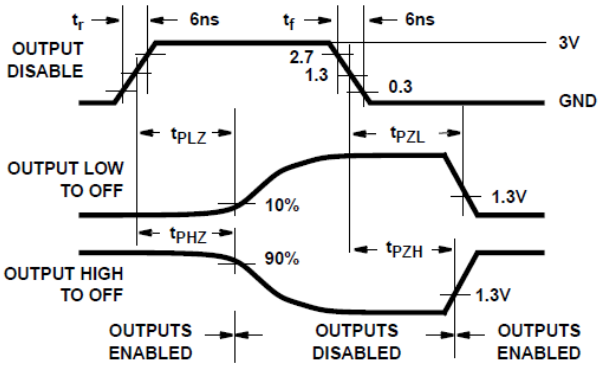
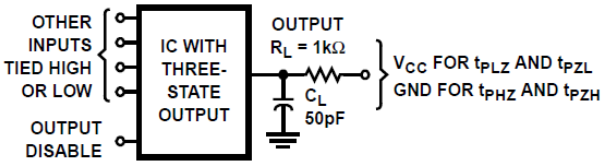


图 6-4. HCT three-state propagation delay waveform



NOTE: Open drain waveforms t_{PLZ} and t_{PZL} are the same as those for three-state shown on the left. The test circuit is Output R_L = 1kΩ to V_{CC}, C_L = 50pF.

图 6-5. HC and HCT three-state propagation delay test circuit

7 Detailed Description

7.1 Overview

The CDx4HC243 and CDx4HCT243 silicon-gate CMOS three-state bidirectional noninverting buffers are intended for two-way asynchronous communication between data buses. They have high-drive-current outputs that enable high-speed operation when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuits and have speeds comparable to low-power Schottky TTL circuits. They can drive 15 LSTTL loads.

The states of the output-enable ($\overline{OEB}$, OEA) inputs determine both the direction of flow (A to B, B to A), and the three-state mode.

7.2 Functional Block Diagram

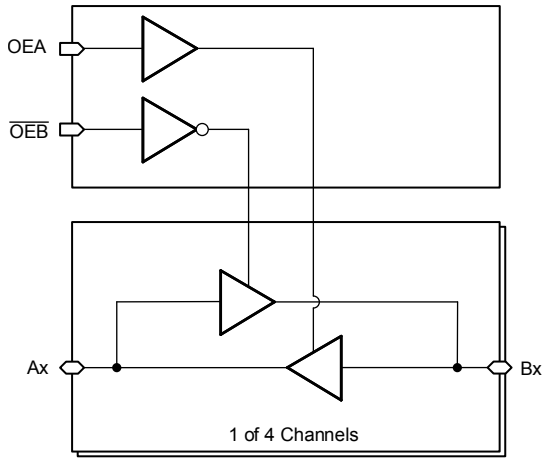


图 7-1. Functional Diagram

7.3 Device Functional Modes

表 7-1. Truth Table[1][2]

Control Inputs		HC, HCT243 Series	
		Data port status	
$\overline{OEB}$	OEA	An	Bn
H	H	O	I
L	H	Z	Z
H	L	Z	Z
L	L	I	O

(1) H = High voltage level. L = Low voltage level. I = Input. O = Output (Same level as input). Z = High Impedance

(2) To prevent excess currents in the High Z modes all I/O terminals hsould be terminated with 10kΩ to 1MΩ resistors.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8409001CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A	Samples
CD54HC243F	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HC243F	Samples
CD54HC243F3A	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8409001CA CD54HC243F3A	Samples
CD74HC243E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC243E	Samples
CD74HC243EE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC243E	Samples
CD74HC243M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC243M	Samples
CD74HCT243E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT243E	Samples
CD74HCT243M	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT243M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD54HC243, CD74HC243 :

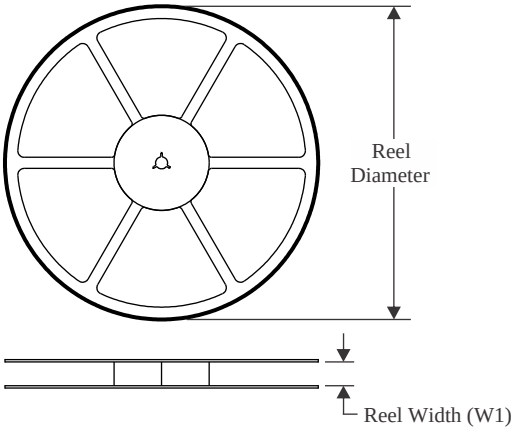
- Catalog : CD74HC243
- Military : CD54HC243

NOTE: Qualified Version Definitions:

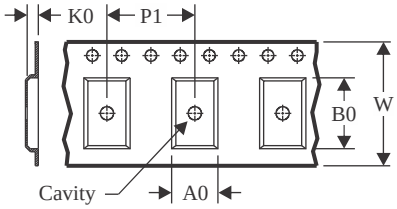
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

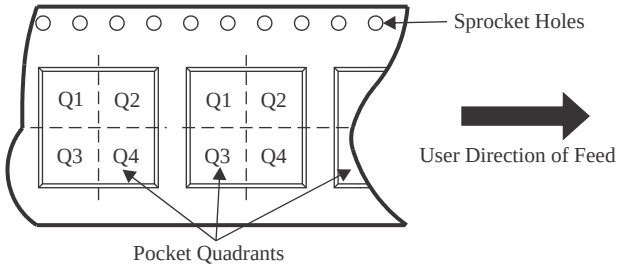


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

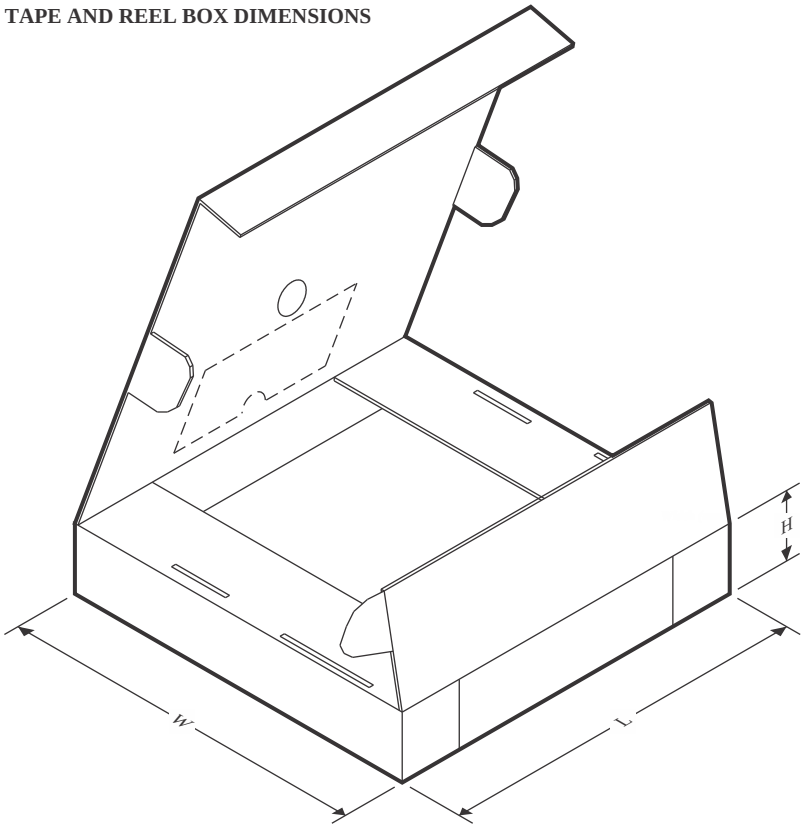
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC243M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

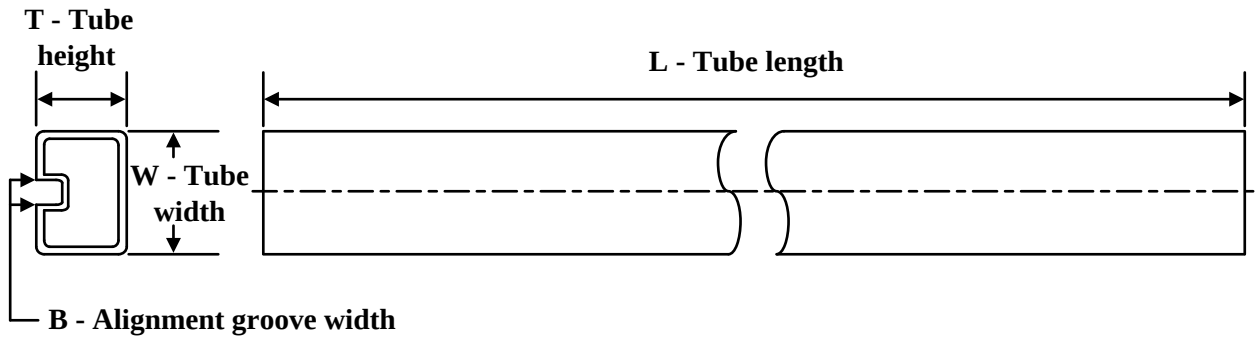
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC243M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC243M96	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



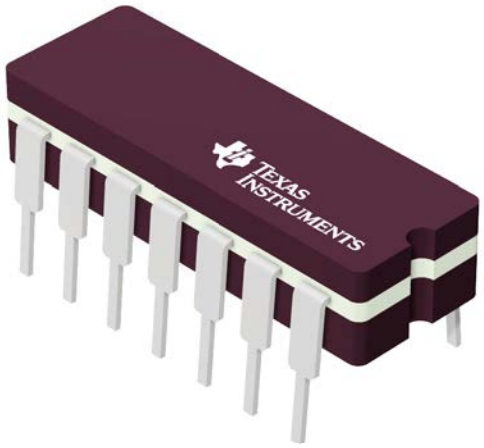
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC243EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT243M	D	SOIC	14	50	506.6	8	3940	4.32

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

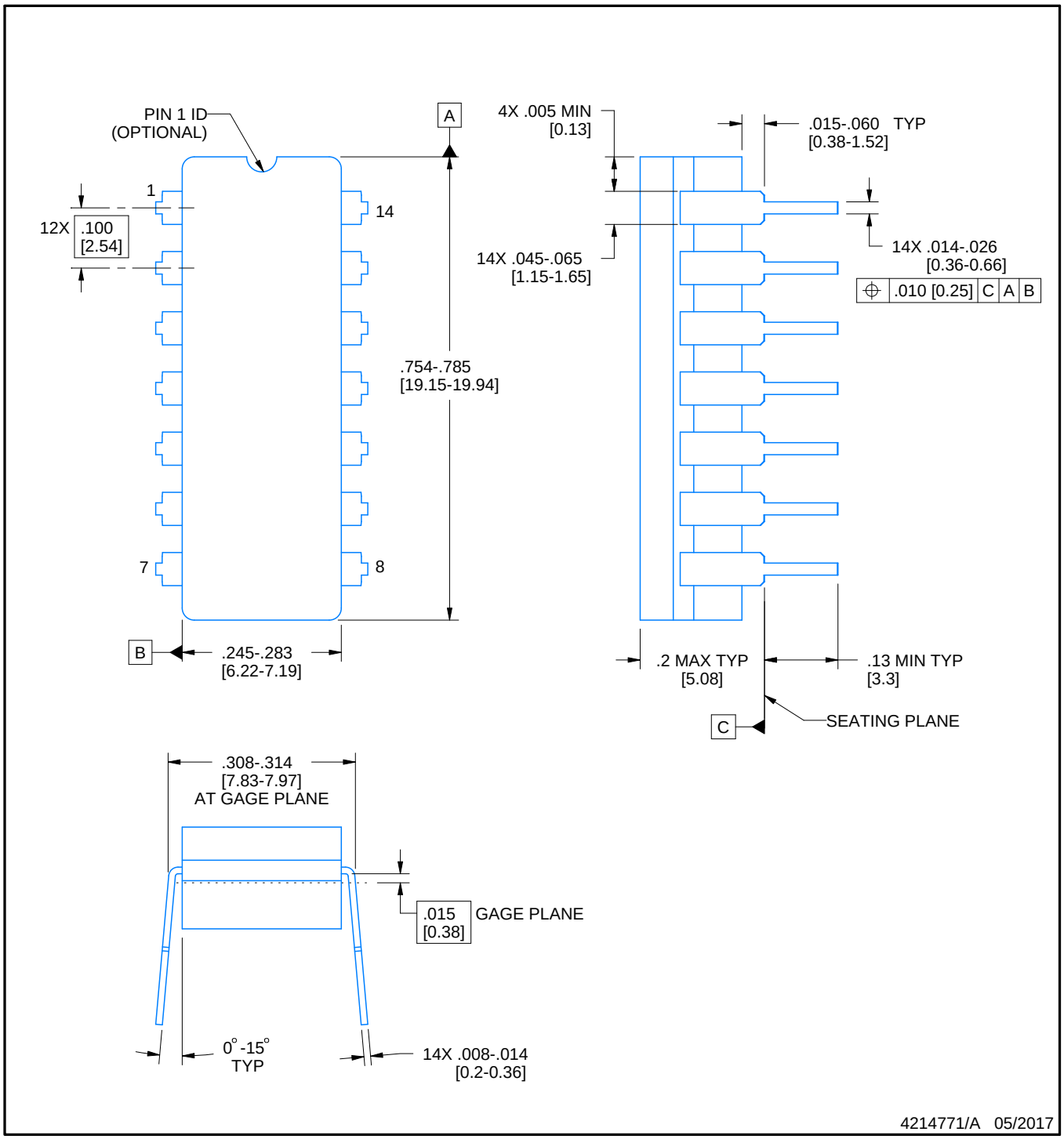
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

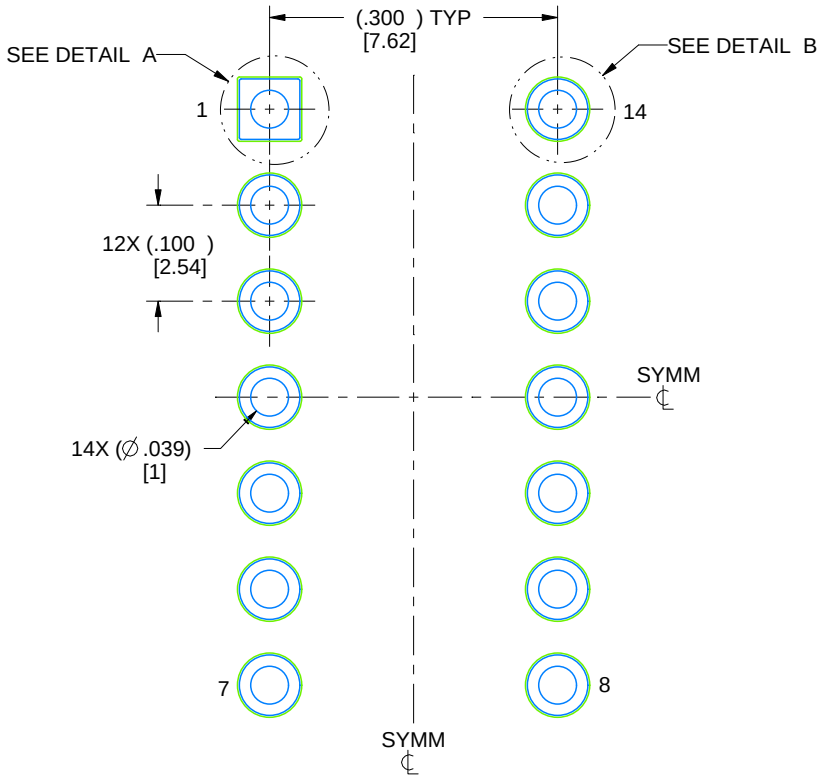
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

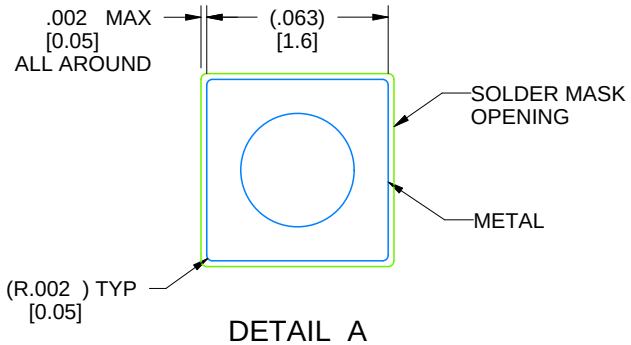
J0014A

CDIP - 5.08 mm max height

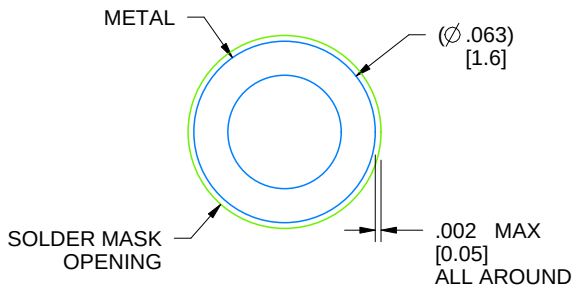
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



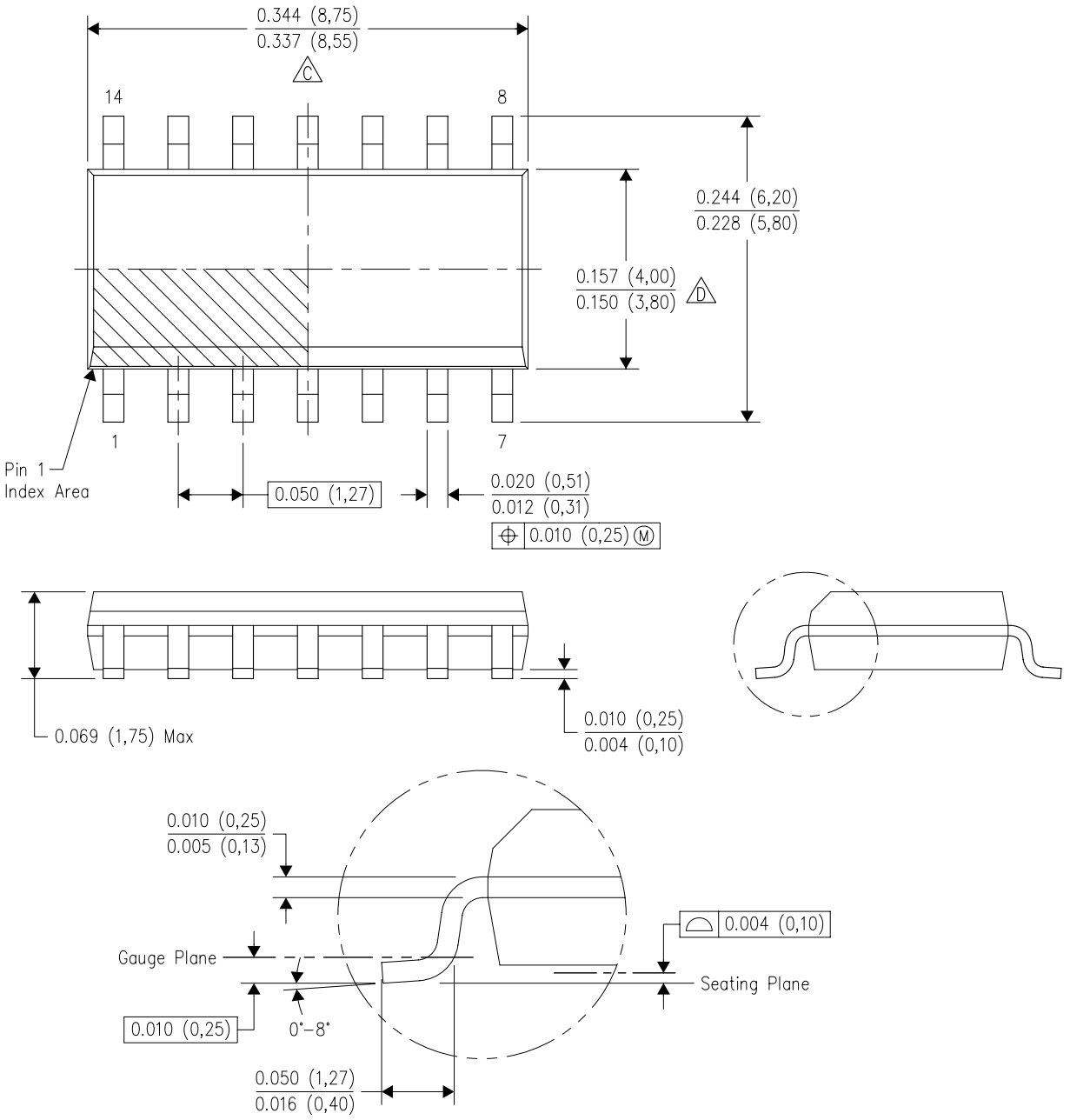
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

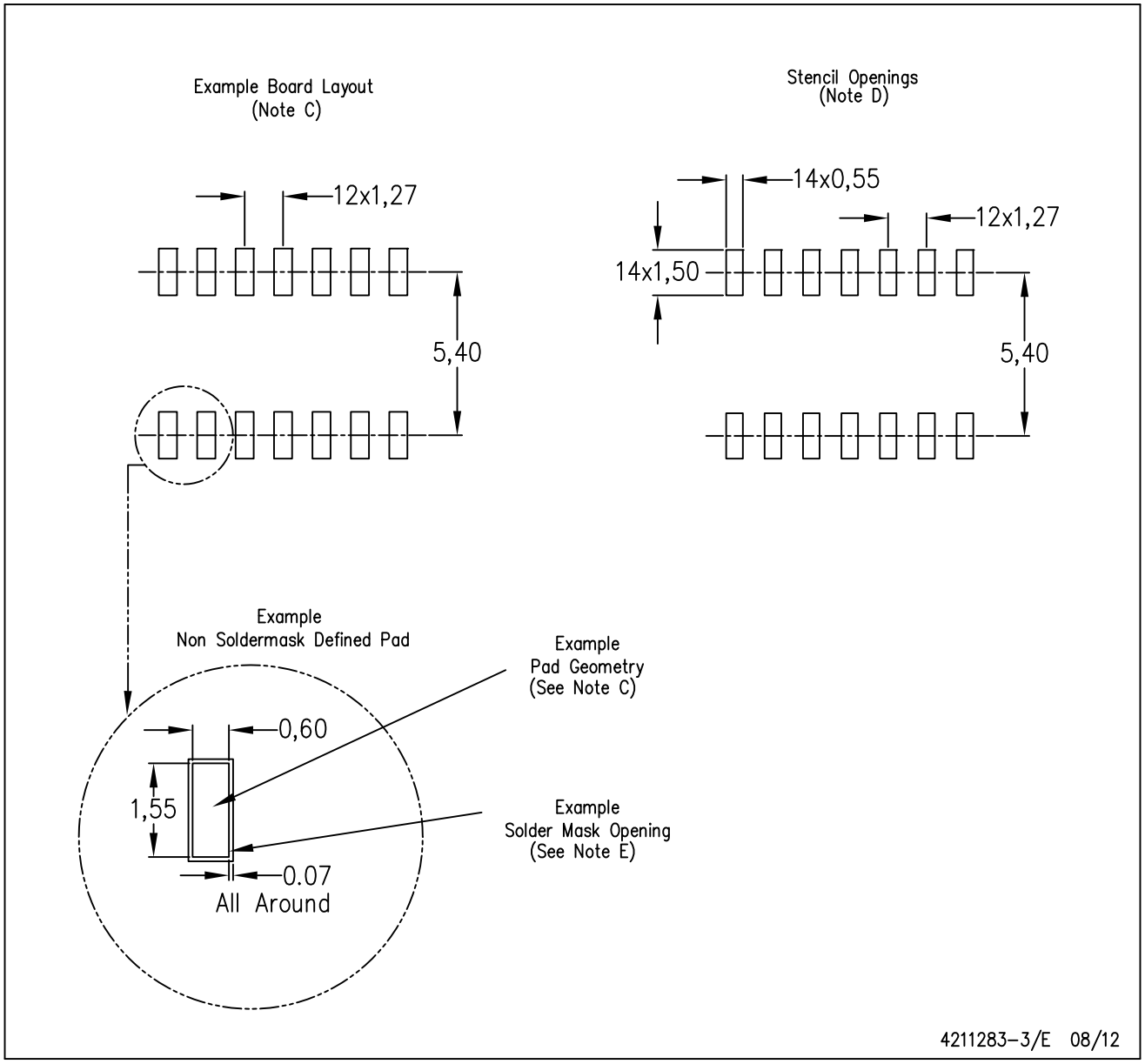
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE

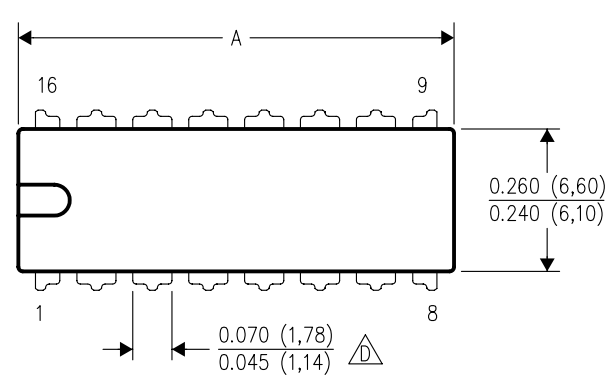


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

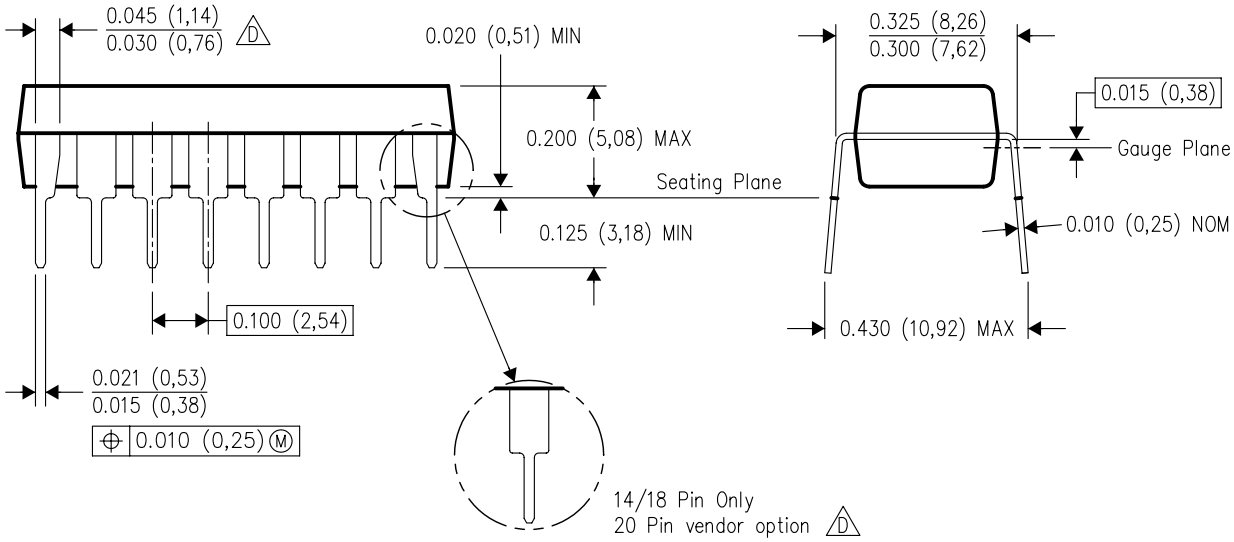
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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