CSD95485RWJ 同步降压 NexFET™智能功率级

1 特性

- 具有 75A 持续工作电流能力
- 30A 电流下系统效率超过 95%
- 工作频率高（高达 1.25MHz）
- 二极管仿真功能
- 温度补偿双向电流感应
- 模拟温度输出
- 故障监控
- 兼容 3.3V 和 5V PWM 信号
- 三态 PWM 输入
- 集成自举开关
- 用于击穿保护的经优化死区时间
- 高密度 5mm × 6mm QFN 封装
- 超低电感封装
- 系统已优化的 PCB 空间占用
- 耐热增强型顶部散热
- 符合 RoHS 标准 – 无铅端子镀层
- 无卤素

2 应用

- 多相同步降压转换器
  - 高频率 应用
  - 高电流、低占空比 应用
- POL 直流/直流转换器
- 存储器和显卡
- 台式机和服务器 VR12.x/VR13.x V-core 同步降压转换器

3 说明

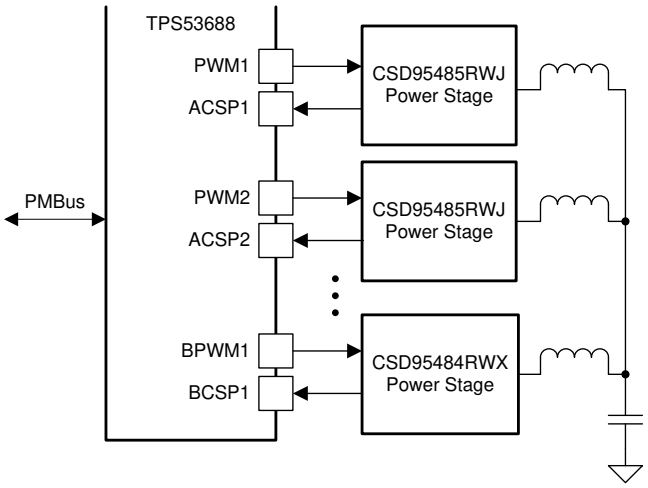
CSD95485RWJ NexFET™功率级是经过高度优化的设计，用于高功率、高功率密度场合的同步降压转换器。这款产品集成了驱动器 IC 和功率 MOSFET 来完善功率级开关功能。该组合采用 5mm × 6mm 小型封装，可实现高电流、高效率以及高速切换功能。它还集成了准确电流检测和温度感测功能，以简化系统设计并提高准确度。此外，PCB 封装已经过优化，可帮助减少设计时间并简化总体系统设计。

器件信息(1)

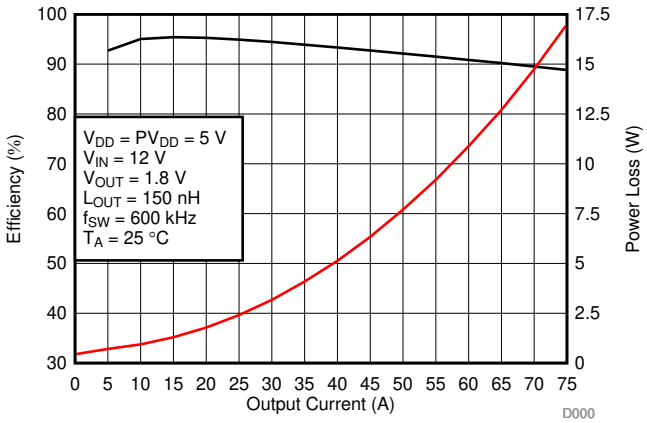
器件	介质	数量	封装	配送
CSD95485RWJ	13 英寸卷带	2500	QFN 5.00mm × 6.00mm 封装	卷带封装
CSD95485RWJT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用图表



典型功率级效率与功率损耗



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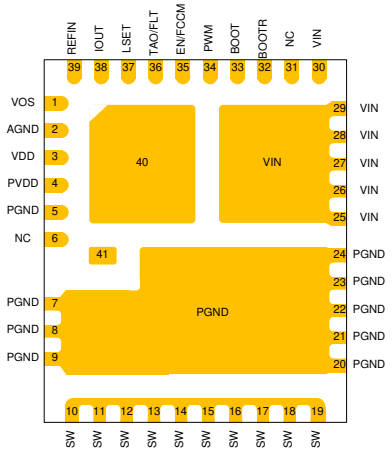
4 修订历史记录

日期	修订版本	说明
2020 年 3 月	*	初始发行版。

5 Pin Configuration and Functions

RWJ Package
41-Pin QFN
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
VOS	1	Output voltage sensing pin for the internal current sensing circuitry.
AGND	2	This pin is internally connected to PGND.
VDD	3	Supply voltage for internal circuitry. This pin should be bypassed directly to pin 2.
PVDD	4	Supply voltage for gate drivers. This pin should be bypassed to PGND.
PGND	5	Power ground.
NC	6	Not connected. This pin needs to be left floating in application.
PGND	7-9	Power ground.
VSW	10-19	Phase node connecting the HS MOSFET source and LS MOSFET drain – pin connection to the output inductor.
PGND	20-24	Power ground.
VIN	25-30	Input voltage pin. Connect input capacitors close to this pin.
NC	31	Not connected. This pin needs to be left floating in application.
BOOTR	32	Return path for HS gate driver. It is connected to VSW internally.
BOOT	33	Bootstrap capacitor connection. Connect a minimum 0.1-µF, 16-V, X5R ceramic capacitor from BOOT to BOOTR pins. The bootstrap capacitor provides the charge to turn on the control FET. The bootstrap diode is integrated.
PWM	34	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Both MOSFET gates are set low if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (T_{3HT}).
EN/FCCM	35	This dual function pin either enables the diode emulation function or can be used as a simple enable for the device. When this pin is driven into the tri-state window and held there for more than the tri-state holdoff time, diode emulation mode is enabled for sync FET. When the pin is high, device operates in forced continuous conduction mode. When the pin is low, both FETs are held off. An internal resistor pulls this pin low if left floating.
TAO/FLT	36	Temperature amplifier output. Reports a voltage proportional to the IC temperature. An ORing diode is integrated in the IC. When used in a multi-phase application, a single wire can be used to connect the TAO pins of all the ICs. Only the highest temperature will be reported. TAO will be pulled up to 3.3 V if thermal shutdown LSOC or HSS detection circuit is tripped.
LSET	37	A resistor from this pin to PGND pin sets the inductor value for the internal current sensing circuitry.
IOUT	38	Output of current sensing amplifier. V(IOUT) – V(REFIN) is proportional to the phase current.
REFIN	39	External reference voltage input for current sensing amplifier.
PGND	40	Power ground.
NC	41	Not connected. This pin needs to be left floating in application.

6 Specifications

6.1 Absolute Maximum Ratings

T_A = 25°C (unless otherwise noted)(1)

			MIN	MAX	UNIT
	V_{IN} to P_{GND}		–0.3	20	V
	V_{IN} to V_{SW}		–0.3	20	V
	V_{IN} to V_{SW} (10 ns)	I_{LOAD} > 0 A(2)		23	V
	V_{SW} to P_{GND}		–0.3	20	V
	V_{SW} to P_{GND} (10 ns)	I_{LOAD} < 0 A(2)		23	V
	V_{SW} to P_{GND} (10 ns)		–7		V
	V_{DD} to P_{GND}		–0.3	7	V
	EN/FCCM, TAO/FLT, LSET to P_{GND}(3)		–0.3	V_{DD} + 0.3	V
	IOUT, VOS, PWM to P_{GND}		–0.3	7	V
	REFIN to P_{GND}		–0.3	3.6	V
	BOOT to P_{GND}		–0.3	30	V
	BOOT to BOOT_R(3)		–0.3	V_{DD} + 0.3	V
T_J	Operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) I_{LOAD} is defined as the current flowing out of the VSW pins.
(3) Should not exceed 7 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±500	

6.3 Recommended Operating Conditions

T_A = 25°C (unless otherwise stated)

			MIN	MAX	UNIT
V_{DD}	Driver supply voltage		4.5	5.5	V
PV_{DD}	Gate drive voltage		4.5	5.5	V
V_{IN}	Input supply voltage(1)		4.5	16	V
V_{OUT}	Output voltage			5.5	V
	PWM to P_{GND}			V_{DD} + 0.3	V
I_{OUT}	Continuous output current	V_{IN} = 12 V, V_{DD} = 5 V, PV_{DD} = 5 V, V_{OUT} = 1.2 V, f_{SW} = 500 kHz(2)		75	A
I_{OUT-PK}	Peak output current(3)			105	A
f_{SW}	Switching frequency	C_{BST} = 0.1 µF (min), V_{OUT} = 2.5 V (max)		1250	kHz
	On-time duty cycle	f_{SW} = 1 MHz		85%	
	Minimum PWM on-time		20		ns
	Operating junction temperature		–40	125	°C

(1) Operating at high V_{IN} can create excessive AC voltage overshoots on the switch node (V_{SW}) during MOSFET switching transients. For reliable operation, the switch node (V_{SW}) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10-µF (TDK C3216X7R1C106KT or equivalent) ceramic capacitors across V_{IN} to P_{GND} pins.
(3) System conditions as defined in Note 2. Peak output current is applied for t_p = 50 µs.

6.4 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
θ_{JC}	Thermal resistance, junction-to-case (top of package)		7.4		°C/W
θ_{JB}	Thermal resistance, junction-to-board(1)		2.2		°C/W
Ψ_{JT}	Junction-to-top characterization parameter		0.9		°C/W

(1) θ_{JB} is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in, 0.06-in (1.52-mm) thick FR4 board based on hottest board temperature within 1 mm of the package.

7 Application Schematic

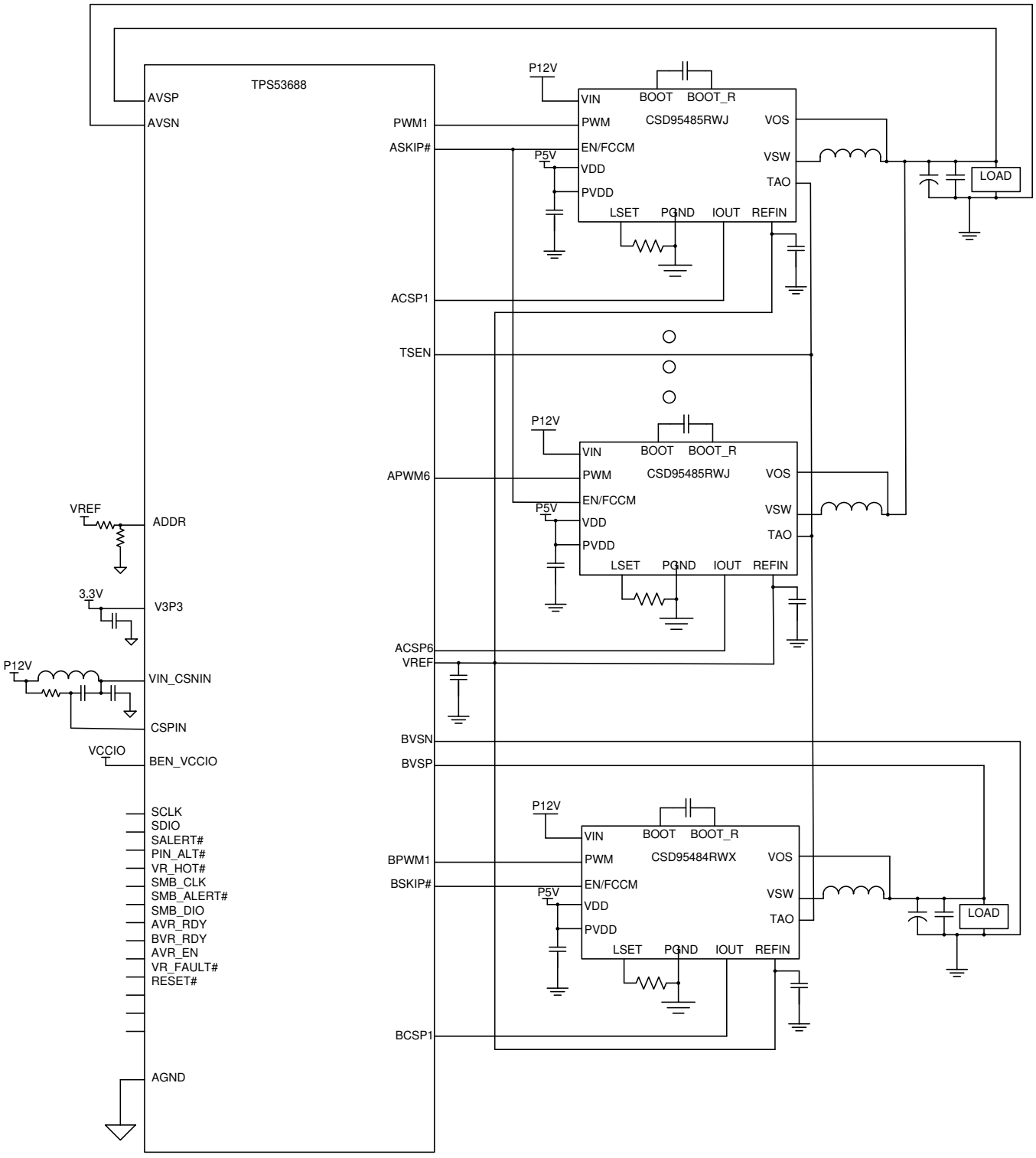


Figure 1. Application Schematic

Note: The schematic in Figure 1 is a conceptual drawing only. Actual designs may require additional components not shown.

8 器件和文档支持

8.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

8.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

8.3 Glossary

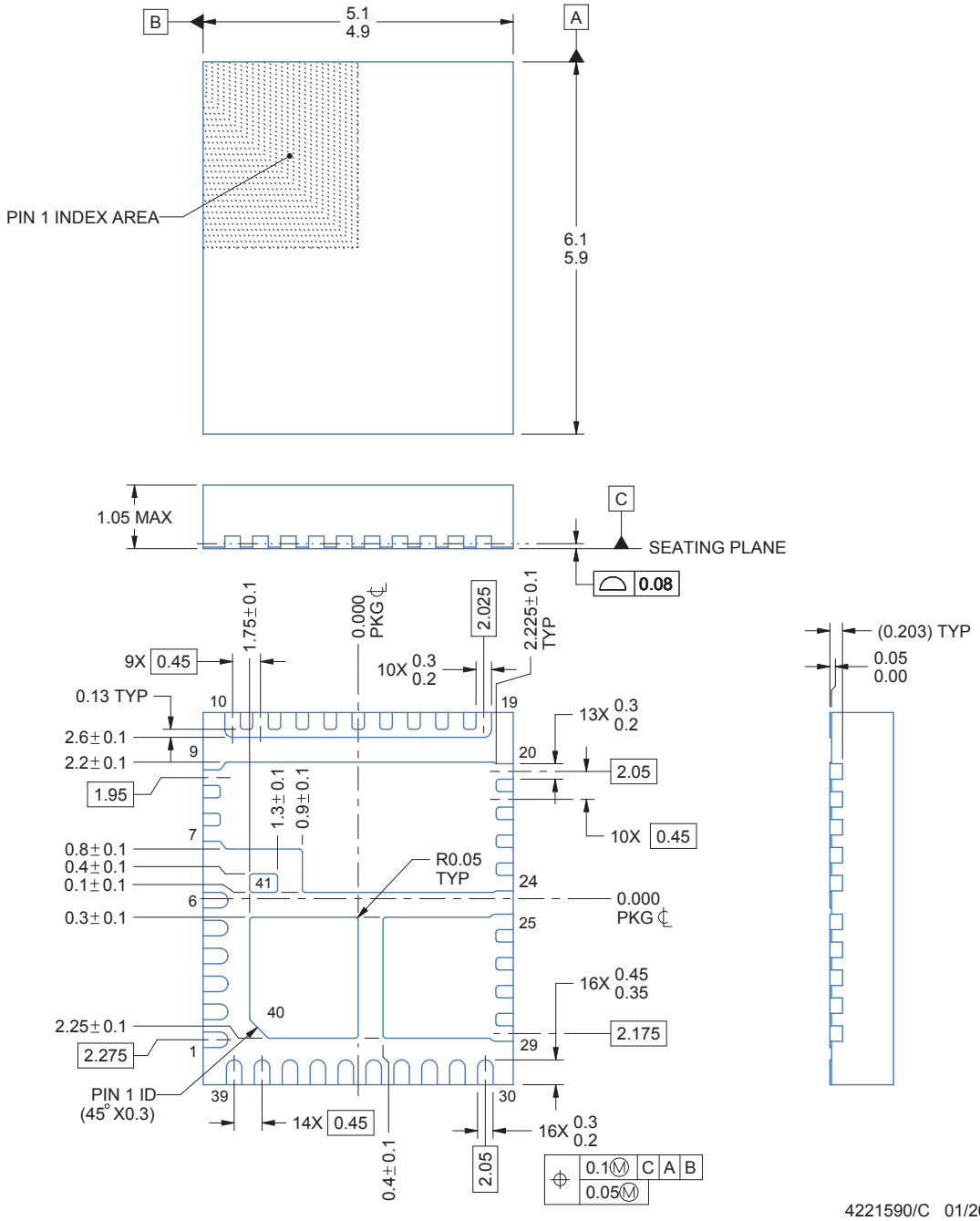
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

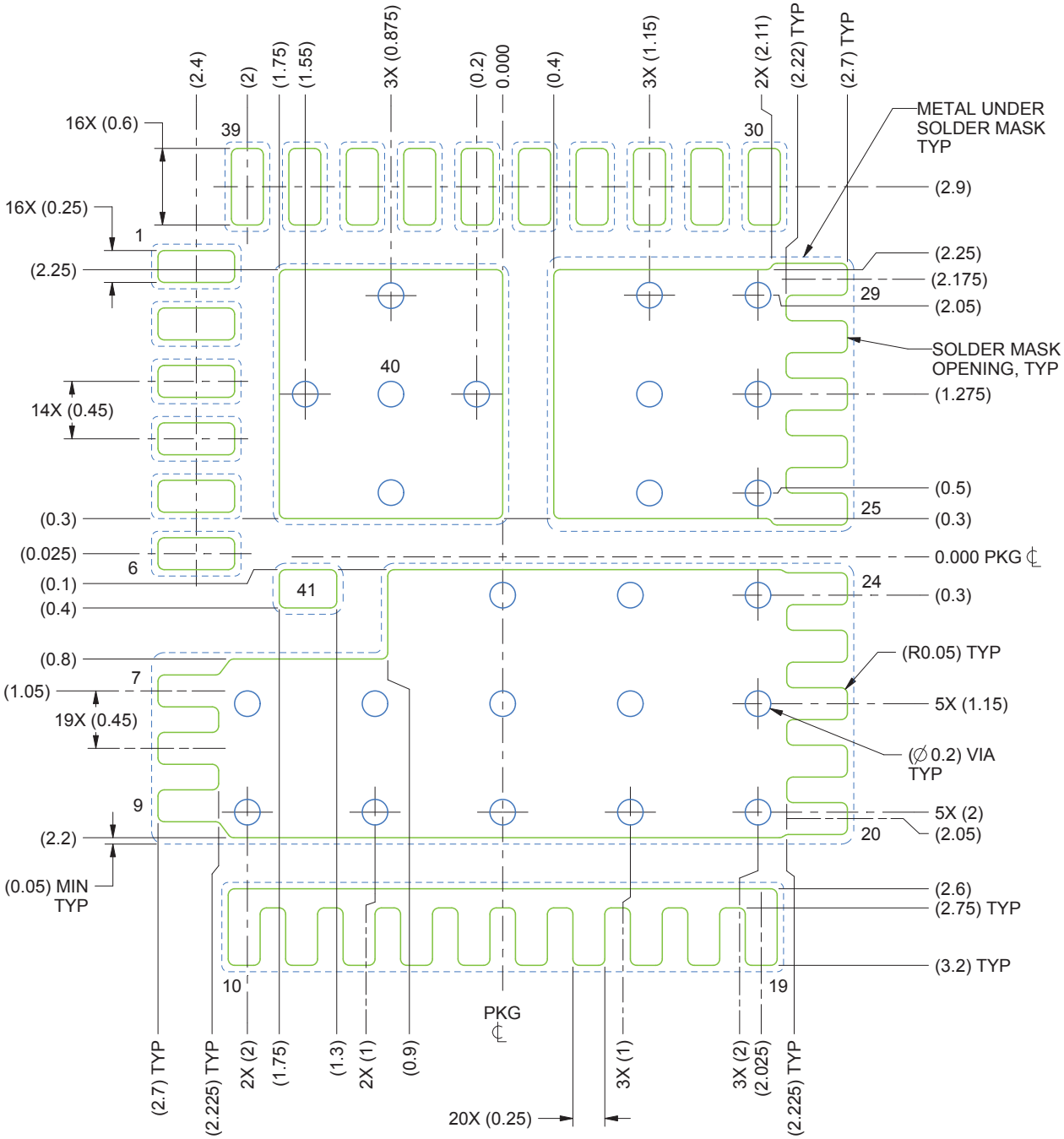
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

9.1 机械制图



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 封装散热焊盘必须焊接在印刷电路板上，才能实现最佳的散热和机械性能。

9.2 推荐 PCB 焊盘图案



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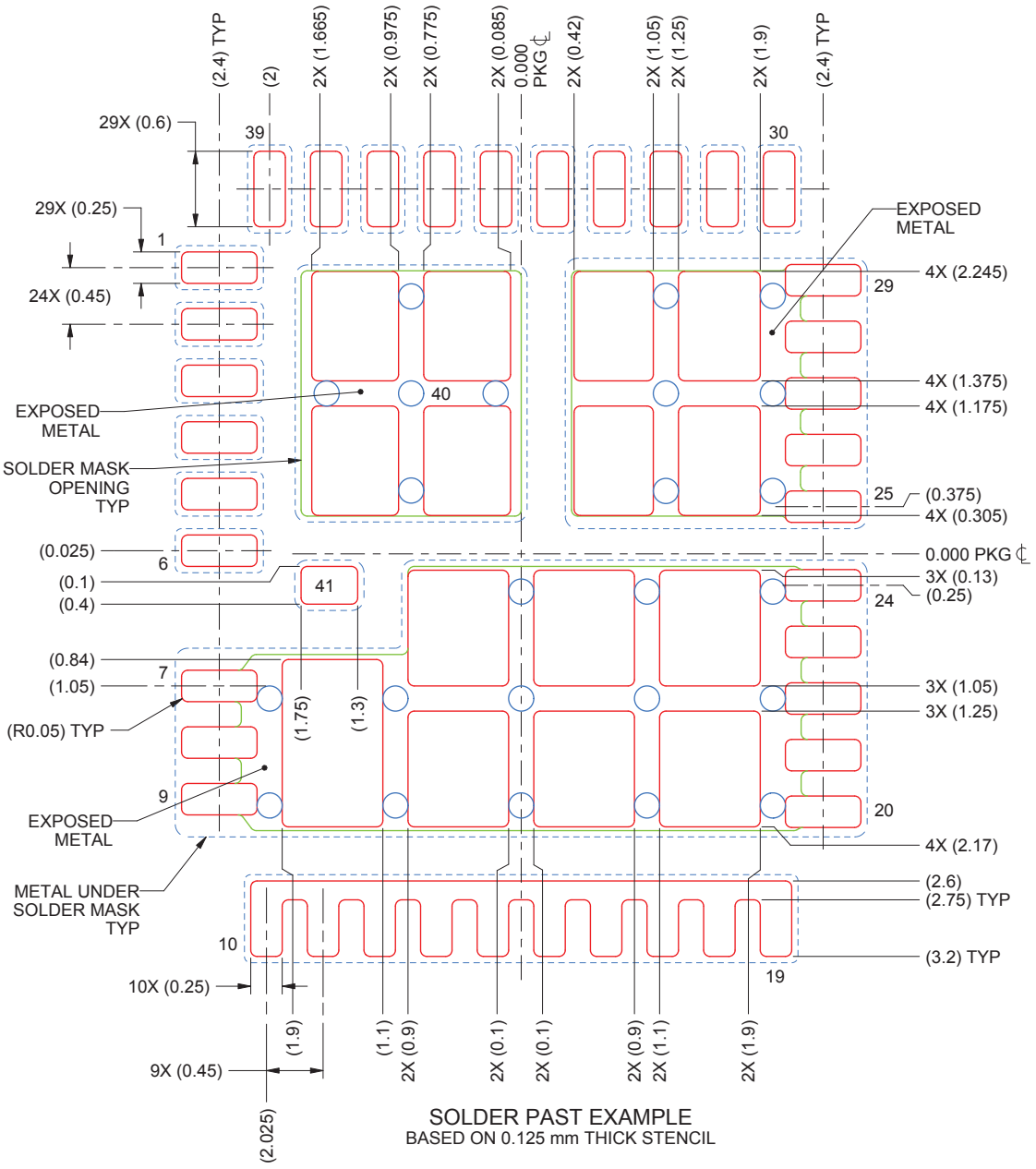
2. 本图如有变更，恕不另行通知。
3. 此封装设计用于焊接到电路板的散热焊盘上。有关更多信息，请参阅《*QFN/SON PCB 连接*》(SLUA271)。

9.3 建议模版开孔



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2. 本图如有变更，恕不另行通知。
3. 具有漏斗形壁和圆角的激光切割孔可提供更佳的锡膏脱离。IPC-7525 可能提供替代设计建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD95485RWJ	ACTIVE	VQFN-CLIP	RWJ	41	2500	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95485RWJ	Samples
CSD95485RWJT	ACTIVE	VQFN-CLIP	RWJ	41	250	RoHS-Exempt & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-55 to 150	95485RWJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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