具有 2.5V、2ppm/°C 内部基准电压的 DAC7568、DAC8168、DAC8568 12/14/16 位、8 通道、超低毛刺、电压输出数模转换器

1 特性

- 相对精度：
  - DAC7568（12 位）：0.3 LSB INL
  - DAC8168（14 位）：1 LSB INL
  - DAC8568（16 位）：4 LSB INL
- 毛刺脉冲能量：0.1nV-s
- 内部基准电压：
  - 2.5V 基准电压（默认为禁用）
  - 0.004% 初始精度（典型值）
  - 2ppm/°C 温漂（典型值）
  - 5ppm/°C 温漂（最大值）
  - 20mA 灌电流/拉电流能力
- 上电复位至零电平或中间电平
- 超低功耗运行：1.25mA/5V（包括内部基准电流）
- 宽电源范围：+2.7V 至 +5.5V
- 在整个温度范围内具有单调性
- 具有施密特触发输入的低功耗串口：高达 50MHz
- 支持轨至轨运行的片上输出缓冲放大器
- 温度范围：-40°C 至 +125°C

2 应用

- 便携式仪表
- 闭环伺服控制/流程控制
- 数据采集系统
- 可编程衰减、数字增益和失调电压调节
- 可编程电压源和电流源

3 说明

DAC7568、DAC8168 和 DAC8568 分别为 12 位、14 位和 16 位低功耗、电压输出、八通道数模转换器 (DAC)。这些器件包括一个 2.5V、2ppm/°C 内部基准电压（默认禁用），可提供 2.5V 或 5V 的满量程输出电压范围。内部基准电压初始精度为 0.004%，而且可在 $V_{REF}IN/V_{REF}OUT$ 引脚上提供高达 20mA 的电流。这些器件具有单调性，可提供出色的线性并降低有害的代码至代码转换时的瞬态电压（毛刺脉冲）。它们使用一个运行时钟速率高达 50MHz 的多用途 3 线制串口。此接口与标准 SPI™、 QSPI™、 Microwire™，以及数字信号处理器 (DSP) 接口兼容。

DAC7568、DAC8168 和 DAC8568 包含一个上电复位电路，此电路确保 DAC 输出在零电平或中间电平时上电，并在一段有效代码被写入器件前保持此状态。这些器件包含一个由串口访问的断电特性，这将器件在电压为 5V 时的流耗减少至 0.18μA（典型值）。3V 时的功耗（包括内部基准）通常为 2.9mW，在断电模式下可降低至低于 1μW。低功耗、内部基准电压和小封装尺寸使得这些器件非常适合于便携式、电池供电类设备。

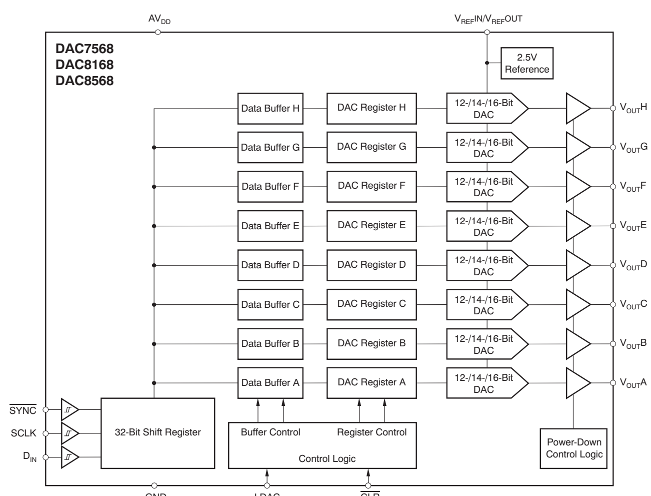
DAC7568、DAC8168 和 DAC8568 互为功能兼容型直接替代产品，可提供 TSSOP-16 和 TSSOP-14 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC7568	TSSOP (14)	5.00mm x 4.40mm
	TSSOP (16)	5.00mm x 4.40mm
DAC8168	TSSOP (14)	5.00mm x 4.40mm
	TSSOP (16)	5.00mm x 4.40mm
DAC8568	TSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

框图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (January 2014) to Revision F — **Page**

- 将数据表更新至 SDS 标准 1
- Added External reference current grades and updated typ values 6
- Added Reference input impedance grades and updated typ values 6
- Changed I_{DD} Normal mode, internal reference switched on, AV_{DD} = 3.6V to 5.5V, $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND maximum value from 2.0mA to 2.5mA 7

Changes from Revision D (May 2012) to Revision E — **Page**

- Changed bit value in last three rows of *Power-Down Commands* section in from '0' to '1' 38

Changes from Revision C (February 2011) to Revision D — **Page**

- Changed Logic Input HIGH Voltage parameter test condition into two rows 7

Changes from Revision B (November 2010) to Revision C — **Page**

- Changed Output Voltage parameter min/max values from 2.4895 and 2.5005 to 2.4975 and 2.5025, respectively 6
- Changed Initial Accuracy parameter min/max values from –0.02 and 0.02 to –0.1 and 0.1, respectively 6

Changes from Revision A (April 2009) to Revision B — **Page**

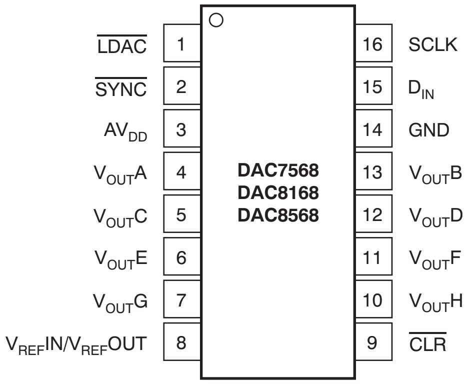
- Changed Logic Input LOW Voltage parameter maximum value from 0.8 to 0.3 × AV_{DD} 7
- Changed Logic Input HIGH Voltage parameter minimum value from 1.8 to 0.7 × AV_{DD} 7
- Updated Figure 122 33

5 Device Comparison Table

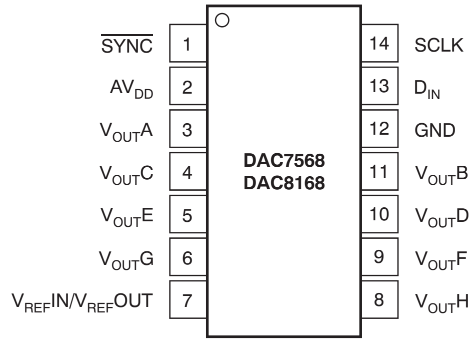
PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY (LSB)	MAXIMUM REFERENCE DRIFT (ppm/°C)	OUTPUT VOLTAGE FULL-SCALE RANGE	RESET TO	RESOLUTION
DAC8568A	±12	±1	25	2.5V	Zero	16
DAC8568B	±12	±1	25	2.5V	Midscale	16
DAC8568C	±12	±1	5	5V	Zero	16
DAC8568D	±12	±1	5	5V	Midscale	16
DAC8168A	±4	±0.5	25	2.5V	Zero	14
DAC8168C	±4	±0.5	5	5V	Zero	14
DAC7568A	±1	±0.25	25	2.5V	Zero	12
DAC7568C	±1	±0.25	5	5V	Zero	12

6 Pin Configuration and Functions

**PW PACKAGE
TSSOP-16
(TOP VIEW)**



**PW PACKAGE
TSSOP-14
(TOP VIEW)**



Pin Functions

16-PIN	14-PIN	NAME	DESCRIPTION
1	—	$\overline{LDAC}$	Load DACs.
2	1	$\overline{SYNC}$	Level-triggered control input (active low). This input is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register, and data are sampled on subsequent falling clock edges. The DAC output updates following the 32nd clock. If $\overline{SYNC}$ is taken high before the 31st clock edge, the rising edge of $\overline{SYNC}$ acts as an interrupt, and the write sequence is ignored by the DAC7568/DAC8168/DAC8568. Schmitt-Trigger logic input.
3	2	AV_{DD}	Power-supply input, 2.7V to 5.5V
4	3	$V_{OUT}A$	Analog output voltage from DAC A
5	4	$V_{OUT}C$	Analog output voltage from DAC C
6	5	$V_{OUT}E$	Analog output voltage from DAC E
7	6	$V_{OUT}G$	Analog output voltage from DAC G
8	7	$V_{REF}IN/$ $V_{REF}OUT$	Positive reference input / reference output 2.5V if internal reference used.(1)
9	—	$\overline{CLR}$	Asynchronous clear input.
10	8	$V_{OUT}H$	Analog output voltage from DAC H
11	9	$V_{OUT}F$	Analog output voltage from DAC F
12	10	$V_{OUT}D$	Analog output voltage from DAC D
13	11	$V_{OUT}B$	Analog output voltage from DAC B
14	12	GND	Ground reference point for all circuitry on the device
15	13	D_{IN}	Serial data input. Data are clocked into the 32-bit input shift register on each falling edge of the serial clock input. Schmitt-Trigger logic input.
16	14	SCLK	Serial clock input. Data can be transferred at rates up to 50MHz. Schmitt-Trigger logic input.

(1) Grades A and B, external $V_{REF}IN$ (max) ≤ AV_{DD}; grades C and D, external $V_{REF}IN$ (max) ≤ $AV_{DD}/2$.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	MAX	UNIT
AV_{DD} to GND	–0.3	6	V
Digital input voltage to GND	–0.3	AV_{DD} + 0.3	V
V_{OUT} to GND	–0.3	AV_{DD} + 0.3	V
V_{REF} to GND	–0.3	AV_{DD} + 0.3	V
Operating temperature range	–40	125	°C
Storage temperature range	–65	150	°C
Junction temperature range (T_J max)		150	°C
Power dissipation	$(T_J \text{ max} – T_A)/\theta_{JA}$		W
Thermal impedance, $R_{\theta JA}$	118		°C/W
Thermal impedance, $R_{\theta JC}$	29		°C/W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Electrical Characteristics

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE(1)						
DAC8568	Resolution		16			Bits
	Relative accuracy	Measured by the line passing through codes 485 and 64714		±4	±12	LSB
	Differential nonlinearity	16-bit monotonic		±0.2	±1	LSB
DAC8168	Resolution		14			Bits
	Relative accuracy	Measured by the line passing through codes 120 and 16200		±1	±4	LSB
	Differential nonlinearity	14-bit monotonic		±0.1	±0.5	LSB
DAC7568	Resolution		12			Bits
	Relative accuracy	Measured by the line passing through codes 30 and 4050		±0.3	±1	LSB
	Differential nonlinearity	12-bit monotonic		±0.05	±0.25	LSB
Offset error		Extrapolated from two-point line(1), unloaded		±1	±4	mV
Offset error drift				±0.5		μV/°C
Full-scale error		DAC register loaded with all '1's		±0.03	±0.2	% of FSR
Zero-code error		DAC register loaded with all '0's		1	4	mV
Zero-code error drift				±2		μV/°C
Gain error		Extrapolated from two-point line(1), unloaded		±0.01	±0.15	% of FSR
Gain temperature coefficient				±1		ppm of FSR/°C

(1) 16-bit: codes 485 and 64714; 14-bit: codes 120 and 16200; 12-bit: codes 30 and 4050

Electrical Characteristics (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS(2)					
Output voltage range	AV_{DD} ≥ 2.7V; grades A and B: maximum output voltage 2.5V when using internal reference	0		AV_{DD}	V
	AV_{DD} ≥ 5V; grades C and D: maximum output voltage 5V when using internal reference				
Output voltage settling time	DACs unloaded; 1/4 scale to 3/4 scale to ±0.024%		5	10	µs
	R_L = 1MΩ		10		
Slew rate			0.75		V/µs
Capacitive load stability	R_L = ∞		1000		pF
	R_L = 2kΩ		3000		
Code change glitch impulse	1LSB change around major carry		0.1		nV-s
Digital feedthrough	SCLK toggling, $\overline{SYNC}$ high		0.1		nV-s
Power-on glitch impulse	R_L = 2kΩ, C_L = 470pF, AV_{DD} = 5.5V		10		mV
	R_L = 2kΩ, C_L = 470pF, AV_{DD} = 2.7V		6		mV
Channel-to-channel dc crosstalk	Full-scale swing on adjacent channel		0.1		LSB
Channel-to-channel ac crosstalk	R_L = 2kΩ, C_L = 420pF, 1kHz full-scale sine wave, outputs unloaded		–109		dB
DC output impedance	At mid-code input		4		Ω
Short-circuit current	DAC outputs at full-scale, DAC outputs shorted to GND		11		mA
Power-up time, including settling time	Coming out of power-down mode		50		µs
AC PERFORMANCE(2)					
SNR	T_A = +25°C, BW = 20kHz, AV_{DD} = 5V, f_{OUT} = 1kHz, first 19 harmonics removed for SNR calculation, at 16-bit level		83		dB
THD			–63		dB
SFDR			63		dB
SINAD			62		dB
DAC output noise density	T_A = +25°C, at zero-code input, f_{OUT} = 1kHz		90		nV/√Hz
DAC output noise	T_A = +25°C, at mid-code input, 0.1Hz to 10Hz		2.6		$µV_{PP}$
REFERENCE					
Internal reference current consumption	AV_{DD} = 5.5V		360		µA
	AV_{DD} = 3.6V		348		µA
External reference current	External V_{REF} = 2.5V (when internal reference is disabled), all eight channels active; Grades A/B		60		µA
	External V_{REF} = 2.5V (when internal reference is disabled), all eight channels active; Grades C/D		115		
V_{REF}IN — Reference input range	Grades A/B, AV_{DD} = 2.7V to 5.5V	0		AV_{DD}	V
	Grades C/D, AV_{DD} = 5.0V to 5.5V	0		$AV_{DD}/2$	V
Reference input impedance	Grades A/B		44		kΩ
	Grades C/D		22		
REFERENCE OUTPUT					
Output voltage	T_A = +25°C; all grades	2.4975	2.5	2.5025	V
Initial accuracy	T_A = +25°C, all grades	–0.1	±0.004	0.1	%
Output voltage temperature drift	DAC7568/DAC8168/DAC8568(3),grades A/B		5	25	ppm/°C
	DAC7568/DAC8168/DAC8568(4), grades C/D		2	5	
Output voltage noise	f = 0.1Hz to 10Hz		12		$µV_{PP}$
Output voltage noise density (high-frequency noise)	T_A = +25°C, f = 1MHz, C_L = 0µF		50		nV/√Hz
	T_A = +25°C, f = 1MHz, C_L = 1µF		20		
	T_A = +25°C, f = 1MHz, C_L = 4µF		16		
Load regulation, sourcing(5)	T_A = +25°C		30		µV/mA
Load regulation, sinking(5)	T_A = +25°C		15		µV/mA

(2) Specified by design or characterization; not production tested.
(3) Reference is trimmed and tested at room temperature, and is characterized from –40°C to +125°C.
(4) Reference is trimmed and tested at two temperatures (+25°C and +105°C), and is characterized from –40°C to +125°C.
(5) Explained in more detail in the *Application Information* section of this data sheet.

Electrical Characteristics (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output current load capability (2)				±20		mA
Line regulation		T_A = +25°C		10		µV/V
Long-term stability/drift (aging) (5)		T_A = +25°C, time = 0 to 1900 hours		50		ppm
Thermal hysteresis (5)		First cycle		100		ppm
		Additional cycles		25		ppm
LOGIC INPUTS (2)						
Input current				±1		µA
$V_{IN}L$	Logic input LOW voltage	2.7V ≤ AV_{DD} ≤ 5.5V			0.3 × AV_{DD}	V
$V_{IN}H$	Logic input HIGH voltage	2.7V ≤ AV_{DD} < 4.5V	0.7 × AV_{DD}			V
		4.5V ≤ AV_{DD} ≤ 5.5V	0.625 × AV_{DD}			V
Pin capacitance					3	pF
POWER REQUIREMENTS						
AV_{DD}			2.7		5.5	V
I_{DD} (6)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.95	1.4	mA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.81	1.3	mA
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.25	2.5	mA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		1.1	1.9	mA
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.18	3	µA
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.10	2.5	µA
Power dissipation (6)	Normal mode, internal reference switched off	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		3.4	7.7	mW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		2.2	4.7	mW
	Normal mode, internal reference switched on	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		4.5	11	mW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		2.9	6.8	mW
	All power-down modes	AV_{DD} = 3.6V to 5.5V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.6	16	µW
		AV_{DD} = 2.7V to 3.6V $V_{IN}H$ = AV_{DD} and $V_{IN}L$ = GND		0.3	9	µW
TEMPERATURE RANGE						
Specified performance			–40		+125	°C

(6) Input code = midscale, no load.

7.3 Timing Requirements (1) (2)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C (unless otherwise noted).

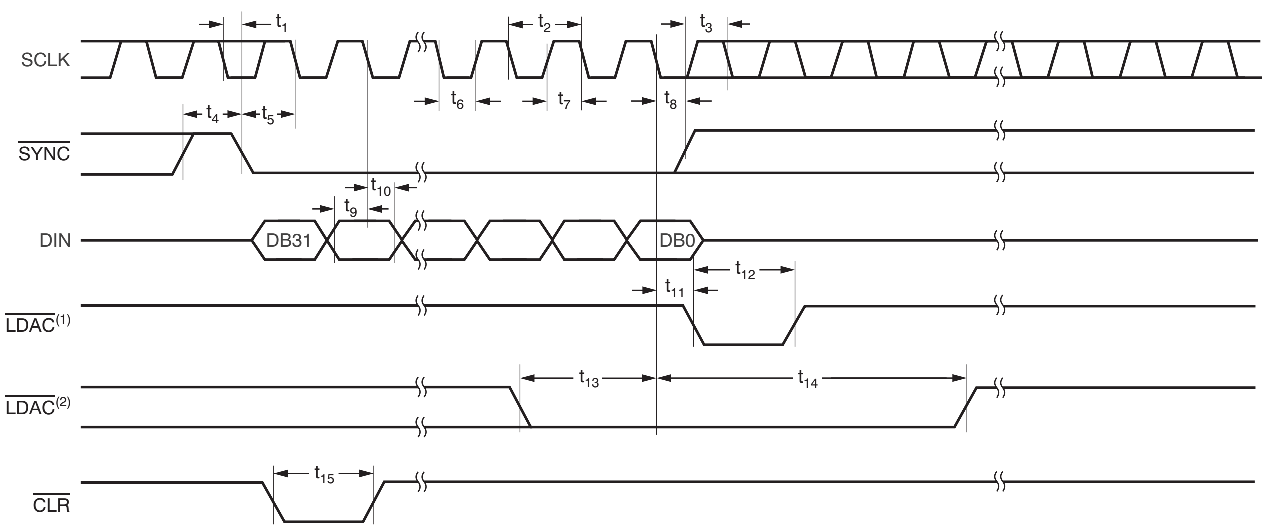
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	SCLK falling edge to $\overline{SYNC}$ falling edge (for successful write operation)	AV_{DD} = 2.7V to 5.5V	10			ns
t_2 (3)	SCLK cycle time	AV_{DD} = 2.7V to 5.5V	20			ns
t_3	$\overline{SYNC}$ rising edge to 31st SCLK falling edge (for successful $\overline{SYNC}$ interrupt)	AV_{DD} = 2.7V to 5.5V	13			ns
t_4	Minimum $\overline{SYNC}$ HIGH time	AV_{DD} = 2.7V to 5.5V	80			ns

(1) All input signals are specified with t_R = t_F = 3ns (10% to 90% of AV_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2.
(2) See the *Serial Write Operation* timing diagram.
(3) Maximum SCLK frequency is 50MHz at AV_{DD} = 2.7V to 5.5V.

Timing Requirements(1) (2) (continued)

At AV_{DD} = 2.7V to 5.5V and over –40°C to +125°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_5	SYNC to SCLK falling edge setup time	AV_{DD} = 2.7V to 5.5V	13			ns
t_6	SCLK LOW time	AV_{DD} = 2.7V to 5.5V	8			ns
t_7	SCLK HIGH time	AV_{DD} = 2.7V to 5.5V	8			ns
t_8	SCLK falling edge to SYNC rising edge	AV_{DD} = 2.7V to 5.5V	10			ns
t_9	Data setup time	AV_{DD} = 2.7V to 5.5V	6			ns
t_{10}	Data hold time	AV_{DD} = 2.7V to 5.5V	4			ns
t_{11}	SCLK falling edge to LDAC falling edge for asynchronous LDAC update mode	AV_{DD} = 2.7V to 5.5V	40			ns
t_{12}	LDAC pulse width LOW time	AV_{DD} = 2.7V to 5.5V	80			ns
t_{13}	LDAC falling edge to SCLK falling edge for synchronous LDAC update mode	AV_{DD} = 2.7V to 5.5V	$4 \times t_1$			ns
t_{14}	32nd SCLK falling edge to LDAC rising edge	AV_{DD} = 2.7V to 5.5V	40			ns
t_{15}	CLR pulse width LOW time	AV_{DD} = 2.7V to 5.5V	80			ns



(1) Asynchronous LDAC update mode. For more information and details, see the *LDAC Functionality* section.

(2) Synchronous LDAC update mode. For more information and details, see the *LDAC Functionality* section.

Figure 1. Serial Write Operation

7.4 Typical Characteristics: Internal Reference

At T_A = +25°C, unless otherwise noted.

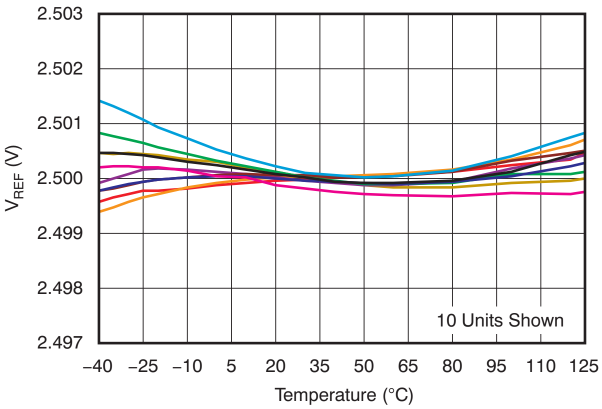


Figure 2. Internal Reference voltage vs Temperature (Grades C and D)

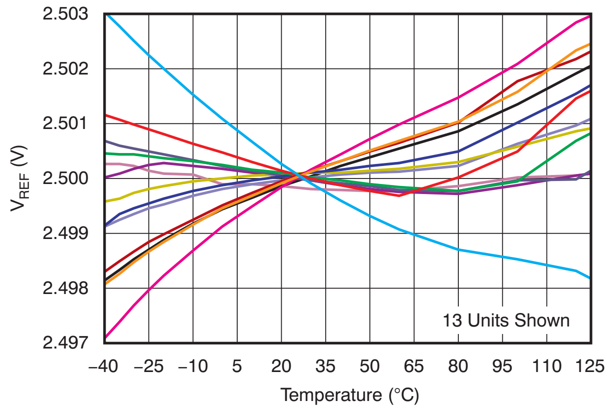


Figure 3. Internal Reference Voltage vs temperature (Grades A and B)

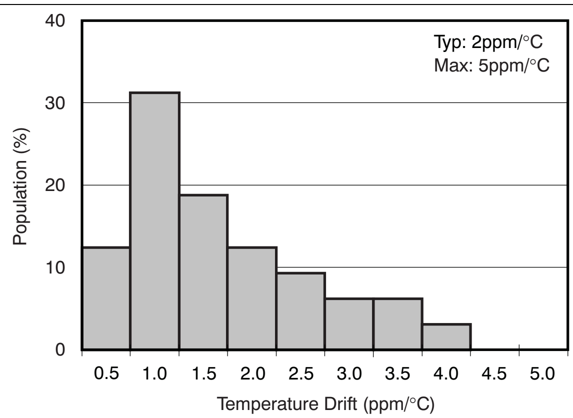


Figure 4. Reference Output Temperature Drift (–40°C to +125°C, Grades C and D)

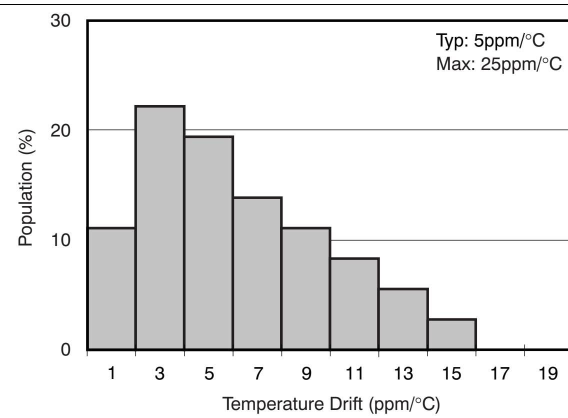


Figure 5. Reference Output Temperature Drift (–40°C to +125°, Grades A and B)

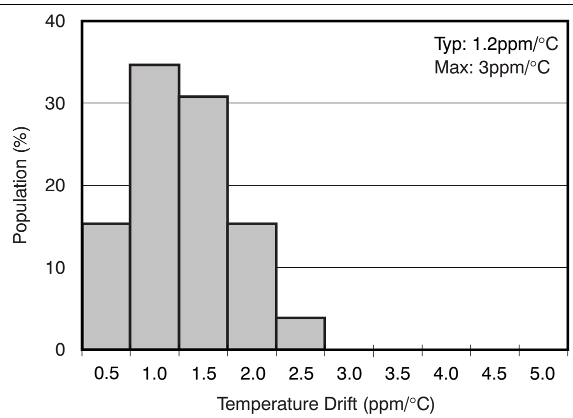
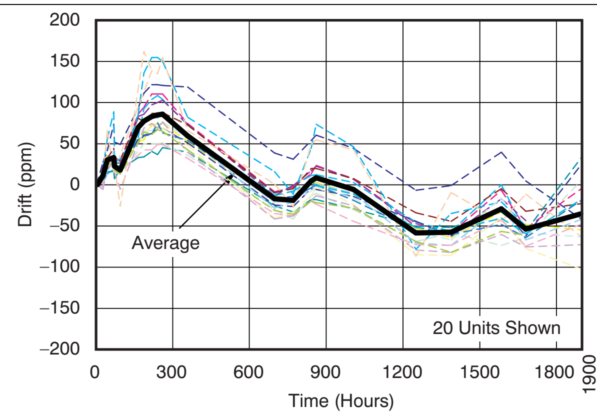


Figure 6. Reference Output Temperature Drift (0°C to +125°C, Grades C and D)

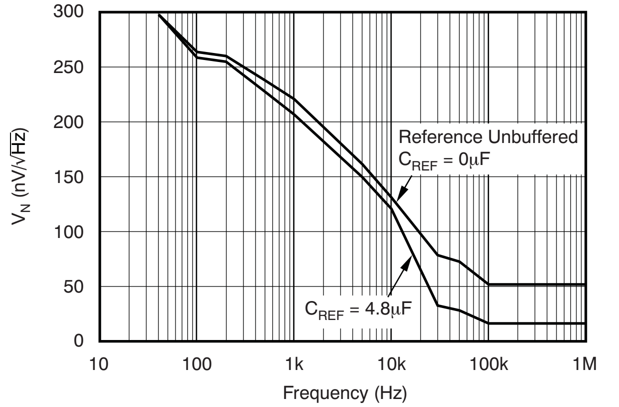


See the *Application Information* section of this data sheet for more details.

Figure 7. Long-Term Stability/Drift

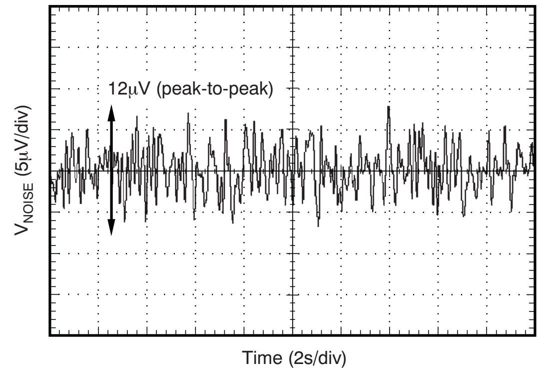
Typical Characteristics: Internal Reference (continued)

At T_A = +25°C, unless otherwise noted.



See the *Application Information* section of this data sheet for more details.

Figure 8. Internal Reference Noise Density vs Frequency



See the *Application Information* section of this data sheet for more details.

Figure 9. Internal Reference Noise 0.1 Hz to 10 Hz

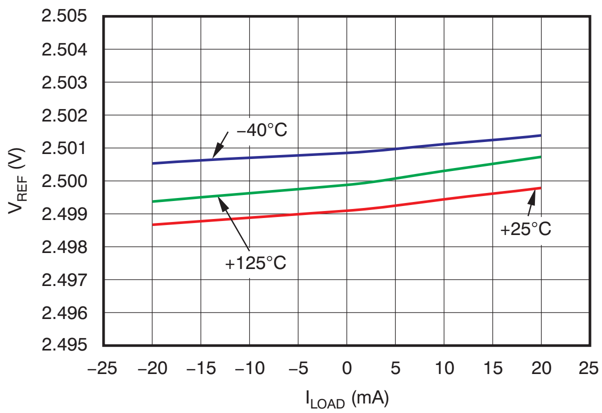


Figure 10. Internal Reference Voltage vs Load Current (Grades C and D)

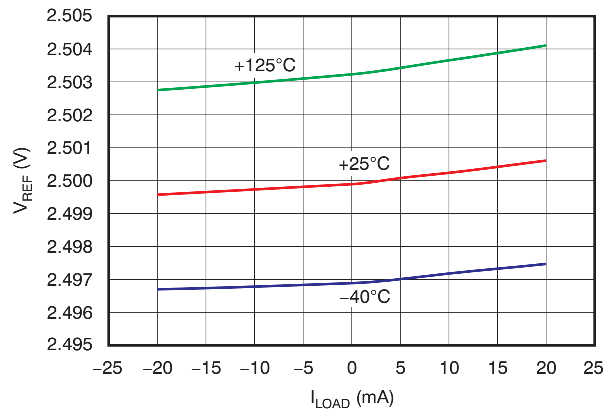


Figure 11. Internal Reference Voltage vs Load Current (Grades A and B)

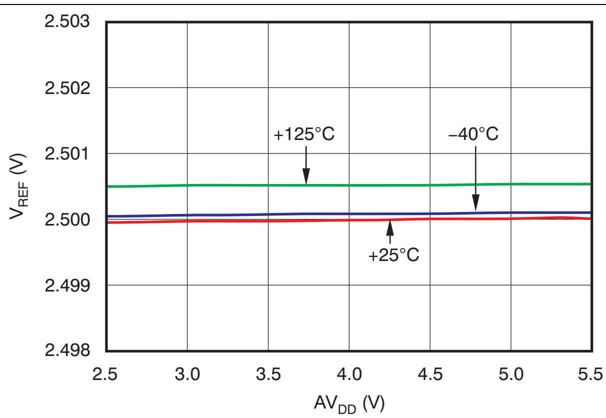


Figure 12. Internal Reference Voltage vs Supply Voltage (Grades C and D)

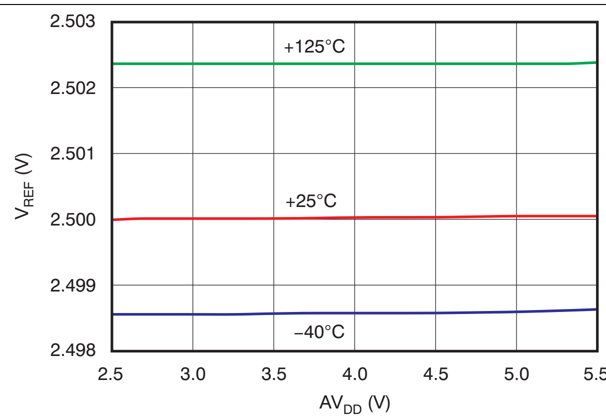


Figure 13. Internal Reference Voltage vs Supply Voltage (Grades A and B)

7.5 Typical Characteristics: DAC at AV_{DD} = 5.5 V

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

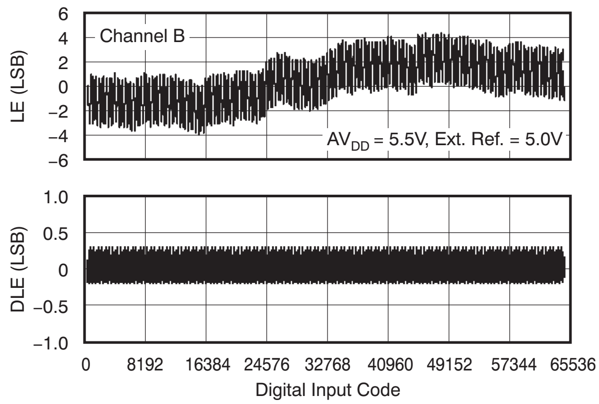


Figure 14. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

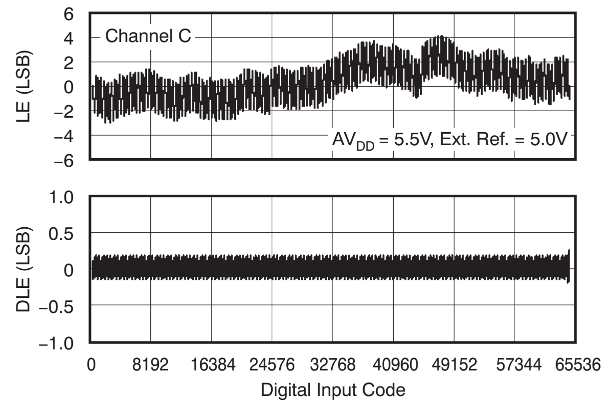


Figure 15. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

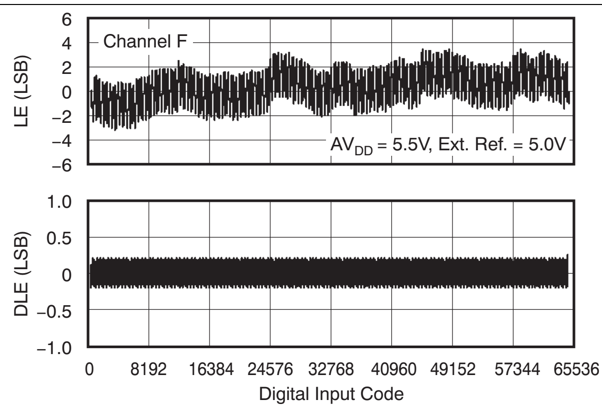


Figure 16. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

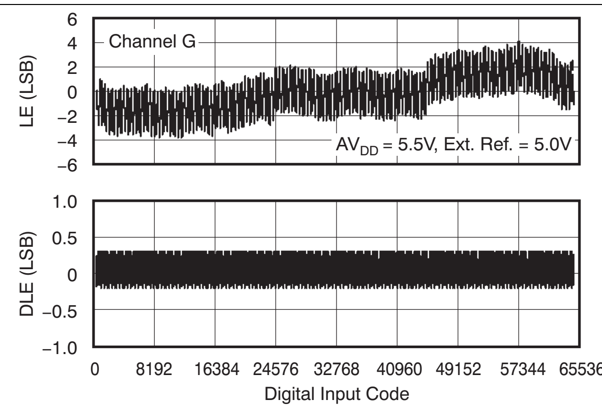


Figure 17. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

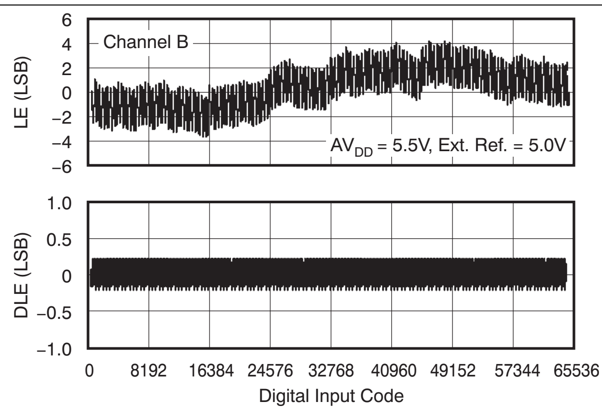


Figure 18. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

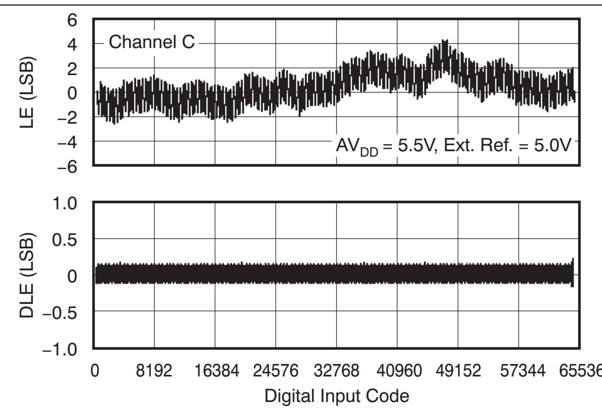


Figure 19. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

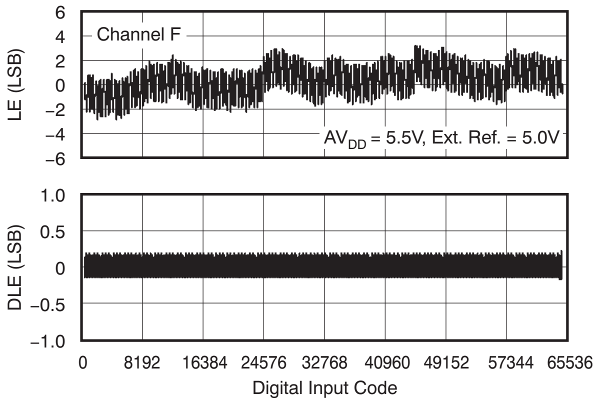


Figure 20. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

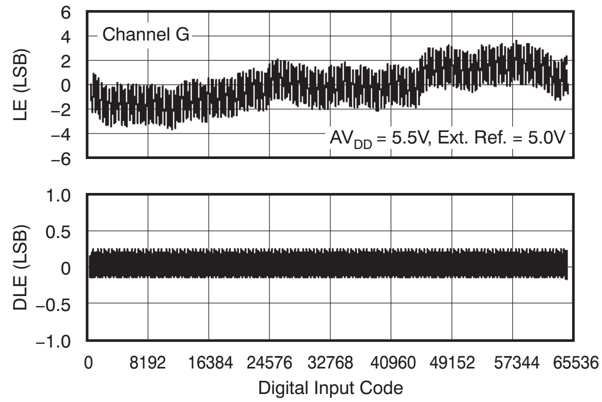


Figure 21. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

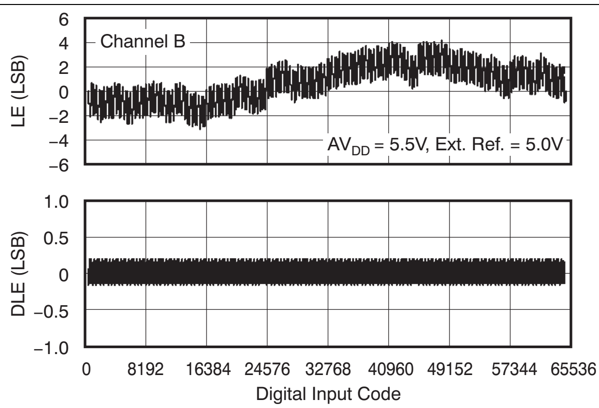


Figure 22. Linearity Error and Differential Linearity Error vs Digital Input Code (+125°C)

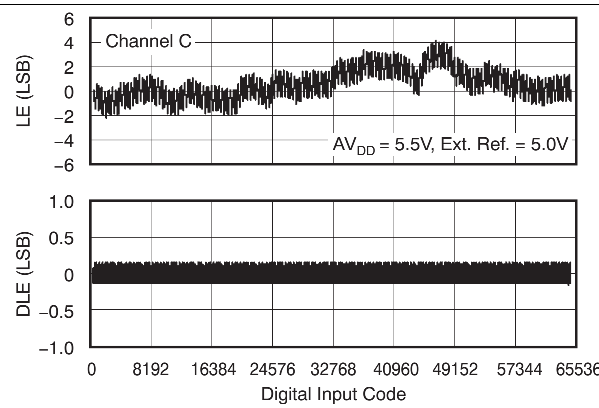


Figure 23. Linearity Error and Differential Linearity Error vs Digital Input Code (+125°C)

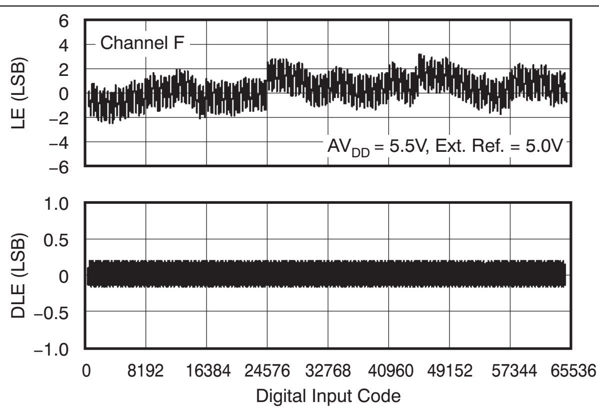


Figure 24. Linearity Error and Differential Linearity Error vs Digital Input Code (+125°C)

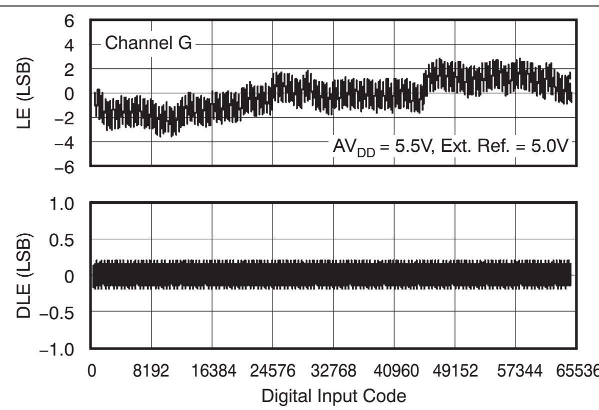


Figure 25. Linearity Error and Differential Linearity Error vs Digital Input Code (+125°C)

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

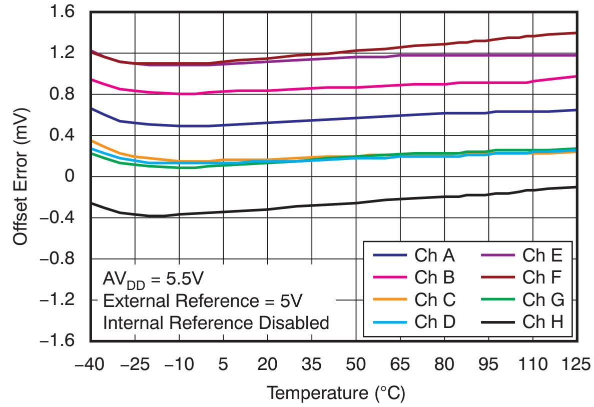


Figure 26. Offset Error vs Temperature

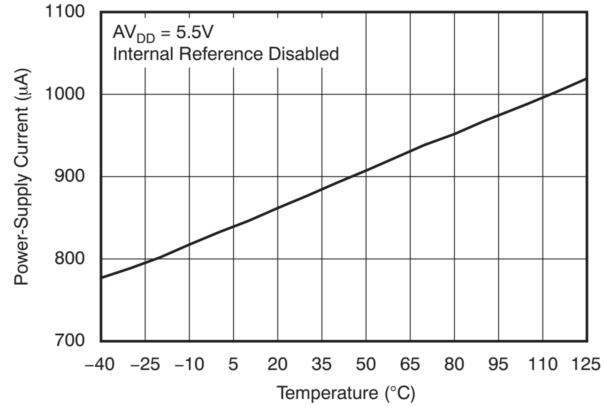


Figure 27. Power-Supply Current vs Temperature

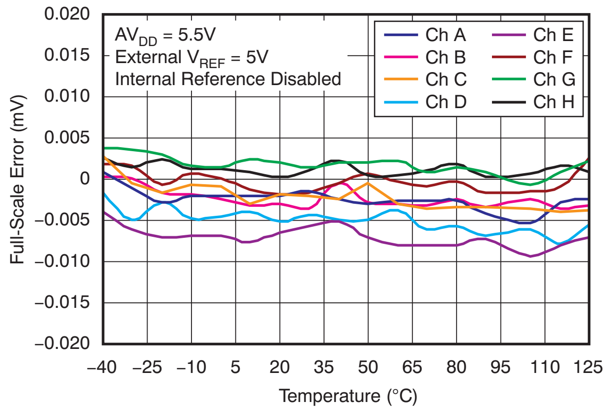


Figure 28. Full-Scale Error vs Temperature

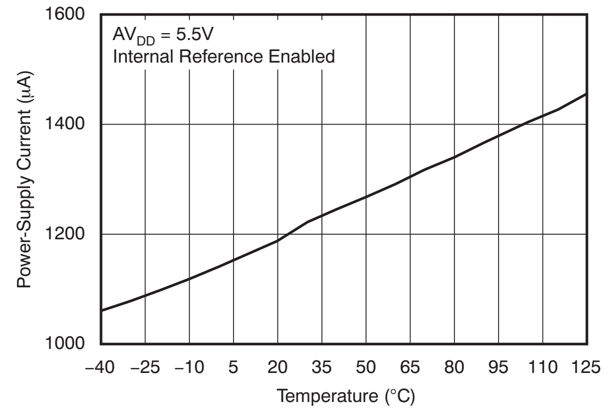


Figure 29. Power-Supply Current vs Temperature

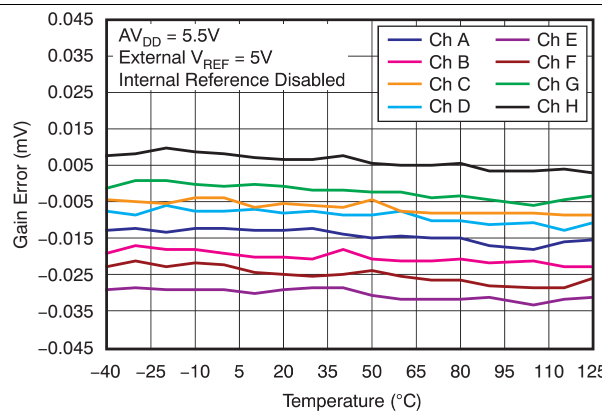


Figure 30. Gain Error vs Temperature

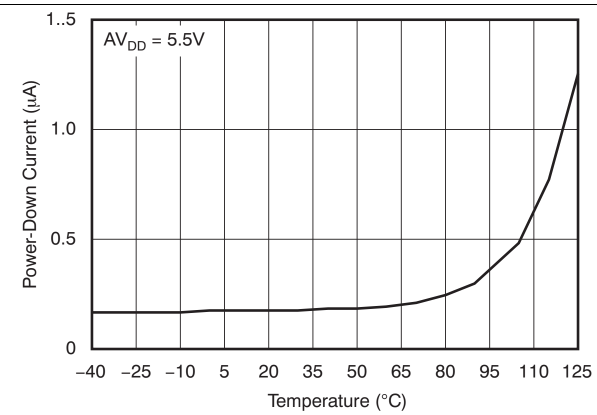


Figure 31. Power-Down Current vs Temperature

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

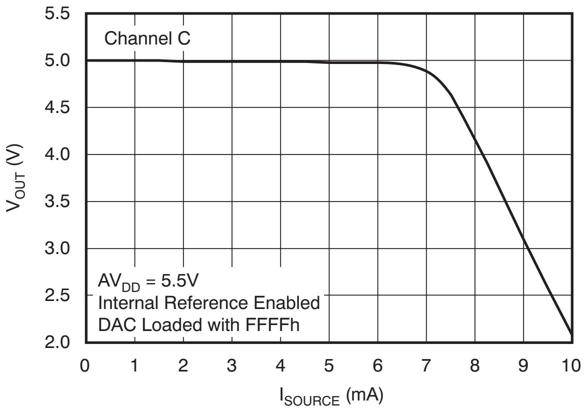


Figure 32. Source Current at Positive Rail (Grades C and D)

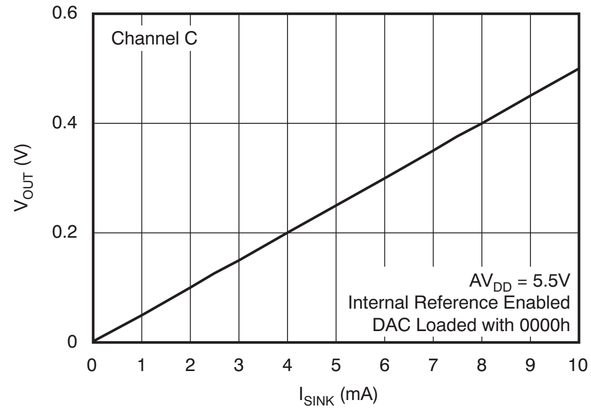


Figure 33. Sink Current at Negative Rail (All Grades)

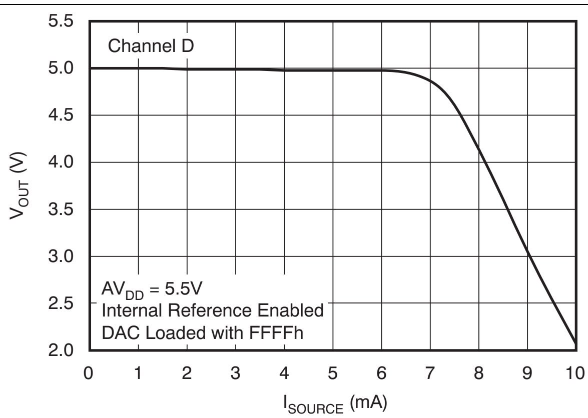


Figure 34. Source Current at Positive Rail (Grades C and D)

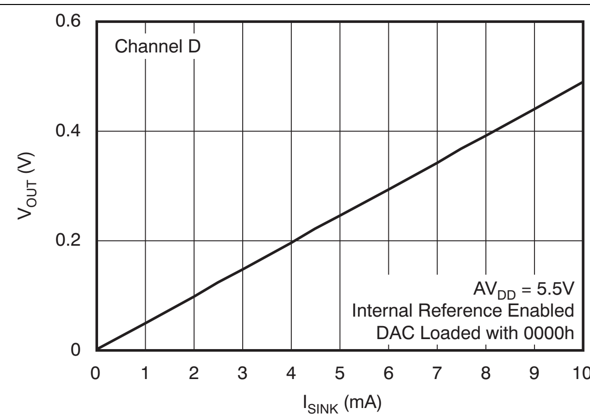


Figure 35. Sink Current at Negative Rail (All Grades)

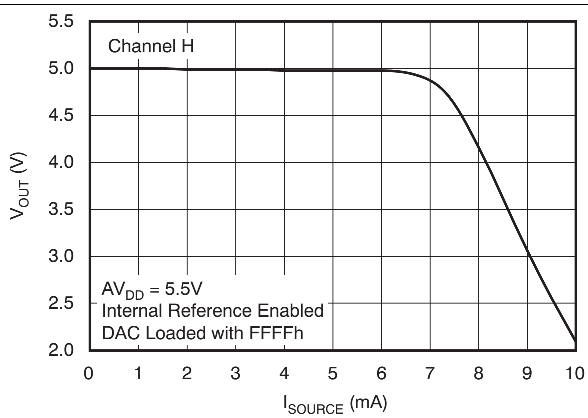


Figure 36. Source Current at Positive Rail (Grades C and D)

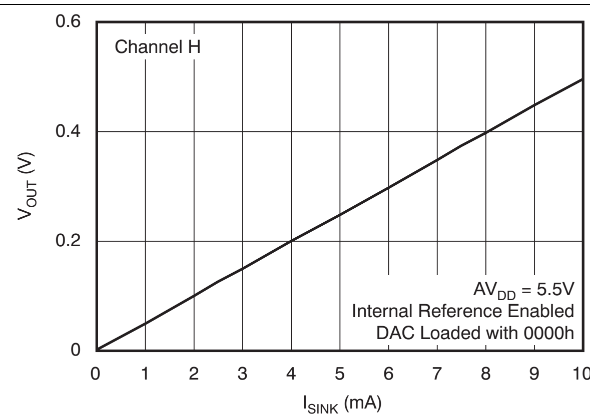


Figure 37. Sink Current at Negative Rail (All Grades)

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

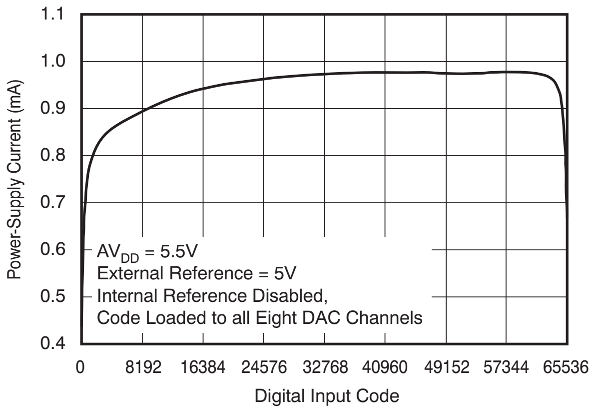


Figure 38. Power-Supply Current vs Digital Input Code

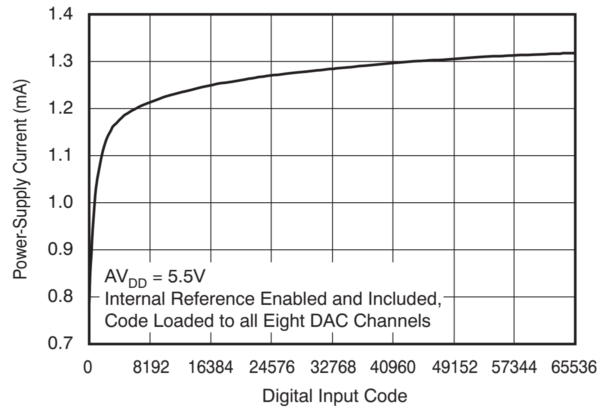


Figure 39. Power-Supply Current vs Digital Input Code

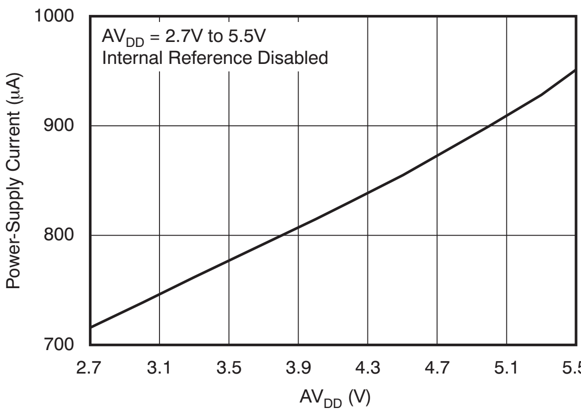


Figure 40. Power-Supply Current vs Power-Supply Voltage

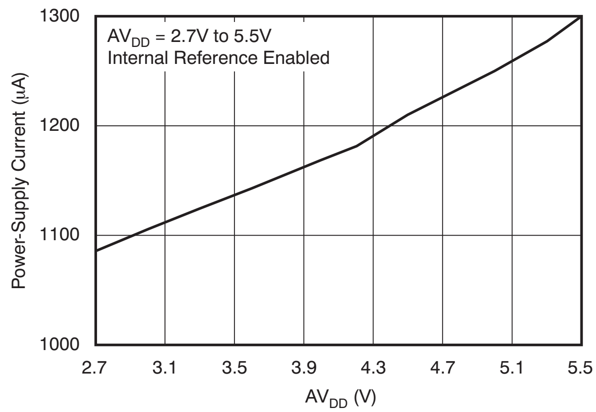


Figure 41. Power-Supply Current vs Power-Supply Voltage

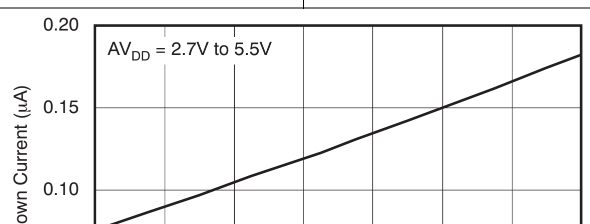


Figure 42. Power-Down Current vs Power-Supply Voltage

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

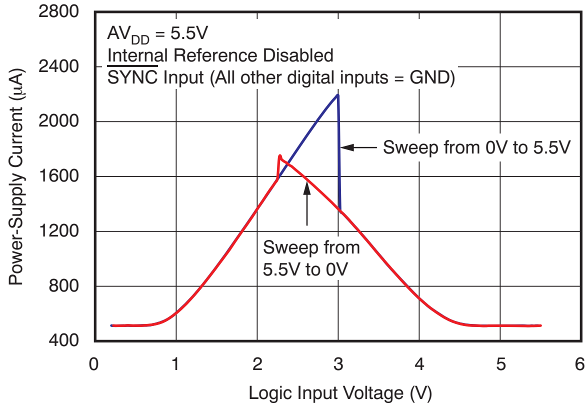


Figure 43. Power-Supply Current vs Logic Input Voltage

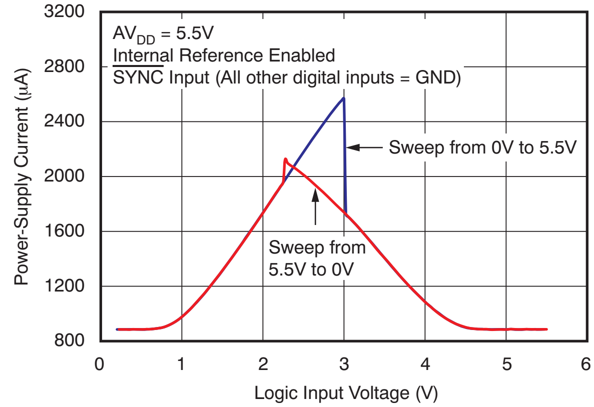


Figure 44. Power-Supply Current vs Logic Input Voltage

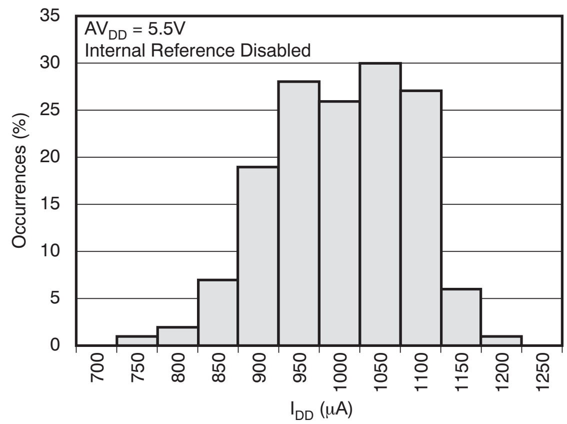


Figure 45. Power-Supply Current Histogram

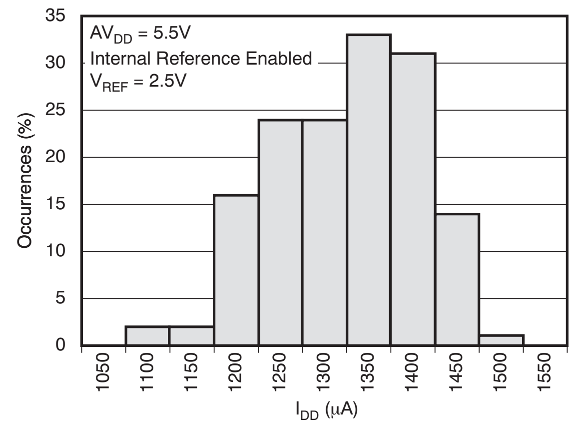


Figure 46. Power-Supply Current Histogram

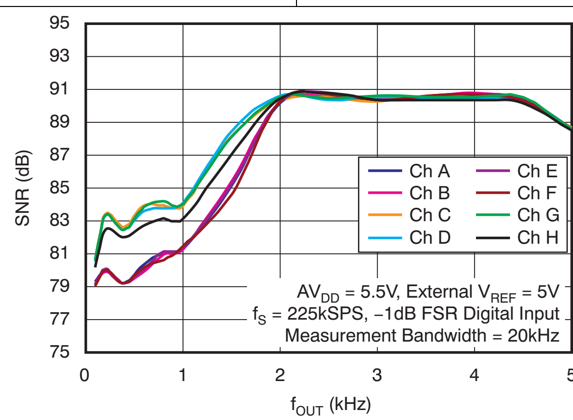


Figure 47. Signal-to-Noise Ratio vs Output Frequency

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

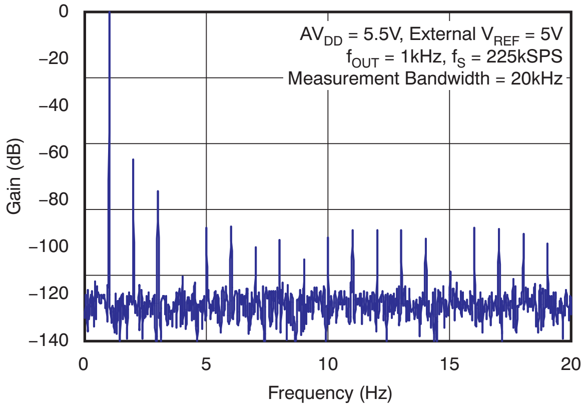


Figure 48. Power Spectral Density

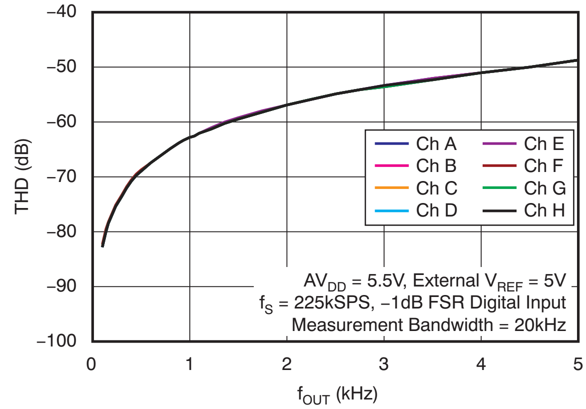


Figure 49. Second Harmonic Distortion vs Output Frequency

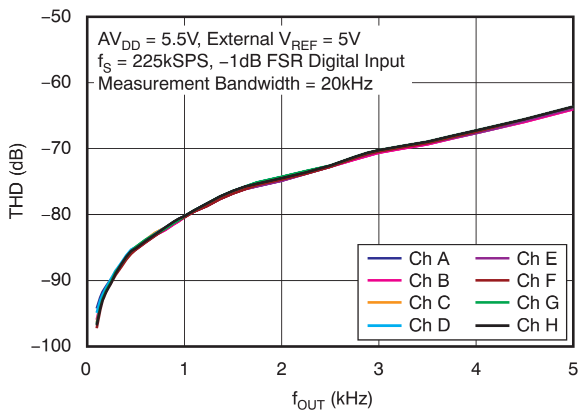


Figure 50. Third Harmonic Distortion vs Output Frequency

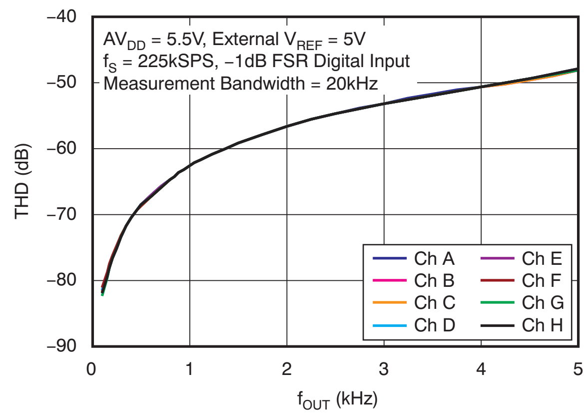


Figure 51. Total Harmonic Distortion vs Output Frequency

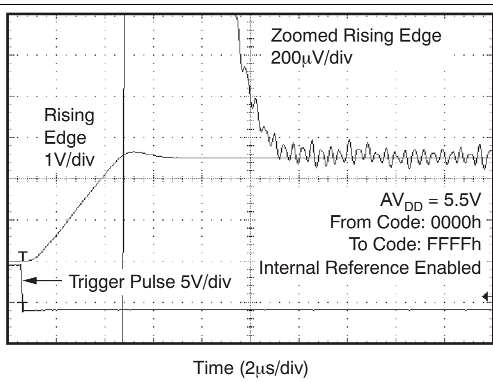


Figure 52. Full-Scale Settling Time: 5-V Rising Edge

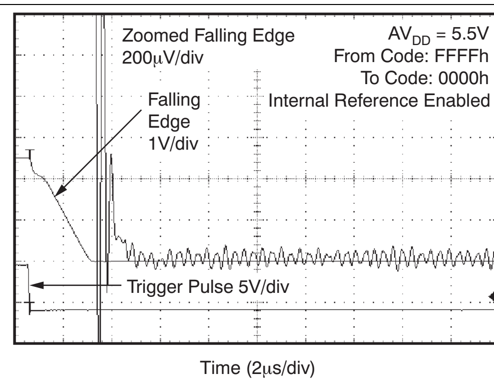


Figure 53. Full-Scale Settling Time: 5-V Falling Edge

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

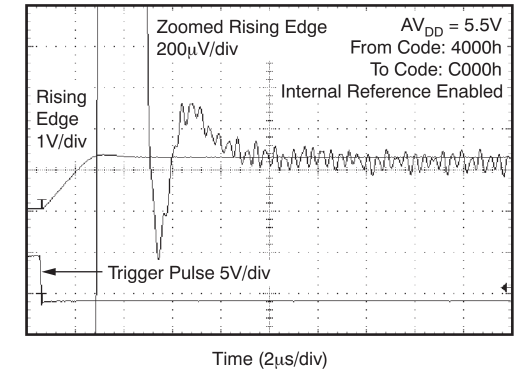


Figure 54. Half-Scale Settling Time: 5-V Rising Edge

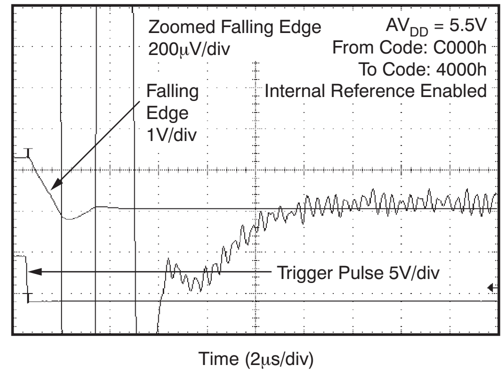


Figure 55. Half-Scale Settling Time: 5-V Falling Edge

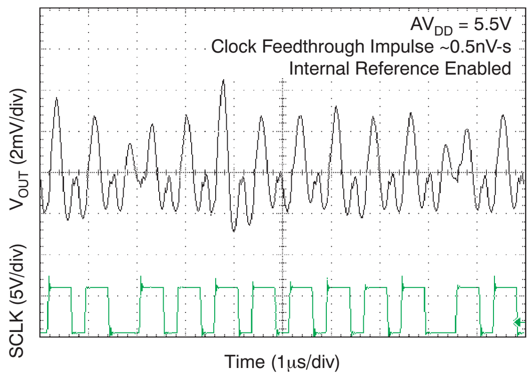


Figure 56. Clock Feedthrough 2 Mhz, Midscale

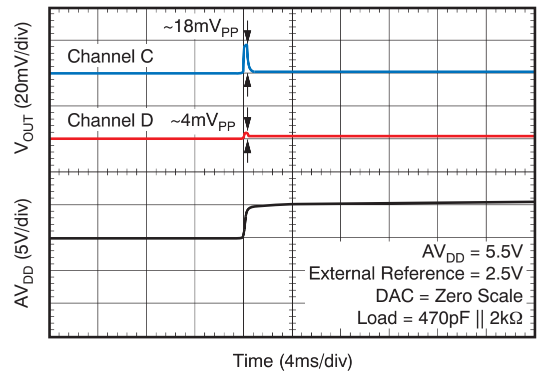


Figure 57. Power-On Glitch Reset to Zero Scale

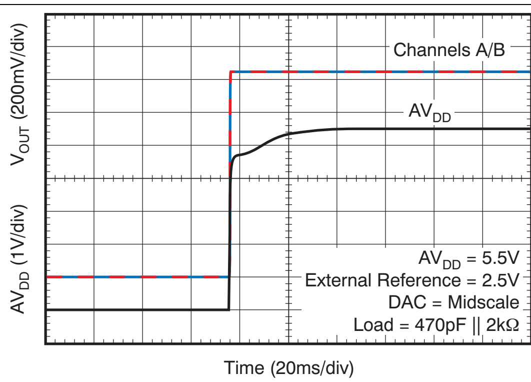


Figure 58. Power-On Glitch Reset To Midscale

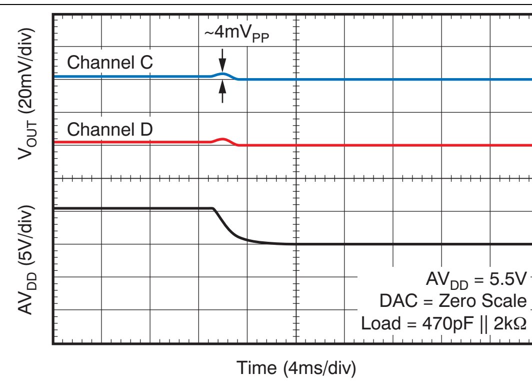


Figure 59. Power-Off Glitch

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.

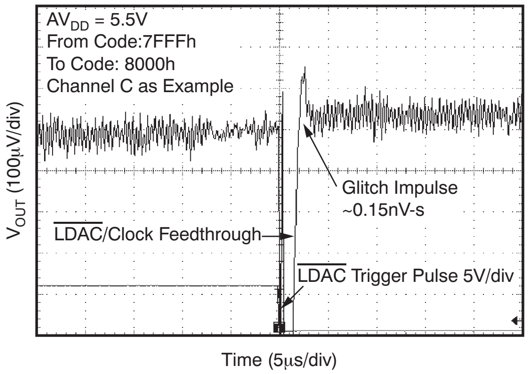


Figure 60. Glitch Energy: 5 V, 1-LSB Step, Rising Edge

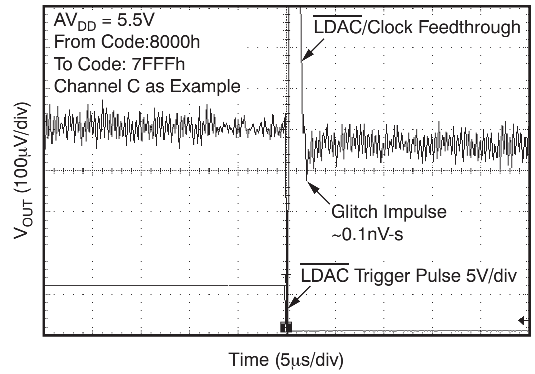


Figure 61. Glitch Energy: 5 V, 1-LSB Step, Falling Edge

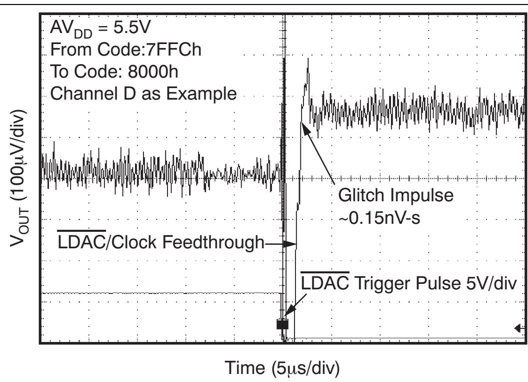


Figure 62. Glitch Energy: 5 V, 4-LSB Step, Rising Edge

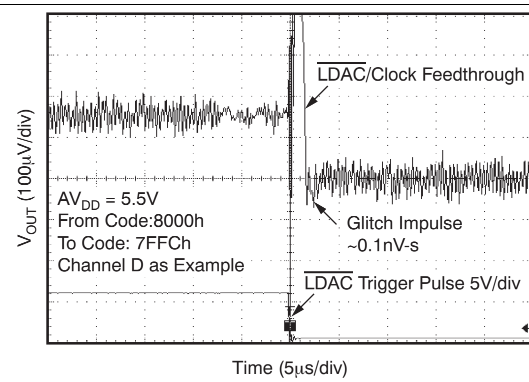


Figure 63. Glitch Energy: 5 V, 4-LSB Step, Falling Edge

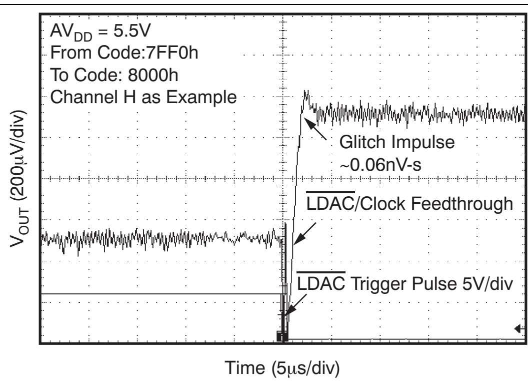


Figure 64. Glitch Energy: 5 V, 16-LSB Step, Rising Edge

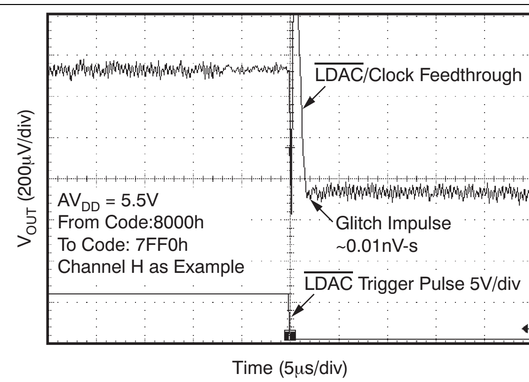
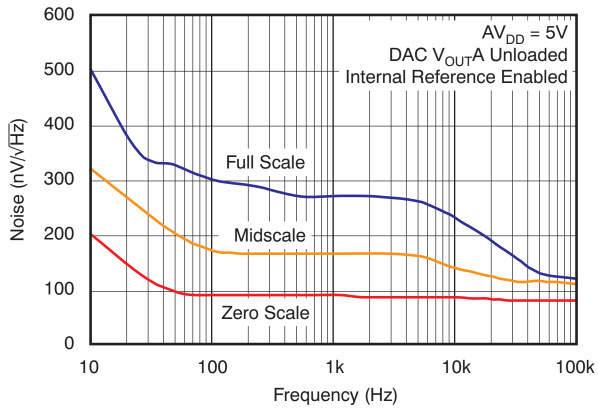


Figure 65. Glitch Energy: 5 V, 16-LSB Step, Falling Edge

Typical Characteristics: DAC at AV_{DD} = 5.5 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, external reference used, DAC output not loaded, and all DAC codes in straight binary data format, unless otherwise noted.



See the *Application Information* section of this data sheet for more details.

Figure 66. DAC Output Noise Density vs Frequency

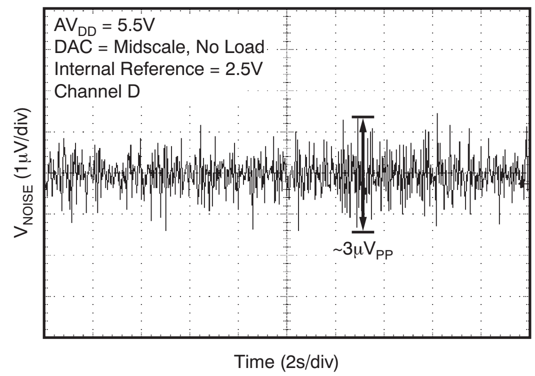


Figure 67. DAC Output Noise 0.1 Hz to 10 Hz

7.6 Typical Characteristics: DAC at AV_{DD} = 3.6 V

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

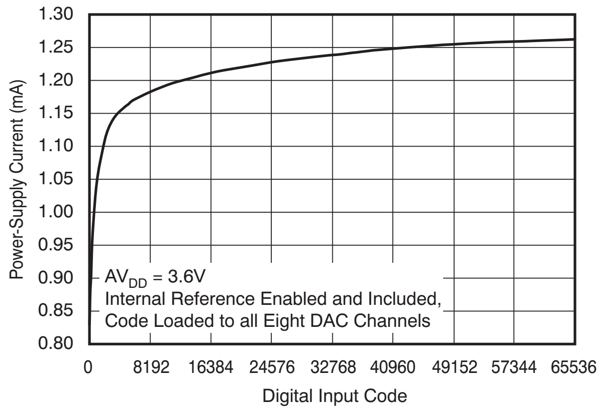


Figure 68. Power-Supply Current vs Digital Input Code

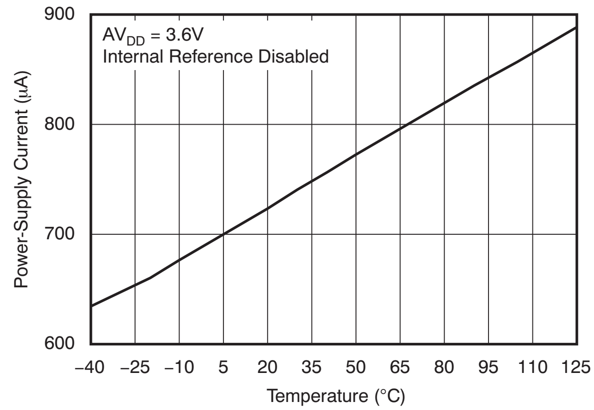


Figure 69. Power-Supply Current vs Temperature

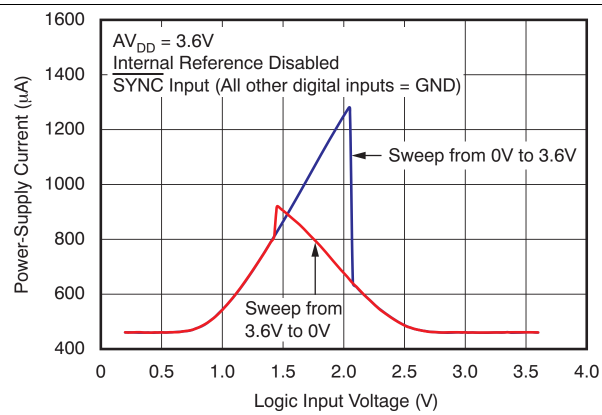


Figure 70. Power-Supply Current vs Logic Input Voltage

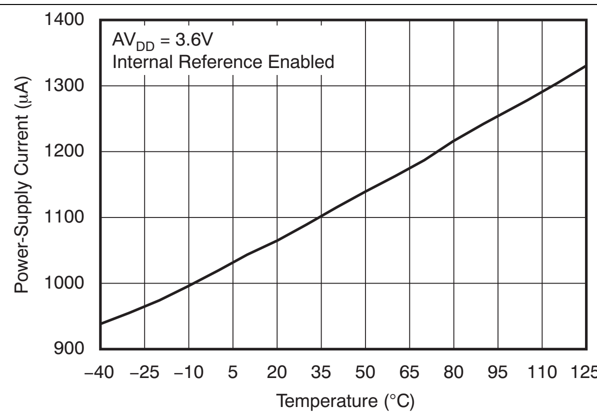


Figure 71. Power-Supply Current vs Temperature

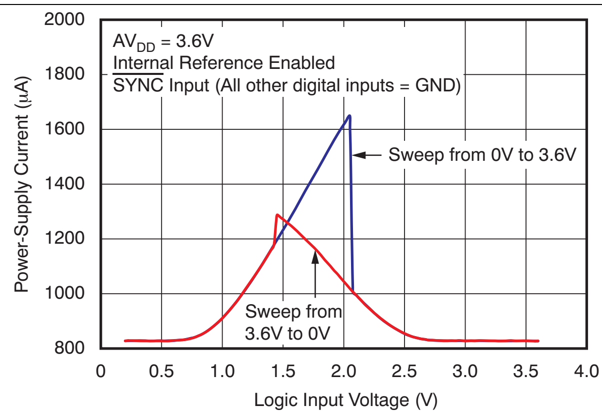


Figure 72. Power-Supply Current vs Logic Input Voltage

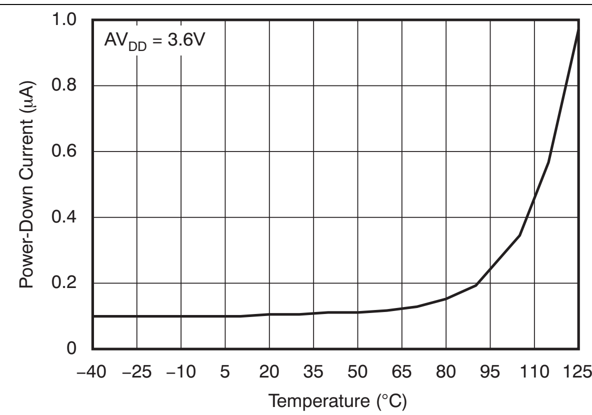


Figure 73. Power-Down Current vs Temperature

Typical Characteristics: DAC at AV_{DD} = 3.6 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

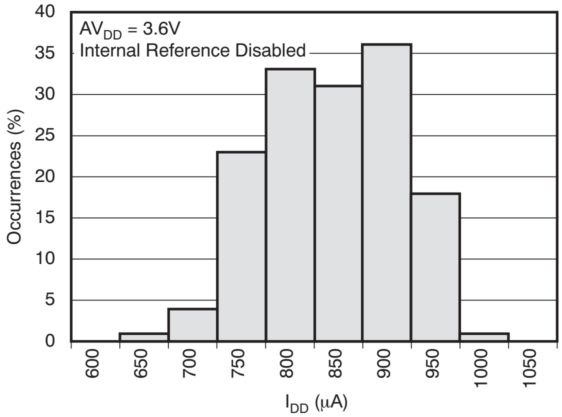


Figure 74. Power-Supply Current Histogram

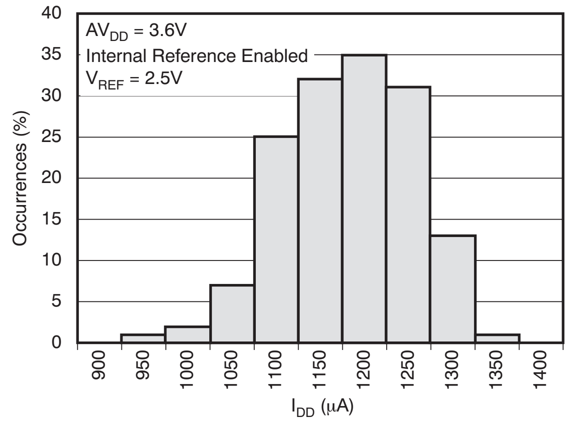


Figure 75. Power-Supply Current Histogram

7.7 Typical Characteristics: DAC at AV_{DD} = 2.7 V

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

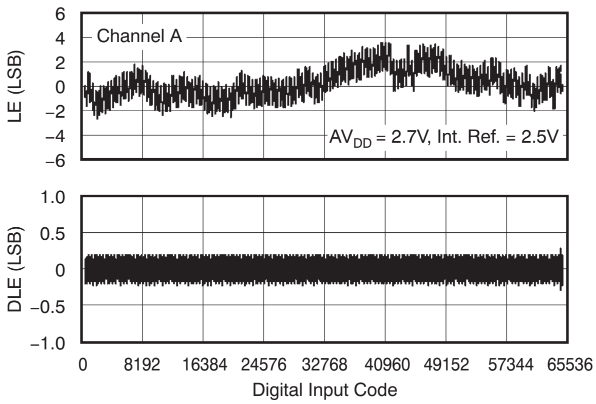


Figure 76. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

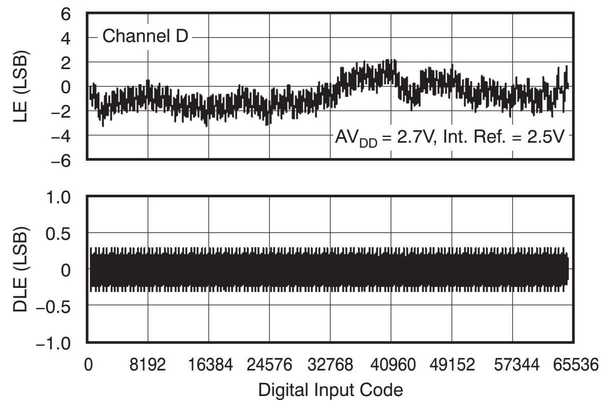


Figure 77. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

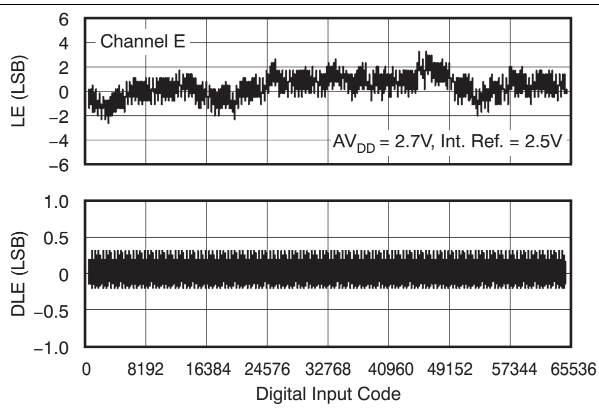


Figure 78. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

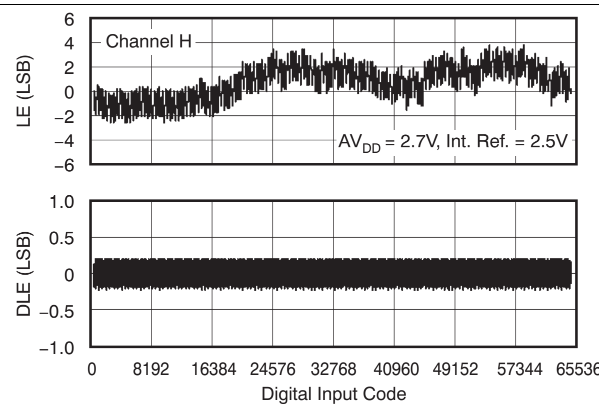


Figure 79. Linearity Error and Differential Linearity Error vs Digital Input Code (–40°C)

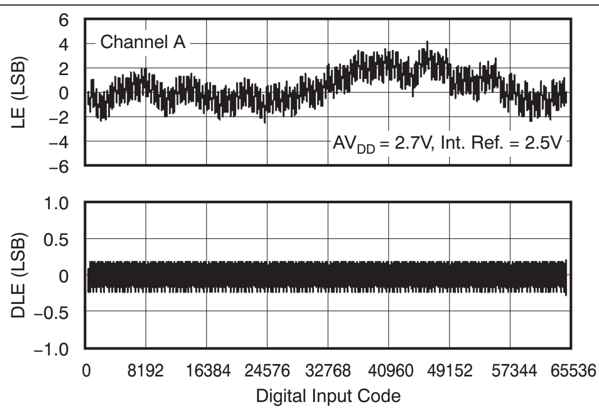


Figure 80. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

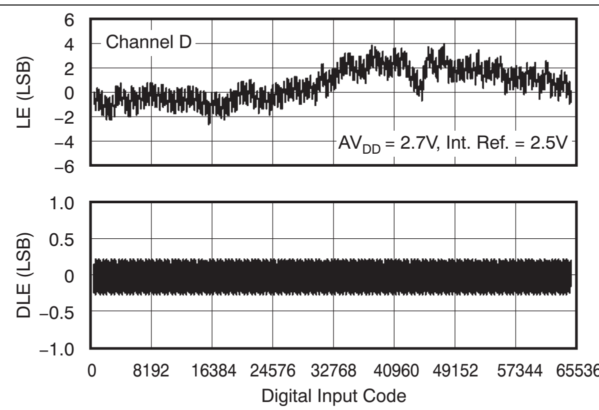


Figure 81. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

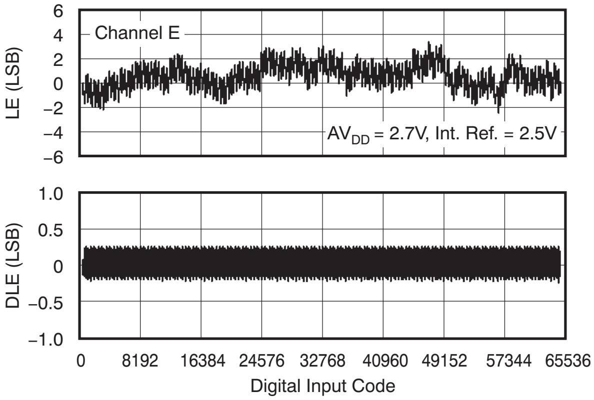


Figure 82. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

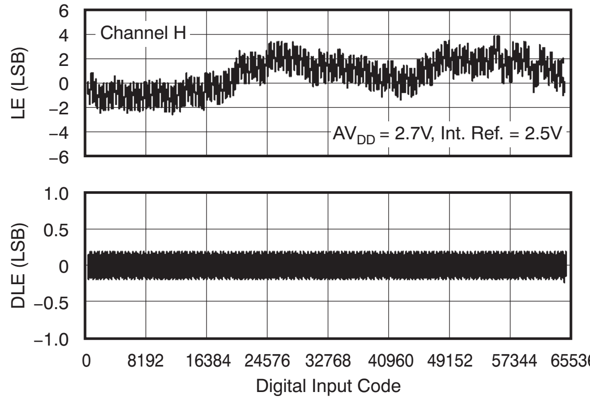


Figure 83. Linearity Error and Differential Linearity Error vs Digital Input Code (+25°C)

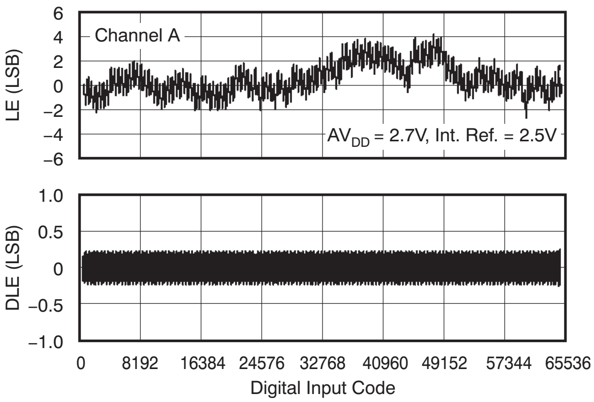


Figure 84. Linearity Error and Differential Linearity Error vs Digital Input Code (+105°C)

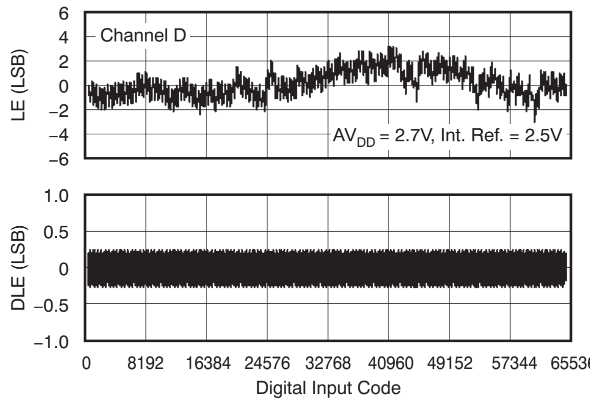


Figure 85. Linearity Error and Differential Linearity Error vs Digital Input Code (+105°C)

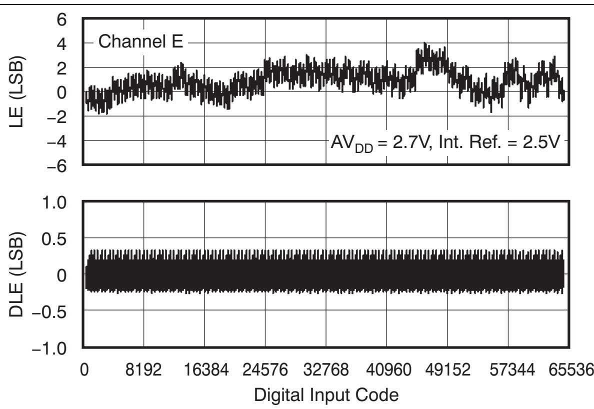


Figure 86. Linearity Error and Differential Linearity Error vs Digital Input Code (+105°C)

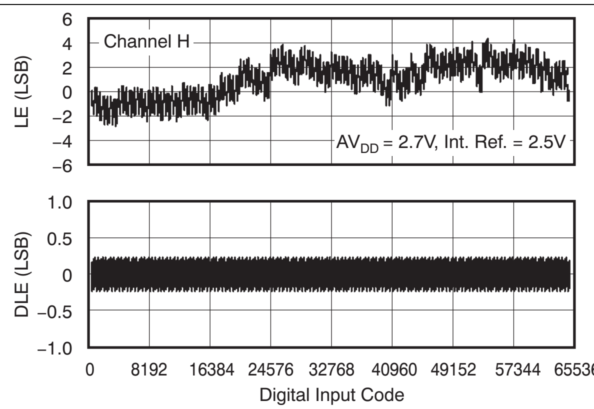


Figure 87. Linearity Error and Differential Linearity Error vs Digital Input Code (+105°C)

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

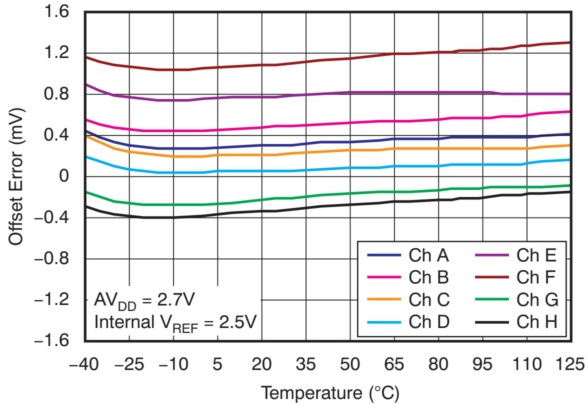


Figure 88. Offset Error vs Temperature

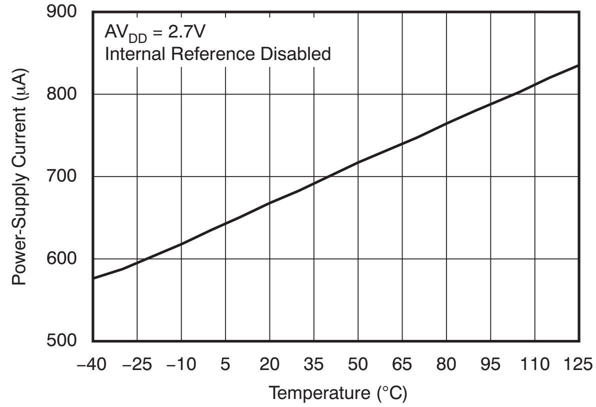


Figure 89. Power-Supply Current vs Temperature

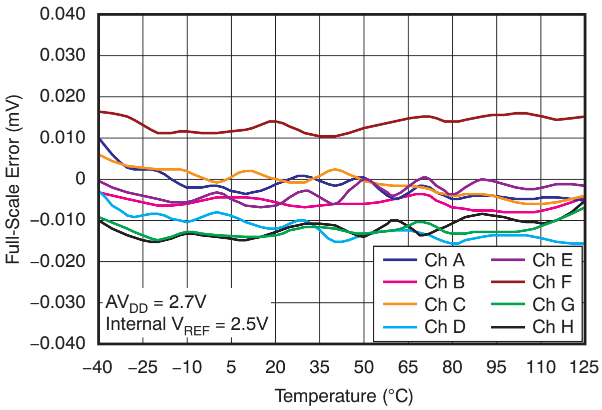


Figure 90. Full-Scale Error vs Temperature

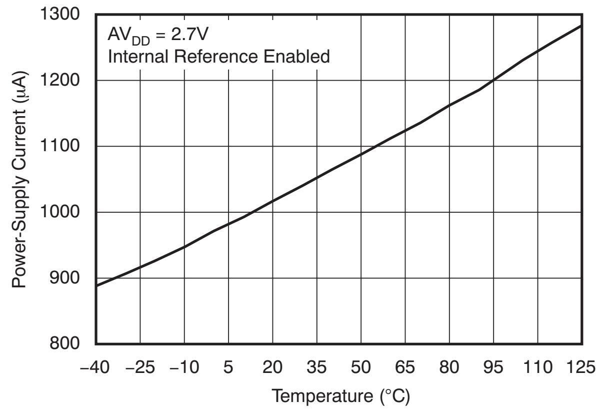


Figure 91. Power-Supply Current vs Temperature

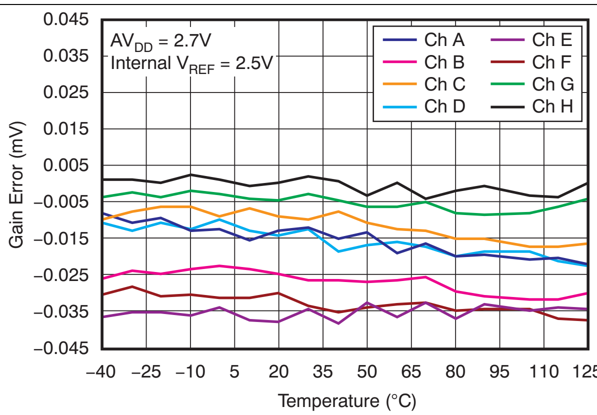


Figure 92. Gain Error vs Temperature

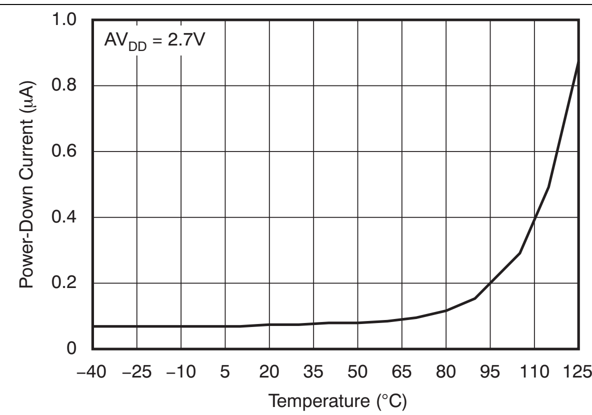


Figure 93. Power-Down Current vs Temperature

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

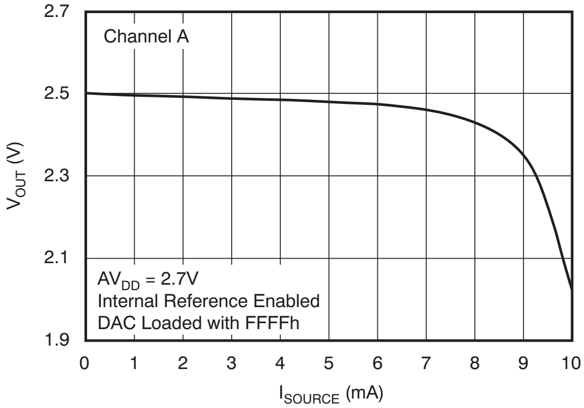


Figure 94. Source Current at Positive Rail (Grades A and B)

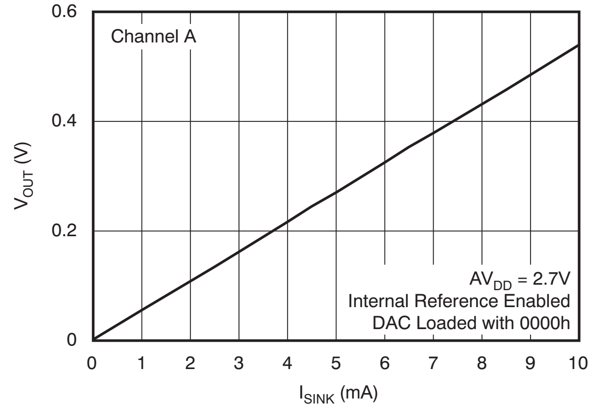


Figure 95. Sink Current at Negative Rail (All Grades)

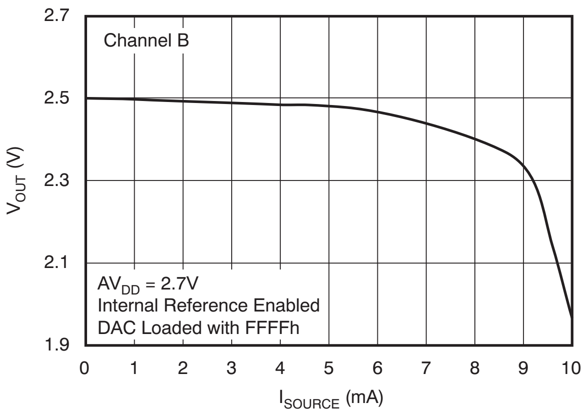


Figure 96. Source Current at Positive Rail (Grades A and B)

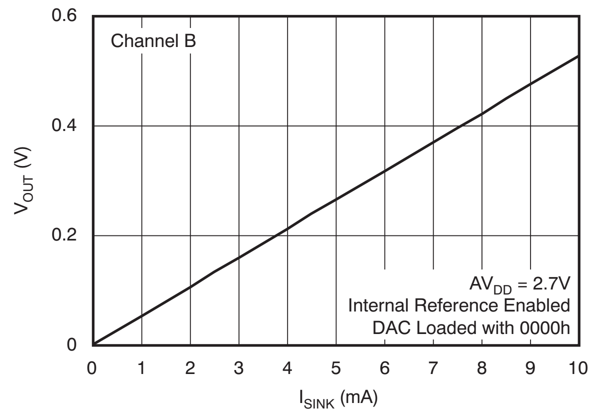


Figure 97. Sink Current at Negative Rail (All Grades)

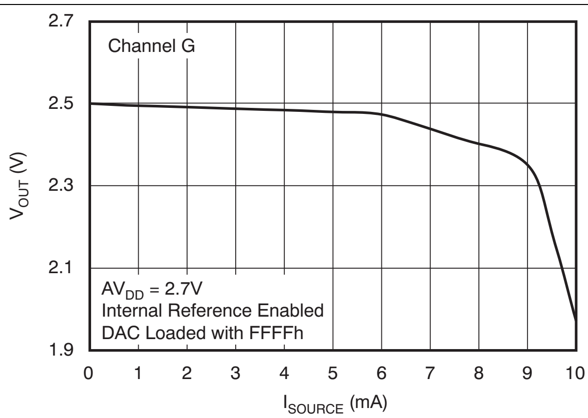


Figure 98. Source Current at Positive Rail (Grades A and B

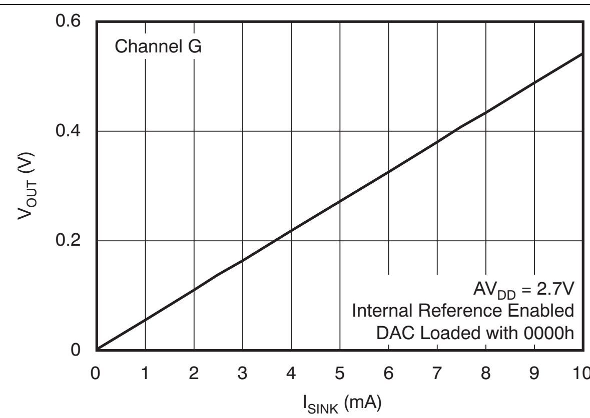


Figure 99. Sink Current at Negative Rail (All Grades)

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

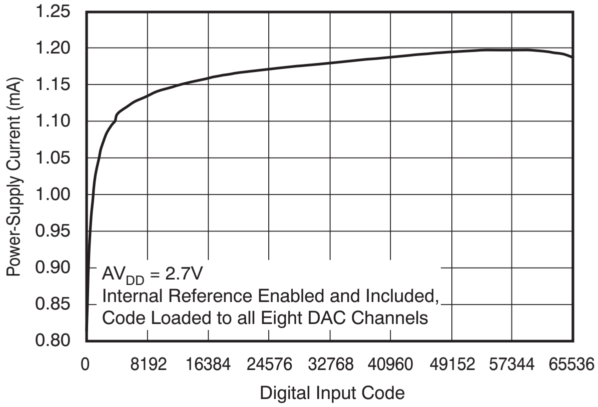


Figure 100. Power-Supply Current Vs Digital Input Code

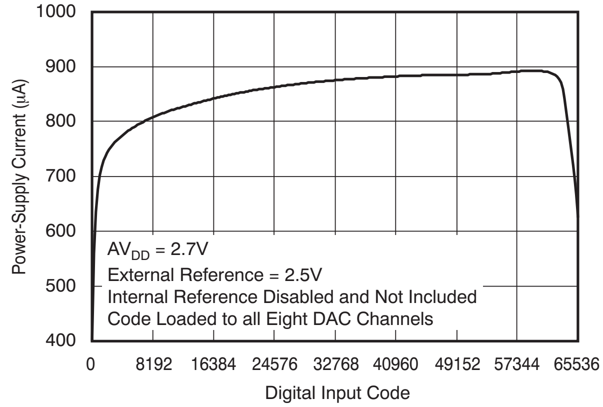


Figure 101. Power-Supply Current vs Digital Input Code

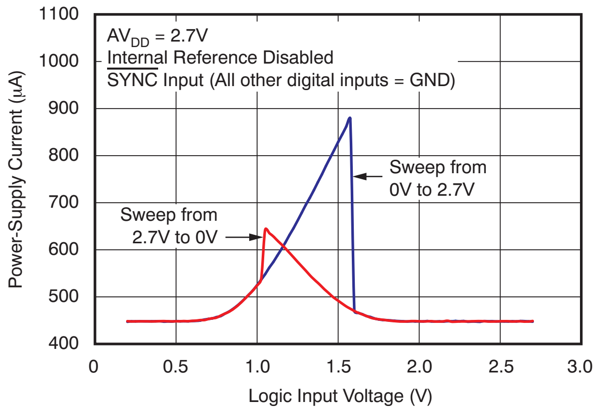


Figure 102. Power-Supply Current vs Logic Input Voltage

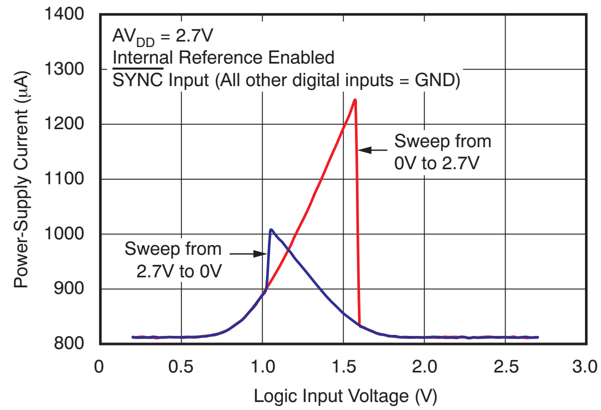


Figure 103. Power-Supply Current vs Logic Input Voltage

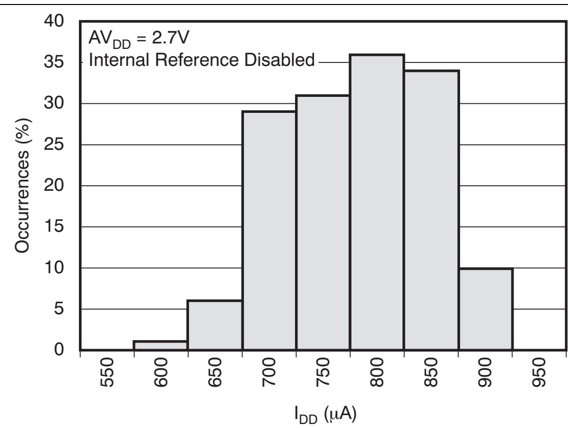


Figure 104. Power-Supply Current Histogram

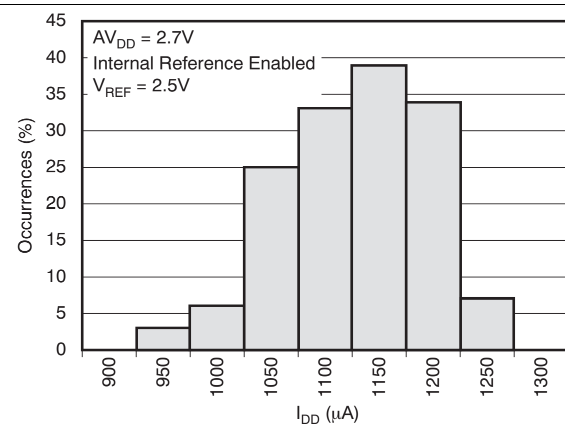


Figure 105. Power-Supply Current Histogram

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

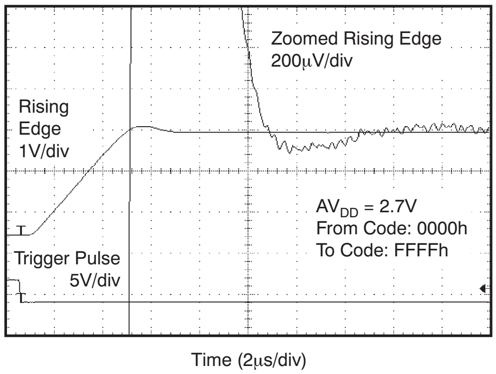


Figure 106. Full-Scale Settling Time: 2.7-V Rising Edge

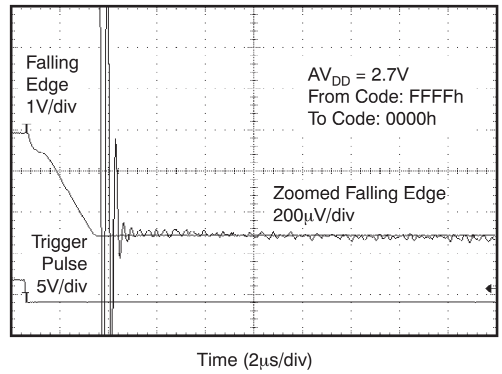


Figure 107. Full-Scale Settling Time: 2.7-V Falling Edge

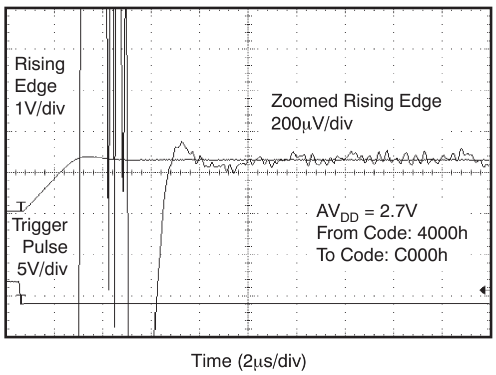


Figure 108. Half-Scale Settling Time: 2.7-V Rising Edge

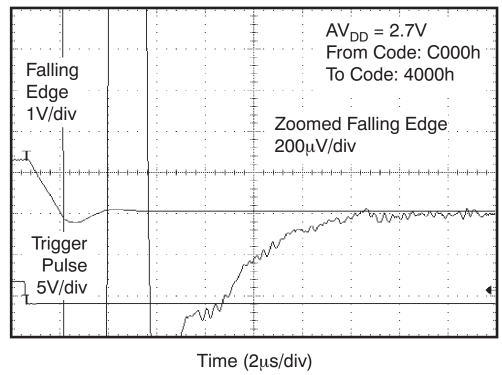


Figure 109. Half-Scale Settling Time: 2.7-V Falling Edge

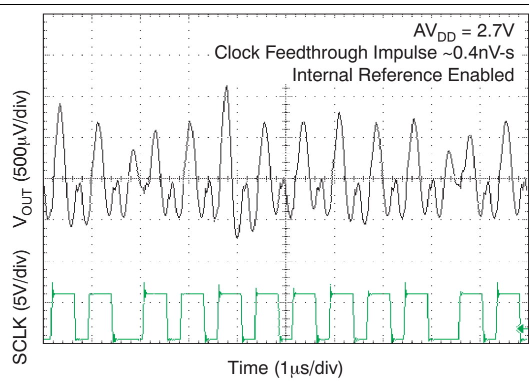


Figure 110. Clock Feedthrough 2.7 V, 2 Mhz, Midscale

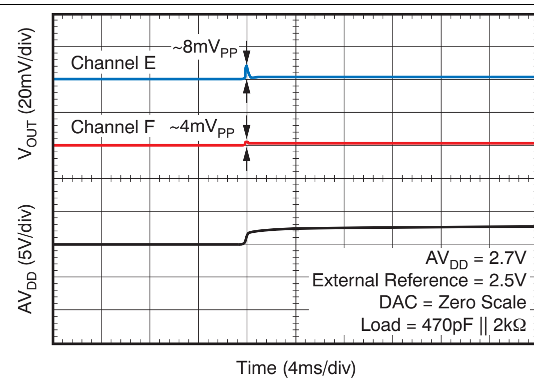


Figure 111. Power-On Glitch Reset to Zero Scale

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

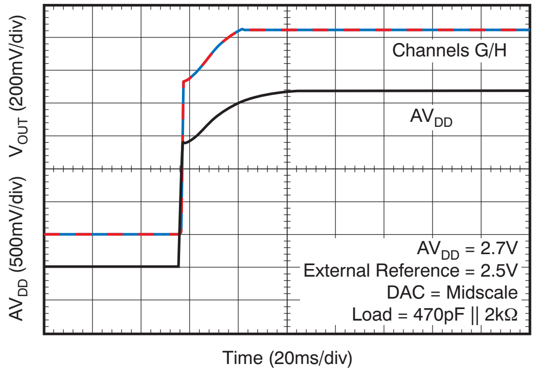


Figure 112. Power-On Glitch Reset to Midscale

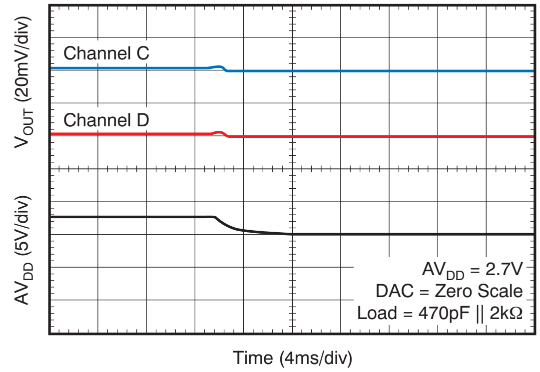


Figure 113. Power-Off Glitch

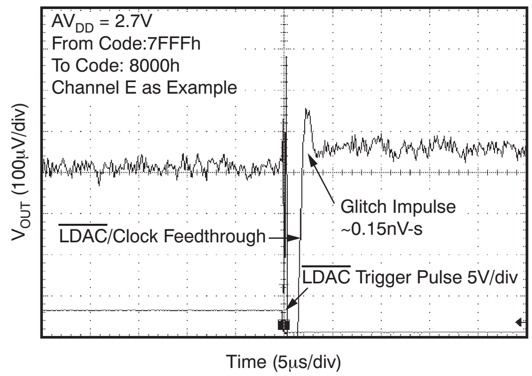


Figure 114. Glitch Energy: 2.7 V, 1-LSB Step, Rising Edge

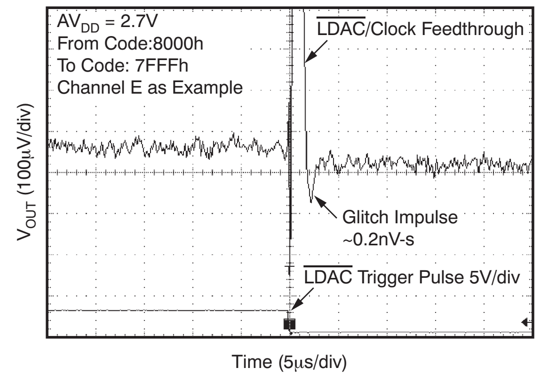


Figure 115. Glitch Energy: 2.7 V, 1-LSB Step, Falling Edge

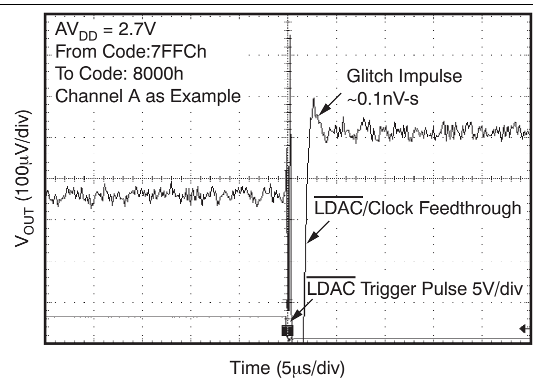


Figure 116. Glitch Energy: 2.7 V, 4-LSB Step, Rising Edge

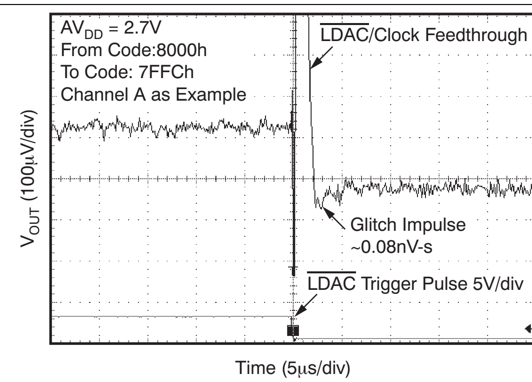


Figure 117. Glitch Energy: 2.7 V, 4-LSB Step, Falling Edge

Typical Characteristics: DAC at AV_{DD} = 2.7 V (continued)

Channel-specific information provided as examples. At T_A = +25°C, internal reference used, and DAC output not loaded, all DAC codes in straight binary data format, unless otherwise noted

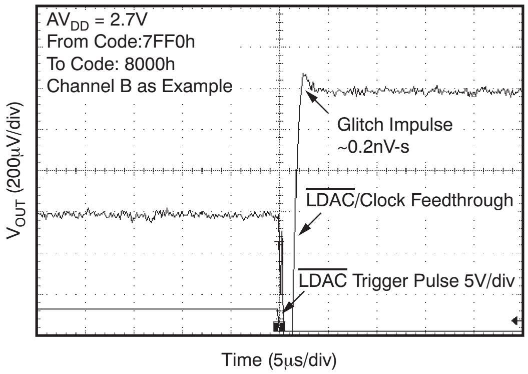


Figure 118. Glitch Energy: 2.7 V, 16-LSB Step, Rising Edge

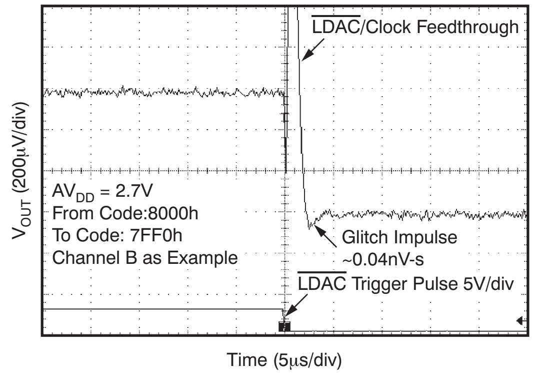
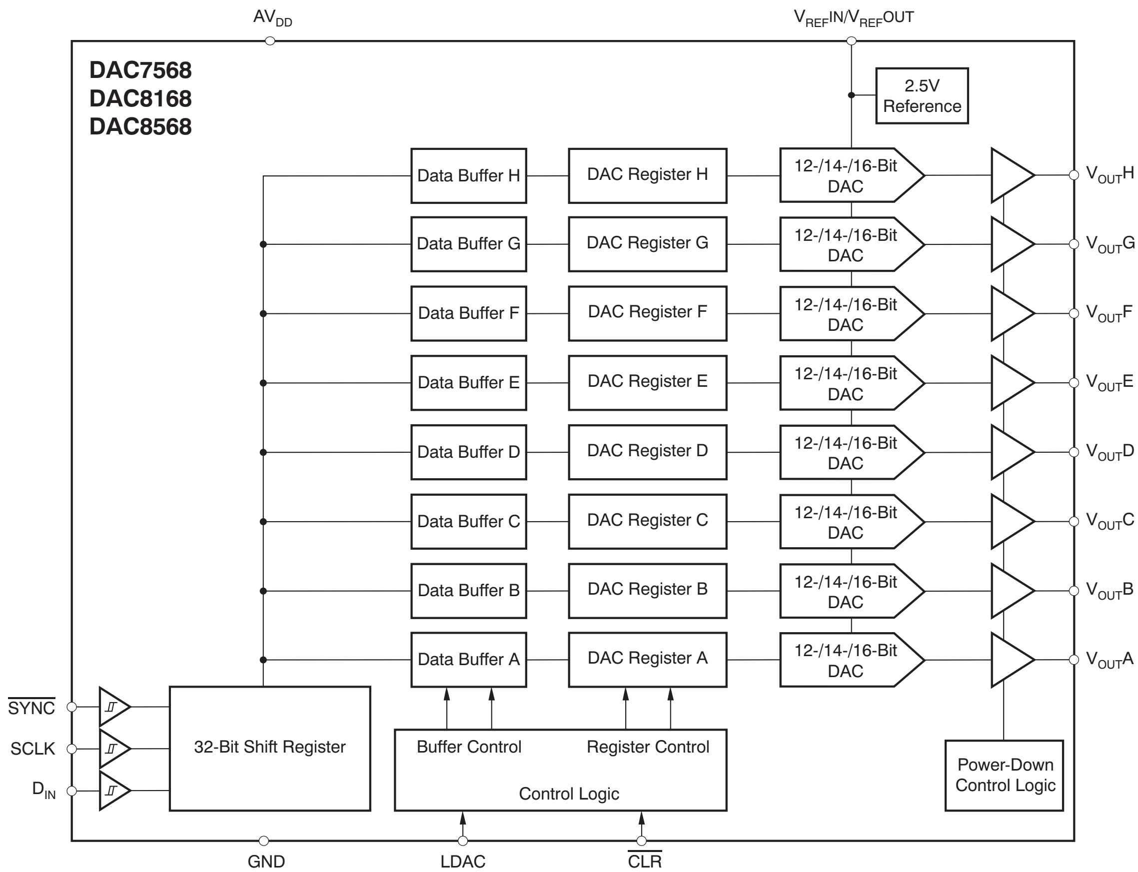


Figure 119. Glitch Energy: 2.7 V, 16-LSB Step, Falling Edge

8 Detailed Description

8.1 Functional Block Diagram



8.2 Feature Description

8.2.1 Digital-to-Analog Converter (DAC)

The DAC7568, DAC8168, and DAC8568 architecture consists of eight string DACs each followed by an output buffer amplifier. The devices include an internal 2.5V reference with 2ppm/°C temperature drift performance, and offer either 5V or 2.5V full scale output voltage. Figure 120 shows a principal block diagram of the DAC architecture.

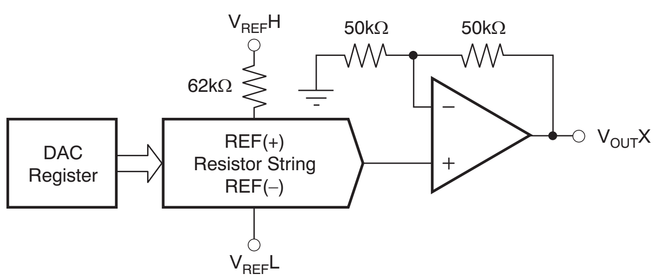


Figure 120. Device Architecture

The input coding to the DAC7568, DAC8168, and DAC8568 is straight binary, so the ideal output voltage is given by Equation 1:

Feature Description (continued)

$$V_{OUT} = \left[\frac{D_{IN}}{2^n} \right] \times V_{REF} \times \text{Gain} \quad (1)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 4095 for DAC7568 (12 bit), 0 to 16,383 for DAC8168 (14 bit), and 0 to 65535 for DAC8568 (16 bit).

n = resolution in bits; either 12 (DAC7568), 14 (DAC8168) or 16 (DAC8568)

Gain = 1 for A/B grades or 2 for C/D grades.

8.2.2 Resistor String

The resistor string section is shown in Figure 121. It is simply a string of resistors, each of value *R*. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier by closing one of the switches connecting the string to the amplifier. It is monotonic because it is a string of resistors.

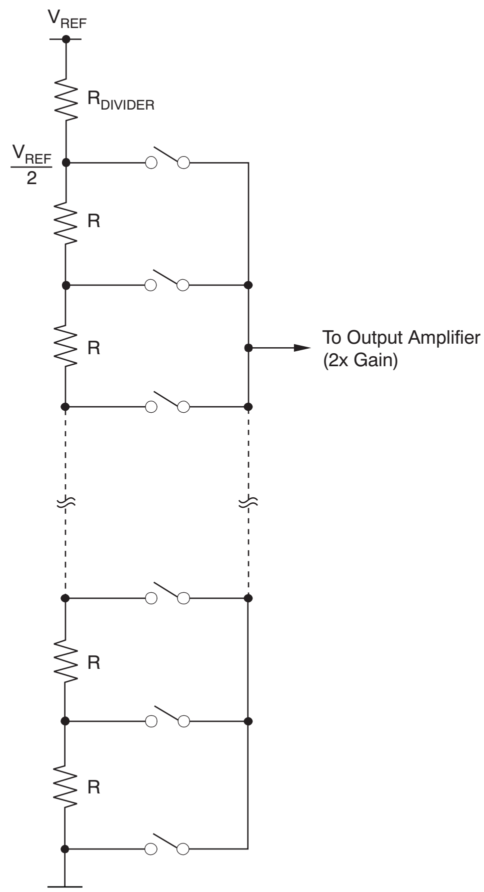


Figure 121. Resistor String

8.2.3 Output Amplifier

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, giving a maximum output range of 0V to AV_{DD}. It is capable of driving a load of 2kΩ in parallel with 3000pF to GND. The source and sink capabilities of the output amplifier can be seen in the *Typical Characteristics*. The typical slew rate is 0.75V/µs, with a typical full-scale settling time of 5µs with the output unloaded.

Feature Description (continued)

8.2.4 Internal Reference

The DAC7568, DAC8168, and DAC8568 include a 2.5V internal reference that is disabled by default. The internal reference is externally available at the $V_{REF}IN/V_{REF}OUT$ pin. A minimum 100nF capacitor is recommended between the reference output and GND for noise filtering.

The internal reference of the DAC7568, DAC8168, and DAC8568 is a bipolar, transistor-based, precision bandgap voltage reference. Figure 122 shows the basic bandgap topology. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base-emitter voltages (V_{BE1} – V_{BE2}) has a positive temperature coefficient and is forced across resistor R_1. This voltage is gained up and added to the base-emitter voltage of Q_2, which has a negative temperature coefficient. The resulting output voltage is virtually independent of temperature. The short-circuit current is limited by design to approximately 100mA.

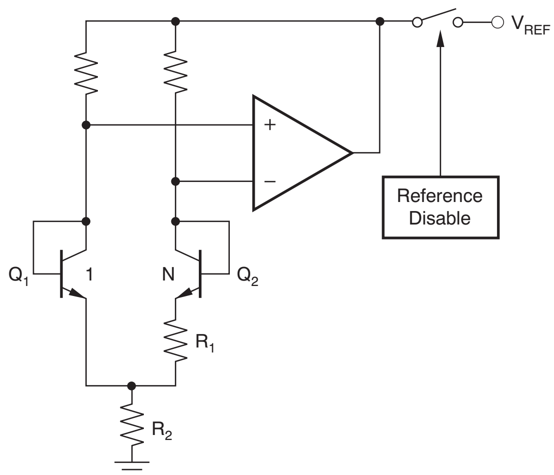


Figure 122. Bandgap Reference Simplified Schematic

Refer to *Enable/Disable Internal Reference* section for information on enabling and disabling the internal reference.

8.2.5 Serial Interface

The DAC7568, DAC8168, and DAC8568 have a 3-wire serial interface ($\overline{SYNC}$, SCLK, and D_{IN}; see the *Pin Configurations*) compatible with SPI, QSPI, and Microwire interface standards, as well as most DSPs. See the Serial Write Operation timing diagram (Figure 1) for an example of a typical write sequence.

The DAC7568, DAC8168, and DAC8568 input shift register is 32-bits wide, consisting of four prefix bits (DB31 to DB28), four control bits (DB27 to DB24), 16 data bits (DB23 to DB4), and four feature bits. The 16 data bits comprise the 16-, 14-, or 12-bit input code. When writing to the DAC register (data transfer), bits DB0 to DB3 (for 16-bit operation), DB0 to DB5 (for 14-bit operation), and DB0 to DB7 (for 12-bit operation) are ignored by the DAC and should be treated as *don't care* bits (see Table 1 to Table 3). All 32 bits of data are loaded into the DAC under the control of the serial clock input, SCLK.

DB31 (MSB) is the first bit that is loaded into the DAC shift register and must be always set to '0'. It is followed by the rest of the 32-bit word pattern, left-aligned. This configuration means that the first 32 bits of data are latched into the shift register and any further clocking of data is ignored. When the DAC registers are being written to, the DAC7568, DAC8168, and DAC8568 receive all 32 bits of data, ignore DB31 to DB28, and decode the second set of four bits (DB27 to DB24) in order to determine the DAC operating/control mode (see). Bits DB23 to DB20 are used to address selected DAC channels. The next 16/14/12 bits of data that follow are decoded by the DAC to determine the equivalent analog output. The last four data bits (DB0 to DB3 for DAC8568), last data six bits (DB0 to DB5 for DAC8168), or last eight data bits (DB0 to DB7 for DAC7568) are ignored in this case. For more details on these and other commands (such as write to LDAC register, power down DACs, etc.), see Table 4.

Feature Description (continued)

The data format is straight binary with all '0's corresponding to 0V output and all '1's corresponding to full-scale output. For all documentation purposes, the data format and representation used here is a true 16-bit pattern (that is, FFFFh for data word for full-scale) that the DAC7568, DAC8168, and DAC8568 require.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the D_{IN} line are clocked into the 32-bit shift register on each falling edge of SCLK. The serial clock frequency can be as high as 50MHz, making the DAC7568, DAC8168, and DAC8568 compatible with high-speed DSPs. On the 32nd falling edge of the serial clock, the last data bit is clocked into the shift register and the shift register locks. Further clocking does not change the shift register data. After receiving the 32nd falling clock edge, the DAC7568, DAC8168, and DAC8568 decode the four control bits and four address bits and 16/14/12 data bits to perform the required function, without waiting for a $\overline{SYNC}$ rising edge. A new write sequence starts at the next falling edge of $\overline{SYNC}$. A rising edge of $\overline{SYNC}$ before the 31st-bit sequence is complete resets the SPI interface; no data transfer occurs. After the 32nd falling edge of SCLK is received, the $\overline{SYNC}$ line may be kept low or brought high. In either case, the minimum delay time from the 32nd falling SCLK edge to the next falling $\overline{SYNC}$ edge must be met in order to properly begin the next cycle; see the Serial Write Operation timing diagram (Figure 1). To assure the lowest power consumption of the device, care should be taken that the levels are as close to each rail as possible. Refer to the 5.5V, 3.6V, and 2.7V Typical Characteristics sections for the *Power-Supply Current vs Logic Input Voltage* graphs (Figure 43, Figure 44, Figure 70, Figure 72, Figure 102, and Figure 103).

Feature Description (continued)

8.2.6 Input Shift Register

The input shift register (SR) of the DAC7568, DAC8168, and DAC8568 is 32 bits wide (as shown in Table 1, Table 2, and Table 3, respectively), and consists of four Prefix bits (DB31 to DB28), four control bits (DB27 to DB24), 16 data bits (DB23 to DB4), and four additional feature bits. The 16 data bits comprise the 16-, 14-, or 12-bit input code.

The DAC7568, DAC8168, and DAC8568 support a number of different load commands. The load commands are summarized in Table 4.

Table 1. DAC8568 Data Input Register Format

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------- Data Bits -------------------------------------| | Feature Bits |

Table 2. DAC8168 Data Input Register Format

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	F3	F2	F1	F0

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------- Data Bits -------------------------------| | Feature Bits |

Table 3. DAC7568 Data Input Register Format

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X	F3	F2	F1	F0

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------- Data Bits -------------------------| | Feature Bits |

Table 4. Control Matrix for the DAC7568, DAC8168, and DAC8568

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16**	**D15**	**D14**	**D13-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 16-BIT DAC8568**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D14**	**D13**	**D12**	**D11-D5**	**D4**	**D3**	**D2**	**D1**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 14-BIT DAC8168**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D12**	**D11**	**D10**	**D9-D3**	**D2**	**D1**	**X**	**X**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 12-BIT DAC7568**
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - Not valid; device does not perform to specified conditions
Write to Selected DAC Input Register																								
0	X	0	0	0	0	0	0	0	0	Data										X	X	X	X	Write to input register - DAC Channel A
0	X	0	0	0	0	0	0	0	1	Data										X	X	X	X	Write to input register - DAC Channel B
0	X	0	0	0	0	0	0	1	0	Data										X	X	X	X	Write to input register - DAC Channel C
0	X	0	0	0	0	0	0	1	1	Data										X	X	X	X	Write to input register - DAC Channel D
0	X	0	0	0	0	0	1	0	0	Data										X	X	X	X	Write to input register - DAC Channel E
0	X	0	0	0	0	0	1	0	1	Data										X	X	X	X	Write to input register - DAC Channel F
0	X	0	0	0	0	0	1	1	0	Data										X	X	X	X	Write to input register - DAC Channel G
0	X	0	0	0	0	0	1	1	1	Data										X	X	X	X	Write to input register - DAC Channel H
0	X	0	0	0	0	1	X	X	X	X										X	X	X	X	Invalid code - No DAC channel is updated
0	X	0	0	0	0	1	1	1	1	Data										X	X	X	X	Broadcast mode - Write to all DAC channels
Update Selected DAC Registers																								
0	X	0	0	0	1	0	0	0	0	Data										X	X	X	X	Update DAC register - DAC Channel A
0	X	0	0	0	1	0	0	0	1	Data										X	X	X	X	Update DAC register - DAC Channel B
0	X	0	0	0	1	0	0	1	0	Data										X	X	X	X	Update DAC register - DAC Channel C
0	X	0	0	0	1	0	0	1	1	Data										X	X	X	X	Update DAC register - DAC Channel D
0	X	0	0	0	1	0	1	0	0	Data										X	X	X	X	Update DAC register - DAC Channel E
0	X	0	0	0	1	0	1	0	1	Data										X	X	X	X	Update DAC register - DAC Channel F
0	X	0	0	0	1	0	1	1	0	Data										X	X	X	X	Update DAC register - DAC Channel G
0	X	0	0	0	1	0	1	1	1	Data										X	X	X	X	Update DAC register - DAC Channel H
0	X	0	0	0	1	1	X	X	X	X										X	X	X	X	Invalid code - No DAC channel is updated
0	X	0	0	0	1	1	1	1	1	Data										X	X	X	X	Broadcast mode - Update all DAC registers
Write to Clear Code Register																								
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	Write to clear code register; clear to zero scale
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	Write to clear code register; clear to midscale
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	Write to clear code register; clear to full-scale
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	Write to clear code register; ignore $\overline{\text{CLR}}$ pin
Write to LDAC Register																								
0	X	0	1	1	0	X	X	X	X	X	X	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Write to LDAC register. Default setting of these bits is '0'. If bit is set to '1', the $\overline{\text{LDAC}}$ pin is overridden. See the LDAC Functionality section for details.
Software Reset																								
0	X	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset (power-on reset)

Table 4. Control Matrix for the DAC7568, DAC8168, and DAC8568 (continued)

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16**	**D15**	**D14**	**D13-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 16-BIT DAC8568**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D14**	**D13**	**D12**	**D11-D5**	**D4**	**D3**	**D2**	**D1**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 14-BIT DAC8168**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D12**	**D11**	**D10**	**D9-D3**	**D2**	**D1**	**X**	**X**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 12-BIT DAC7568**
Write to Selected DAC Input Register and Update All DAC Registers																								
0	X	0	0	1	0	0	0	0	0	Data										X	X	X	X	Write to DAC input register Ch A and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	0	0	1	Data										X	X	X	X	Write to DAC Input Register Ch B and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	0	1	0	Data										X	X	X	X	Write to DAC Input Register Ch C and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	0	1	1	Data										X	X	X	X	Write to DAC Input Register Ch D and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	1	0	0	Data										X	X	X	X	Write to DAC Input Register Ch E and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	1	0	1	Data										X	X	X	X	Write to DAC Input Register Ch F and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	1	1	0	Data										X	X	X	X	Write to DAC Input Register Ch G and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	0	1	1	1	Data										X	X	X	X	Write to DAC Input Register Ch H and update all DAC registers (SW $\overline{LDAC}$)
0	X	0	0	1	0	1	X	X	X	X										X	X	X	X	Invalid code - No DAC Channel is updated
0	X	0	0	1	0	1	1	1	1	Data										X	X	X	X	Broadcast mode - Write to all DAC input registers and update all DAC registers (SW $\overline{LDAC}$)
Write to Selected DAC Input Register and Update Respective DAC Register																								
0	X	0	0	1	1	0	0	0	0	Data										X	X	X	X	Write to DAC input register Ch A and update DAC register Ch A
0	X	0	0	1	1	0	0	0	1	Data										X	X	X	X	Write to DAC Input Register Ch B and update DAC register Ch B
0	X	0	0	1	1	0	0	1	0	Data										X	X	X	X	Write to DAC Input Register Ch C and update DAC register Ch C
0	X	0	0	1	1	0	0	1	1	Data										X	X	X	X	Write to DAC Input Register Ch D and update DAC register Ch D
0	X	0	0	1	1	0	1	0	0	Data										X	X	X	X	Write to DAC Input Register Ch E and update DAC register Ch E
0	X	0	0	1	1	0	1	0	1	Data										X	X	X	X	Write to DAC Input Register Ch F and update DAC register Ch F
0	X	0	0	1	1	0	1	1	0	Data										X	X	X	X	Write to DAC Input Register Ch G and update DAC register Ch G
0	X	0	0	1	1	0	1	1	1	Data										X	X	X	X	Write to DAC Input Register Ch H and update DAC register Ch H
0	X	0	0	1	1	1	X	X	X	X										X	X	X	X	Invalid code - No DAC channel is updated
0	X	0	0	1	1	1	1	1	1	Data										X	X	X	X	Broadcast mode - Write to all DAC input registers and update all DAC registers (SW $\overline{LDAC}$)

Table 4. Control Matrix for the DAC7568, DAC8168, and DAC8568 (continued)

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16**	**D15**	**D14**	**D13-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 16-BIT DAC8568**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D14**	**D13**	**D12**	**D11-D5**	**D4**	**D3**	**D2**	**D1**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 14-BIT DAC8168**
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D12**	**D11**	**D10**	**D9-D3**	**D2**	**D1**	**X**	**X**	**X**	**X**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT FOR 12-BIT DAC7568**
Power-Down Commands																								
0	X	0	1	0	0	X	X	X	X	X	X	X	X	0	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Power-up DAC A, B, C, D, E, F, G, H by setting respective bit to '1'
0	X	0	1	0	0	X	X	X	X	X	X	X	X	0	1	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Power-down DAC A, B, C, D, E, F, G, H, 1kΩ to GND by setting respective bit to '1'
0	X	0	1	0	0	X	X	X	X	X	X	X	X	1	0	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Power-down DAC A, B, C, D, E, F, G, H, 100kΩ to GND by setting respective bit to '1'
0	X	0	1	0	0	X	X	X	X	X	X	X	X	1	1	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A	Power-down DAC A, B, C, D, E, F, G, H, High-Z to GND by setting respective bit to '1'
Internal Reference Commands																								
0	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	Power down internal reference - static mode (default), must use external reference to operate device; see Table 8
0	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	Power up internal reference - static mode; see Table 7 (NOTE: When all DACs power down, the reference powers down; when any DAC powers up, the reference powers up)
0	X	1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	Power up internal reference - flexible mode; see Table 9 (NOTE: When all DACs power down, the reference powers down; when any DAC powers up, the reference powers up)
0	X	1	0	0	1	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	Power up internal reference all the time regardless of state of DACs - flexible mode; see Table 10
0	X	1	0	0	1	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	Power down internal reference all the time regardless of state of DACs - flexible mode; see Table 11 (NOTE: External reference must be used to operate device)
0	X	1	0	0	1	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X	X	X	Switching internal reference mode from flexible mode to static mode
Reserved Bits																								
0	X	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions
0	X	1	0	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions
0	X	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions
0	X	1	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions
0	X	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions
0	X	1	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Reserved Bit - not valid; device does not perform to specified conditions

8.2.7 SYNC Interrupt

In a normal write sequence, the SYNC line stays low for at least 32 falling edges of SCLK and the addressed DAC register updates on the 32nd falling edge. However, if SYNC is brought high before the 31st falling edge, it acts as an interrupt to the write sequence; the shift register resets and the write sequence is discarded. Neither an update of the data buffer contents, DAC register contents, nor a change in the operating mode occurs (as shown in Figure 123).

8.2.8 Power-on Reset to Zero Scale or Midscale

The DAC7568, DAC8168, and DAC8568 contain a power-on reset circuit that controls the output voltage during power-up. For device grades A and C on power-up, all DAC registers are filled with zeros and the output voltages of all DAC channels are set to zero scale. For device grades B and D all DAC registers are set to have all DAC channels power up in midscale. All DAC channels remain that way until a valid write sequence and load command are made to the respective DAC channel. The power-on reset is useful in applications where it is important to know the state of the output of each DAC while the device is in the process of powering up. No device pin should be brought high before power is applied to the device. The internal reference is powered off / down by default and remains that way until a valid reference-change command is executed.

8.2.9 Clear Code Register and CLR Pin

The DAC7568, DAC8168, and DAC8568 contain a clear code register. The clear code register can be accessed via the serial peripheral interface (SPI) and is user-configurable. Bringing the CLR pin low clears the content of all DAC registers and all DAC buffers, and replaces the code with the code determined by the clear code register. The clear code register can be written to by applying the commands showed in Table 5. The control bits must be set as follows to access the clear code register that is programmed via the feature bits, F0 and F1: C3 = '0', C2 = '1', C1 = '0', and C0 = '1'. The default setting of the clear code register sets the output of all DAC channels to 0V when CLR pin is brought low. The CLR pin is falling-edge triggered; therefore, the device exits clear code mode on the 32nd falling edge of the next write sequence. If CLR pin is brought low during a write sequence, this write sequence is aborted and the DAC registers and DAC buffers are cleared as described previously.

When performing a software reset of the device, the clear code register is set back to its default mode (DB1 = DB0 = '0'). Setting the clear code register to DB1 = DB0 = '1' ignores any activity on the external CLR pin.

8.2.10 Software Reset Function

The DAC7568, DAC8168, and DAC8568 contain a software reset feature. If the software reset feature is executed, all registers inside the device are reset to default settings; that is, all DAC channels are reset to the power-on reset code (power on reset to zero scale for grades A and C; power on reset to midscale for grades B and D).

Table 5. Clear Code Register

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT**
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	Clear all DAC outputs to zero scale (default mode)
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	Clear all DAC outputs to midscale
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	Clear all DAC outputs to full-scale
0	X	0	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	Ignore external CLR pin

Table 6. Software Reset

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**	**GENERAL DATA FORMAT**
0	X	0	1	1	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Software reset

8.2.11 Operating Examples: DAC7568/DAC8168/DAC8568

For the following examples X = *don't care*; value can be either '0' or '1'.

Example 1: Write to Data Buffer A, B, G, H; Load DAC A, B, G, H Simultaneously

1st: Write to Data Buffer A:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	0	0	0	0	0	0	DATA							X	X	X	X

2nd: Write to Data Buffer B:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	0	0	0	0	0	1	DATA							X	X	X	X

3rd: Write to Data Buffer G:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	0	0	0	1	1	0	DATA							X	X	X	X

4th: Write to Data Buffer H and Simultaneously Update all DACs:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	1	0	0	1	1	1	DATA							X	X	X	X

The DAC A, DAC B, DAC G, and DAC H analog outputs simultaneously settle to the specified values upon completion of the 4th write sequence. (The DAC voltages update simultaneously after the 32nd SCLK falling edge of the fourth write cycle).

Example 2: Load New Data to DAC C, D, E, F Sequentially

1st: Write to Data Buffer C and Load DAC C: DAC C Output Settles to Specified Value Upon Completion:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	1	1	0	0	1	0	DATA							X	X	X	X

2nd: Write to Data Buffer D and Load DAC D: DAC D Output Settles to Specified Value Upon Completion:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	1	1	0	0	1	1	DATA							X	X	X	X

3rd: Write to Data Buffer E and Load DAC E: DAC E Output Settles to Specified Value Upon Completion:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	1	1	0	1	0	0	DATA							X	X	X	X

4th: Write to Data Buffer F and Load DAC F: DAC F Output Settles to Specified Value Upon Completion:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	0	1	1	0	1	0	1	DATA							X	X	X	X

After completion of each write cycle, the DAC analog output settles to the voltage specified.

Example 3: Power-Down DAC A, DAC B and DAC H to 1kΩ and Power-Down DAC C, DAC D, and DAC F to 100kΩ

1st: Write Power-Down Command to DAC Channel A and DAC Channel B: DAC A and DAC B to 1kΩ.

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1

2nd: Write Power-Down Command to DAC Channel H: DAC H to 1kΩ.

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0

3rd: Write Power-Down Command to DAC Channel C and DAC Channel D: DAC C and DAC D to 100kΩ.

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0

4th: Write Power-Down Command to DAC Channel F: DAC F to 100kΩ.

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**Don't Care**	**C3**	**C2**	**C1**	**C0**	**A3**	**A2**	**A1**	**A0**	**D16-D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**F3**	**F2**	**F1**	**F0**
0	X	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0

The DAC A, DAC B, DAC C, DAC D, DAC F, and DAC H analog outputs power-down to each respective specified mode.

Example 4: Power-Down All Channels Simultaneously while Reference is Always Powered Up

1st: Write Sequence for Enabling the DAC7568, DAC8168, and DAC8568 Internal Reference All the Time:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16-DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	Don't Care	C3	C2	C1	C0	A3	A2	A1	A0	D16	D15	D14	D13-D4	D3	D2	D1	F3	F2	F1	F0
0	X	1	0	0	1	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X

2nd: Write Sequence to Power-Down All DACs to High-Impedance:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	Don't Care	C3	C2	C1	C0	A3	A2	A1	A0	D16-D7	D6	D5	D4	D3	D2	D1	F3	F2	F1	F0
0	X	0	1	0	0	X	X	X	X	X	1	1	1	1	1	1	1	1	1	1

The DAC A, DAC B, DAC C, DAC D, DAC E, DAC F, DAC G, and DAC H analog outputs simultaneously power-down to high-impedance upon completion of the first and second write sequences, respectively.

Example 5: Write a Specific Value to All DACs while Reference is Always Powered Down

1st: Write Sequence for Disabling the DAC7568, DAC8168, and DAC8568 Internal Reference All the Time (after this sequence, these devices require an external reference source to function):

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16-DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	Don't Care	C3	C2	C1	C0	A3	A2	A1	A0	D16	D15	D14	D13-D4	D3	D2	D1	F3	F2	F1	F0
0	X	1	0	0	1	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X

2nd: Write Sequence to Write Specified Data to All DACs:

DB31	DB30-DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19-DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	Don't Care	C3	C2	C1	C0	A3	A2	A1	A0	D16-D7	D6	D5	D4	D3	D2	D1	F3	F2	F1	F0
0	X	0	0	1	1	1	1	1	1	DATA							X	X	X	X

The DAC A, DAC B, DAC C, DAC D, DAC E, DAC F, DAC G, and DAC H analog outputs simultaneously settle to the specified values upon completion of the second write sequence. (The DAC voltages update simultaneously after the 32nd SCLK falling edge of the second write cycle). Reference is always powered-down (External reference must be used for proper operation).

8.3 Device Functional Modes

8.3.1 Enable/Disable Internal Reference

The internal reference in the DAC7568, DAC8168, and DAC8568 is disabled by default for debugging, evaluation purposes, or when using an external reference. The internal reference can be powered up and powered down using a serial command that requires a 32-bit write sequence (see the *Serial Interface* section), as shown in Table 7 and Table 9. During the time that the internal reference is disabled, the DAC functions normally using an external reference. At this point, the internal reference is disconnected from the V_{REF}IN/V_{REF}OUT pin (3-state output). Do not attempt to drive the V_{REF}IN/V_{REF}OUT pin externally and internally at the same time indefinitely.

There are two modes that allow communication with the internal reference: Static and Flexible. In Flexible mode, DB19 must be set to '1'.

8.3.1.1 Static Mode

(see Table 7 and Table 8)

Enabling Internal Reference:

To enable the internal reference, write the 32-bit serial command shown in Table 7. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. If the internal reference is powered up, it automatically powers down when all DACs power down in any of the power-down modes (see the *Power Down Modes* section). The internal reference automatically powers up when any DAC is powered up.

Disabling Internal Reference:

To disable the internal reference, write the 32-bit serial command shown in Table 8. When performing a power cycle to reset the device, the internal reference is put back into its default mode and switched off (default mode).

**Table 7. Write Sequence for Enabling Internal Reference (Static Mode)
(Internal Reference Powered On—08000001h)**

DB31 DB27 DB23 DB19 DB4 DB0

0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------ Data Bits ------------------------------------| | Feature Bits |

**Table 8. Write Sequence for Disabling Internal Reference (Static Mode)
(Internal Reference Powered On—08000000h)**

DB31 DB27 DB23 DB19 DB4 DB0

0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------ Data Bits ------------------------------------| | Feature Bits |

8.3.1.2 Flexible Mode

(see Table 9, Table 10, and Table 11)

Enabling Internal Reference:

Method 1) To enable the internal reference, write the 32-bit serial command shown in Table 9. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. If the internal reference is powered up, it automatically powers down when all DACs power down in any of the power-down modes (see the *Power Down Modes* section). The internal reference powers up automatically when any DAC is powered up.

Device Functional Modes (continued)

(see Table 9, Table 10, and Table 11)

Method 2) To always enable the internal reference, write the 32-bit serial command shown in Table 10. When the internal reference is always enabled, any power-down command to the DAC channels does not change the internal reference operating mode. When performing a power cycle to reset the device, the internal reference is switched off (default mode). In the default mode, the internal reference is powered down until a valid write sequence is applied to power up the internal reference. When the internal reference is powered up, it remains powered up, regardless of the state of the DACs.

Disabling Internal Reference:

To disable the internal reference, write the 32-bit serial command shown in Table 11. When performing a power cycle to reset the device, the internal reference is switched off (default mode).

When the internal reference is operated in Flexible mode, Static mode is disabled and does not work. To switch from Flexible mode to Static mode, use the command shown in Table 12.

Table 9. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Powered On—09080000h)

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	1	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------- Data Bits -------------------------------------| | Feature Bits |

Table 10. Write Sequence for Enabling Internal Reference (Flexible Mode) (Internal Reference Always Powered On—090A0000h)

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	1	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------- Data Bits -------------------------------------| | Feature Bits |

Table 11. Write Sequence for Disabling Internal Reference (Flexible Mode) (Internal Reference Always Powered Down—090C0000h)

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	1	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------- Data Bits -------------------------------------| | Feature Bits |

Table 12. Write Sequence for Switching from Flexible Mode to Static Mode for Internal Reference (Internal Reference Always Powered Down—09000000h)

DB31				DB27				DB23				DB19															DB4				DB0
0	X	X	X	C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	F3	F2	F1	F0
0	X	X	X	1	0	0	1	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

|-- Prefix Bits --| |- Control Bits -| | Address Bits | |------------------------------------- Data Bits -------------------------------------| | Feature Bits |

8.3.2 $\overline{\text{LDAC}}$ Functionality

The DAC7568, DAC8168, and DAC8568 offer both a software and hardware simultaneous update and control function. The DAC double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs.

DAC7568, DAC8168, and DAC8568 data updates can be performed either in *synchronous* or in *asynchronous* mode.

Device Functional Modes (continued)

In *synchronous* mode, data are updated with the falling edge of the 32nd SCLK cycle, which follows a falling edge of SYNC. For such *synchronous* updates, the LDAC pin is not required and it must be connected to GND permanently.

In *asynchronous* mode, the LDAC pin is used as a negative edge triggered timing signal for simultaneous DAC updates. Multiple single-channel updates can be done in order to set different channel buffers to desired values and then make a falling edge on LDAC pin to simultaneously update the DAC output registers. Data buffers of all channels must be loaded with desired data before an LDAC falling edge. After a high-to-low LDAC transition, all DACs are simultaneously updated with the last contents of the corresponding data buffers. If the content of a data buffer is not changed, the corresponding DAC output remains unchanged after the LDAC pin is triggered.

Alternatively, all DAC outputs can be updated simultaneously using the built-in software function of LDAC. The LDAC register offers additional flexibility and control by allowing the selection of which DAC channel(s) should be updated simultaneously when the LDAC pin is being brought low. The LDAC register is loaded with an 8-bit word (DB0 to DB7) using control bits C3, C2, C1, and C0 (see). The default value for each bit, and therefore for each DAC channel, is zero. The external LDAC pin operates in normal mode. If the LDAC register bit is set to '1', it overrides the LDAC pin (the LDAC pin is internally tied low for that particular DAC channel) and this DAC channel updates synchronously after the falling edge of the 32nd SCLK cycle. However, if the LDAC register bit is set to '0', the DAC channel is controlled by the LDAC pin.

The combination of software and hardware simultaneous update functions is particularly useful in applications when updating only selective DAC channels simultaneously, while keeping the other channels unaffected and updating those channels synchronously; see for more information.

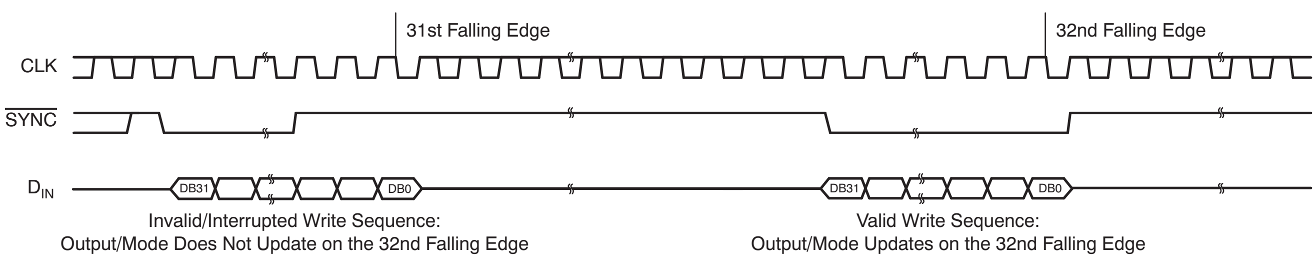


Figure 123. SYNC Interrupt Facility

8.3.3 Power-Down Modes

The DAC7568, DAC8168, and DAC8568 have two separate sets of power-down commands. One set is for the DAC channels and the other set is for the internal reference. For more information on powering down the reference, see the *Enable/Disable Internal Reference* section.

8.3.3.1 DAC Power-Down Commands

The DAC7568, DAC8168, and DAC8568 use four modes of operation. These modes are accessed by setting control bits C3, C2, C1, and C0, and power-down register bits DB8 and DB9. The control bits must be set to '0100'. Once the control bits are set correctly, the four different power down modes are software programmable by setting bits DB8 and DB9 in the control register. and Table 13 shows how to control the operating mode with data bits PD0 (DB8), and PD1 (DB9).

Table 13. DAC Operating Modes

PD1 (DB9)	PD0 (DB8)	DAC OPERATING MODES
0	0	Power up selected DACs
0	1	Power down selected DACs 1kΩ to GND
1	0	Power down selected DACs 100kΩ to GND
1	1	Power down selected DACs High-Z to GND

The DAC7568, DAC8168, and DAC8568 treat the power-down condition as data; all the operational modes are still valid for power-down. It is possible to broadcast a power-down condition to all the DAC8568, DAC8168, DAC7568s in a system. It is also possible to power-down a channel and update data on other channels. Furthermore, it is possible to write to the DAC register/buffer of the DAC channel that is powered down. When the DAC channel is then powered up, it will power up to this new value (see the *Operating Examples* section).

When both the PD0 and PD1 bits are set to '0', the device works normally with its typical current consumption of 1.25mA at 5.5V. The reference current is included with the operation of all eight DACs. However, for the three power-down modes, the supply current falls to 0.18μA at 5.5V (0.10μA at 3.6V). Not only does the supply current fall, but the output stage also switches internally from the output of the amplifier to a resistor network of known values.

The advantage of this switching is that the output impedance of the device is known while it is in power-down mode. As described in Table 13, there are three different power-down options. V_{OUT} can be connected internally to GND through a 1kΩ resistor, a 100kΩ resistor, or open circuited (High-Z). The output stage is shown in Figure 124. In other words, DB27, DB26, DB25, and DB24 = '0100' and DB9 and DB8 = '11' represent a power-down condition with High-Z output impedance for a selected channel. DB9 and DB8 = '01' represents a power-down condition with 1kΩ output impedance, and '10' represents a power-down condition with 100kΩ output impedance.

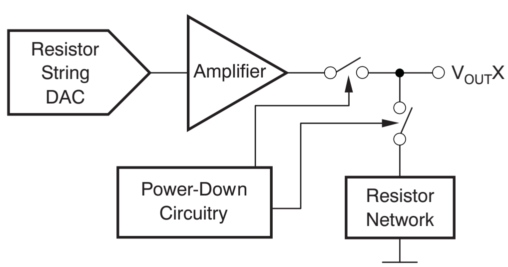


Figure 124. Output Stage During Power-Down

All analog channel circuits are shut down when the power-down mode is exercised. However, the contents of the DAC register are unaffected when in power down. By setting both bits, DB8 and DB9, to different values, any combination of DAC channels can be powered down or powered up. If a DAC channel is being powered up from a previously power down situation, this DAC channel powers up to the value in its DAC register. The time required to exit power-down is typically 2.5μs for AV_{DD} = 5V, and 4μs for AV_{DD} = 3V. See the *Typical Characteristics* section for more information.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

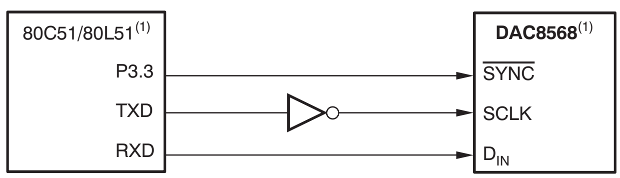
9.1 Application Information

Typical applications are discussed in the following section.

9.2 Typical Applications - Microprocessor Interfacing

9.2.1 DAC7568/DAC8168/DAC8568 to an 8051 Interface

Figure 125 shows a serial interface between the DAC7568, DAC8168, and DAC8568 and a typical 8051-type microcontroller. The setup for the interface is as follows: TXD of the 8051 drives SCLK of the DAC7568, DAC8168, or DAC8568, while RXD drives the serial data line of the device. The SYNC signal is derived from a bit-programmable pin on the port of the 8051; in this case, port line P3.3 is used. When data are to be transmitted to the DAC7568, DAC8168, and DAC8568, P3.3 is taken low. The 8051 transmits data in 8-bit bytes; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted; then, a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the third write cycle. The 8051 outputs the serial data in a format that has the LSB first. The DAC7568, DAC8168, and DAC8568 require the data with the MSB as the first bit received. Therefore, the 8051 transmit routine must take this requirement into account, and *mirror* the data as needed.



NOTE: (1) Also applies to DAC7568 and DAC8168. Additional pins omitted for clarity.

Figure 125. DAC7568/DAC8168/DAC8568 to 80C51/80L51 Interface

9.2.1.1 Detailed Design Procedure

9.2.1.1.1 Internal Reference

The internal reference of the DAC7568, DAC8168, and DAC8568 does not require an external load capacitor for stability because it is stable with any capacitive load. However, for improved noise performance, an external load capacitor of 150nF or larger connected to the $V_{REF}H/V_{REF}OUT$ output is recommended. Figure 126 shows the typical connections required for operation of the DAC7568, DAC8168, and DAC8568 internal reference. A supply bypass capacitor at the AV_{DD} input is also recommended.

Typical Applications - Microprocessor Interfacing (continued)

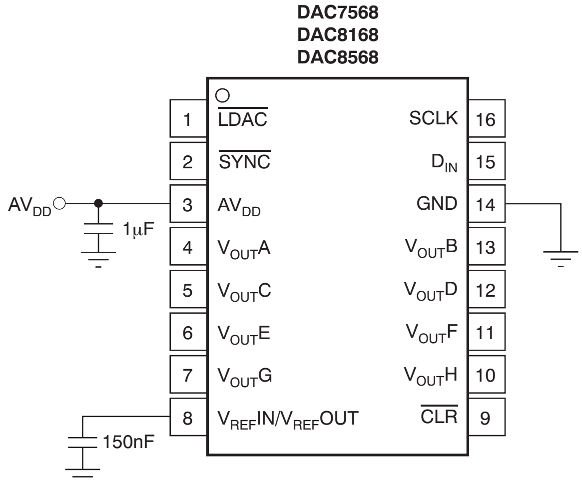


Figure 126. Typical Connections for Operating the DAC7568/DAC8168/DAC8568 Internal Reference (16-Pin Version Shown)

9.2.1.1.1.1 Supply Voltage

The internal reference features an extremely low dropout voltage. It can be operated with a supply of only 5mV above the reference output voltage in an unloaded condition. For loaded conditions, refer to the *Load Regulation* section. The stability of the internal reference with variations in supply voltage (line regulation, dc PSRR) is also exceptional. Within the specified supply voltage range of 2.7V to 5.5V, the variation at $V_{REF}H/V_{REF}OUT$ is less than 10µV/V; see the *Typical Characteristics* section.

9.2.1.1.1.2 Temperature Drift

The internal reference is designed to exhibit minimal drift error, defined as the change in reference output voltage over varying temperature. The drift is calculated using the *box* method described by Equation 2:

$$\text{Drift Error} = \left(\frac{V_{REF\_MAX} - V_{REF\_MIN}}{V_{REF} \times T_{RANGE}} \right) \times 10^{6} \ (\text{ppm/°C}) \tag{2}$$

Where:

V_{REF_MAX} = maximum reference voltage observed within temperature range T_{RANGE}.
V_{REF_MIN} = minimum reference voltage observed within temperature range T_{RANGE}.
V_{REF} = 2.5V, target value for reference output voltage.

The internal reference (grade C only) features an exceptional typical drift coefficient of 2ppm/°C from –40°C to +125°C. Characterizing a large number of units, a maximum drift coefficient of 5ppm/°C (grade C only) is observed. Temperature drift results are summarized in the *Typical Characteristics* section.

9.2.1.1.1.3 Noise Performance

Typical 0.1Hz to 10Hz voltage noise can be seen in Figure 9, *Internal Reference Noise*. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade the ac performance. The output noise spectrum at $V_{REF}H/V_{REF}OUT$ without any external components is depicted in Figure 8, *Internal Reference Noise Density vs Frequency*. A second noise density spectrum is also shown in Figure 8. This spectrum was obtained using a 4.8µF load capacitor at $V_{REF}H/V_{REF}OUT$ for noise filtering. Internal reference noise impacts the DAC output noise; see the *DAC Noise Performance* section for more details.

Typical Applications - Microprocessor Interfacing (continued)

9.2.1.1.1.4 Load Regulation

Load regulation is defined as the change in reference output voltage as a result of changes in load current. The load regulation of the internal reference is measured using force and sense contacts as shown in Figure 127. The force and sense lines reduce the impact of contact and trace resistance, resulting in accurate measurement of the load regulation contributed solely by the internal reference. Measurement results are summarized in the *Typical Characteristics* section. Force and sense lines should be used for applications that require improved load regulation.

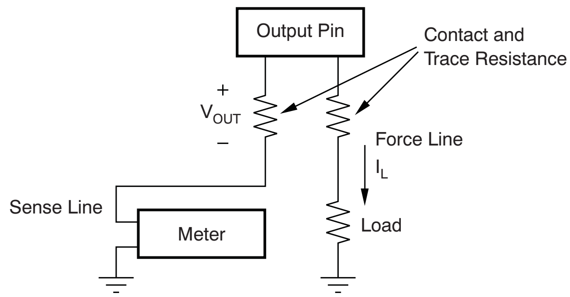


Figure 127. Accurate Load Regulation of the DAC7568/DAC8168/DAC8568 Internal Reference

9.2.1.1.1.5 Long-Term Stability

Long-term stability/aging refers to the change of the output voltage of a reference over a period of months or years. This effect lessens as time progresses (see Figure 7, the typical long-term stability curve). The typical drift value for the internal reference is 50ppm from 0 hours to 1900 hours. This parameter is characterized by powering-up 20 units and measuring them at regular intervals for a period of 1900 hours.

9.2.1.1.1.6 Thermal Hysteresis

Thermal hysteresis for a reference is defined as the change in output voltage after operating the device at +25°C, cycling the device through the operating temperature range, and returning to +25°C. Hysteresis is expressed by Equation 3:

$$V_{HYST} = \left(\frac{|V_{REF\_PRE} - V_{REF\_POST}|}{V_{REF\_NOM}} \right) \times 10^6 \text{ (ppm/°C)} \tag{3}$$

Where:

V_{HYST} = thermal hysteresis.

V_{REF_PRE} = output voltage measured at +25°C pre-temperature cycling.

V_{REF_POST} = output voltage measured after the device cycles through the temperature range of –40°C to +125°C, and returns to +25°C.

9.2.1.1.2 DAC Noise Performance

Typical noise performance for the DAC7568, DAC8168, and DAC8568 with the internal reference enabled is shown in Figure 66 to Figure 67. Output noise spectral density at the V_{OUT} pin versus frequency is depicted in Figure 66 for full-scale, midscale, and zero-scale input codes. The typical noise density for midscale code is 120nV/√Hz at 1kHz and 100nV/√Hz at 1MHz. High-frequency noise can be improved by filtering the reference noise. Integrated output noise between 0.1Hz and 10Hz is close to 6µV_{PP} (midscale), as shown in Figure 67.

9.2.1.1.3 Bipolar Operation Using The DAC7568/DAC8168/DAC8568

The DAC7568, DAC8168, and DAC8568 are designed for single-supply operation, but a bipolar output range is also possible using the circuit in either Figure 128 or Figure 129. The circuit shown gives an output voltage range of ±V_{REF}. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

The output voltage for any input code can be calculated with Equation 4:

Typical Applications - Microprocessor Interfacing (continued)

$$V_{OUT} = \left[V_{REF} \times Gain \times \left(\frac{D_{IN}}{2^n} \right) \times \left(\frac{R_1 + R_2}{R_1} \right) - V_{REF} \times \left(\frac{R_2}{R_1} \right) \right] \quad (4)$$

Where:

D_{IN} = decimal equivalent of the binary code that is loaded to the DAC register. It can range from 0 to 4095 for DAC7568 (12 bit), 0 to 16,383 for DAC8168 (14 bit), and 0 to 65535 for DAC8568 (16 bit).

n = resolution in bits; either 12 (DAC7568), 14 (DAC8168) or 16 (DAC8568)

Gain = 1 for A/B grades or 2 for C/D grades.

With V_{REF}IN/V_{REF}OUT = 5V, $R_1 = R_2 = 10k\Omega$, for grades A and B.

$$V_{OUT} = \left(\frac{10 \times D_{IN}}{2^n} \right) - 5V \quad (5)$$

This result has an output voltage range of ±5V with 0000h corresponding to a –5V output and FFFFh corresponding to a +5V output for the 16-bit DAC8568, as shown in Figure 128. Similarly, using the internal reference, a ±2.5V output voltage range can be achieved, as Figure 129 shows.

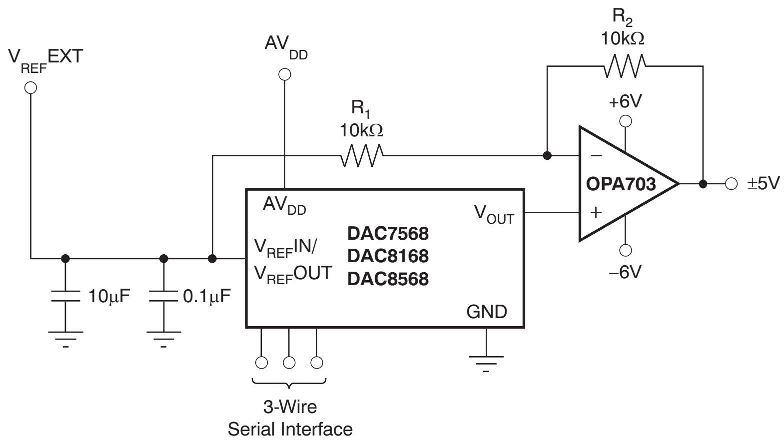


Figure 128. Bipolar Output Range Using External Reference at 5V

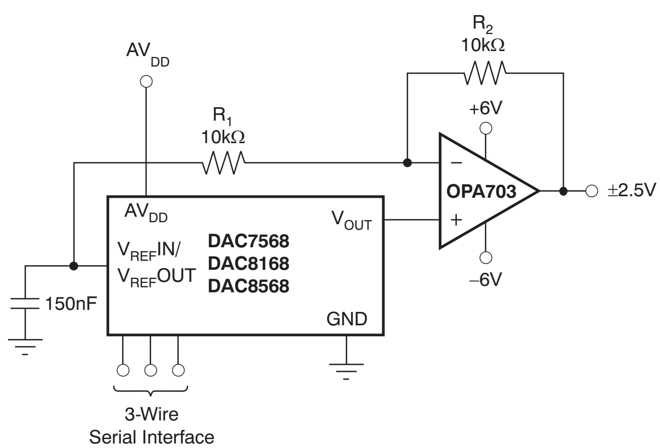
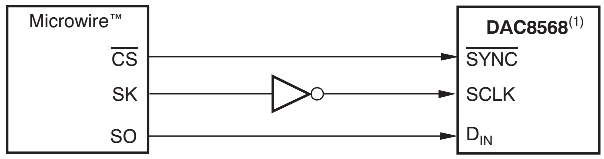


Figure 129. Bipolar Output Range Using Internal Reference

9.2.2 DAC7568/DAC8168/DAC8568 to Microwire Interface

Figure 130 shows an interface between the DAC7568, DAC8168, and DAC8568 and any Microwire-compatible device. Serial data are shifted out on the falling edge of the serial clock and are clocked into the DAC7568, DAC8168, and DAC8568 on the rising edge of the SK signal.

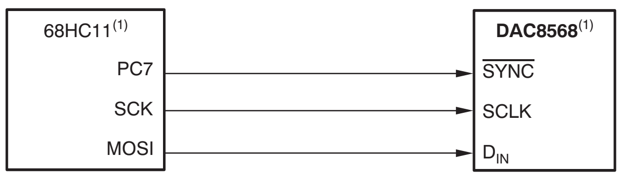


NOTE: (1) Also applies to DAC7568 and DAC8168. Additional pins omitted for clarity.

Figure 130. DAC7568/DAC8168/DAC8568 to Microwire Interface

9.2.3 DAC7568/DAC8168/DAC8568 to 68HC11 Interface

Figure 131 shows a serial interface between the DAC7568/DAC8168/DAC8568 and the 68HC11 microcontroller. SCK of the 68HC11 drives the SCLK of the DAC7568, DAC8168, and DAC8568, while the MOSI output drives the serial data line of the DAC. The SYNC signal derives from a port line (PC7), similar to the 8051 diagram.



NOTE: (1) Also applies to DAC7568 and DAC8168. Additional pins omitted for clarity.

Figure 131. DAC7568/DAC8168/DAC8568 to 68HC11 Interface

The 68HC11 should be configured so that its CPOL bit is '0' and its CPHA bit is '1'. This configuration causes data appearing on the MOSI output to be valid on the falling edge of SCK. When data are being transmitted to the DAC, the SYNC line is held low (PC7). Serial data from the 68HC11 are transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. (Data are transmitted MSB first.) In order to load data to the DAC7568, DAC8168, and DAC8568, PC7 is left low after the first eight bits are transferred; then, a second and third serial write operation are performed to the DAC. PC7 is taken high at the end of this procedure.

10 Layout

10.1 Layout Guidelines

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies.

The DAC7568, DAC8168, and DAC8568 offer single-supply operation, and are often used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to keep digital noise from appearing at the output.

As a result of the single ground pin of the DAC7568, DAC8168, and DAC8568, all return currents (including digital and analog return currents for the DAC) must flow through a single point. Ideally, GND would be connected directly to an analog ground plane. This plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The power applied to AV_{DD} should be well-regulated and low noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, AV_{DD} should be connected to a power-supply plane or trace that is separate from the connection for digital logic until they are connected at the power-entry point. In addition, a 1μF to 10μF capacitor and 0.1μF bypass capacitor are strongly recommended. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor or even a *Pi* filter made up of inductors and capacitors—all designed to essentially low-pass filter the supply and remove the high-frequency noise.

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

由于产品数据表中所列的许多不同技术参数的复杂度的增加，这一部分总结了选出的与数模转换器相关的技术参数。

11.1.1.1 静态性能

静态性能参数是诸如微分非线性 (DNL) 或积分非线性 (INL) 等的技术规格。这些是直流技术规格，并且提供与 DAC 精度有关的信息。这些技术规格 对于 信号变化缓慢且具有精度要求的应用极为重要。

11.1.1.1.1 分辨率

总的来讲，DAC 分辨率可用不同的形式表示。诸如 IEC 60748-4 的技术规格承认数字、模拟和相对分辨率。数字分辨率被定义为在选用的编号系统中需要表达传输特性步长总数的数字的数量，在这里，一个步长代表一个数字输入代码和相应的离散模拟输出值。数据表中提出的最常用的分辨率定义是以位表示的数字分辨率。

11.1.1.1.2 最低有效位 (LSB)

最低有效位 (LSB) 被定义为一个二进制编码系统中的最小值。通过用 2^n除以满量程输出电压来计算 LSB 的值，在这里，*n*是转换器的分辨率。

11.1.1.1.3 最高有效位 (MSB)

最高有效位 (MSB) 被定义为一个二进制编码系统中的最大值。可以用 2 除以满量程输出电压来计算 MSB 的值。它的值是满量程的一半。

11.1.1.1.4 相对精度或积分非线性 (INL)

相对精度或积分非线性 (INL) 被定义为实际转换功能与一条通过理想 DAC 转换功能端点的直线之间的最大偏离。DNL 以 LSB 为单位进行测量。

11.1.1.1.5 微分非线性 (DNL)

微分非线性 (DNL) 被定义为实际 LSB 步长与理想 1LSB 步长的偏离。理想状态下，任意两个与输出模拟电压相对应的相邻数字代码恰好相隔一个 LSB。如果 DNL 少于 1LSB，DAC 被称为单调转换。

11.1.1.1.6 满量程误差

满量程误差被定义为 DAC 寄存器被载入满量程代码 (0xFFFF) 时，实际满量程输出电压与理想输出电压的偏离。理想状态下，输出应该为 AV_{DD} – 1LSB。满量程误差被表示为满量程范围的百分比 (%FSR)。

11.1.1.1.7 偏移误差

偏移误差被定义为转换函数的线性区域内实际输出电压与理想输出电压间的差异。这个差异通过使用一条；两个代码（代码 485 和 64714）定义的直线进行计算。由于用一条直线定义偏移误差，它的值可为正，也可为负。偏移误差的单位为 mV。

11.1.1.1.8 零代码误差

零代码误差被定义为 DAC 输出电压。此时全 '0' 被载入到 DAC 寄存器中。零量程误差是实际输出电压与理想输出电压 (0V) 间差异的测量值。它的单位为 mV。它主要由输出放大器内的偏移所导致。

11.1.1.1.9 增益误差

增益误差被定义为实际 DAC 转换特性与理想转换功能在斜率上的偏离。增益误差表示为满量程范围的百分比 (% FSR)。

11.1.1.1.10 满量程误差漂移

满量程误差漂移被定义为温度变化时满量程误差的变化。满量程误差漂移的单位为 %FSR/°C。

器件支持 **(**接下页**)**

11.1.1.1.11 偏移误差漂移

偏移误差漂移被定义为温度变化时，偏移误差的变化。偏移误差漂移的表示单位为 μV/°C。

11.1.1.1.12 零代码误差漂移

零代码误差漂移被定义随温度变化的零代码误差的变换值。零代码误差漂移的表示单位为 μV/°C。

11.1.1.1.13 增益温度系数

增益温度系数被定义为随温度变换的增益误差的变化值。增益温度系数的表示方法为 FSR/°C 的 ppm 值。

11.1.1.1.14 电源抑制比 **(PSRR)**

电源抑制比 (PSRR) 被定义为，针对 DAC 的一个满量程输出，输出电压的变化与电源电压的比率。一个器件的 PSRR 表示 DAC 的输出是如何受到电源电压的变化的影响。PSRR 的测量单位为分贝 (dB)。

11.1.1.1.15 单调性

单调性被定义为一个信号不发生变化的斜坡。如果一个 DAC 是单调的，输出变化处于同一方向，或者在输入代码中针对每个步长增加（或减少）保持至少恒定。

11.1.1.2 *动态性能*

动态性能参数是指诸如稳定时间或压摆率等技术规格，这些参数 对于 信号迅速变化和/或存在高频信号的应用非常重要。

11.1.1.2.1 压摆率

一个放大器或其它电子电路的输出压摆率 (SR) 被定义为针对所有可能的输入信号，输出电压的最大变化率。

$$SR = \max\left(\left|\frac{\Delta V_{OUT}(t)}{\Delta t}\right|\right)$$

其中，$\Delta V_{输出}(t)$ 是放大器作为时间t的函数所产生的输出。

11.1.1.2.2 输出电压稳定时间

稳定时间是输入变化后，在其最终值附近的一个误差范围内，DAC 输出稳定的总时间（其中包括转换时间）稳定时间被指定为满量程范围 (FSR) 的 ±0.003% 以内（或者指定的任何值）。

11.1.1.2.3 代码更改**/**数模转换毛刺脉冲能量

数模转换毛刺脉冲是在输入代码处于 DAC 寄存器变化状态时，被注入模拟输出的脉冲。此特性通常规定为以毫微伏秒 (nV-s) 为单位的毛刺面积，并且在数字输入编码在主进位跳变处改变 1LSB 时测量。

11.1.1.2.4 数字馈通

数字馈通被定为 DAC 输出上（来自 DAC 的数字输入）可见的脉冲。它在 DAC 输出未被更新时测得。它被指定为 nV-s，并且在数据总线上用满量程代码变化测得；也就是说，从全 '0' 至全 '1'，反之亦然。

11.1.1.2.5 通道到通道直流串扰

通道至通道直流串扰被定义为，一个 DAC 通道的输出电平相对应于其它 DAC 通道的输出的变化所发生的直流变化。它在监视其它保持在中量程上的 DAC 通道的同时，用一个 DAC 通道上的满量程输出变化进行测量。它表示为 LSB。

11.1.1.2.6 通道到通道交流串扰

多通道 DAC 中交流串扰被定义为在某一频率 (f) （和它的谐波）时，一个通道的输出上所经历的交流干扰的数量，此时一个相邻通道的输出以频率 (f) 的速率改变它的值。它测量为以 1kHz 频率正弦波振荡的通道输出，同时监视一个相邻 DAC 通道输出上 1kHz 谐波的振幅（保持在零量程）。它的单位为 dB。

器件支持 (接下页)

11.1.1.2.7 信噪比 (SNR)

信噪比 (SNR) 被定义为输出信号的均方根 (RMS) 值除以所有其他二分之一输出频率以下的光谱分量总和的 RMS 值的比率，其中不包括谐波或交流值。SNR 以 dB 为单位测量。

11.1.1.2.8 总谐波失真 (THD)

总谐波失真 + 噪声被定义为谐波和噪声的 RMS 值与基本频率值的比率。它表示为采样率 f_S上基本频率振幅的百分比。

11.1.1.2.9 无杂散动态范围 (SFDR)

无杂散动态范围 (SFDR) 是杂散噪声干扰或基本信号失真前可用的 DAC 动态范围。SFDR 是基本频率与直流到完全那奎斯特带宽（DAC 采样速率的一半，或者 $f_S/2$）范围内最大谐波或非谐波相关杂散之间振幅差异的测量值。一个杂散是频谱分析仪上的任一频率窗口，或者来自 DAC 模拟输出的一个傅里叶变换。SFDR 被指定为相对于载波的分贝值 (dBc)。

11.1.1.2.10 信噪比和失真率 (SINAD)

除了量化任一内部随机噪声功率，SINAD 包括全部以输出噪声功率为定义的谐波和突出的杂散分量。SINAD 在指定的输入频率和采样速率上表示为 dB，f_S。

11.1.1.2.11 DAC 输出噪声密度

输出噪声密度被定义为内部生产的随机噪声。随机噪声的特点是频谱密度 ($nV/\sqrt{Hz}$)。通过将 DAC 载入中量程并测量输出上的噪声来测量这个值。

11.1.1.2.12 DAC 输出噪声

DAC 输出噪声被定义为 DAC 输出与所希望得到的值之间的任一电压偏离（在一个特定的频段内）。它用保持在中量程的 DAC 通道进行测量，同时过滤 0.1Hz 至 10Hz 波段内的输出电压，并且测量其振幅峰值。它表示为峰值到峰值电压 (V_{PP})。

11.1.1.2.13 满量程范围 (FSR)

满量程范围 (FSR) 是 DAC 额定提供的最大和最小模拟输出值之间的差值；通常情况下，也指定了最大和最小值。对于一个*n*位 DAC，这些值通常作为与代码 0 和 2^n相匹配的值给出。

11.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件以及申请样片或购买产品的快速访问链接。

表 **14.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
DAC7568	单击此处	单击此处	单击此处	单击此处	单击此处
DAC8168	单击此处	单击此处	单击此处	单击此处	单击此处
DAC8568	单击此处	单击此处	单击此处	单击此处	单击此处

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.5 商标

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7568IAPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA7568A	Samples
DAC7568IAPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA7568A	Samples
DAC7568ICPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA7568C	Samples
DAC7568ICPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA7568C	Samples
DAC8168IAPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8168A	Samples
DAC8168IAPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8168A	Samples
DAC8168ICPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8168C	Samples
DAC8168ICPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8168C	Samples
DAC8568IAPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568A	Samples
DAC8568IAPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568A	Samples
DAC8568IBPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568B	Samples
DAC8568IBPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568B	Samples
DAC8568ICPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568C	Samples
DAC8568ICPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568C	Samples
DAC8568IDPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568D	Samples
DAC8568IDPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DA8568D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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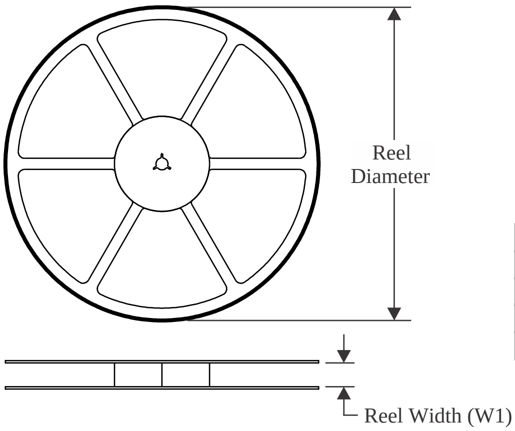
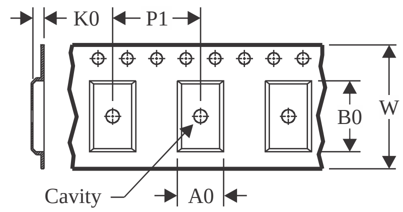
TAPE AND REEL INFORMATION

REEL DIMENSIONS

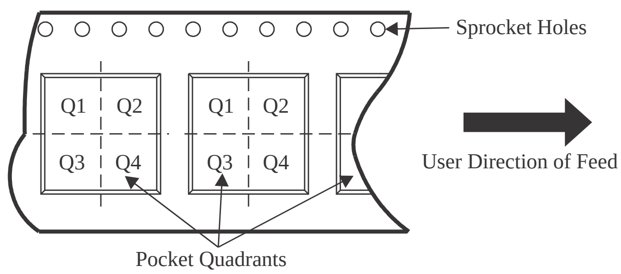


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

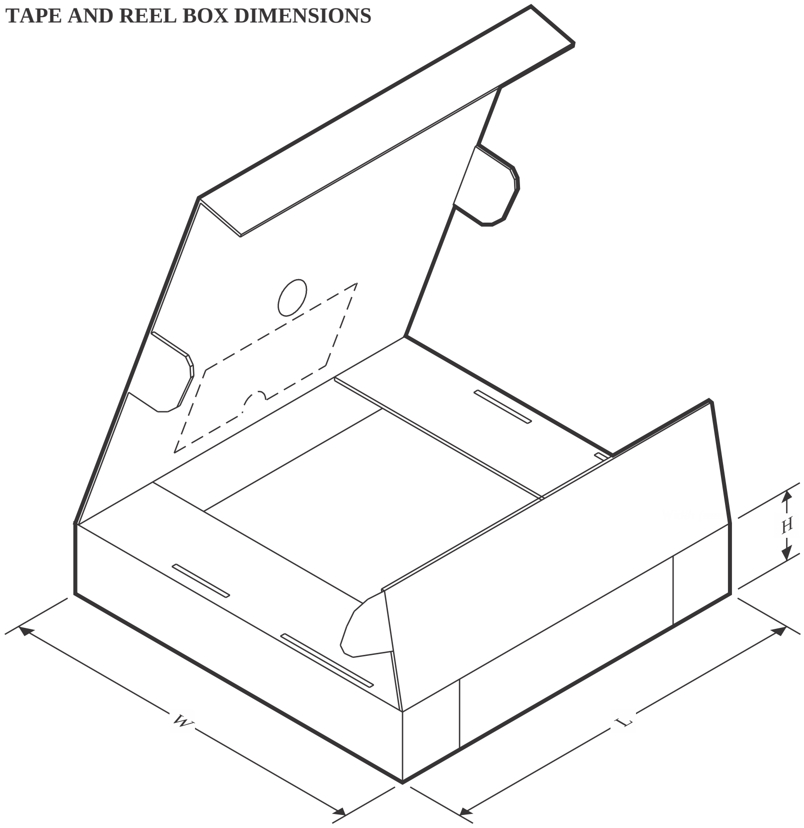
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8168IAPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DAC8168ICPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

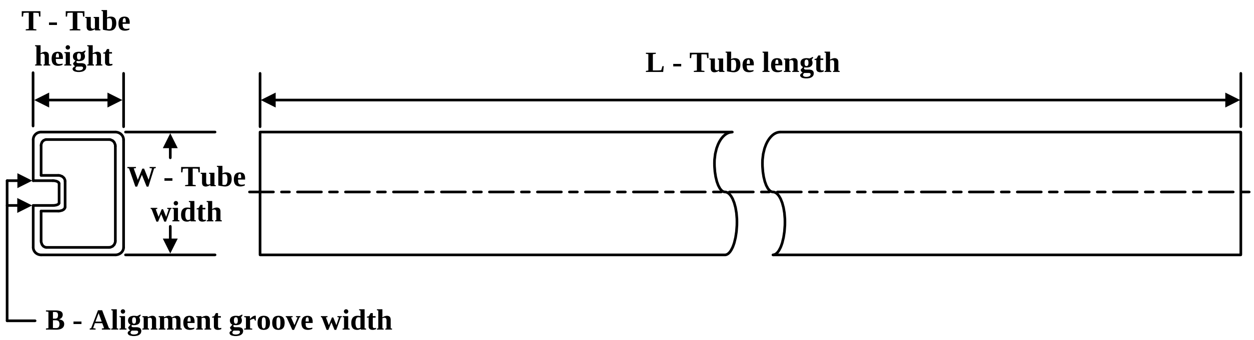
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

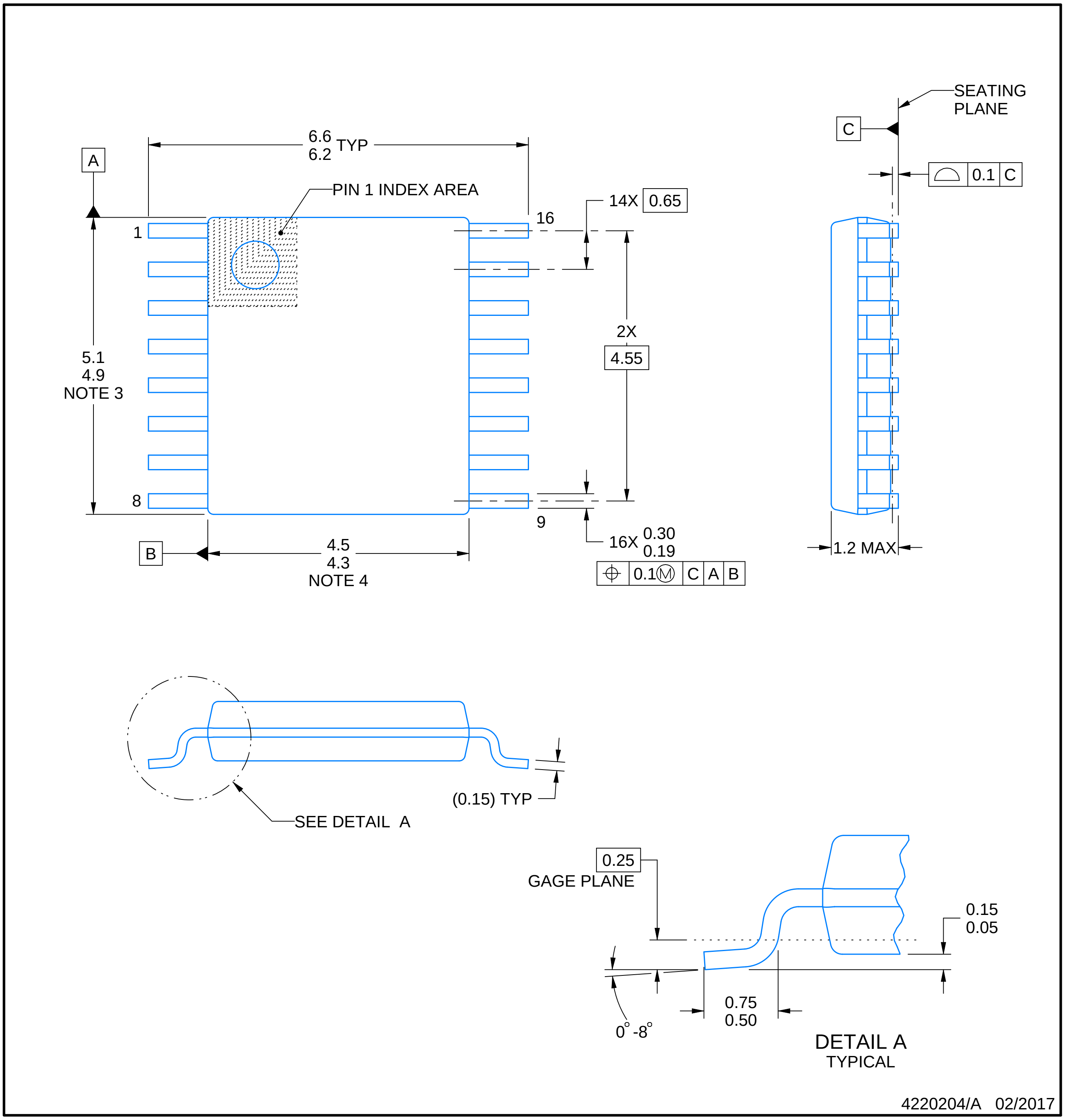
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8168IAPWR	TSSOP	PW	14	2000	350.0	350.0	43.0
DAC8168ICPWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



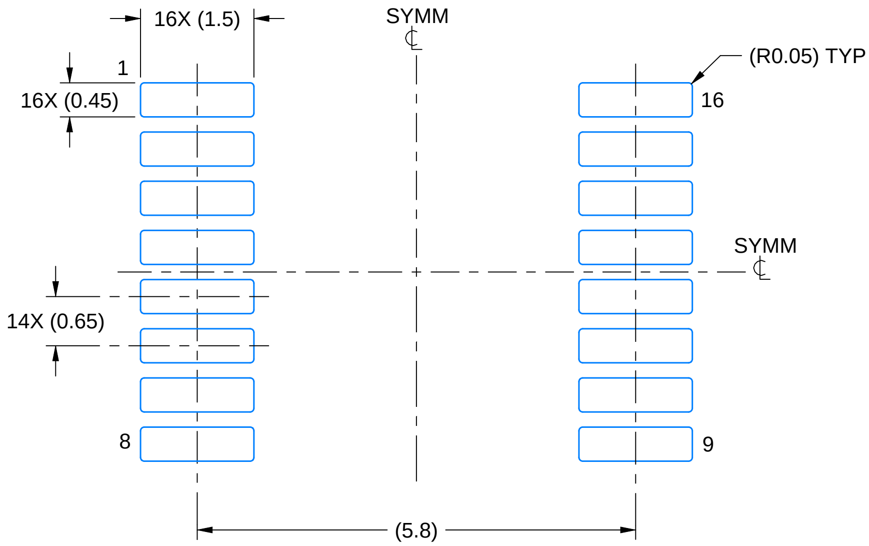
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7568IAPW	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC7568ICPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC7568ICPW	PW	TSSOP	16	90	508	8.5	3250	2.8
DAC8168IAPW	PW	TSSOP	14	90	530	10.2	3600	3.5
DAC8168ICPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8568IAPW	PW	TSSOP	16	90	508	8.5	3250	2.8
DAC8568IAPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8568IBPW	PW	TSSOP	16	90	508	8.5	3250	2.8
DAC8568IBPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8568ICPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8568ICPW	PW	TSSOP	16	90	508	8.5	3250	2.8
DAC8568IDPW	PW	TSSOP	16	90	530	10.2	3600	3.5
DAC8568IDPW	PW	TSSOP	16	90	508	8.5	3250	2.8

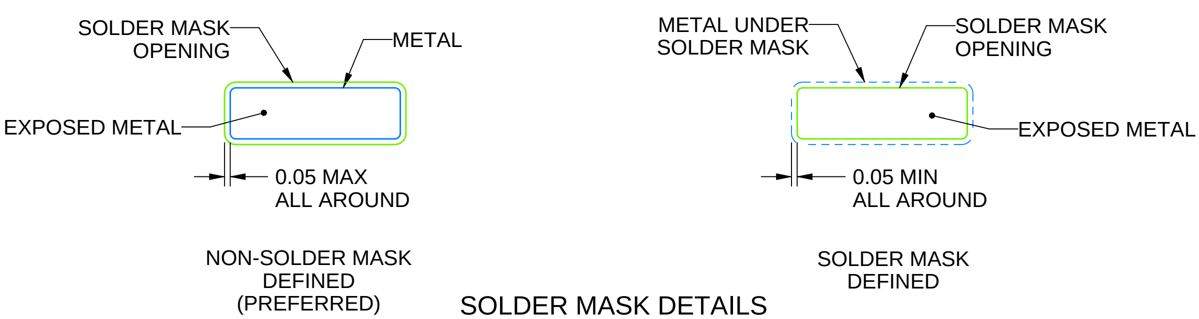


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

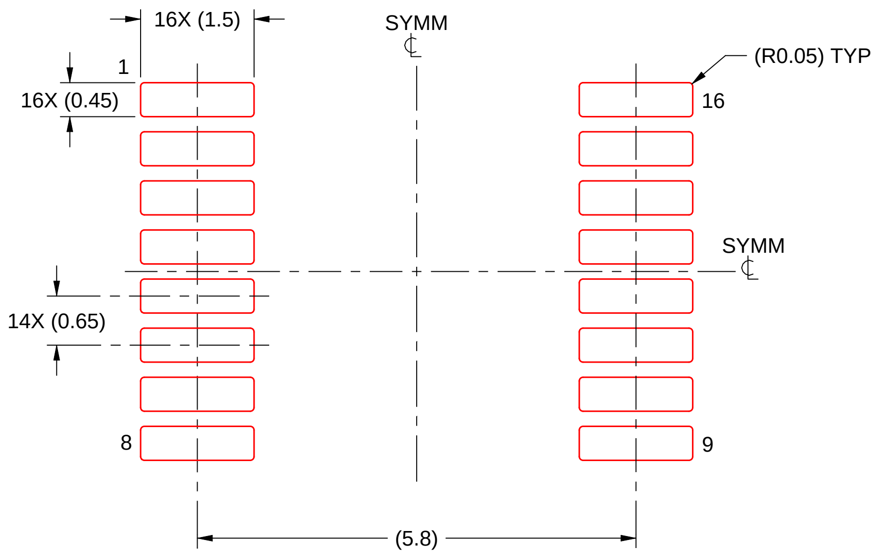


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



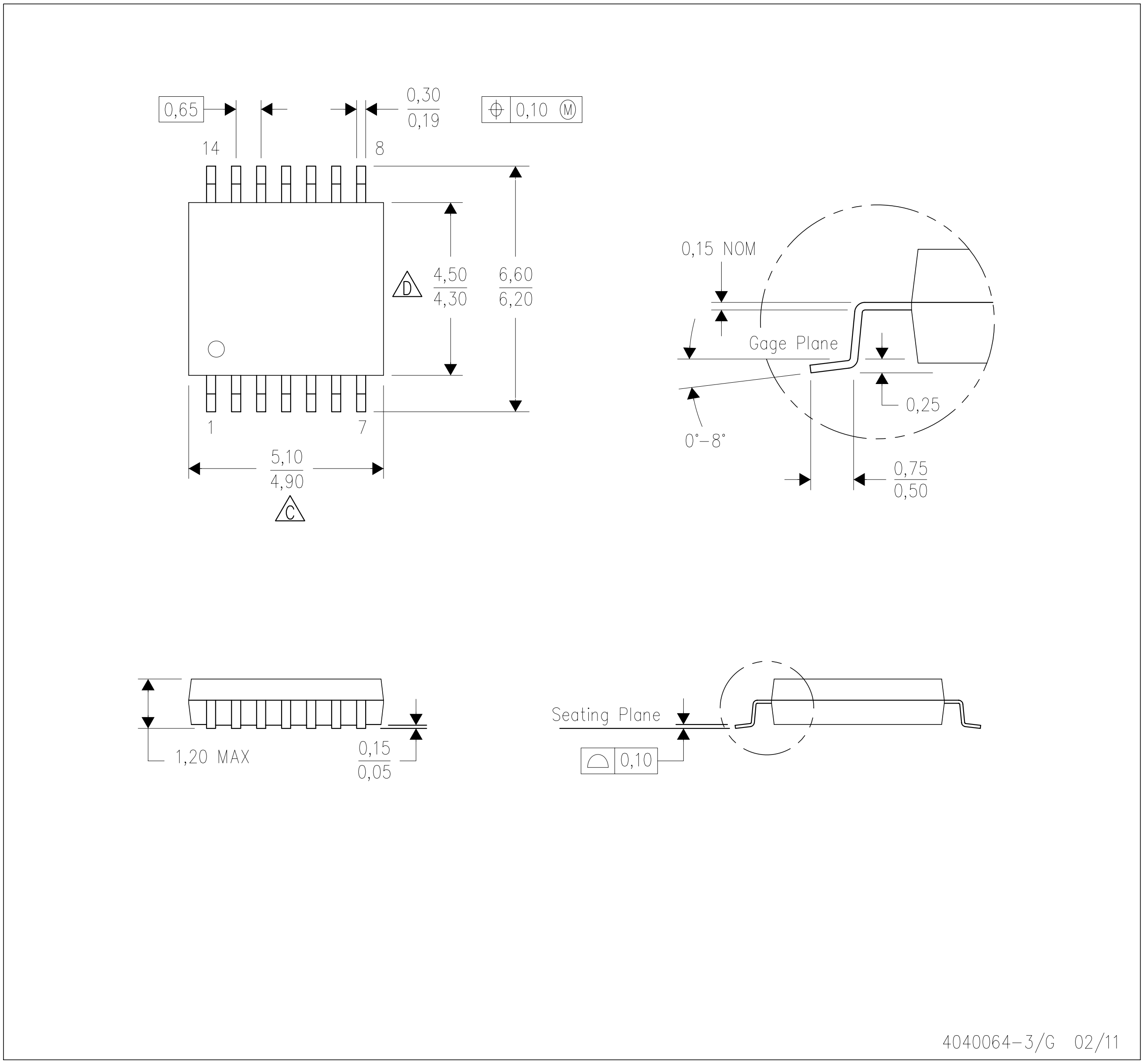
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

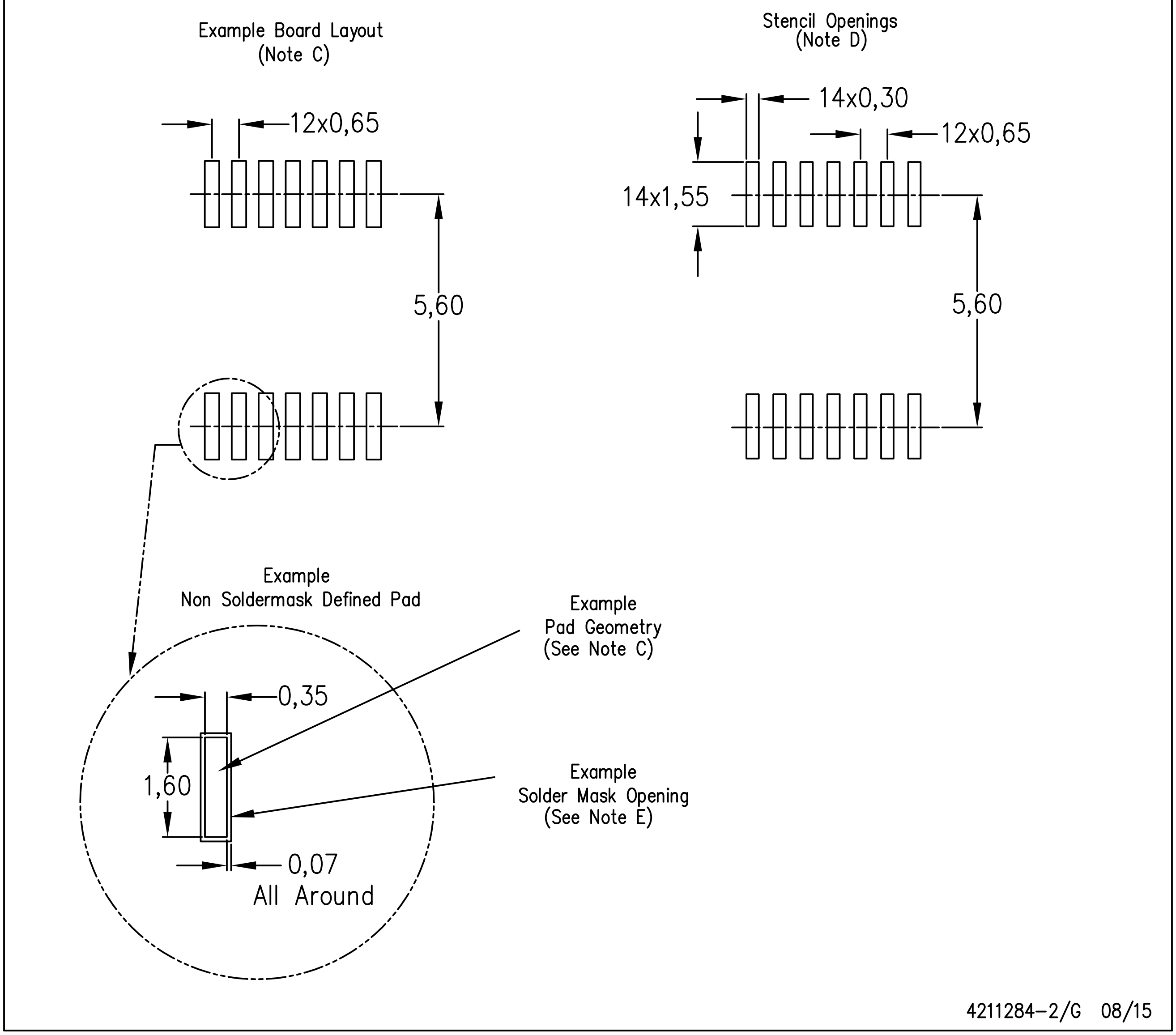
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265