DLP230NP 和 DLP230NPSE 0.23 1080P 数字微镜器件

1 特性

- 超紧凑 0.23 英寸 (5.95mm) 对角线微镜阵列
  - 1920 × 1080 像素屏幕显示
  - 5.4µm 微镜间距
  - 17° 微镜倾斜（相对于平坦表面）
  - 采用侧面照明，实现最优的效率和光学引擎尺寸
  - 偏振无关型铝微镜表面
- 8 位 SubLVDS 输入数据总线
- 显示应用专用的 DLPC34x6 控制器
- 专用 DLPA2000、DLPA2005、DLPA3000 或 DLPA3005 PMIC/LED 驱动器，确保可靠运行

2 显示应用

- DLP 标牌
- 移动投影仪
- 智能扬声器
- 虚拟现实及增强现实耳机和眼镜
- 移动式附件
- 智能家居显示器
- Pico 投影仪

3 说明

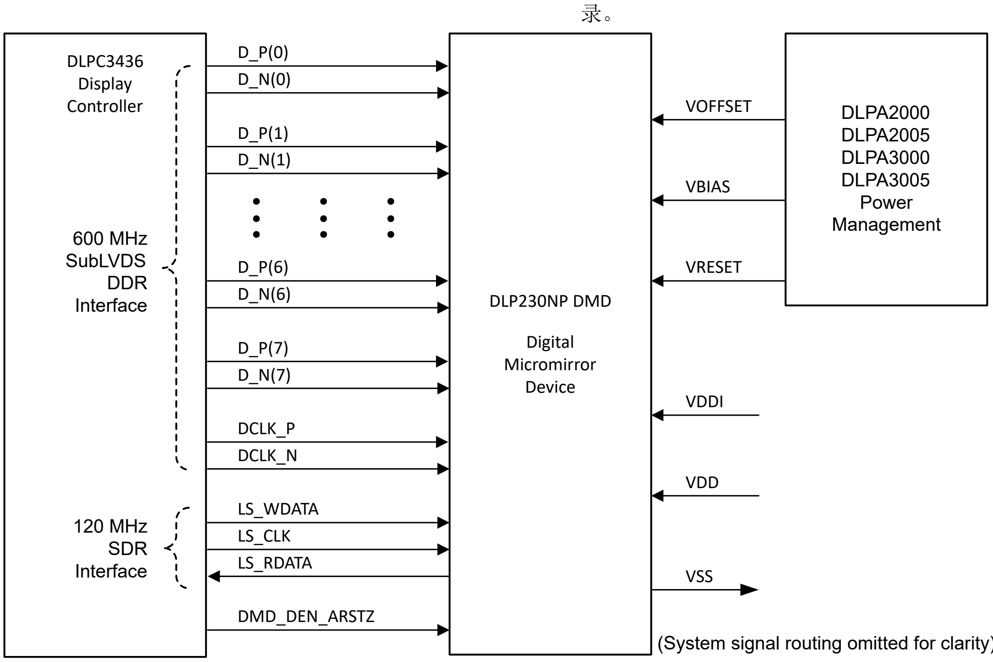
DLP230NP 和 DLP230NPSE .23 1080p 数字微镜器件 (DMD) 是数控微光机电系统 (MOEMS) 空间照明调制器 (SLM)。当与适当的光学系统搭配使用时，这些 DMD 可显示清晰和高质量的 1080p 图像或视频。芯片组中包含 .23 1080p DMD 和 DLPC3436 或 DLPC3426 控制器。DLPA2000、DLPA2005、DLPA3000 和 DLPA3005 PMIC/LED 驱动器支持 DLP230NP 芯片组；DLPA3000 驱动器支持 DLP230NPSE 芯片组。此器件外形小巧，适用于重视高画质、小尺寸和低功耗的便携设备。

器件信息

DMD	控制器	说明
DLP230NP	DLPC3436	亮度更高
DLP230NPSE	DLPC3426	亮度更低

器件型号	封装(1)	封装尺寸（标称值）
DLP230NP	FQP (54)	16.8mm × 5.92mm × 3.58mm
DLP230NPSE		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (March 2023) to Revision E (April 2023) **Page**

- 添加了 DLP230NPSE 器件及其控制器信息........ 1
- 添加了“说明（续）”........ 3
- Added the DLP230NPSE device and its controller information........ 20
- Added new parts to table........ 34

Changes from Revision C (May 2022) to Revision D (March 2023) **Page**

- 添加了对 DLPA3005 的支持........ 1
- 更新了*简化版应用* 以添加 DLPA3005........ 1
- Added DLPA3005 support........ 21
- Added DLPA3005 support........ 27
- Added DLPA3005 resources........ 34

5 说明（续）

请访问 *TI DLP Pico 显示技术入门*页，了解有关 DMD 技术的更多信息。

DMD 提供现成的资源，可帮助用户缩短设计周期。这些资源包括可直接用于生产环境的光学模块、光学模块制造商和设计公司。

6 Pin Configuration and Functions

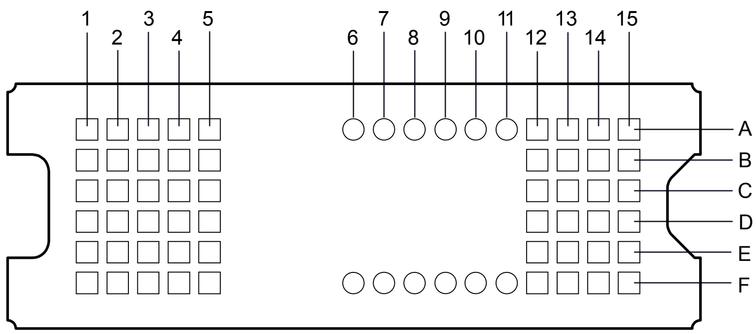


图 6-1. FQP Package, 54-Pin CLGA (Bottom View)

表 6-1. Pin Functions – Connector Pins

PIN[(1)]		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[(2)] (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	A2	I	SubLVDS	Double	Data, negative	1.96
D_N(1)	A1	I	SubLVDS	Double	Data, negative	1.42
D_N(2)	C1	I	SubLVDS	Double	Data, negative	1.35
D_N(3)	B4	I	SubLVDS	Double	Data, negative	3.36
D_N(4)	F5	I	SubLVDS	Double	Data, negative	4.29
D_N(5)	D4	I	SubLVDS	Double	Data, negative	3.20
D_N(6)	E1	I	SubLVDS	Double	Data, negative	1.76
D_N(7)	F3	I	SubLVDS	Double	Data, negative	2.66
D_P(0)	A3	I	SubLVDS	Double	Data, positive	1.97
D_P(1)	B1	I	SubLVDS	Double	Data, positive	1.49
D_P(2)	C2	I	SubLVDS	Double	Data, positive	1.44
D_P(3)	A4	I	SubLVDS	Double	Data, positive	3.45
D_P(4)	E5	I	SubLVDS	Double	Data, positive	4.32
D_P(5)	D5	I	SubLVDS	Double	Data, positive	3.27
D_P(6)	E2	I	SubLVDS	Double	Data, positive	1.85
D_P(7)	F2	I	SubLVDS	Double	Data, positive	2.75
DCLK_N	C3	I	SubLVDS	Double	Clock, negative	1.94
DCLK_P	D3	I	SubLVDS	Double	Clock, positive	2.02
CONTROL INPUTS						
LS_WDATA	A12	I	LPSDR[(1)]	Single	Write data for low speed interface	2.16
LS_CLK	B12	I	LPSDR	Single	Clock for low-speed interface	3.38
DMD_DEN_ARSTZ	B14	I	LPSDR	Single	Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	0.67
DMD_DEN_ARSTZ	F1	I	LPSDR	Single		14.90

表 6-1. Pin Functions – Connector Pins (continued)

PIN[1] NAME	PIN[1] NO.	TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH[2] (mm)
LS_RDATA	C13	O	LPSDR	Single	Read data for low-speed interface	2.44
POWER						
V_{BIAS} [3]	A15	Power			Supply voltage for positive bias level at micromirrors	
V_{BIAS} [3]	A5	Power				
V_{OFFSET} [3]	F13	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors	
V_{OFFSET} [3]	F4	Power				
V_{RESET}	B15	Power			Supply voltage for negative reset level at micromirrors	
V_{RESET}	B5	Power				
V_{DD} [3]	C15	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes	
V_{DD}	C5	Power				
V_{DD}	D14	Power				
V_{DD}	D15	Power				
V_{DD}	E14	Power				
V_{DD}	E15	Power				
V_{DD}	F14	Power				
V_{DD}	F15	Power				
V_{DDI}	C14	Power			Supply voltage for SubLVDS receivers	
V_{DDI}	C4	Power				
V_{DDI}	D13	Power				
V_{DDI}	E13	Power				
V_{SS}	A13	Ground			Common return. Ground for all power	
V_{SS}	A14	Ground				
V_{SS}	B13	Ground				
V_{SS}	B2	Ground				
V_{SS}	B3	Ground				
V_{SS}	C12	Ground				
V_{SS}	D1	Ground				
V_{SS}	D12	Ground				
V_{SS}	D2	Ground				
V_{SS}	E12	Ground				
V_{SS}	E3	Ground				
V_{SS}	E4	Ground				
V_{SS}	F12	Ground				

(1) Low speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)*. See JESD209B.
(2) Net trace lengths inside the package:
Relative dielectric constant for the FQP ceramic package is 9.8.
Propagation speed = 11.8 / sqrt (9.8) = 3.769 in/ns.
Propagation delay = 0.265 ns/inch = 265 ps/in = 10.43 ps/mm
(3) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.

表 6-2. Pin Functions – Test Pads

NUMBER	SYSTEM BOARD
A6	Do not connect.
A7	Do not connect.
A8	Do not connect.
A9	Do not connect.
A10	Do not connect.
A11	Do not connect.
F6	Do not connect.
F7	Do not connect.
F8	Do not connect.
F9	Do not connect.
F10	Do not connect.
F11	Do not connect.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted[1])

			MIN	MAX	UNIT
Supply voltage	V_{DD}	Supply voltage for LVCMOS core logic[2] Supply voltage for LPSDR low speed interface	–0.5	2.3	V
	V_{DDI}	Supply voltage for SubLVDS receivers[2]	–0.5	2.3	V
	V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode[2] [3]	–0.5	11	V
	V_{BIAS}	Supply voltage for micromirror electrode[2]	–0.5	19	V
	V_{RESET}	Supply voltage for micromirror electrode[2]	–15	0.5	V
	$\|V_{DDI} – V_{DD}\|$	Supply voltage delta (absolute value)[4]		0.3	V
	$\|V_{BIAS} – V_{OFFSET}\|$	Supply voltage delta (absolute value)[5]		11	V
	$\|V_{BIAS} – V_{RESET}\|$	Supply voltage delta (absolute value)[6]		34	V
Input voltage	Input voltage for other inputs LPSDR[2]		–0.5	V_{DD} + 0.5	V
	Input voltage for other inputs SubLVDS[2] [7]		–0.5	V_{DDI} + 0.5	V
Input pins	$\|V_{ID}\|$	SubLVDS input differential voltage (absolute value)[7]		810	mV
	I_{ID}	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high speed interface DCLK		620	MHz
Environmental	T_{ARRAY} and T_{WINDOW}	Temperature – operational [8]	–20	90	°C
		Temperature – non-operational[8]	–40	90	°C
	$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1[9]		30	°C
	T_{DP}	Dew Point - operating and non-operating		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the ground terminals (V_{SS}). The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable absolute voltage difference between V_{DDI} and V_{DD} may result in excessive current draw.
(5) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(6) Exceeding the recommended allowable absolute voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. SubLVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated in 节 8.6) or of any point along the window edge is defined in 图 8-1. The location of thermal test point TP2 in 图 8-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 8-1. The window test point TP2 shown in 图 8-1 is intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

7.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system.

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	85	°C
T_{DP}	Average dew point temperature (non-condensing) (1)		24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

7.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE(3)					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(4)	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	–14.5	–14	–13.5	V
$\|V_{DDI} – V_{DD}\|$	Supply voltage delta (absolute value)(5)			0.3	V
$\|V_{BIAS} – V_{OFFSET}\|$	Supply voltage delta (absolute value)(6)			10.5	V
$\|V_{BIAS} – V_{RESET}\|$	Supply voltage delta (absolute value)(7)			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low speed interface LS_CLK(8)	108		120	MHz
f_{clock}	Clock frequency for high speed interface DCLK(9)	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE(9)					
$\|V_{ID}\|$	SubLVDS input differential voltage (absolute value). See 图 7-8, 图 7-9.	150	250	350	mV
V_{CM}	Common mode voltage. See 图 7-8, 图 7-9.	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage. See 图 7-8, 图 7-9.	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance. See 图 7-10.	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm

7.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	NOM	MAX	UNIT
ENVIRONMENTAL					
T_{ARRAY}	Array temperature – long-term operational[(10)] [(11)] [(12)] [(13)]	0		40 to 70[(12)]	°C
	Array temperature – short-term operational, 25 hr max[(11)] [(14)]	–20		–10	°C
	Array temperature – short-term operational, 500 hr max[(11)] [(14)]	–10		0	°C
	Array temperature – short-term operational, 500 hr max[(11)] [(14)]	70		75	°C
T_{WINDOW}	Window temperature – operational[(15)] [(16)]			90	°C
$\|T_{DELTA}\|$	Absolute temperature diffference between any point on the window edge and the ceramic test point TP1[(17)]			15	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) [(18)]			24	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) [(19)]	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			6	months
ILL_{UV}	Illumination wavelengths < 420 nm [(10)]			0.68	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 420 nm and 700 nm			Thermally limited	
ILL_{IR}	Illumination wavelengths > 700 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle[(15)]			55	degrees

(1) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the *Recommended Operating Conditions*. No level of performance is implied when operating the device above or below the *Recommended Operating Conditions* limits.
(2) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required.
(3) All voltage values are with respect to the ground pins (V_{SS}).
(4) V_{OFFSET} supply transients must fall within specified max voltages.
(5) To prevent excess current, the supply voltage delta $|V_{DDI} – V_{DD}|$ must be less than the specified limit.
(6) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than the specified limit.
(7) To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit.
(8) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
(9) Refer to the SubLVDS timing requirements in 节 7.7.
(10) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination will reduce device lifetime.
(11) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 8-1 and the package thermal resistance using the calculation in 节 8.6.
(12) Per 图 7-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to 节 8.7 for a definition of micromirror landed duty cycle.
(13) Long-term is defined as the usable life of the device.
(14) Short-term is the total cumulative time over the useful life of the device.
(15) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including at the pond of micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document and may negatively affect lifetime.
(16) Window temperature is the highest temperature on the window edge shown in 图 8-1. The location of thermal test point TP2 in 图 8-1 is intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
(17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 图 8-1. The window test point TP2 shown in 图 8-1 is intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
(18) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.

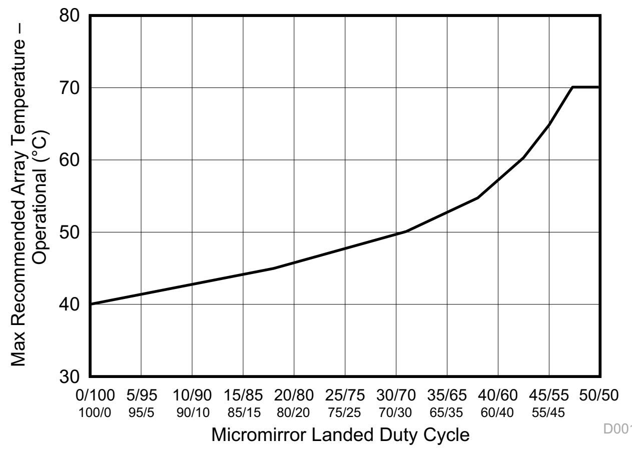


图 7-1. Maximum Recommended Array Temperature – Derating Curve

7.5 Thermal Information

THERMAL METRIC(1)		DLP230NP/NPSE FQP (CLGA) 54 PINS	UNIT
Thermal resistance	Active area to test point 1 (TP1)(1)	9.0	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in 节 7.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area, although other contributions include light energy absorbed by the window aperture and electrical power dissipated by the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

7.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
CURRENT						
I_{DD}	Supply current: V_{DD} (3) (4)	V_{DD} = 1.95 V			65	mA
		V_{DD} = 1.8 V		53		
I_{DDI}	Supply current: V_{DDI} (3) (4)	V_{DDI} = 1.95 V			12	mA
		V_{DD} = 1.8 V		11		
I_{OFFSET}	Supply current: V_{OFFSET} (5) (6)	V_{OFFSET} = 10.5 V			1.5	mA
		V_{OFFSET} = 10 V		1.4		
I_{BIAS}	Supply current: V_{BIAS} (5) (6)	V_{BIAS} = 18.5 V			0.3	mA
		V_{BIAS} = 18 V		0.29		
I_{RESET}	Supply current: V_{RESET} (6)	V_{RESET} = – 14.5 V			– 1.3	mA
		V_{RESET} = – 14 V		– 1.2		
POWER(7)						
P_{DD}	Supply power dissipation: V_{DD} (3) (4)	V_{DD} = 1.95 V			126.75	mW
		V_{DD} = 1.8 V		95.4		
P_{DDI}	Supply power dissipation: V_{DDI} (3) (4)	V_{DDI} = 1.95 V			23.4	mW
		V_{DD} = 1.8 V		19.8		
P_{OFFSET}	Supply power dissipation: V_{OFFSET} (5) (6)	V_{OFFSET} = 10.5 V			15.75	mW
		V_{OFFSET} = 10 V		14		

7.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
P_{BIAS}	Supply power dissipation: V_{BIAS} (5) (6)	V_{BIAS} = 18.5 V			5.55	mW
		V_{BIAS} = 18 V		5.22		
P_{RESET}	Supply power dissipation: V_{RESET} (6)	V_{RESET} = –14.5 V			18.85	mW
		V_{RESET} = –14 V		16.80		
P_{TOTAL}	Supply power dissipation: Total			151.22	190.3	mW
LPSDR INPUT(8)						
$V_{IH(DC)}$	DC input high voltage(9)		0.7 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(9)		–0.3		0.3 × V_{DD}	V
$V_{IH(AC)}$	AC input high voltage(9)		0.8 × V_{DD}		V_{DD} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(9)		–0.3		0.2 × V_{DD}	V
ΔV_T	Hysteresis (V_{T+} – V_{T-})	图 7-10	0.1 × V_{DD}		0.4 × V_{DD}	V
I_{IL}	Low–level input current	V_{DD} = 1.95 V; V_I = 0 V	–100			nA
I_{IH}	High–level input current	V_{DD} = 1.95 V; V_I = 1.95 V			100	nA
LPSDR OUTPUT(10)						
V_{OH}	DC output high voltage	I_{OH} = –2 mA	0.8 × V_{DD}			V
V_{OL}	DC output low voltage	I_{OL} = 2 mA			0.2 × V_{DD}	V
CAPACITANCE						
C_{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			20	pF
C_{OUT}	Output capacitance	f = 1 MHz			10	pF
C_{RESET}	Reset group capacitance	f = 1 MHz; (540 × 120) micromirrors	90		150	pF

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
(2) All voltage values are with respect to the ground pins (V_{SS}).
(3) To prevent excess current, the supply voltage delta |V_{DDI} – V_{DD}| must be less than the specified limit.
(4) Supply power dissipation based on non–compressed commands and data.
(5) To prevent excess current, the supply voltage delta |V_{BIAS} – V_{OFFSET}| must be less than the specified limit.
(6) Supply power dissipation based on 3 global resets in 200 µs.
(7) The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, V_{RESET}. All V_{SS} connections are also required.
(8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
(9) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR)* JESD209B.
(10) LPSDR specification is for pin LS_RDATA.

7.7 Timing Requirements

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

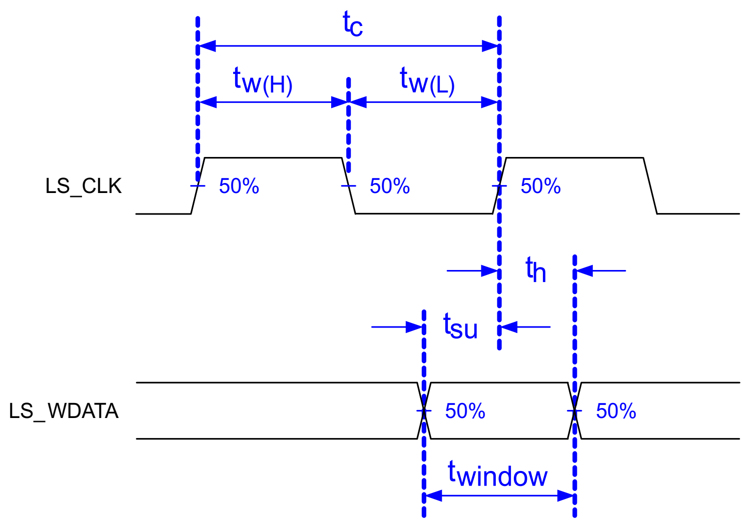
			MIN	NOM	MAX	UNIT
LPSDR						
t_r	Rise slew rate(1)	(30% to 80%) × V_{DD}, 图 7-3	1		3	V/ns
t_f	Fall slew rate(1)	(70% to 20%) × V_{DD}, 图 7-3	1		3	V/ns
t_r	Rise slew rate(2)	(20% to 80%) × V_{DD}, 图 7-3	0.25			V/ns
t_f	Fall slew rate(2)	(80% to 20%) × V_{DD}, 图 7-3	0.25			V/ns
t_c	Cycle time LS_CLK	图 7-2	7.7	8.3		ns
$t_{W(H)}$	Pulse duration LS_CLK high	50% to 50% reference points, 图 7-2	3.1			ns
$t_{W(L)}$	Pulse duration LS_CLK low	50% to 50% reference points, 图 7-2	3.1			ns

7.7 Timing Requirements (continued)

Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

			MIN	NOM	MAX	UNIT
t_{su}	Setup time	LS_WDATA valid before LS_CLK ↑, 图 7-2	1.5			ns
t_h	Hold time	LS_WDATA valid after LS_CLK ↑, 图 7-2	1.5			ns
t_{WINDOW}	Window time(1) (3)	Setup time + hold time, 图 7-2	3			ns
$t_{DERATING}$	Window time derating(1) (3)	For each 0.25 V/ns reduction in slew rate below 1 V/ns, 图 7-5		0.35		ns
SubLVDS						
t_r	Rise slew rate	20% to 80% reference points, 图 7-4	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points, 图 7-4	0.7	1		V/ns
t_c	Cycle time DCLK	图 7-6	1.79	1.85		ns
$t_{W(H)}$	Pulse duration DCLK high	50% to 50% reference points, 图 7-6	0.79			ns
$t_{W(L)}$	Pulse duration DCLK low	50% to 50% reference points, 图 7-6	0.79			ns
t_{su}	Setup time	D(0:7) valid before DCLK ↑ or DCLK ↓, 图 7-6				
t_h	Hold time	D(0:7) valid after DCLK ↑ or DCLK ↓, 图 7-6				
t_{WINDOW}	Window time	Setup time + hold time, 图 7-6, 图 7-7			0.3	ns
$t_{LVDS\text{-}ENABLE+REFGEN}$	Power-up receiver(4)				2000	ns

(1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in 图 7-3.
(2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in 图 7-3.
(3) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 to 3.7 ns.
(4) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.



Low-speed interface is LPSDR and adheres to 节 7.6 and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* JESD209B.

图 7-2. LPSDR Switching Parameters

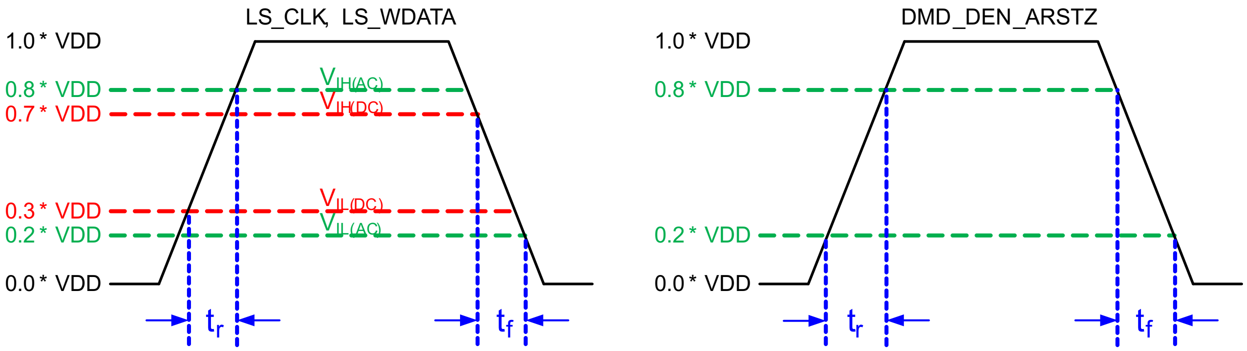


图 7-3. LPSDR Input Rise and Fall Slew Rate

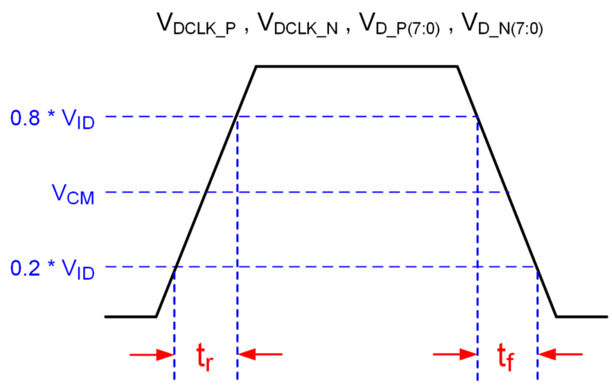


图 7-4. SubLVDS Input Rise and Fall Slew Rate

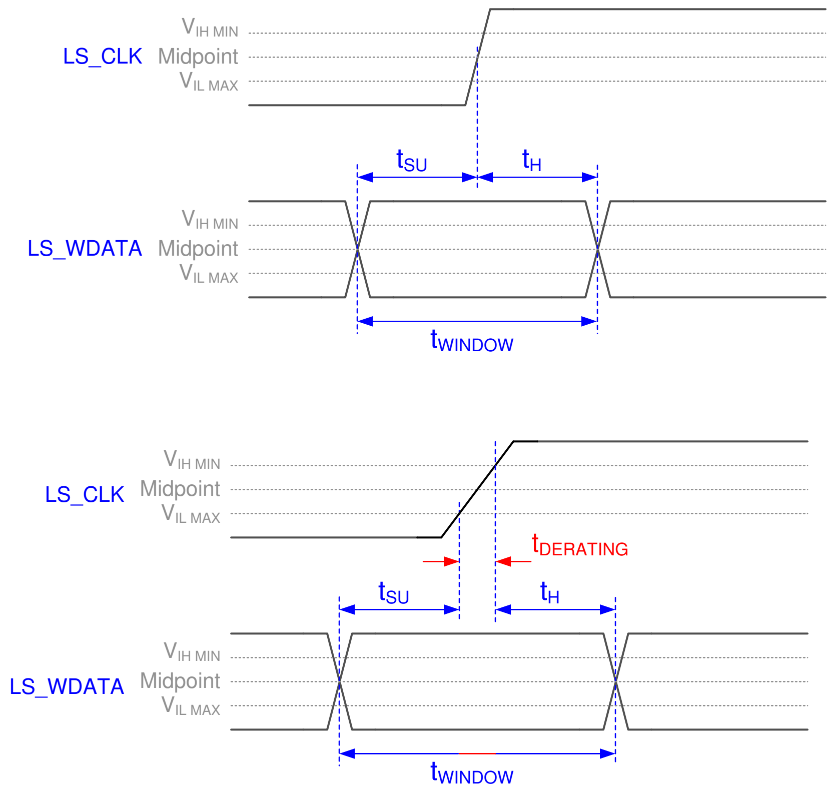


图 7-5. Window Time Derating Concept

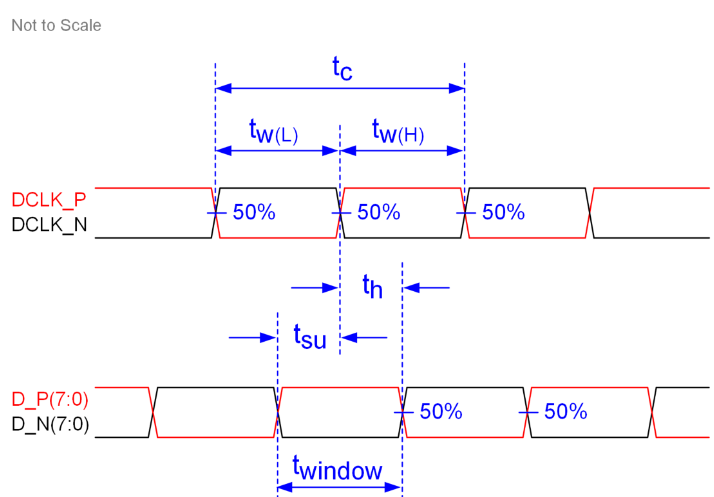
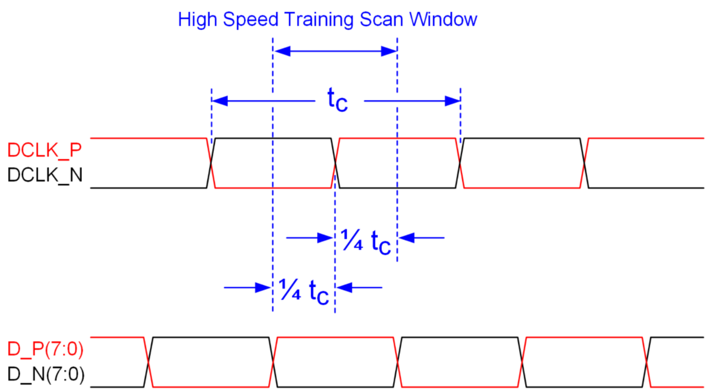


图 7-6. SubLVDS Switching Parameters



Note: Refer to 节 8.3.3 for details.

图 7-7. High-Speed Training Scan Window

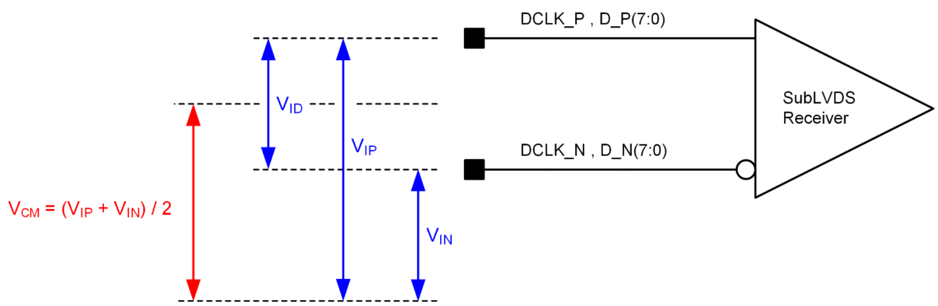


图 7-8. SubLVDS Voltage Parameters

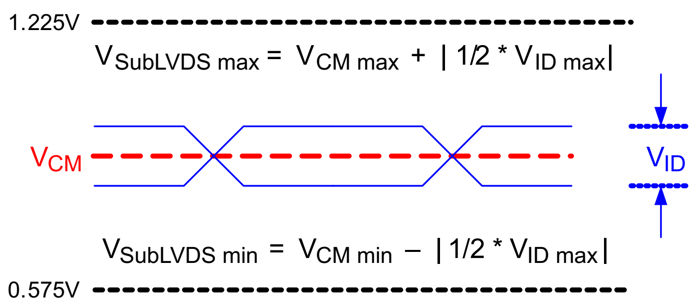


图 7-9. SubLVDS Waveform Parameters

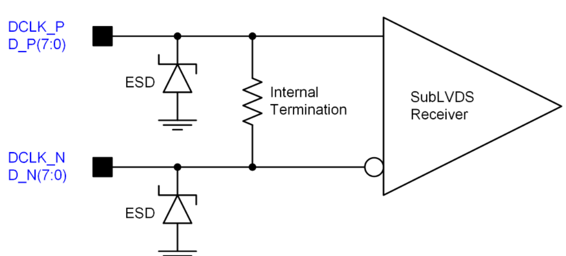


图 7-10. SubLVDS Equivalent Input Circuit

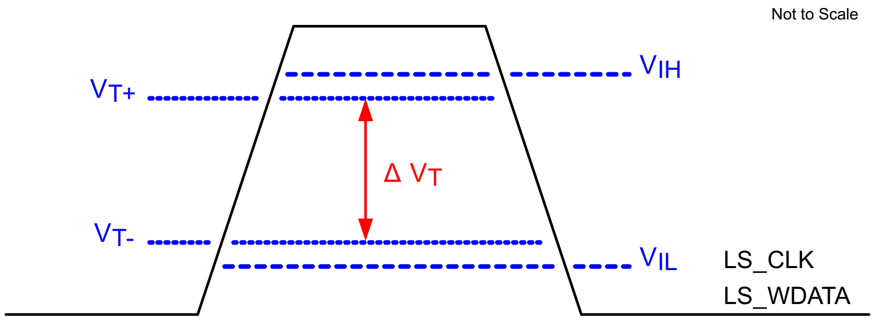


图 7-11. LPSDR Input Hysteresis

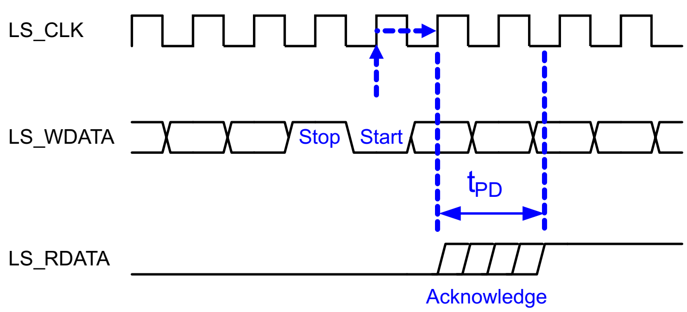
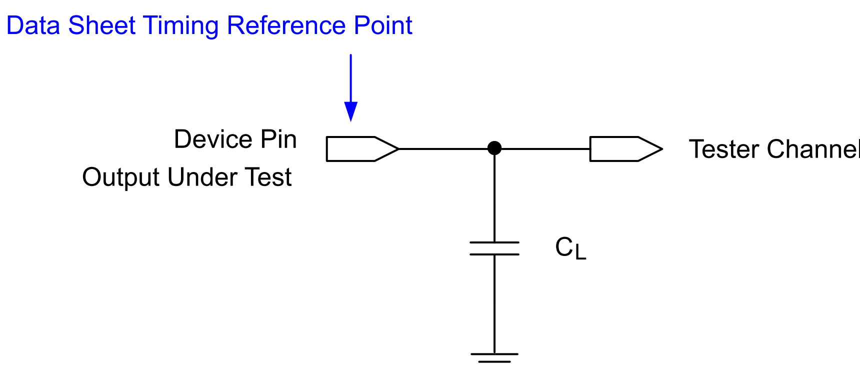


图 7-12. LPSDR Read Out



See 节 8.3.4 for more information.

图 7-13. Test Load Circuit for Output Propagation Measurement

7.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted). (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Output propagation, clock to Q, rising edge of LS_CLK input to LS_RDATA output. See 图 7-12.	C_L = 5 pF			11.1	ns
		C_L = 10 pF			11.3	ns
		C_L = 85 pF			15	ns
	Slew rate, LS_RDATA		0.5			V/ns
	Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics comply with the values in 节 7.4 unless otherwise noted.

7.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:				
• Thermal interface area (1)			45	N
• Clamping and electrical interface area (1)			100	N

(1) Uniformly distributed within area shown in 图 7-14.

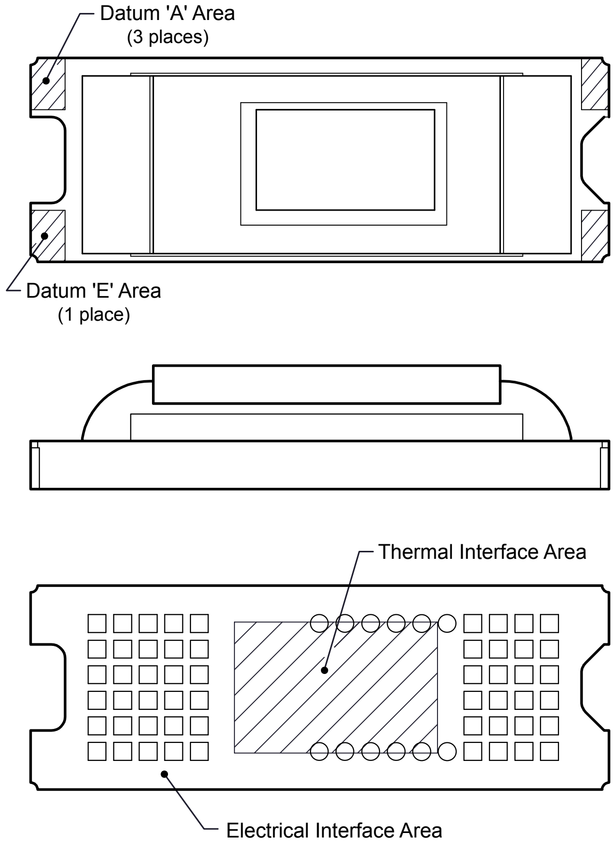


图 7-14. System Interface Loads

7.10 Micromirror Array Physical Characteristics

PARAMETER		VALUE	UNIT
Number of active columns[(1)]	See 图 7-15.	960	micromirrors
Number of active rows[(1)]	See 图 7-15.	540	micromirrors
Micromirror (pixel) pitch	See 图 7-16.	5.4	µm
Micromirror active array width	Micromirror pitch × number of active columns; see 图 7-15	5.184	mm
Micromirror active array height	Micromirror pitch × number of active rows; see 图 7-15.	2.916	mm
Micromirror active border	Pond of micromirror (POM)[(2)]	20	micromirrors/side

(1) The fast switching speed of the DMD micromirrors combined with advanced DLP image processing algorithms enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 1920 × 1080 pixel image being displayed.
(2) The structure and qualities of the border around the active array include a band of partially functional micromirrors called the POM. These micromirrors are structurally or electrically prevented from tilting toward the bright or ON state, but require an electrical bias to tilt toward OFF.

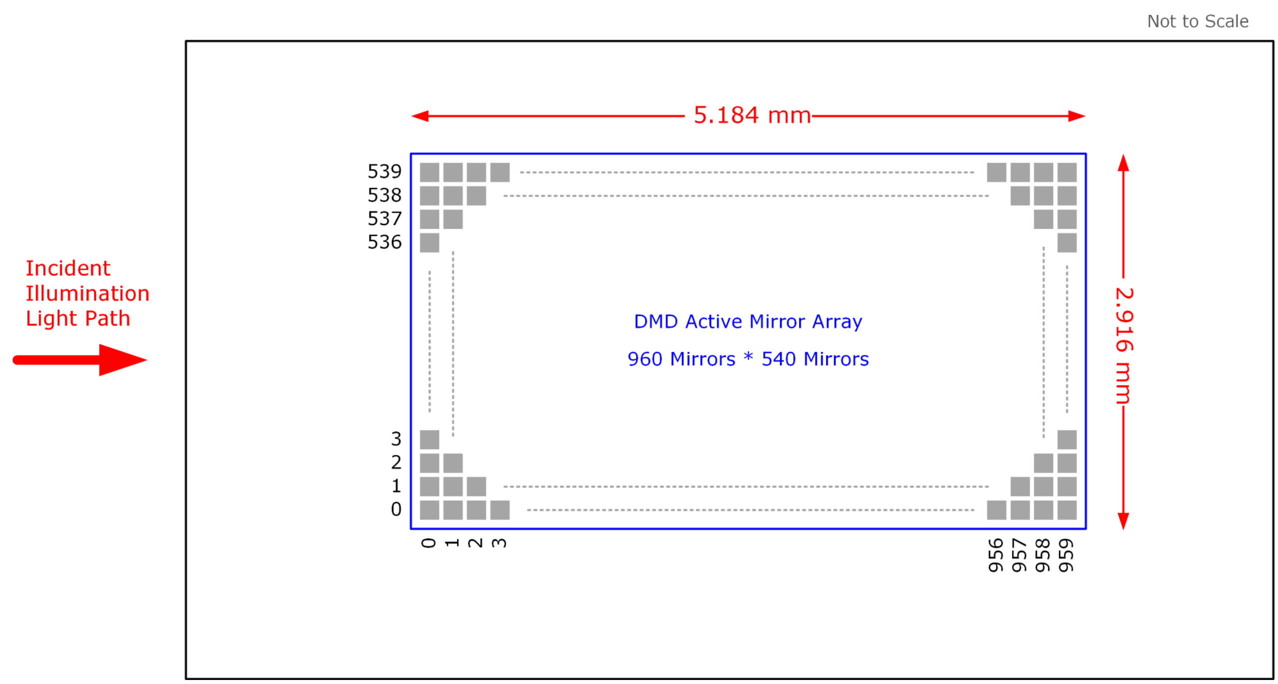


图 7-15. Micromirror Array Physical Characteristics

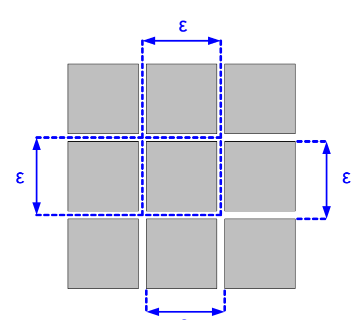


图 7-16. Mirror (Pixel) Pitch

7.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state[(1)]		17		°
Micromirror tilt angle tolerance[(2) (3) (4) (5)]			–1.4		1.4	°
Micromirror tilt direction[(6) (7)]		Landed ON state		180		°
		Landed OFF state		270		
Micromirror crossover time[(8)]		Typical performance		1	3	µs
Micromirror switching time[(9)]		Typical performance	10			
Image performance[(10)]	Bright pixel(s) in active area [(11)]	Gray 10 screen [(12)]			0	micromirrors
	Bright pixel(s) in the POM [(13)]	Gray 10 screen [(12)]			1	
	Dark pixel(s) in the active area [(14)]	White screen			4	
	Adjacent pixel(s) [(15)]	Any screen			0	
	Unstable pixel(s) in active area [(16)]	Any screen			0	

(1) Measured relative to the plane formed by the overall micromirror array.
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See 图 7-17 .
(7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
(8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
(9) The minimum time between successive transitions of a micromirror
(10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
    Test set degamma shall be linear
    Test set brightness and contrast shall be set to nominal
    The diagonal size of the projected image shall be a minimum of 20 inches
    The projections screen shall be 1X gain
    The projected image shall be inspected from a 38-inch minimum viewing distance
    The image shall be in focus during all image quality tests
(11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
(12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
    Red = 10/255
    Green = 10/255
    Blue = 10/255
(13) POM definition: Rectangular border of off-state mirrors surrounding the active area
(14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
(15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
(16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image.

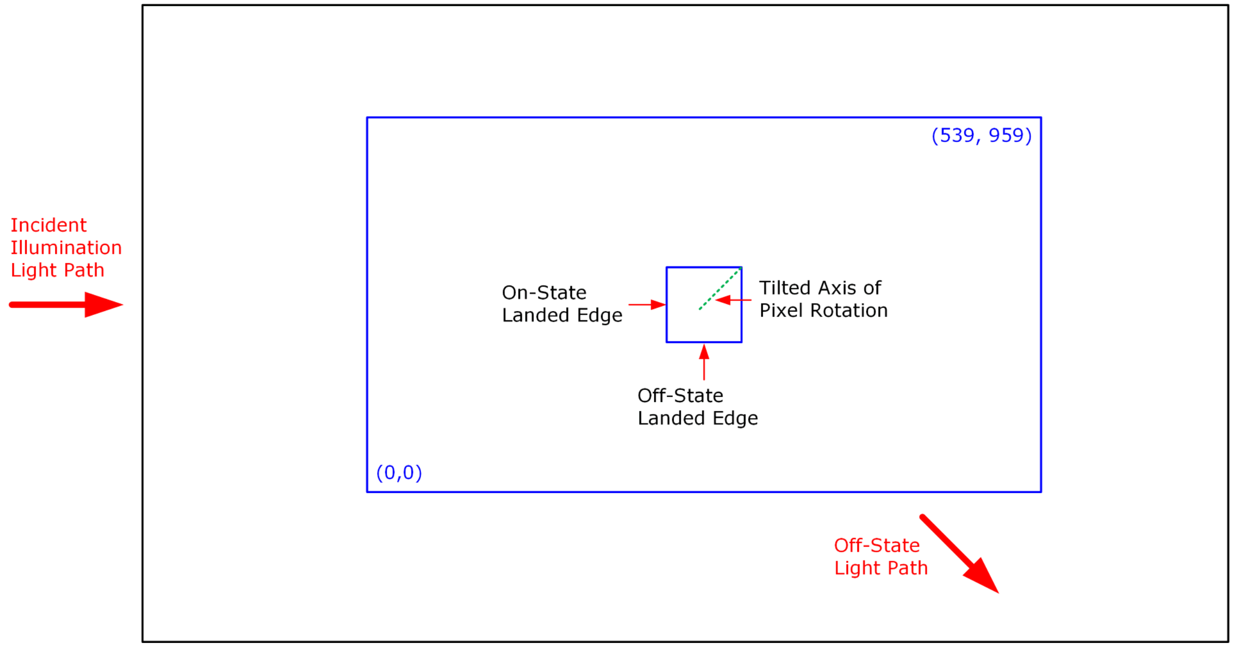


图 7-17. Landed Pixel Orientation and Tilt

7.12 Window Characteristics

PARAMETER[(1)]		MIN	NOM	MAX	UNIT
Window material designation			Corning Eagle XG		
Window refractive index	At wavelength 546.1 nm		1.5119		
Window aperture[(2)]				See [(2)]	
Illumination overfill[(3)]				See [(3)]	
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 to 680 nm. Applies to all angles 0° to 30° AOI	97%			
	Average over the wavelength range 420 to 680 nm. Applies to all angles 30° to 45° AOI	97%			

(1) See 节 8.5 for more information.
(2) See the package mechanical characteristics for details regarding the size and location of the window aperture.
(3) The active area of the device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.

7.13 Chipset Component Usage Specification

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The is a component of one or more DLP® chipsets. Reliable function and operation of the requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology consists of the TI technology and devices used for operating or controlling a DLP DMD.

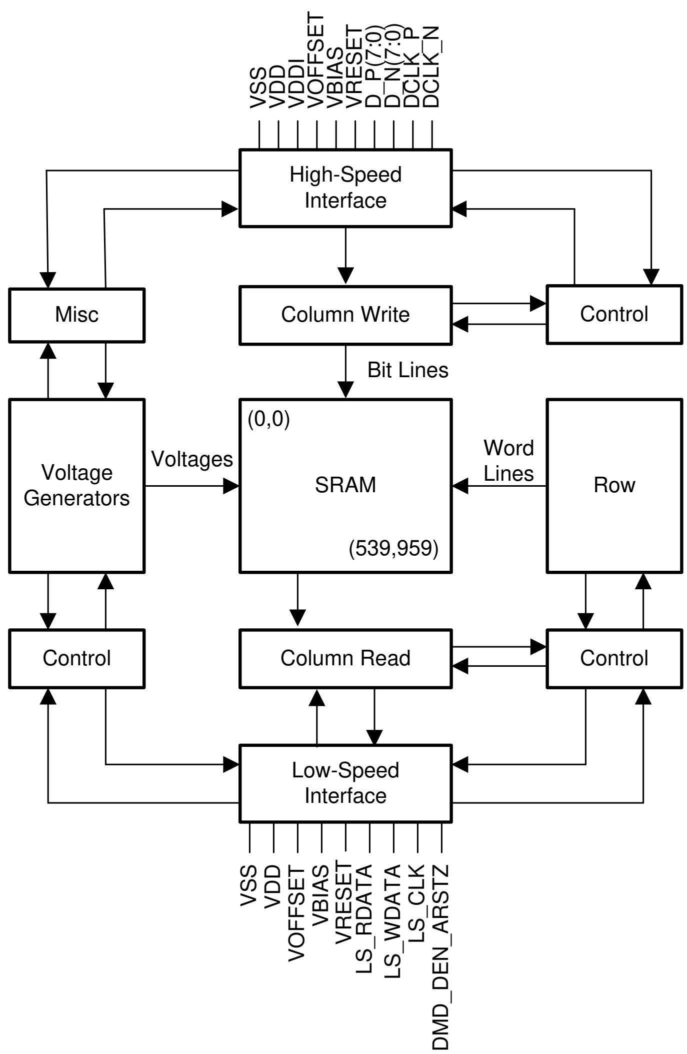
8 Detailed Description

8.1 Overview

The DLP230NP and DLP230NPSE devices are 0.23-inch diagonal spatial light modulators of aluminum micromirrors. The micromirror array size is 960 columns by 540 rows in a square micromirror arrangement. The fast switching speed of the DMD micromirrors, combined with advanced DLP image processing algorithms, enables each micromirror to display four distinct pixels on the screen during every frame, resulting in a full 1920 × 1080 pixel image display. The electrical interface is sub-low voltage differential signaling (SubLVDS) data.

For the DLP230NP device, the DLPA2000, DLPA2005, DLPA3000, and DLPA3005 PMIC/LED drivers support this chipset. Currently, only the DLPA3000 driver supports the DLP230NPSE DMD. To ensure reliable operation, the DLP230NP/NPSE DMD must always be used with the DLPC34x6 ZVB display controller and the DLPA2000, DLPA2005, DLPA3000, or DLPA3005 PMIC/LED driver.

8.2 Functional Block Diagram



A. Details omitted for clarity.

8.3 Feature Description

8.3.1 Power Interface

The power management IC DLPA2000, DLPA2005, DLPA3000, and DLPA3005 contain three regulated DC supplies for the DMD reset circuitry: V_{BIAS}, V_{RESET} and V_{OFFSET}, as well as the two regulated DC supplies for the DLPC34x6ZVB controller.

8.3.2 Low-Speed Interface

The low speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low – speed clock, and LS_WDATA is the low speed data input.

8.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs with a dedicated clock.

8.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 图 7-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

8.4 Device Functional Modes

The DLPC34x6 controller manages the functional modes of the DMD. For more information, download the controller data sheet or contact a TI applications engineer.

8.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

8.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the ON optical path from any other light path, including undesirable flat – state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display’s border and/or active area could occur.

8.5.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display’s border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

8.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

8.6 Micromirror Array Temperature Calculation

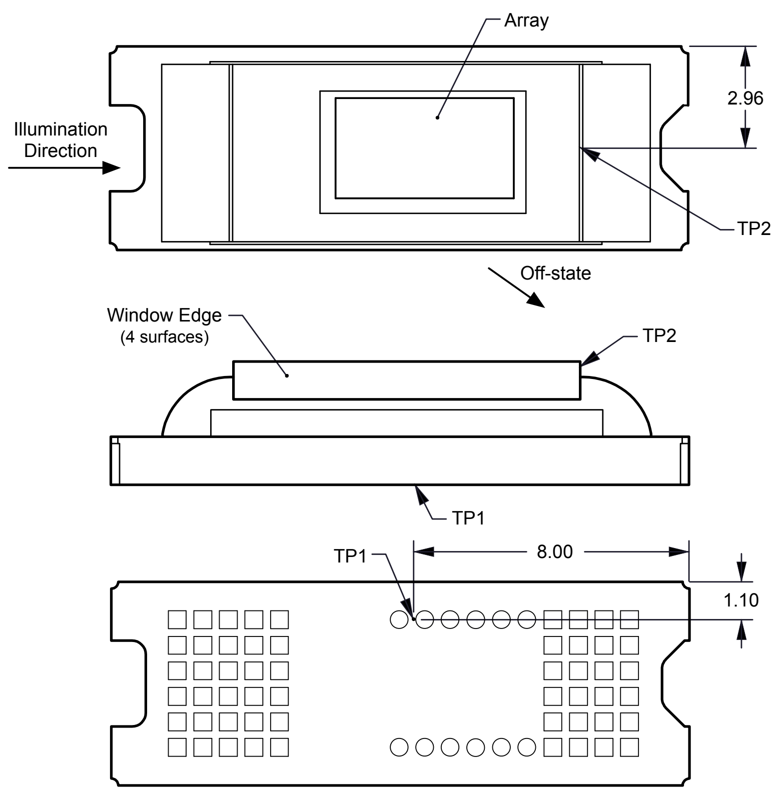


图 8-1. DMD Thermal Test Points

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test point TP1 in 图 8-1) is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY-TO-CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL)$$

where

- T_{ARRAY} = Computed DMD array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in 图 8-1
- $R_{ARRAY-TO-CERAMIC}$ = Thermal resistance from array to TP1 on ceramic (°C/W) specified in 节 7.5
- Q_{ARRAY} = Total (electrical + absorbed) DMD power on array (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W)
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. Nominal electrical power dissipation to use when calculating array temperature is 0.17 W. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant C_{L2W} is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

Sample calculations for typical projection application:

$T_{CERAMIC}$ = 55°C (measured)

SL = 200 lm (measured)

$Q_{ELECTRICAL}$ = 0.17 W

C_{L2W} = 0.00266 W/lm

Q_{ARRAY} = 0.17 W + (0.00266 W/lm × 200 lm) = 0.702 W

T_{ARRAY} = 55°C + (0.702 W × 9°C/W) = 61.32°C

8.7 Micromirror Landed-On/Landed-Off Duty Cycle

8.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 75/25 indicates that the referenced pixel is in the ON state 75% of the time and in the OFF state 25% of the time, whereas 25/75 would indicate that the pixel is in the ON state 25% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) nominally add to 100.

8.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

8.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the DMD’s usable life. This is quantified in the de-rating curve shown in 图 7-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature that the DMD should be operated at for a given long-term average landed duty cycle.

8.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the nominal landed duty cycle of a given pixel is determined by the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience very close to a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience very close to a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the gray scale value, as shown in 表 8-1.

表 8-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Nominal Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color scale value (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the nominal landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_%×Blue_Scale_Value) (1)

where

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that red, green, and blue are displayed (respectively) to achieve the desired white point.

For example, assuming that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the nominal landed duty cycle for various combinations of red, green, blue color intensities would be as shown in 表 8-2.

表 8-2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

Red Scale Value	Green Scale Value	Blue Scale Value	Nominal Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLP controller DLPC3434ZVB, the three functions which influence the actual landed duty cycle are gamma, IntelliBright™, and bitplane sequencing rules.

Gamma is a power function of the form Output_Level = A × Input_Level^{Gamma}, where A is a scaling factor that is typically set to 1.

In the DLPC3434ZVB controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in 图 8-2.

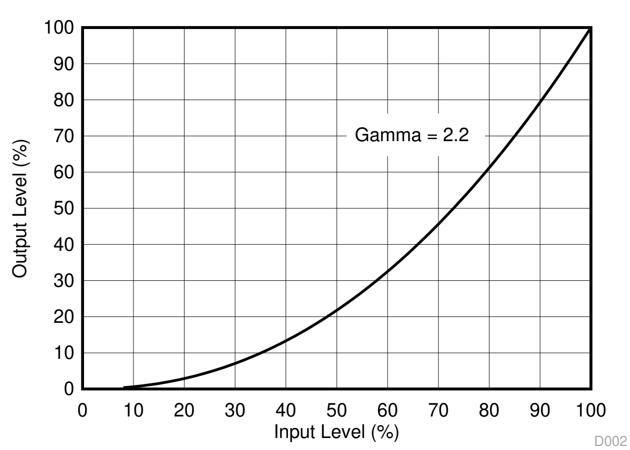


图 8-2. Example of Gamma = 2.2

For example, from 图 8-2, if the gray scale value of a given input pixel is 40% (before gamma is applied), then the gray scale value is 13% after gamma is applied. This reduction indicates that gamma has a direct impact on the displayed gray scale level of a pixel, and it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithm for content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the gray scale level of each pixel.

But while the amount of gamma applied to every pixel of every frame is constant (the exponent, gamma, is constant), CAIC and LABB are both adaptive functions that can apply different amounts of either boost or compression to every pixel of every frame.

Give consideration to any image processing which occurs before the DLPC34x6 controller.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC34x6 controller. The new high tilt pixel in the side-illuminated DMD increases brightness performance and enables a smaller system footprint for thickness-constrained applications. Applications of interest include projection technology embedded in display devices such as ultra low-power battery operated mobile accessory projectors, phones, tablets, ultra mobile low end smart TVs, and virtual assistants.

The PMIC/LED driver strictly controls the DMD power-up and power-down sequencing. Refer to 节 10 for power-up and power-down specifications. To ensure reliable operation, the DMD must always be used with the DLPC34x6 display controller and either the DLPA2000, DLPA2005, DLPA3000, or DLPA3005 PMIC/LED driver.

9.2 Typical Application

A common application when using a DLP230NP/NPSE DMD and a DLPC34x6 is for creating a Pico projector that can be used as an accessory to a smartphone, tablet, or a laptop. The DLPC34x6 controller in the Pico projector receives images from a multimedia front end within the product as shown in 图 9-1.

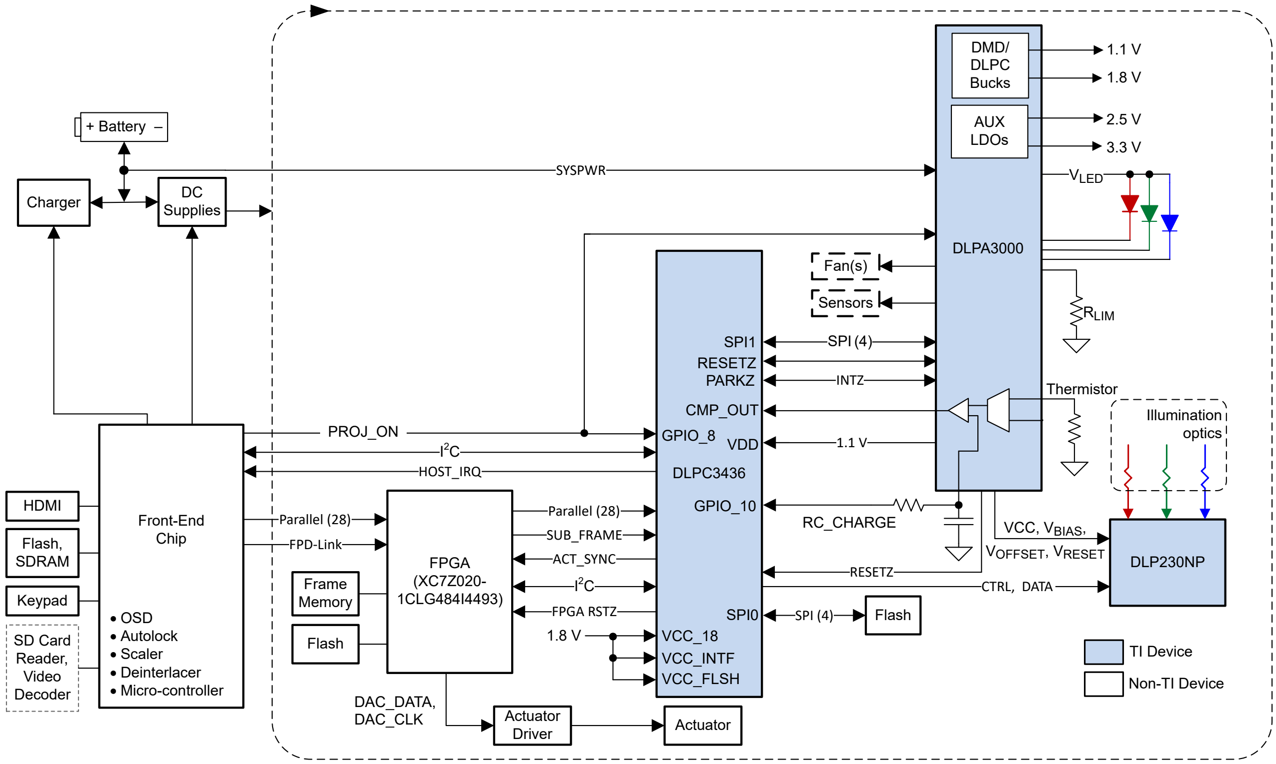


图 9-1. Typical Application Diagram

9.2.1 Design Requirements

A Pico projector is created by using a DLP chipset with a DLP230NP/NPSE (.23 1080p) digital micromirror device (DMD), a DLPC34x6 controller, a XC7Z020-1CLG484|4493 FPGA, and a DLPAxxxx PMIC/LED driver. The DLPC34x6 controller performs the digital image processing, the DLPA2000/2005/3000/3005 provides the needed analog functions for the projector, and the DLP230NP/NPSE DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chipset, other chips are needed. At a minimum, a flash part is needed to store the DLPC34x6 controller software.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the Pico projector.

Power to the entire Pico projector can be controlled with a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws microamps of current on SYSPWR. When PROJ_ON is set low, the 1.8-V supply can remain at 1.8 V and used by other non-projector sections of the product. If PROJ_ON is low, the PMIC/LED driver does not draw current on the 1.8-V supply.

9.2.2 Detailed Design Procedure

For connecting the DLPC34x6 controller, the DLPAxxxx PMIC/LED driver, and the (.23 1080p) DMD, see the reference design schematic. The reference design describes an application on which a very small circuit board can be used. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

An optical OEM that specializes in designing optics for DLP projectors typically supplies the optical engine including mounted LED packages and mounted DMD.

9.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in 图 9-2. For the LED currents shown, it is assumed that the same current amplitude is applied to the red, green, and blue LEDs.

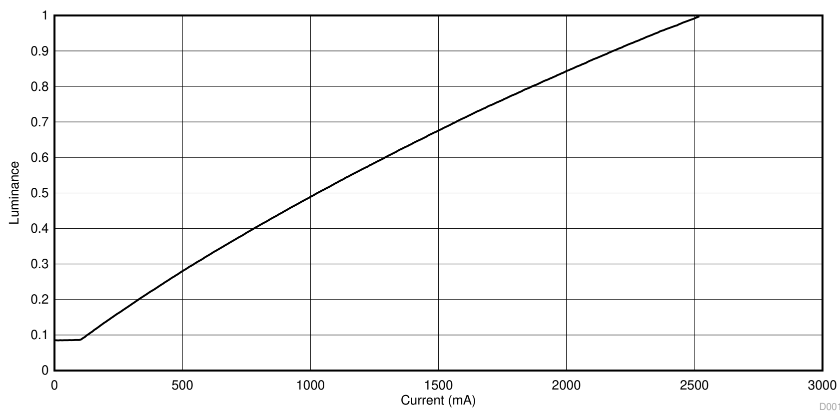


图 9-2. Luminance vs LED Current

10 Power Supply Recommendations

The following power supplies are all required to operate the DMD: V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET}. All V_{SS} connections are also required. DMD power-up and power-down sequencing is strictly controlled by the DLPA2000/2005/3000 devices.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

V_{DD}, V_{DDI}, V_{OFFSET}, V_{BIAS}, and V_{RESET} power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the specified requirements results in a significant reduction in the DMD reliability and lifetime. Refer to 图 10-2. V_{SS} must also be connected.

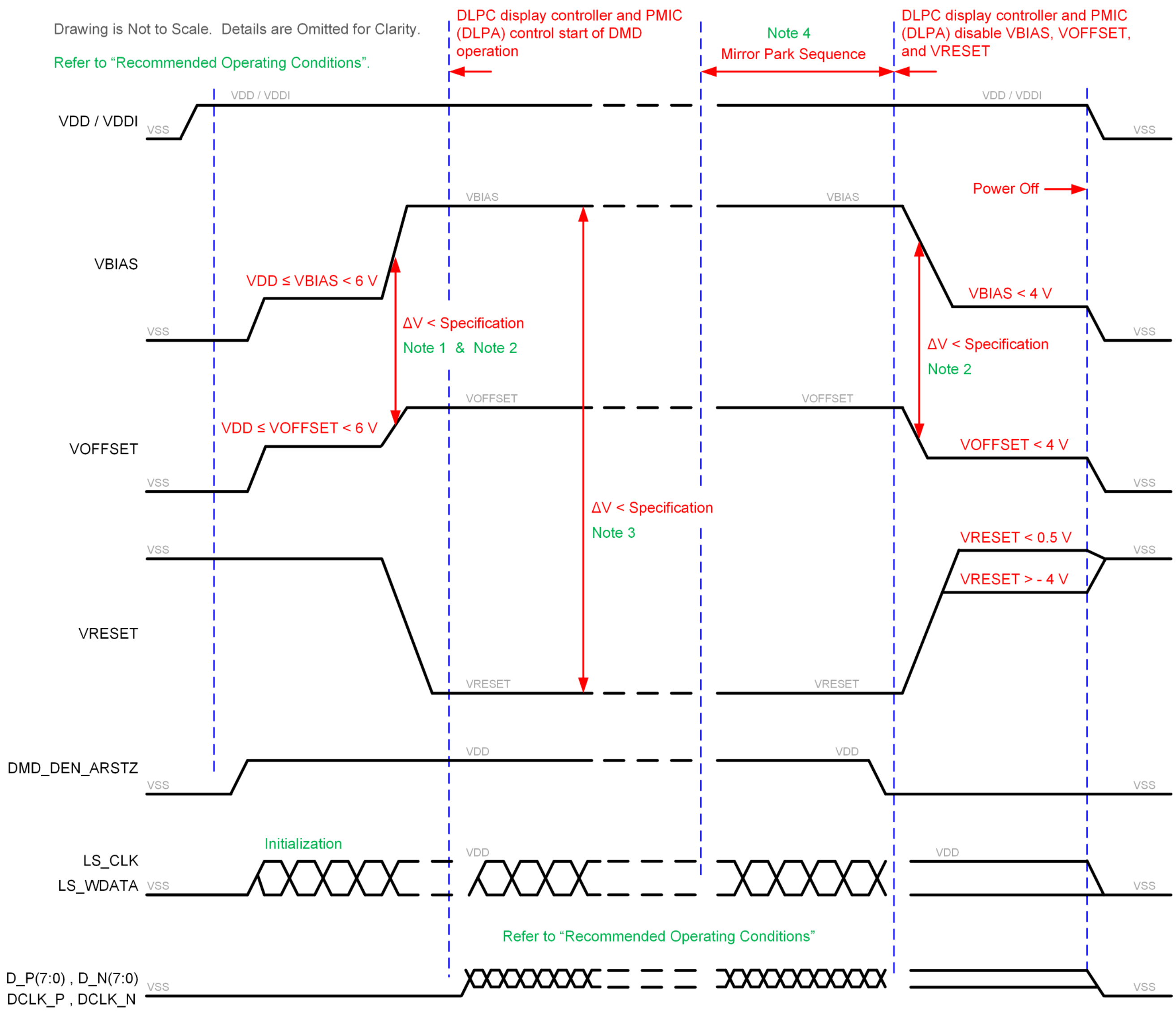
10.1 Power Supply Power-Up Procedure

- During power-up, V_{DD} and V_{DDI} must always start and settle before V_{OFFSET}, V_{BIAS}, and V_{RESET} voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in 节 7.4. Refer to 图 10-2 for power-up delay requirements.
- During power-up, the DMD’s LPSDR input pins shall not be driven high until after V_{DD} and V_{DDI} have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in 图 10-1.

10.2 Power Supply Power-Down Procedure

- The power-down sequence is the reverse order of the previous power-up sequence. V_{DD} and V_{DDI} must be supplied until after V_{BIAS}, V_{RESET}, and V_{OFFSET} are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving V_{BIAS} prior to V_{OFFSET}, but it is a strict requirement that the delta between V_{BIAS} and V_{OFFSET} must be within the specified limit shown in 节 7.4 (Refer to Note 2 for 图 10-1).
- During power-down, the DMD’s LPSDR input pins must be less than V_{DDI}, the specified limit shown in 节 7.4.
- During power-down, there is no requirement for the relative timing of V_{RESET} with respect to V_{OFFSET} and V_{BIAS}.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in 图 10-1.

10.3 Power Supply Sequencing Requirements



A. Refer to 表 10-1 and 图 10-2 for critical power-up sequence delay requirements.

B. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{OFFSET}|$ must be less than specified in 节 7.4. OEMs may find that the most reliable way to ensure this is to power V_{OFFSET} prior to V_{BIAS} during power-up and to remove V_{BIAS} prior to V_{OFFSET} during power-down. Refer to 表 10-1 and 图 10-2 for power-up delay requirements.

C. To prevent excess current, the supply voltage delta $|V_{BIAS} – V_{RESET}|$ must be less than the specified limit shown in 节 7.4.

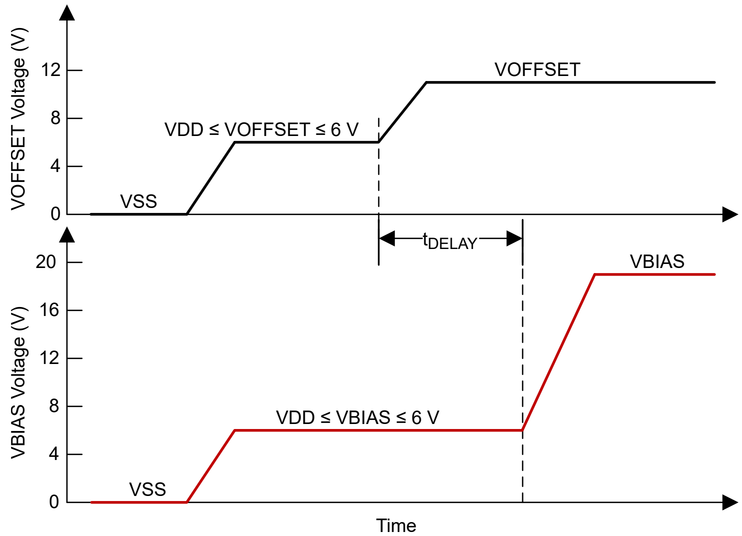
D. When system power is interrupted, the DLPA2000/2005/3000 initiates hardware power-down that disables V_{BIAS}, V_{RESET} and V_{OFFSET} after the micromirror park sequence.

E. Drawing is not to scale and details are omitted for clarity.

图 10-1. Power Supply Sequencing Requirements (Power Up and Power Down)

表 10-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from V_{OFFSET} power up to V_{BIAS} power up	2		ms
V_{OFFSET}	Supply voltage level at beginning of power – up sequence delay (see 图 10-2)		6	V
V_{BIAS}	Supply voltage level at end of power – up sequence delay (see 图 10-2)		6	V



Refer to 表 10-1 for V_{OFFSET} and V_{BIAS} supply voltage levels during power-up sequence delay.

图 10-2. Power-Up Sequence Delay Requirement

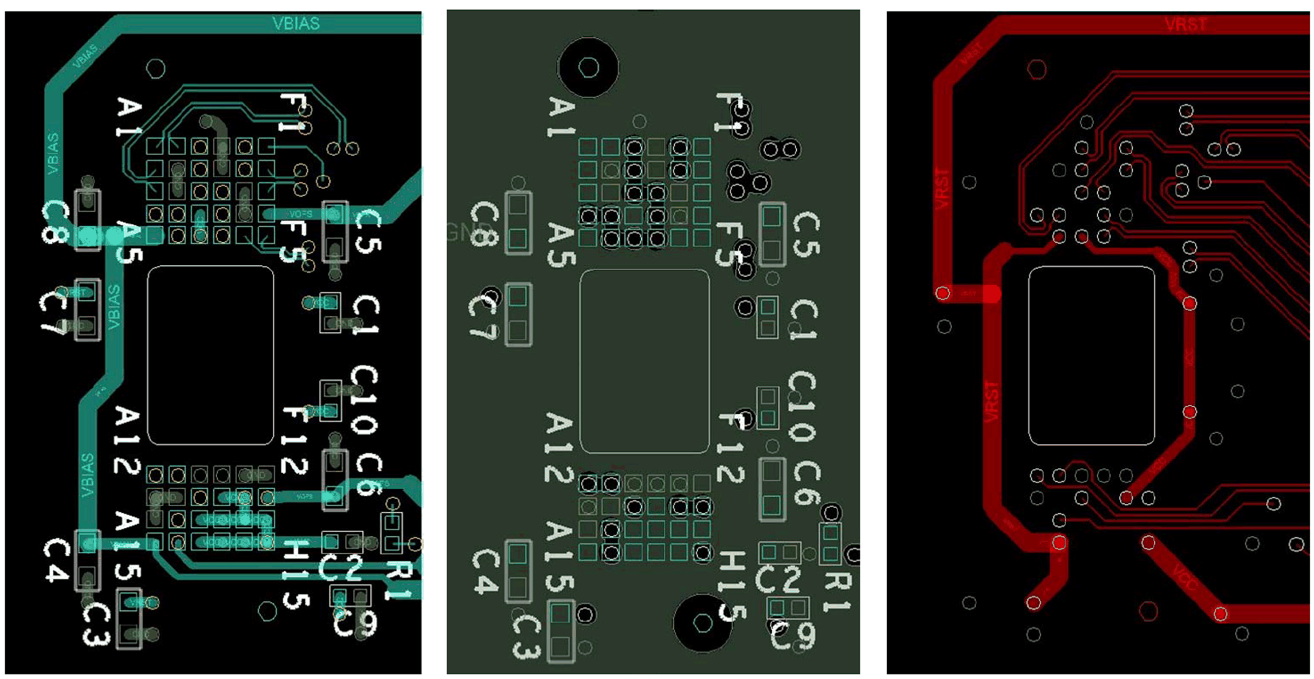
11 Layout

11.1 Layout Guidelines

The DMD connects to a PCB or a flex circuit using an interposer. For additional layout guidelines regarding length matching, and impedance, see the DLPC34x6 controller data sheet. For a detailed layout example refer to the layout design files. Some layout guidelines for routing to the DMD are:

- Match lengths for the LS_WDATA nd LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 图 11-1.
- Minimum of two 100-nF (25 V) capacitors - one close to V_{BIAS} pin. Capacitors C4 and C8 in 图 11-1.
- Minimum of two 100-nF (25 V) capacitors - one close to each V_{RST} pin. Capacitors C3 and C7 in 图 11-1.
- Minimum of two 220-nF (25 V) capacitors - one close to each V_{OFS} pin. Capacitors C5 and C6 in 图 11-1.
- Minimum of four 100-nF (6.3 V) capacitors - two close to each side of the DMD. Capacitors C1, C2, C9 and C10 in 图 11-1.

11.2 Layout Example



Layer 1 (top)   Layer 2 (gnd)   Layer 3 (bottom)

图 11-1. Power Supply Connections

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.1.2 Device Nomenclature

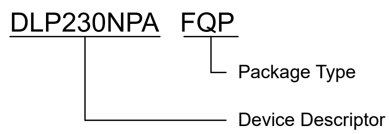


图 12-1. Part Number Description

12.1.3 Device Markings

The device marking includes the legible character string GHJJJJK. DLP230NPAFQP is the device marking.

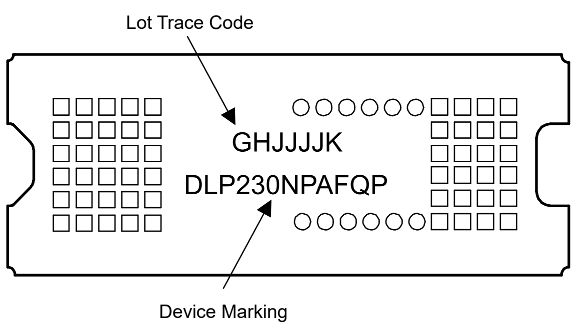


图 12-2. DMD Marking

12.2 Chipset Resources

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 12-1. Chipset Resources

CHIP SET COMPONENTS	PRODUCT FOLDER	ORDERING and QUALITY	TECHNICAL DOCUMENTATION	DESIGN and DEVELOPMENT	SUPPORT and TRAINING
DLP230NP/NPSE	Click here	Click here	Click here	Click here	Click here
DLPA2000	Click here	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here
DLPA3005	Click here	Click here	Click here	Click here	Click here
DLPC34x6	Click here	Click here	Click here	Click here	Click here

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

IntelliBright™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of TI.
所有商标均为其各自所有者的财产。

12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP230NPAFQP	ACTIVE	CLGA	FQP	54	140	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples
DLP230NPSEFQP	ACTIVE	CLGA	FQP	54	140	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

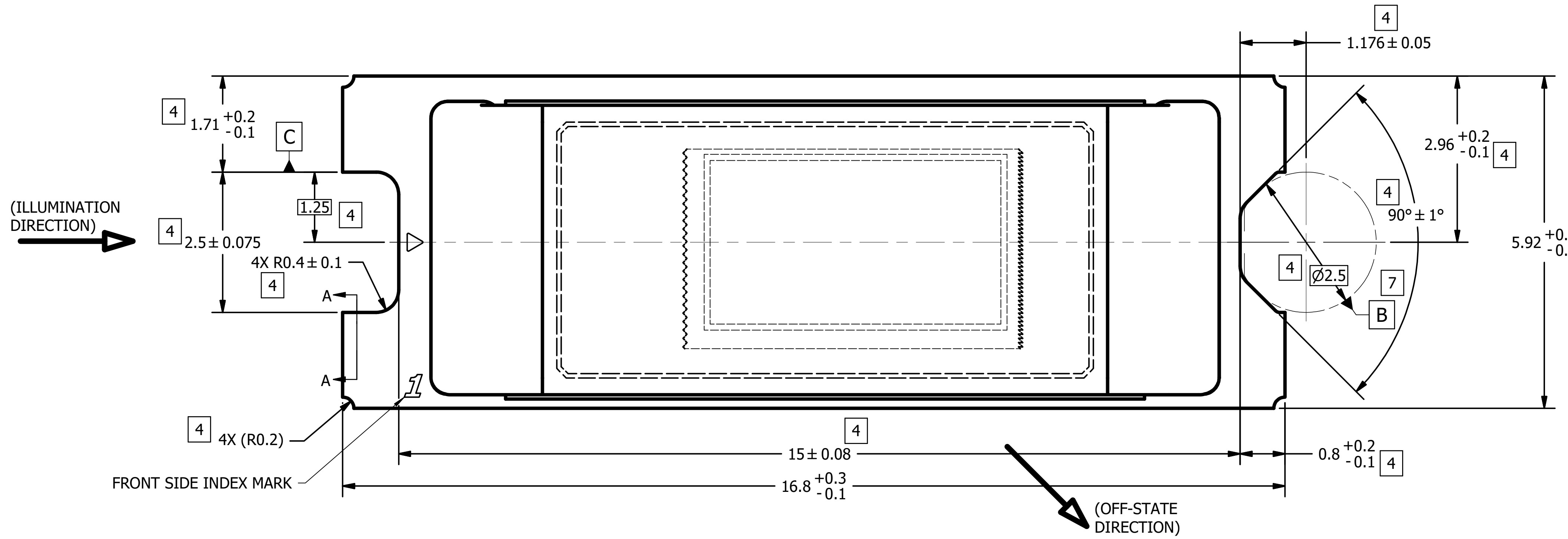
DWG NO. 2515699 SH 1

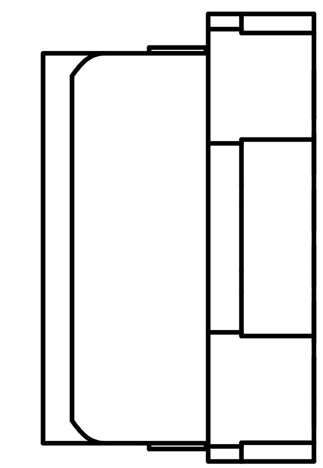
REVISIONS

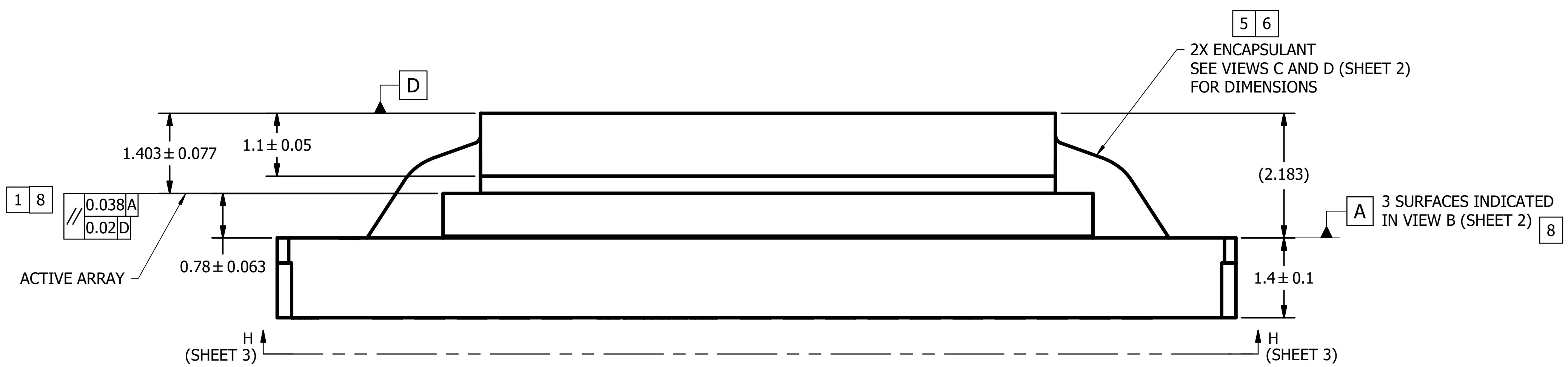
REV	DESCRIPTION	DATE	BY
A	ECO 2168534: INITIAL RELEASE	9/5/2017	BMH
B	ECO 2168970: CORRECT SUBSTRATE THICKNESS TOL; ENLARGE APERTURE SLIGHTLY	9/15/17	BMH
C	ECO 2186788: ADD APERTURE SLOT PICTORIALLY	4/7/2020	BMH

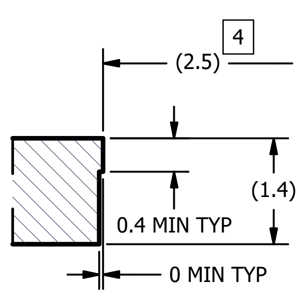
NOTES UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
3. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
4. NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
5. ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
6. ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
7. DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
8. WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.









SECTION A-A
(ROTATED 90°)
SCALE 20 : 1

NEXT ASSY	USED ON
	0314DA

APPLICATION

THIRD ANGLE PROJECTION

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
  - ANGLES ± 1°
  - 2 PLACE DECIMALS ± 0.25
  - 1 PLACE DECIMALS ± 0.50
- ~~DIMENSIONAL LIMITS APPLY BEFORE PROCESSES~~
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- ~~REMOVE ALL BURRS AND SHARP EDGES~~
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

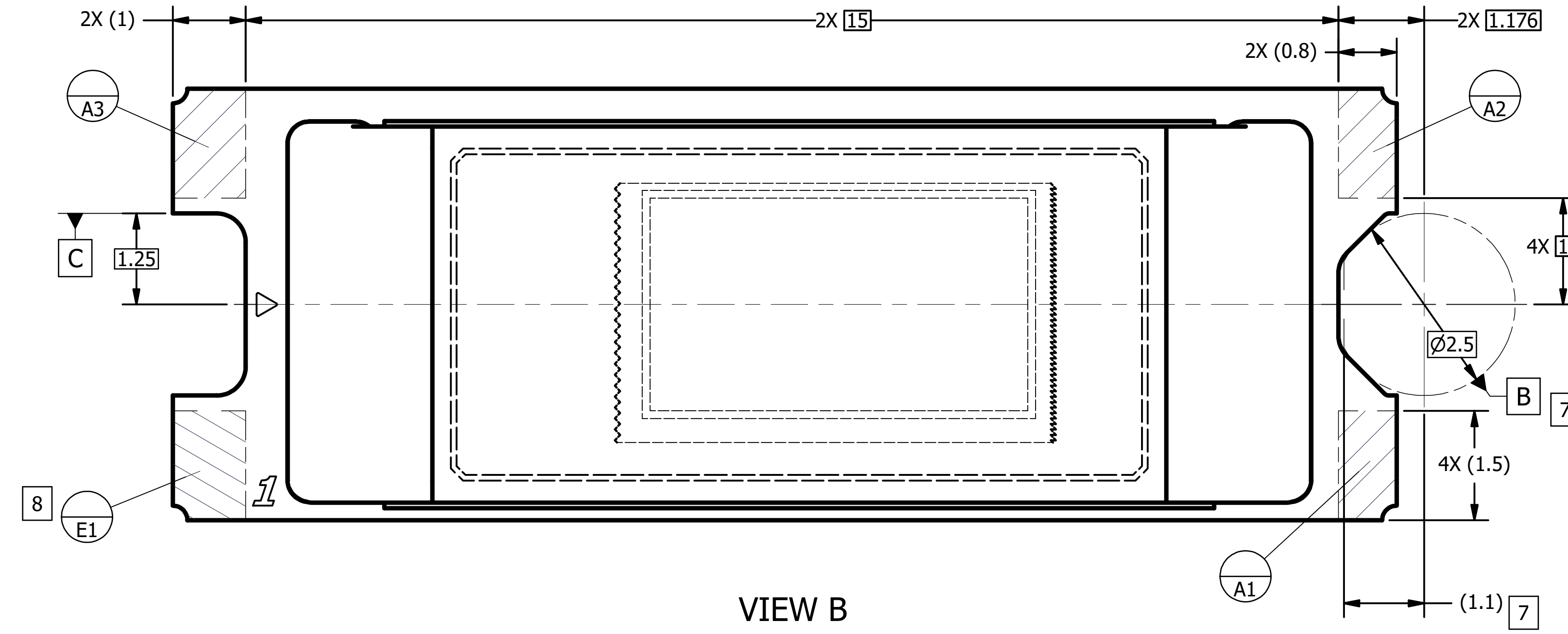
		DATE
DRAWN	B. HASKETT	9/5/2017
ENGINEER	B. HASKETT	9/5/2017
QA/CE	P. KONRAD	9/10/2017
CM	J. GRIMMETT	9/6/2017
	M. DORAK	9/5/2017
APPROVED	R. LONG	9/11/2017

TEXAS INSTRUMENTS
Dallas Texas

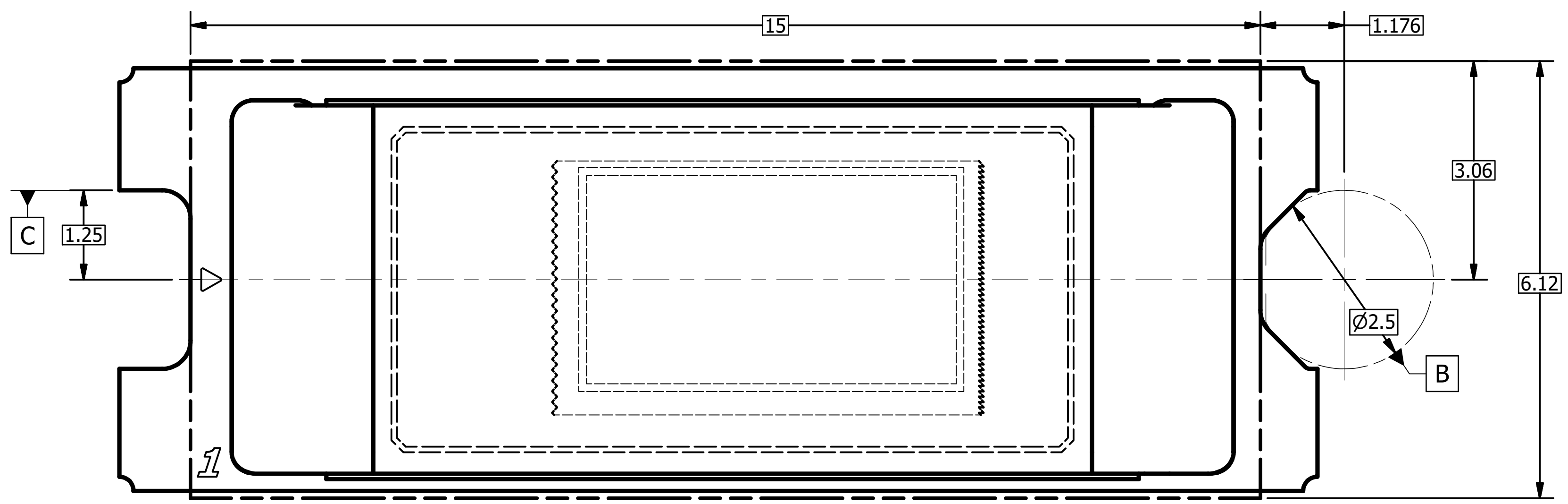
TITLE
ICD, MECHANICAL, DMD, .23 TRP SERIES 246 (FQP PACKAGE)

SIZE D | DWG NO 2515699 | REV C
SCALE 20:1 | SHEET 1 OF 3

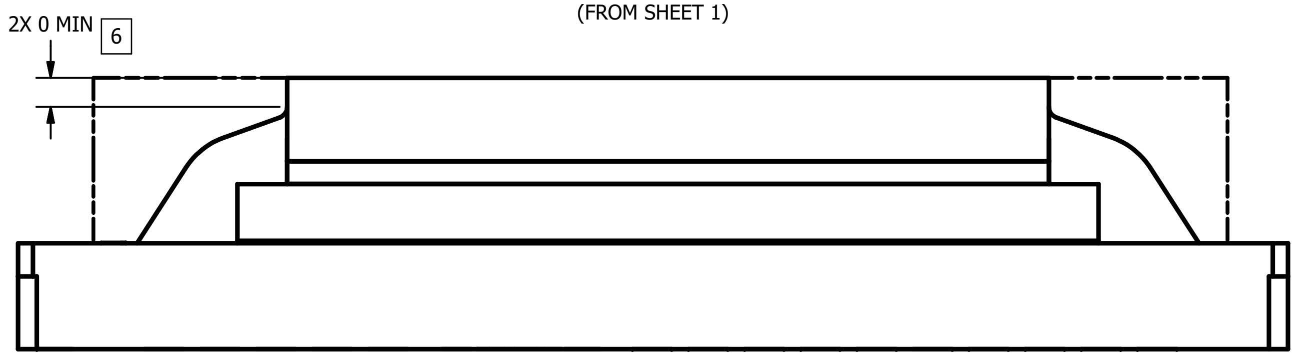
INV11-2006a



VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)

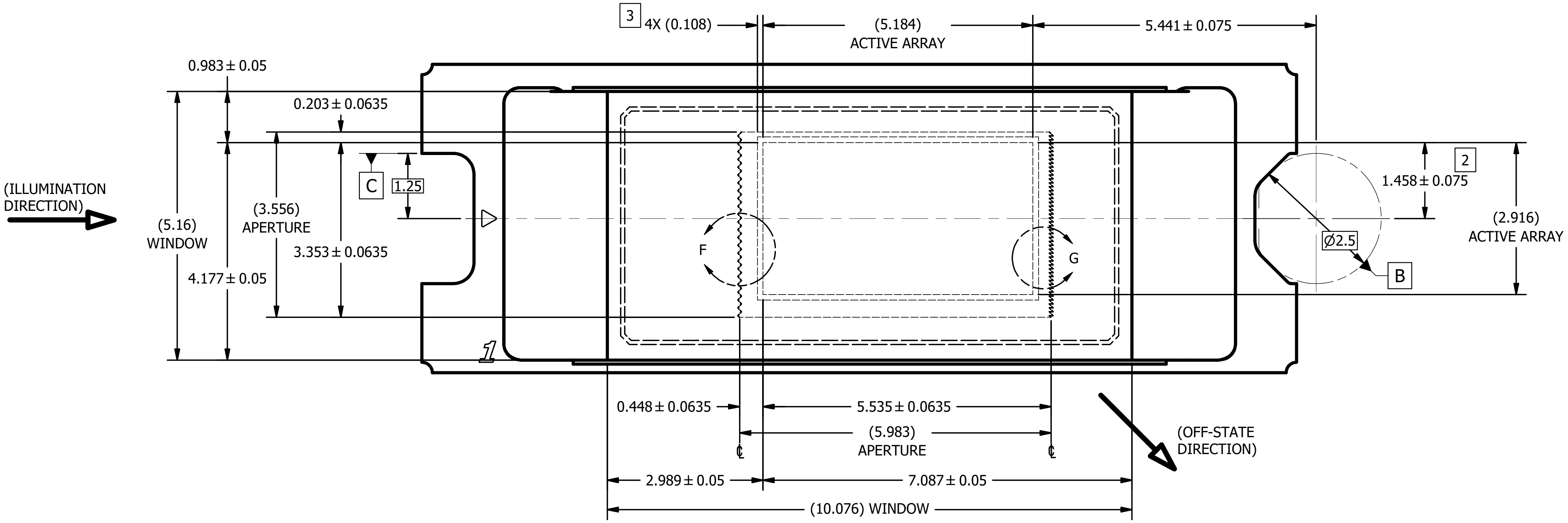


VIEW C 5
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)

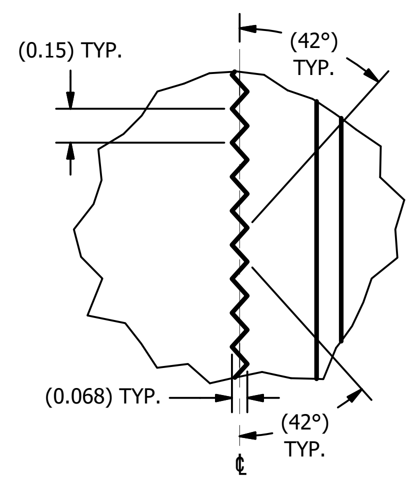


VIEW D
ENCAPSULANT MAXIMUM HEIGHT

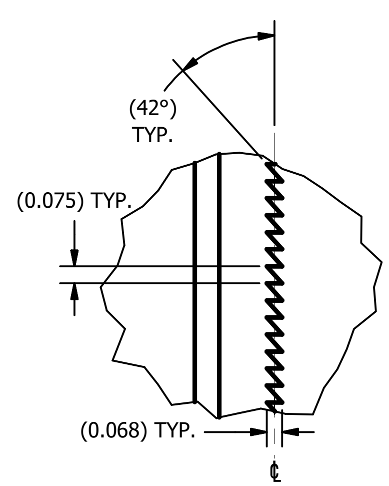
TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 9/5/2017	SIZE D	DWG NO 2515699	REV C
			SCALE	SHEET 2 OF 3	



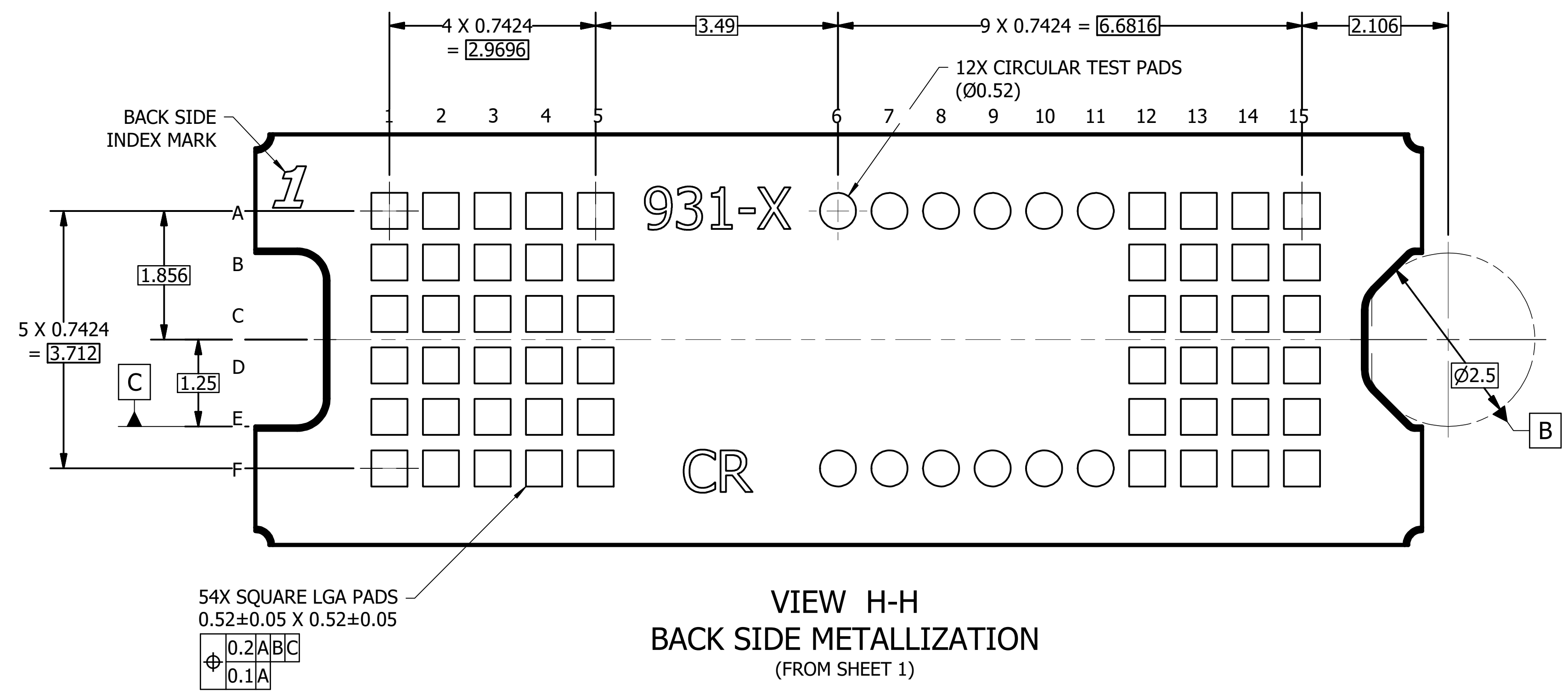
VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL F
APERTURE LEFT EDGE
SCALE 60 : 1



DETAIL G
APERTURE RIGHT EDGE
SCALE 60 : 1



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

TEXAS INSTRUMENTS Dallas Texas	DRAWN B. HASKETT	DATE 9/5/2017	SIZE D	DWG NO 2515699	REV C
			SCALE	SHEET 3 OF 3	

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265