

DLP3010 0.3 720p DMD

1 特性

- 0.3 英寸 (7.93mm) 对角线微镜阵列
 - 1280 × 720 铝制微米级微镜阵列，正交布局
 - 5.4 μ m 微镜间距
 - $\pm 17^\circ$ 微镜倾斜度（相对于平面）
 - 侧面照明，实现最优的效率和光学引擎尺寸
 - 偏振无关型铝微镜表面
- 8 位 SubLVDS 输入数据总线
- 专用 DLPC3433 或 DLPC3438 显示控制器和 DLPA200x/DLPA3000 PMIC/LED 驱动器，确保可靠运行

2 应用

- 电池供电的移动式附件高清 (HD) 投影仪
- 电池供电的智能 HD 投影仪
- 数字标牌
- 交互式表面投影
- 低延迟游戏显示屏
- 交互式显示

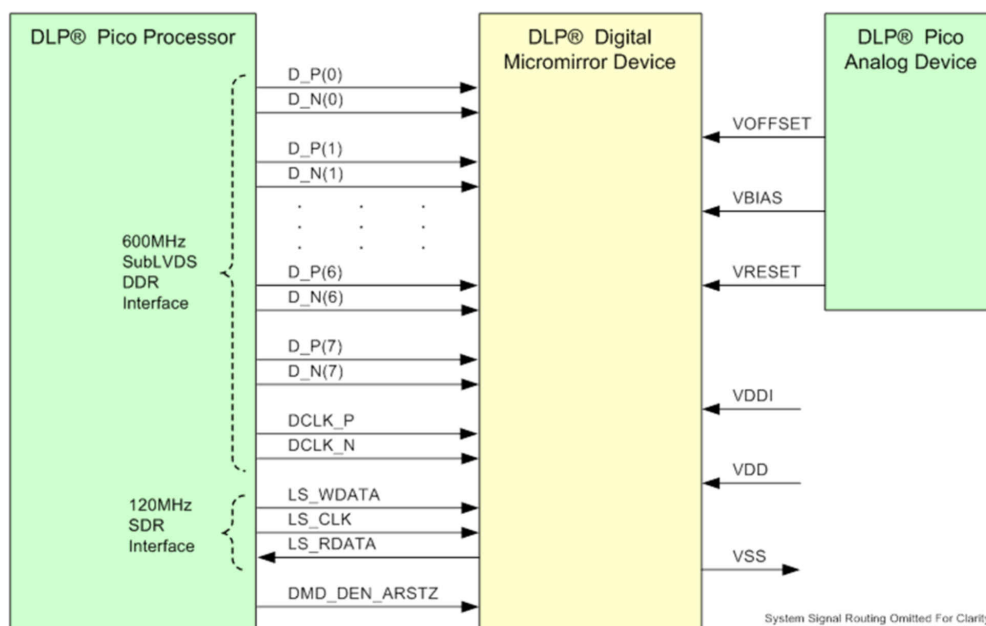
3 说明

DLP3010 数字微镜器件 (DMD) 是一款数控微光机电系统 (MOEMS) 空间照明调制器 (SLM)。当与适当的光学系统配合使用时，DLP3010 DMD 可显示非常清晰的高质量图像或视频。DLP3010 是 DLP3010 DMD、DLPC3433 或 DLPC3438 显示控制器和 DLPA200x/DLPA3000 PMIC/LED 驱动器所组成的芯片组的一部分。DLP3010 紧凑的物理尺寸连同控制器和 PMIC/LED 驱动器共同组成了完整的系统解决方案，从而实现了小外形尺寸、低功耗以及高分辨率高清显示屏。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
DLP3010	FQK (57)	18.20mm × 7.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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DLP® DLP3010 0.3 720p 芯片组



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (October 2021) to Revision B (May 2022)	Page
• Updated Absolute Maximum Ratings disclosure to the latest TI standard.....	6
• Updated <i>Micromirror Array Optical Characteristics</i>	18
• Added <i>Third-Party Products Disclaimer</i>	35

Changes from Revision * (February 2018) to Revision A (October 2021)	Page
• 更新了整个文档中的表、图和交叉参考的编号格式.....	1
• Updated T _{DELTA} MAX from 30°C to 15°C.....	7

5 Pin Configuration and Functions

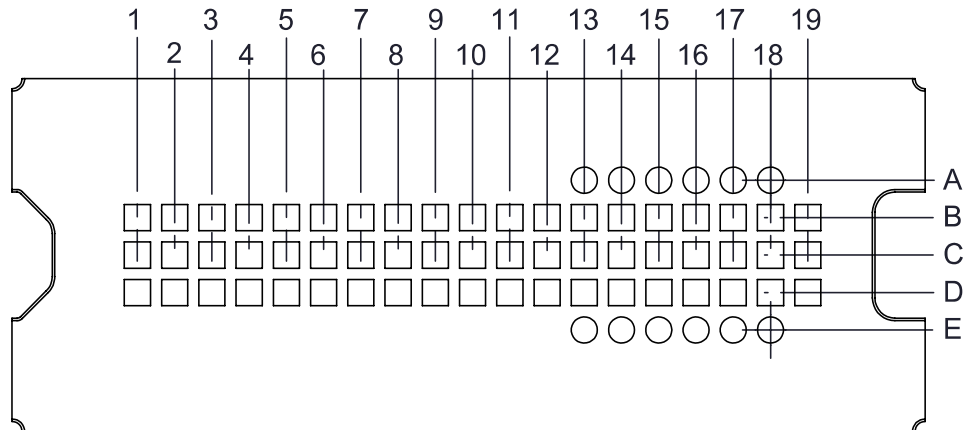


图 5-1. FQK Package. 57-Pin LGA. BOTTOM VIEW.

表 5-1. Pin Functions - Connector Pins

PIN ⁽¹⁾		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH ⁽²⁾ (mm)
NAME	NO.					
DATA INPUTS						
D_N(0)	C9	I	SubLVDS	Double	Data, Negative	10.54
D_P(0)	B9	I	SubLVDS	Double	Data, Positive	10.54
D_N(1)	D10	I	SubLVDS	Double	Data, Negative	13.14
D_P(1)	D11	I	SubLVDS	Double	Data, Positive	13.14
D_N(2)	C11	I	SubLVDS	Double	Data, Negative	14.24
D_P(2)	B11	I	SubLVDS	Double	Data, Positive	14.24
D_N(3)	D12	I	SubLVDS	Double	Data, Negative	14.35
D_P(3)	D13	I	SubLVDS	Double	Data, Positive	14.35
D_N(4)	D4	I	SubLVDS	Double	Data, Negative	5.89
D_P(4)	D5	I	SubLVDS	Double	Data, Positive	5.89
D_N(5)	C5	I	SubLVDS	Double	Data, Negative	5.45
D_P(5)	B5	I	SubLVDS	Double	Data, Positive	5.45
D_N(6)	D6	I	SubLVDS	Double	Data, Negative	8.59
D_P(6)	D7	I	SubLVDS	Double	Data, Positive	8.59
D_N(7)	C7	I	SubLVDS	Double	Data, Negative	7.69
D_P(7)	B7	I	SubLVDS	Double	Data, Positive	7.69
DCLK_N	D8	I	SubLVDS	Double	Clock, Negative	8.10
DCLK_P	D9	I	SubLVDS	Double	Clock, Positive	8.10
CONTROL INPUTS						
LS_WDATA	C12	I	LPSDR ⁽¹⁾	Single	Write data for low-speed interface.	7.16
LS_CLK	C13	I	LPSDR	Single	Clock for low-speed interface.	7.89
DMD_DEN_ARSTZ	C14	I	LPSDR		Asynchronous reset DMD signal. A low signal places the DMD in reset. A high signal releases the DMD from reset and places it in active mode.	
LS_RDATA	C15	O	LPSDR	Single	Read data for low-speed interface.	
POWER						
VBIAS ⁽³⁾	C1	Power			Supply voltage for positive bias level at micromirrors.	
VBIAS ⁽³⁾	C18	Power				

表 5-1. Pin Functions - Connector Pins (continued)

PIN ⁽¹⁾		TYPE	SIGNAL	DATA RATE	DESCRIPTION	PACKAGE NET LENGTH ⁽²⁾ (mm)	
NAME	NO.						
VOFFSET ⁽³⁾	D1	Power			Supply voltage for HVCMOS core logic. Supply voltage for stepped high level at micromirror address electrodes. Supply voltage for offset level at micromirrors.		
VOFFSET ⁽³⁾	D17	Power					
VRESET	B1	Power			Supply voltage for negative reset level at micromirrors.		
VRESET	B18	Power					
VDD	B6	Power			Supply voltage for LVCMOS core logic. Supply voltage for LPSDR inputs. Supply voltage for normal high level at micromirror address electrodes.		
VDD	B10	Power					
VDD	B19	Power					
VDD ⁽³⁾	C6	Power					
VDD	C10	Power					
VDD	C19	Power					
VDD	D2	Power					
VDD	D18	Power					
VDD	D19	Power					
VDDI	B2	Power				Supply voltage for SubLVDS receivers.	
VDDI	C2	Power					
VDDI	C3	Power					
VDDI	D3	Power					
VSS	B3	Ground			Common return. Ground for all power.		
VSS	B4	Ground					
VSS	B8	Ground					
VSS	B12	Ground					
VSS	B13	Ground					
VSS	B14	Ground					
VSS	B15	Ground					
VSS	B16	Ground					
VSS	B17	Ground					
VSS	C4	Ground					
VSS	C8	Ground					
VSS	C16	Ground					
VSS	C17	Ground					
VSS	D14	Ground					
VSS	D15	Ground					
VSS	D16	Ground					

- Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR)* [JESD209B](#).
- Net trace lengths inside the package:
Relative dielectric constant for the FQK ceramic package is 9.8.
Propagation speed = $11.8 / \sqrt{9.8} = 3.769$ in/ns.
Propagation delay = 0.265 ns/in = 265 ps/in = 10.43 ps/mm.
- The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.

表 5-2. Pin Functions - Test Pads

NUMBER	SYSTEM BOARD
A13	Do not connect
A14	Do not connect
A15	Do not connect
A16	Do not connect
A17	Do not connect
A18	Do not connect
E13	Do not connect
E14	Do not connect
E15	Do not connect
E16	Do not connect
E17	Do not connect
E18	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
Supply voltage	VDD	Supply voltage for LVCMOS core logic ⁽²⁾ Supply voltage for LPSDR low-speed interface	- 0.5	2.3	V
	VDDI	Supply voltage for SubLVDS receivers ⁽²⁾	- 0.5	2.3	
	VOFFSET	Supply voltage for HVCMOS and micromirror electrode ^{(2) (3)}	- 0.5	11	
	VBIAS	Supply voltage for micromirror electrode ⁽²⁾	- 0.5	19	
	VRESET	Supply voltage for micromirror electrode ⁽²⁾	- 15	0.5	
	VDDI - VDD	Supply voltage delta (absolute value) ⁽⁴⁾		0.3	
	VBIAS - VOFFSET	Supply voltage delta (absolute value) ⁽⁵⁾		11	
	VBIAS - VRESET	Supply voltage delta (absolute value) ⁽⁶⁾		34	
Input voltage	Input voltage for other inputs LPSDR ⁽²⁾		- 0.5	VDD + 0.5	V
	Input voltage for other inputs SubLVDS ^{(2) (7)}		- 0.5	VDDI + 0.5	
Input pins	VID	SubLVDS input differential voltage (absolute value) ⁽⁷⁾		810	mV
	IID	SubLVDS input differential current		10	mA
Clock frequency	f_{clock}	Clock frequency for low-speed interface LS_CLK		130	MHz
	f_{clock}	Clock frequency for high-speed interface DCLK		560	
Environmental	T _{ARRAY} and T _{WINDOW}	Temperature - operational ⁽⁸⁾	- 20	90	°C
		Temperature - non-operational ⁽⁸⁾	- 40	90	
	T _{DP}	Dew point temperature - operating and non-operating (non-condensing)		81	
	T _{DELTA}	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 ⁽⁹⁾		30	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the ground terminals (VSS). The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
- (3) VOFFSET supply transients must fall within specified voltages.
- (4) Exceeding the recommended allowable absolute voltage difference between VDDI and VDD may result in excessive current draw.
- (5) Exceeding the recommended allowable absolute voltage difference between VBIAS and VOFFSET may result in excessive current draw.
- (6) Exceeding the recommended allowable absolute voltage difference between VBIAS and VRESET may result in excessive current draw.
- (7) This maximum input voltage rating applies when each input of a differential pair is at the same voltage potential. Sub-LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
- (8) The highest temperature of the active array (as calculated by the [§ 7.6](#)) or of any point along the window edge as defined in [图 7-1](#). The locations of thermal test points TP2 and TP3 in [图 7-1](#) are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
- (9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [图 7-1](#). The window test points TP2 and TP3 shown in [图 7-1](#) are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

6.2 Storage Conditions

applicable for the DMD as a component or non-operational in a system

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	- 40	85	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing) ⁽¹⁾		24	°C
T_{DP-ELR}	Elevated dew point temperature range, (non-condensing) ⁽²⁾	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		6	Months

- (1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR} .

6.3 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGE RANGE⁽⁴⁾					
V_{DD}	Supply voltage for LVCMOS core logic Supply voltage for LPSDR low-speed interface	1.65	1.8	1.95	V
V_{DDI}	Supply voltage for SubLVDS receivers	1.65	1.8	1.95	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode ⁽⁵⁾	9.5	10	10.5	V
V_{BIAS}	Supply voltage for mirror electrode	17.5	18	18.5	V
V_{RESET}	Supply voltage for micromirror electrode	- 14.5	- 14	- 13.5	V
$ V_{DDI} - V_{DD} $	Supply voltage delta (absolute value) ⁽⁶⁾			0.3	V
$ V_{BIAS} - V_{OFFSET} $	Supply voltage delta (absolute value) ⁽⁷⁾			10.5	V
$ V_{BIAS} - V_{RESET} $	Supply voltage delta (absolute value) ⁽⁸⁾			33	V
CLOCK FREQUENCY					
f_{clock}	Clock frequency for low-speed interface LS_CLK ⁽⁹⁾	108		120	MHz
f_{clock}	Clock frequency for high-speed interface DCLK ⁽¹⁰⁾	300		540	MHz
	Duty cycle distortion DCLK	44%		56%	
SUBLVDS INTERFACE⁽¹⁰⁾					
$ V_{ID} $	SubLVDS input differential voltage (absolute value), see 图 6-8 and 图 6-9	150	250	350	mV
V_{CM}	Common mode voltage, see 图 6-8 图 6-8 and 图 6-9	700	900	1100	mV
$V_{SUBLVDS}$	SubLVDS voltage, see 图 6-8 and 图 6-9	575		1225	mV
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Z_{IN}	Internal differential termination resistance, see 图 6-10	80	100	120	Ω
	100-Ω differential PCB trace	6.35		152.4	mm
ENVIRONMENTAL					

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted)^{(1) (2) (3)}

		MIN	NOM	MAX	UNIT
T _{ARRAY}	Array temperature - long-term operational ^{(11) (13) (14) (15)}	0		40 to 70	°C
	Array temperature - short-term operational, 25 hr maximum ^{(13) (16)}	- 20		- 10	
	Array temperature - short-term operational, 500 hr maximum ^{(13) (16)}	- 10		0	
	Array temperature - short-term operational, 500 hr maximum ^{(13) (16)}	70		75	
T _{DELTA}	Absolute temperature delta between any point on the window edge and the ceramic test point TP1 ⁽¹⁷⁾			15	°C
T _{WINDOW}	Window temperature - operational ^{(11) (18)}			90	°C
T _{DP-AVG}	Average dew point temperature (non-condensing) ⁽²⁰⁾			24	°C
T _{DP-ELR}	Elevated dew point temperature range (non-condensing) ⁽¹⁹⁾	28		36	°C
CT _{ELR}	Cumulative time in elevated dew point temperature range			6	Months
ILL _{UV}	Illumination wavelengths < 420 nm ⁽¹¹⁾			0.68	mW/cm ²
ILL _{VIS}	Illumination wavelengths between 420 nm and 700 nm			Thermally limited	
ILL _{IR}	Illumination wavelengths > 700 nm			10	mW/cm ²
ILL _θ	Illumination marginal ray angle ⁽¹²⁾			55	deg

- (1) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET.
- (2) § 6.4 are applicable after the DMD is installed in the final product.
- (3) The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by the § 6.4. No level of performance is implied when operating the device above or below the § 6.4 limits.
- (4) All voltage values are with respect to the ground pins (VSS).
- (5) VOFFSET supply transients must fall within specified maximum voltages.
- (6) To prevent excess current, the supply voltage delta |VDDI - VDD| must be less than specified limit.
- (7) To prevent excess current, the supply voltage delta |VBIAS - VOFFSET| must be less than specified limit.
- (8) To prevent excess current, the supply voltage delta |VBIAS - VRESET| must be less than specified limit.
- (9) LS_CLK must run as specified to ensure internal DMD timing for reset waveform commands.
- (10) Refer to the SubLVDS timing requirements in § 6.7.
- (11) Simultaneous exposure of the DMD to the maximum § 6.4 for temperature and UV illumination will reduce device lifetime.
- (12) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), should not exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.
- (13) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 7-1 and the package thermal resistance using § 7.6.
- (14) Per 图 6-1, the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to § 7.7 for a definition of micromirror landed duty cycle.
- (15) Long-term is defined as the usable life of the device
- (16) Short-term is the total cumulative time over the useful life of the device.
- (17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge shown in 图 7-1. The window test points TP2 and TP3 shown in 图 7-1 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.
- (18) Window temperature is the highest temperature on the window edge shown in 图 7-1. The locations of thermal test points TP2 and TP3 in 图 7-1 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point should be used.
- (19) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT_{ELR}.
- (20) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.

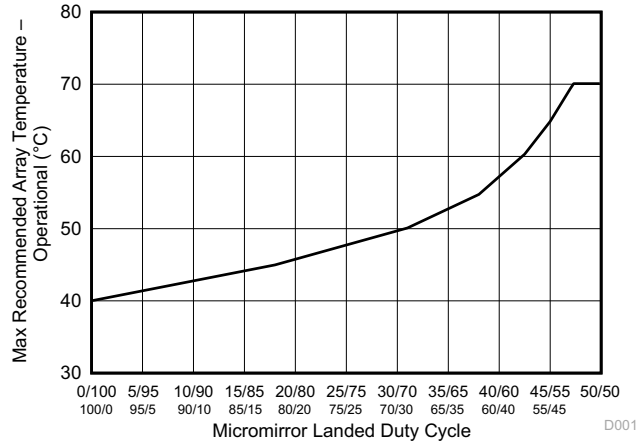


图 6-1. Maximum Recommended Array Temperature - Derating Curve

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		DLP3010	UNIT
		FQK (LGA)	
		57 PINS	
Thermal resistance	Active area to test point 1 (TP1) ⁽¹⁾	5.4	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions*. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS ⁽³⁾	MIN	TYP	MAX	UNIT
CURRENT						
I _{DD}	Supply current: VDD ^{(4) (6)}	VDD = 1.95 V			60.5	mA
		VDD = 1.8 V		54		
I _{DDI}	Supply current: VDDI ^{(4) (6)}	VDDI = 1.95 V			16.5	mA
		VDD = 1.8 V		11.3		
I _{OFFSET}	Supply current: VOFFSET ^{(5) (7)}	VOFFSET = 10.5 V			2.2	mA
		VOFFSET = 10 V		1.5		
I _{BIAS}	Supply current: VBIAS ^{(5) (7)}	VBIAS = 18.5 V			0.6	mA
		VBIAS = 18 V		0.3		
I _{RESET}	Supply current: VRESET ⁽⁷⁾	VRESET = - 14.5 V			2.4	mA
		VRESET = - 14 V		1.7		
POWER⁽²⁾						
P _{DD}	Supply power dissipation: VDD ^{(4) (6)}	VDD = 1.95 V			118	mW
		VDD = 1.8 V		97.2		
P _{DDI}	Supply power dissipation: VDDI ^{(4) (6)}	VDDI = 1.95 V			32	mW
		VDD = 1.8 V		20		
P _{OFFSET}	Supply power dissipation: VOFFSET ^{(5) (7)}	VOFFSET = 10.5 V			23	mW
		VOFFSET = 10 V		15		
P _{BIAS}	Supply power dissipation: VBIAS ^{(5) (7)}	VBIAS = 18.5 V			11	mW
		VBIAS = 18 V		6		
P _{RESET}	Supply power dissipation: VRESET ⁽⁷⁾	VRESET = - 14.5 V			35	mW
		VRESET = - 14 V		24		
P _{TOTAL}	Supply power dissipation: Total			162.2	219	mW
LPSDR INPUT⁽⁸⁾						
V _{IH(DC)}	DC input high voltage ⁽¹⁰⁾		0.7 × VDD		VDD + 0.3	V
V _{IL(DC)}	DC input low voltage ⁽¹⁰⁾		- 0.3		0.3 × VDD	V
V _{IH(AC)}	AC input high voltage ⁽¹⁰⁾		0.8 × VDD		VDD + 0.3	V
V _{IL(AC)}	AC input low voltage ⁽¹⁰⁾		- 0.3		0.2 × VDD	V
ΔV _T	Hysteresis (V _{T+} - V _{T-})	See 图 6-10	0.1 × VDD		0.4 × VDD	V
I _{IL}	Low - level input current	VDD = 1.95 V; V _I = 0 V	- 100			nA
I _{IH}	High - level input current	VDD = 1.95 V; V _I = 1.95 V			100	nA
LPSDR OUTPUT⁽⁹⁾						

6.6 Electrical Characteristics (continued)

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS ⁽³⁾	MIN	TYP	MAX	UNIT
V _{OH}	DC output high voltage	I _{OH} = - 2 mA	0.8 × VDD			V
V _{OL}	DC output low voltage	I _{OL} = 2 mA		0.2 × VDD		V
CAPACITANCE						
C _{IN}	Input capacitance LPSDR	f = 1 MHz			10	pF
	Input capacitance SubLVDS	f = 1 MHz			10	
C _{OUT}	Output capacitance	f = 1 MHz			10	pF
C _{RESET}	Reset group capacitance	f = 1 MHz; (720 × 160) micromirrors	200		220	pF

- (1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.
- (2) The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, VRESET.
- (3) All voltage values are with respect to the ground pins (VSS).
- (4) To prevent excess current, the supply voltage delta |VDDI - VDD| must be less than specified limit.
- (5) To prevent excess current, the supply voltage delta |VBIAS - VOFFSET| must be less than specified limit.
- (6) Supply power dissipation based on non - compressed commands and data.
- (7) Supply power dissipation based on 3 global resets in 200 μs.
- (8) LPSDR specifications are for pins LS_CLK and LS_WDATA.
- (9) LPSDR specification is for pin LS_RDATA.
- (10) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low-Power Double Data Rate (LPDDR) JESD209B*.

6.7 Timing Requirements

Device electrical characteristics are over [# 6.4](#) unless otherwise noted.

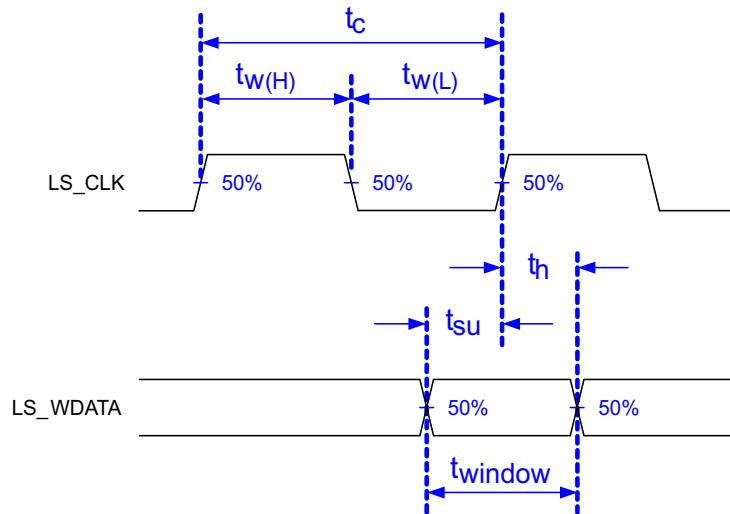
			MIN	NOM	MAX	UNIT
LPSDR						
t _r	Rise slew rate ⁽¹⁾	(30% to 80%) × VDD, see 图 6-3	1		3	V/ns
t _f	Fall slew rate ⁽¹⁾	(70% to 20%) × VDD, see 图 6-3	1		3	V/ns
t _r	Rise slew rate ⁽²⁾	(20% to 80%) × VDD, see 图 6-3	0.25			V/ns
t _f	Fall slew rate ⁽²⁾	(80% to 20%) × VDD, see 图 6-3	0.25			V/ns
t _c	Cycle time LS_CLK,	See 图 6-2	7.7	8.3		ns
t _{W(H)}	Pulse duration LS_CLK high	50% to 50% reference points, see 图 6-2	3.1			ns
t _{W(L)}	Pulse duration LS_CLK low	50% to 50% reference points, see 图 6-2	3.1			ns
t _{su}	Setup time	LS_WDATA valid before LS_CLK ↑, see 图 6-2	1.5			ns
t _h	Hold time	LS_WDATA valid after LS_CLK ↑, see 图 6-2	1.5			ns
t _{WINDOW}	Window time ^{(1) (4)}	Setup time + hold time, see 图 6-2	3			ns
t _{DERATING}	Window time derating ^{(1) (4)}	For each 0.25-V/ns reduction in slew rate below 1 V/ns, see 图 6-5		0.35		ns
SubLVDS						
t _r	Rise slew rate	20% to 80% reference points, see 图 6-4	0.7	1		V/ns
t _f	Fall slew rate	80% to 20% reference points, see 图 6-4	0.7	1		V/ns
t _c	Cycle time DCLK,	See 图 6-6	1.79	1.85		ns
t _{W(H)}	Pulse duration DCLK high	50% to 50% reference points, see 图 6-6	0.79			ns
t _{W(L)}	Pulse duration DCLK low	50% to 50% reference points, see 图 6-6	0.79			ns
t _{su}	Setup time	D(0:3) valid before DCLK ↑ or DCLK ↓, see 图 6-6				
t _h	Hold time	D(0:3) valid after DCLK ↑ or DCLK ↓, see 图 6-6				
t _{WINDOW}	Window time	Setup time + hold time, see 图 6-6 and 图 6-7			0.3	ns

6.7 Timing Requirements (continued)

Device electrical characteristics are over [# 6.4](#) unless otherwise noted.

	MIN	NOM	MAX	UNIT
$t_{LVDS-ENABLE+REFGEN}$ Power-up receiver ⁽³⁾			2000	ns

- (1) Specification is for LS_CLK and LS_WDATA pins. Refer to LPSDR input rise slew rate and fall slew rate in [图 6-3](#).
- (2) Specification is for DMD_DEN_ARSTZ pin. Refer to LPSDR input rise and fall slew rate in [图 6-3](#).
- (3) Specification is for SubLVDS receiver time only and does not take into account commanding and latency after commanding.
- (4) Window time derating example: 0.5-V/ns slew rate increases the window time by 0.7 ns, from 3 ns to 3.7 ns.



Low-speed interface is LPSDR and adheres to the [# 6.6](#) and AC/DC Operating Conditions table in JEDEC Standard No. 209B, *Low Power Double Data Rate (LPDDR) JESD209B*.

图 6-2. LPSDR Switching Parameters

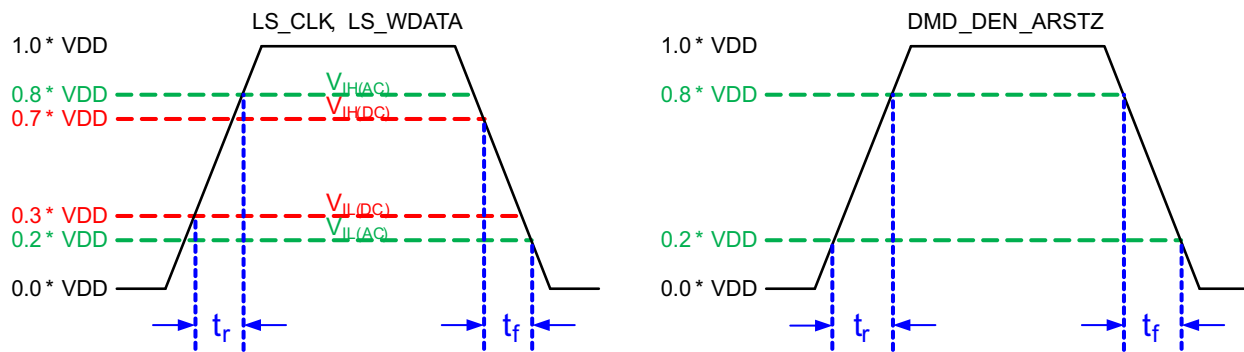


图 6-3. LPSDR Input Rise and Fall Slew Rate

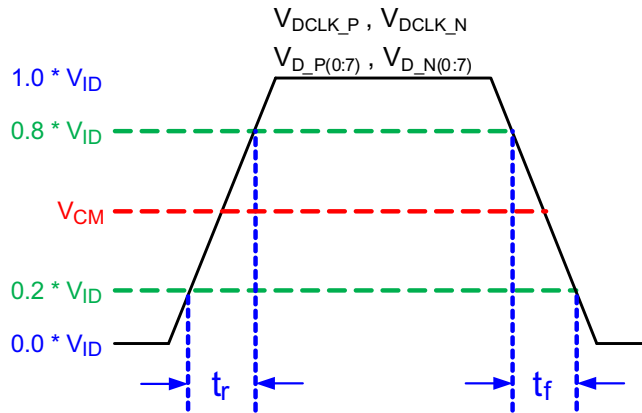


图 6-4. SubLVDS Input Rise and Fall Slew Rate

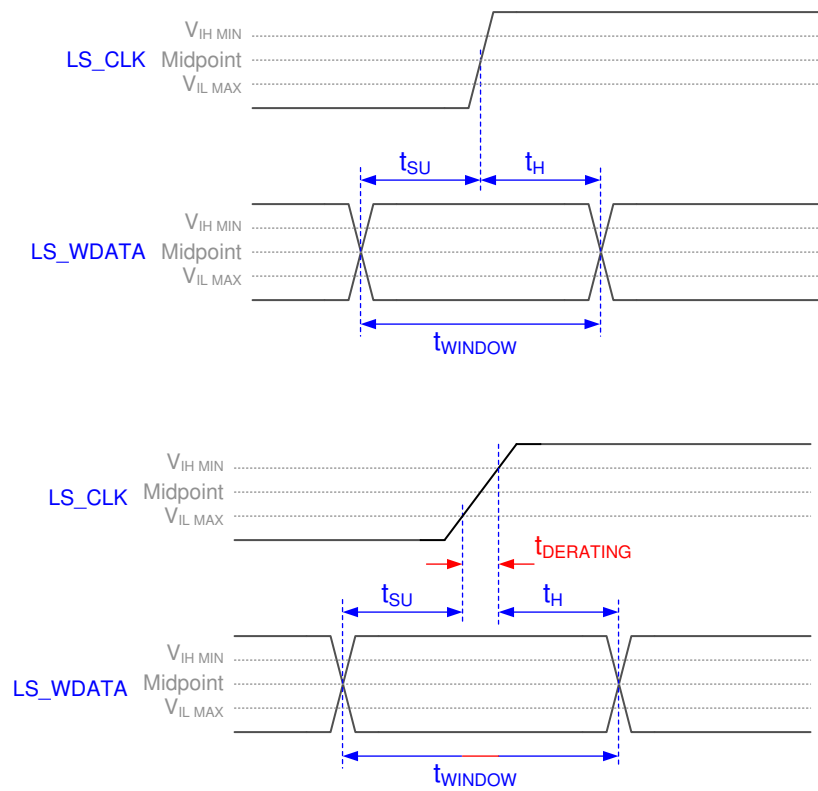


图 6-5. Window Time Derating Concept

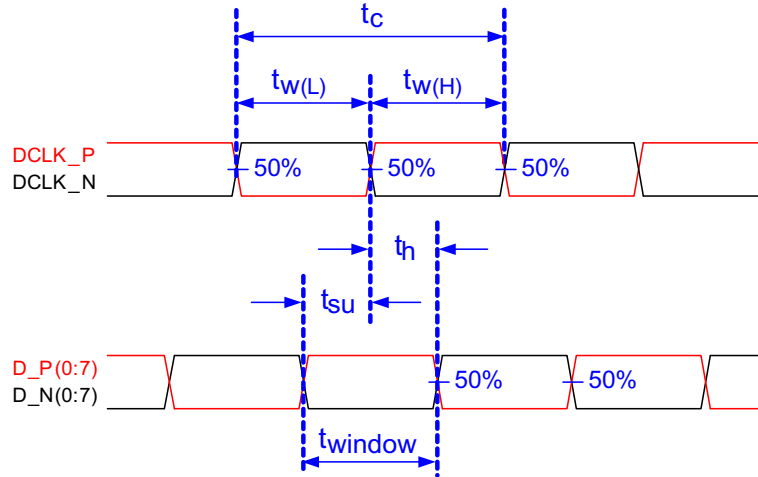
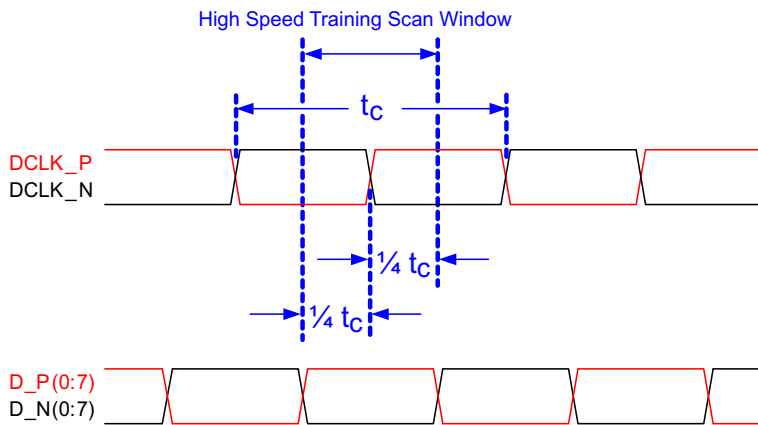


图 6-6. SubLVDS Switching Parameters



Note: Refer to 7.3.3 for details.

图 6-7. High-Speed Training Scan Window

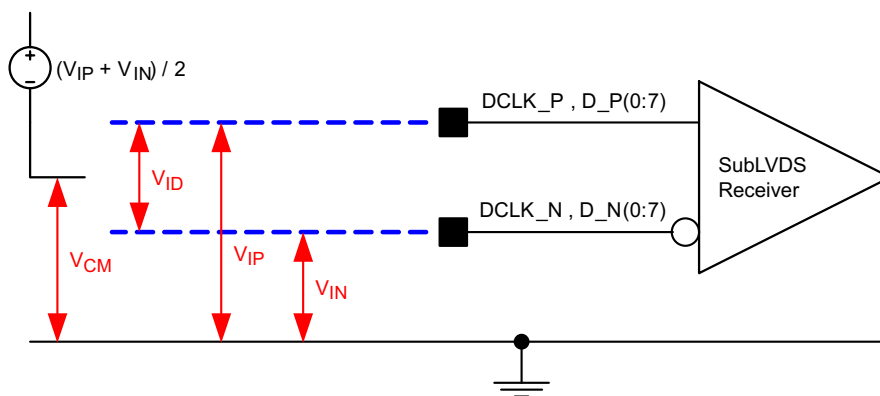


图 6-8. SubLVDS Voltage Parameters

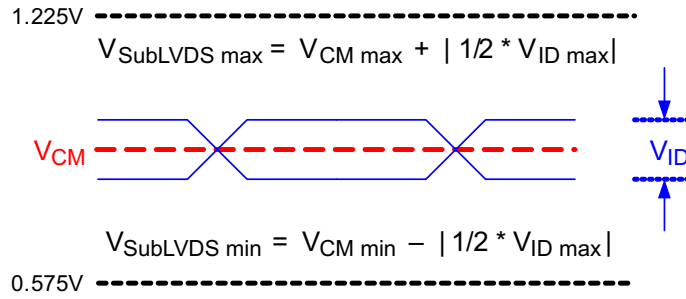


图 6-9. SubLVDS Waveform Parameters

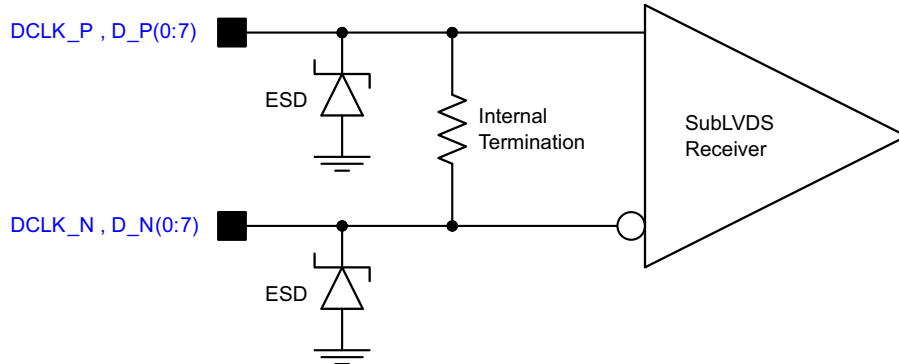


图 6-10. SubLVDS Equivalent Input Circuit

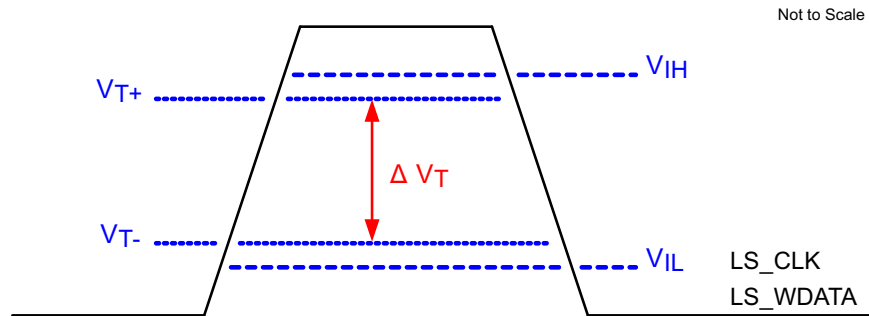


图 6-11. LPSDR Input Hysteresis

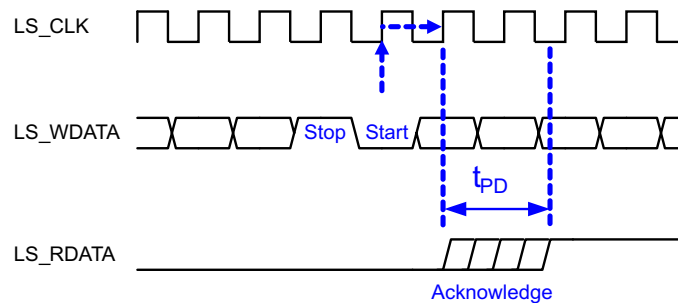
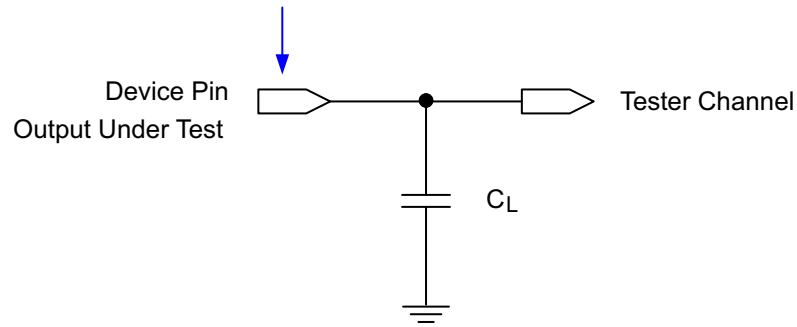


图 6-12. LPSDR Read Out

Data Sheet Timing Reference Point



See #7.3.4 for more information.

图 6-13. Test Load Circuit for Output Propagation Measurement

6.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PD}	C _L = 5 pF			11.1	ns
	C _L = 10 pF			11.3	
	C _L = 85 pF			15	
Slew rate, LS_RDATA		0.5			V/ns
Output duty cycle distortion, LS_RDATA		40%		60%	

(1) Device electrical characteristics are over *Recommended Operating Conditions* unless otherwise noted.

6.9 System Mounting Interface Loads

PARAMETER	MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Electrical interface area, see 图 6-14		125	N
	Clamping and thermal interface area, see 图 6-14		67	

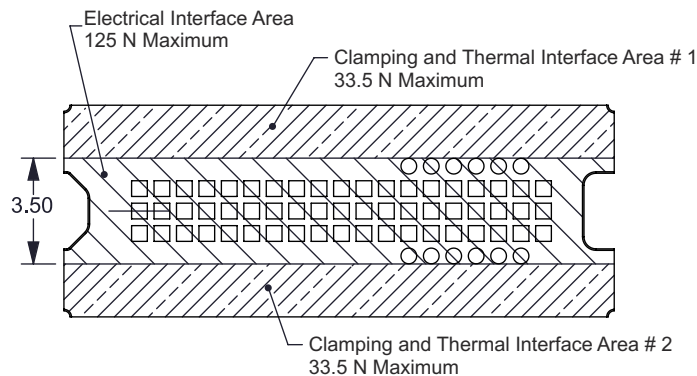


图 6-14. System Interface Loads

6.10 Micromirror Array Physical Characteristics

PARAMETER		VALUE	UNIT
Number of active columns	See 图 6-15	1280	micromirrors
Number of active rows	See 图 6-15	720	micromirrors
ϵ Micromirror (pixel) pitch	See 图 6-16	5.4	μm
Micromirror active array width	Micromirror pitch \times number of active columns; see 图 6-15	6.912	mm
Micromirror active array height	Micromirror pitch \times number of active rows; see 图 6-15	3.888	mm
Micromirror active border	Pond of micromirror (POM) ⁽¹⁾	20	micromirrors/side

- (1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.

Not To Scale

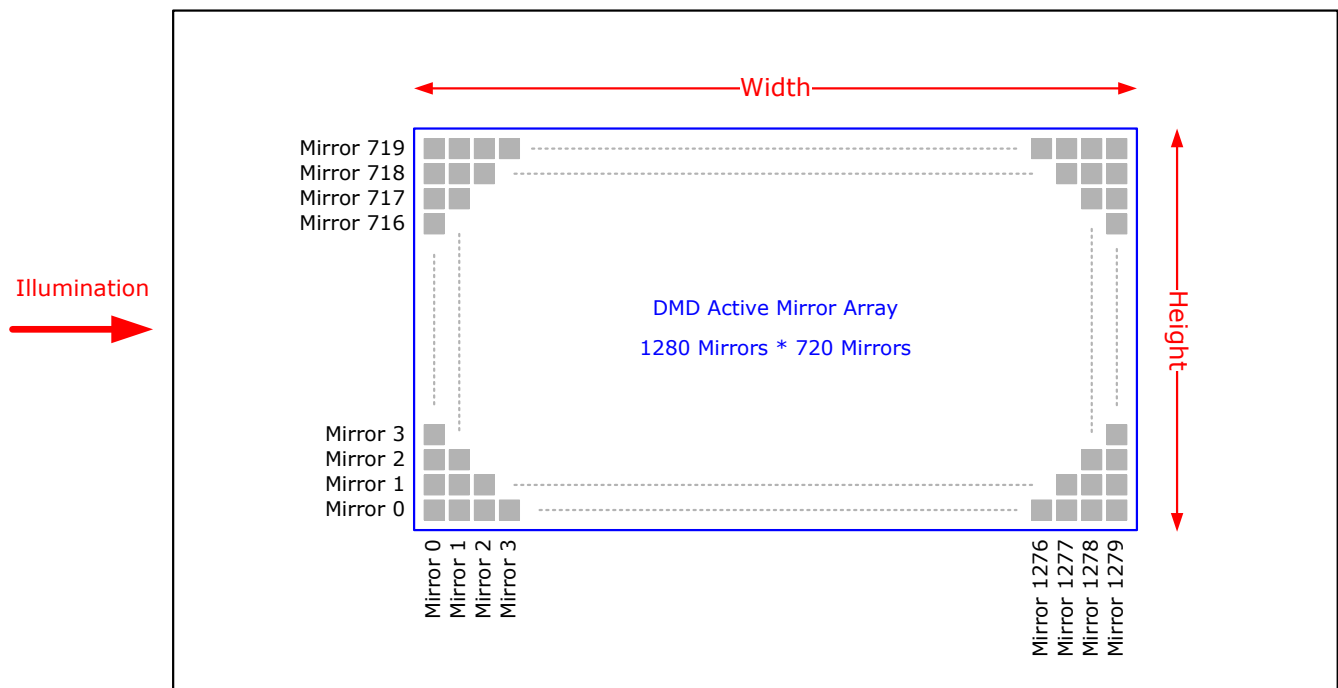


图 6-15. Micromirror Array Physical Characteristics

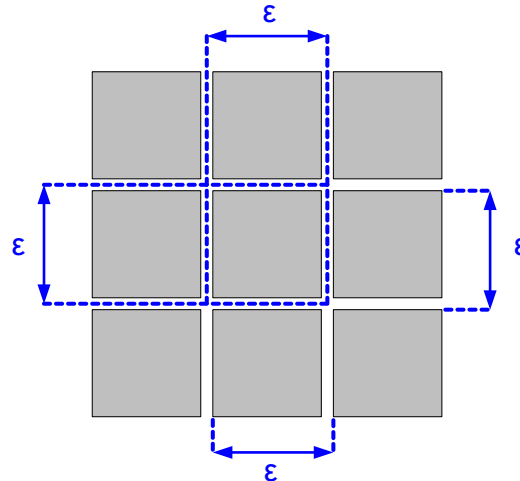


图 6-16. Mirror (Pixel) Pitch

6.11 Micromirror Array Optical Characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle		DMD landed state ⁽¹⁾		17		degree
Micromirror tilt angle tolerance ^{(2) (3) (4) (5)}			- 1.4		1.4	degree
Micromirror tilt direction ^{(6) (7)}		Landed ON state		180		degree
		Landed OFF state		270		
Micromirror crossover time ⁽⁸⁾		Typical performance		1	3	μs
Micromirror switching time ⁽⁹⁾		Typical performance	10			
Image performance ⁽¹⁰⁾	Bright pixel(s) in active area ⁽¹¹⁾	Gray 10 Screen ⁽¹²⁾			0	micromirrors
	Bright pixel(s) in the POM ⁽¹³⁾	Gray 10 Screen ⁽¹²⁾			1	
	Dark pixel(s) in the active area ⁽¹⁴⁾	White Screen			4	
	Adjacent pixel(s) ⁽¹⁵⁾	Any Screen			0	
	Unstable pixel(s) in active area ⁽¹⁶⁾	Any Screen			0	

- (1) Measured relative to the plane formed by the overall micromirror array.
- (2) Additional variation exists between the micromirror array and the package datums.
- (3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
- (4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
- (5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations, or system contrast variations.
- (6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON state direction. A binary value of 0 results in a micromirror landing in the OFF state direction. See 图 6-17.
- (7) Micromirror tilt direction is measured as in a typical polar coordinate system: Measuring counter-clockwise from a 0° reference which is aligned with the +X Cartesian axis.
- (8) The time required for a micromirror to nominally transition from one landed state to the opposite landed state.
- (9) The minimum time between successive transitions of a micromirror.
- (10) Conditions of Acceptance: All DMD image quality returns will be evaluated using the following projected image test conditions:
 - Test set degamma shall be linear
 - Test set brightness and contrast shall be set to nominal
 - The diagonal size of the projected image shall be a minimum of 20 inches
 - The projections screen shall be 1X gain
 - The projected image shall be inspected from a 38 inch minimum viewing distance
 - The image shall be in focus during all image quality tests

- (11) Bright pixel definition: A single pixel or mirror that is stuck in the ON position and is visibly brighter than the surrounding pixels
- (12) Gray 10 screen definition: All areas of the screen are colored with the following settings:
 Red = 10/255
 Green = 10/255
 Blue = 10/255
- (13) POM definition: Rectangular border of off-state mirrors surrounding the active area
- (14) Dark pixel definition: A single pixel or mirror that is stuck in the OFF position and is visibly darker than the surrounding pixels
- (15) Adjacent pixel definition: Two or more stuck pixels sharing a common border or common point, also referred to as a cluster
- (16) Unstable pixel definition: A single pixel or mirror that does not operate in sequence with parameters loaded into memory. The unstable pixel appears to be flickering asynchronously with the image

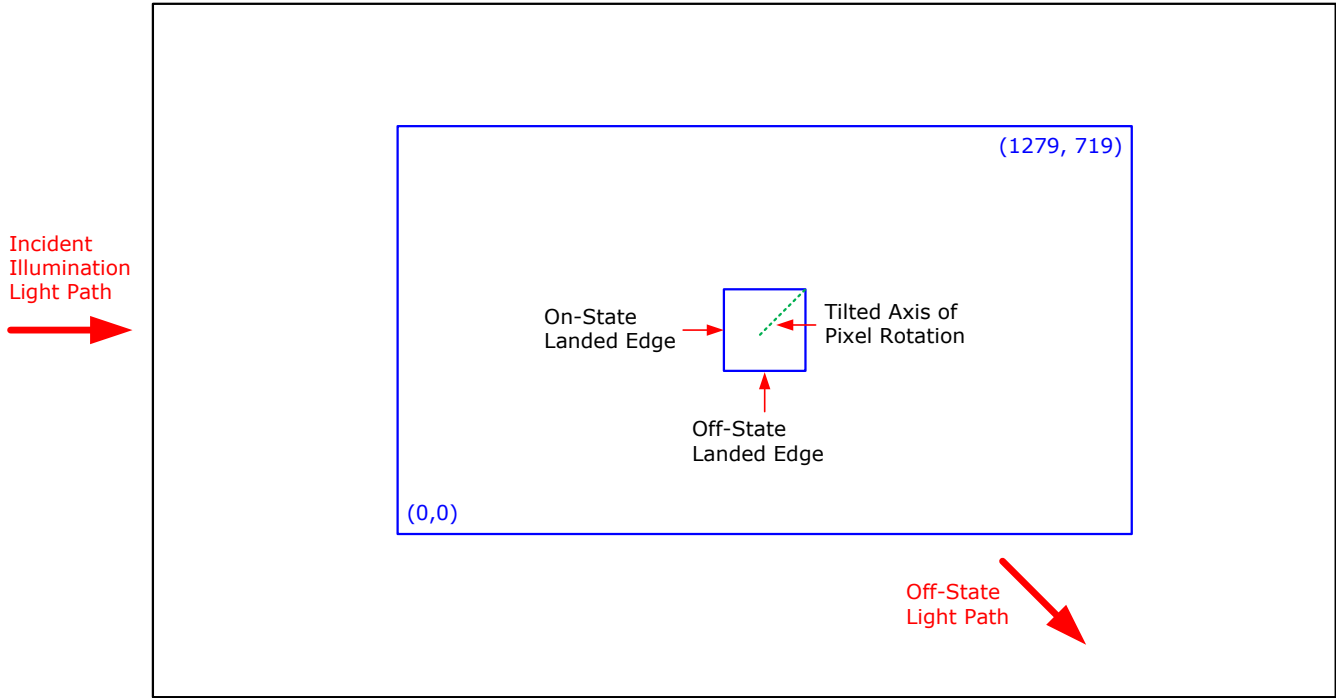


图 6-17. Landed Pixel Orientation and Tilt

6.12 Window Characteristics

PARAMETER ⁽³⁾		MIN	NOM	MAX	UNIT
Window material designation		Corning Eagle XG			
Window refractive index	at wavelength 546.1 nm	1.5119			
Window aperture ⁽¹⁾					See ⁽¹⁾
Illumination overfill ⁽²⁾					See ⁽²⁾
Window transmittance, single-pass through both surfaces and glass	Minimum within the wavelength range 420 nm to 680 nm. Applies to all angles 0° to 30° AOI.	97%			
Window transmittance, single-pass through both surfaces and glass	Average over the wavelength range 420 nm to 680 nm. Applies to all angles 30° to 45° AOI.	97%			

- (1) See the package mechanical characteristics for details regarding the size and location of the window aperture.
- (2) The active area of the DLP3010 device is surrounded by an aperture on the inside of the DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical conditions. Overfill light illuminating the area outside the active array can scatter and create adverse effects to the performance of an end application using the DMD. The illumination optical system should be designed to limit light flux incident outside the active array to less than 10% of the average flux level in the active area. Depending on the particular system's optical architecture and assembly tolerances, the amount of overfill light on the outside of the active array may cause system performance degradation.
- (3) See [Optical Interface and System Image Quality Considerations](#) for more information.

6.13 Chipset Component Usage Specification

备注

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

The DLP3010 is a component of one or more DLP® chipsets. Reliable function and operation of the DLP3010 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

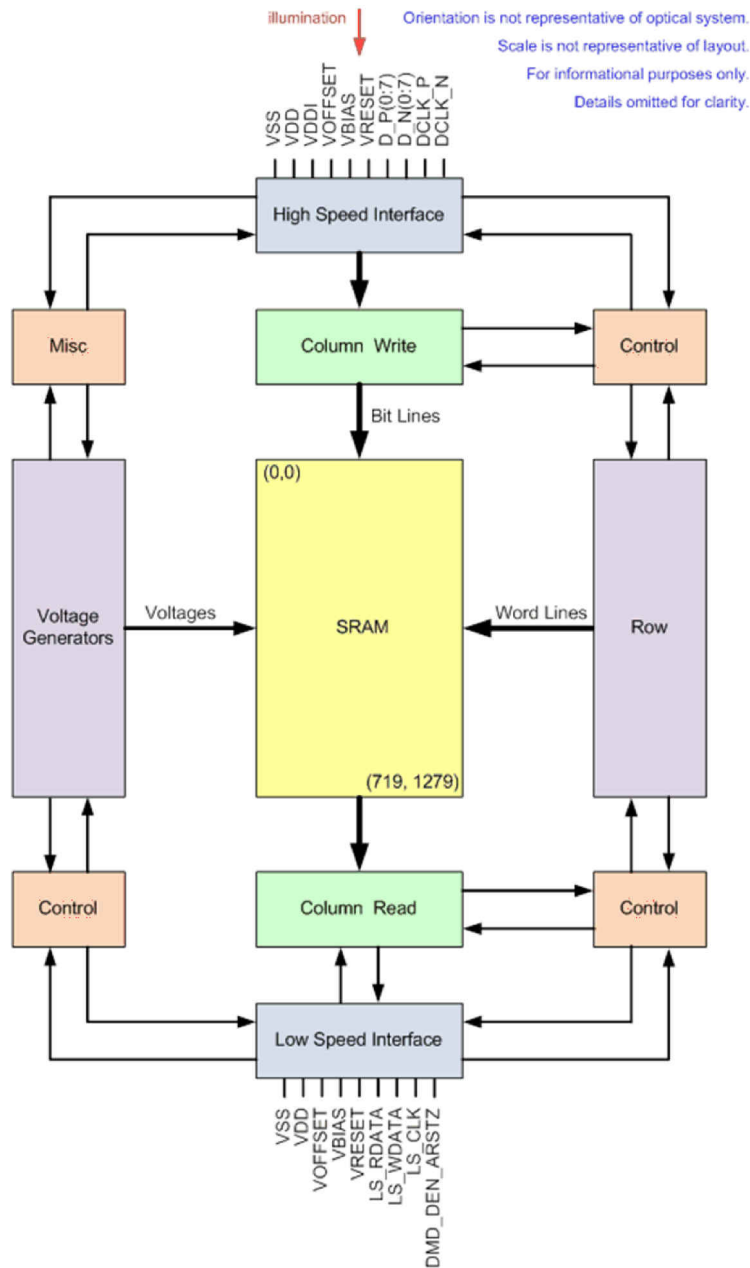
7 Detailed Description

7.1 Overview

The DLP3010 is a 0.3-in diagonal spatial light modulator of aluminum micromirrors. Pixel array size is 1280 columns by 720 rows in a square grid pixel arrangement. The electrical interface is sub low voltage differential signaling (SubLVDS) data.

DLP3010 is part of the chipset comprising of the DLP3010 DMD, DLPC3433 or DLPC3438 display controller and DLPA200x/DLPA3000 PMIC/LED driver. To ensure reliable operation, DLP3010 DMD must always be used with DLPC3433 or DLPC3438 display controller and DLPA200x/DLPA3000 PMIC/LED driver.

7.2 Functional Block Diagram



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A. Details omitted for clarity.

7.3 Feature Description

7.3.1 Power Interface

The power management IC, DLPA200x/DLPA3000, contains 3 regulated DC supplies for the DMD reset circuitry: VBIAS, VRESET and VOFFSET, as well as the two regulated DC supplies for the DLPC3433 or DLPC3438 controller.


7.3.2 Low-Speed Interface

The low-speed interface handles instructions that configure the DMD and control reset operation. LS_CLK is the low-speed clock, and LS_WDATA is the low-speed data input.

7.3.3 High-Speed Interface

The purpose of the high-speed interface is to transfer pixel data rapidly and efficiently, making use of high-speed DDR transfer and compression techniques to save power and time. The high-speed interface is composed of differential SubLVDS receivers for inputs, with a dedicated clock.

7.3.4 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account.  6-13 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC3433 or DLPC3438 controller. See the [DLPC3430](#) or [DLPC3435](#) controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), contrast degradation and objectionable artifacts in the display border and/or active area could occur.

7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

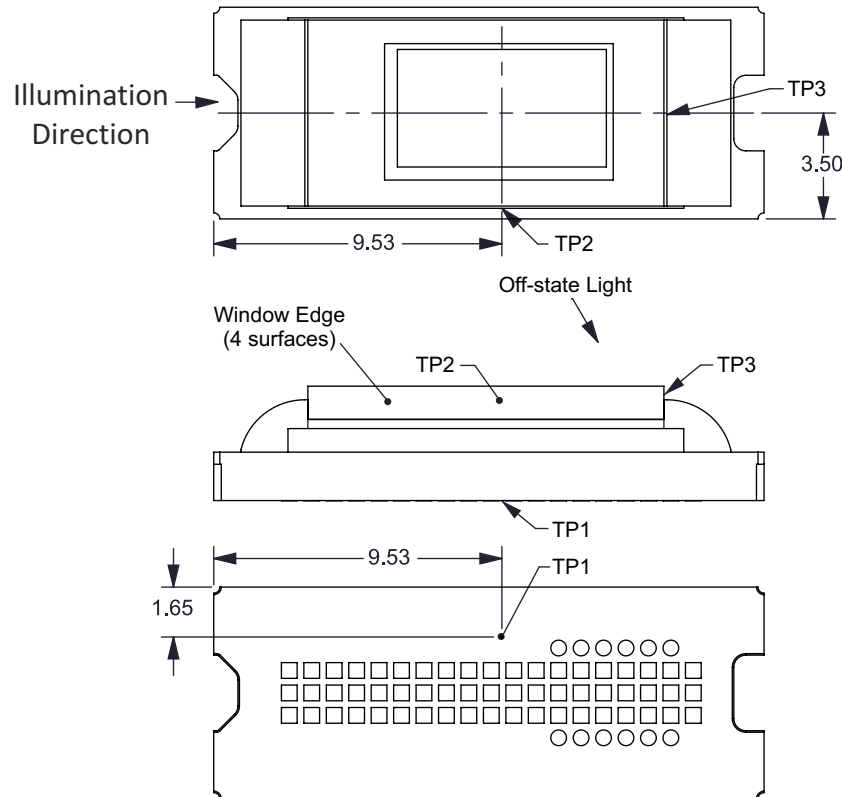


图 7-1. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY - TO - CERAMIC}}) \quad (1)$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}} \quad (2)$$

$$Q_{\text{ILLUMINATION}} = (C_{\text{L2W}} \times \text{SL}) \quad (3)$$

- T_{ARRAY} = Computed DMD array temperature (°C)
- T_{CERAMIC} = Measured ceramic temperature (°C), TP1 location in [图 7-1](#)
- $R_{\text{ARRAY - TO - CERAMIC}}$ = DMD package thermal resistance from array to outside ceramic (°C/W) specified in [Thermal Information](#)
- Q_{ARRAY} = Total DMD power; electrical plus absorbed (calculated) (W)
- $Q_{\text{ELECTRICAL}}$ = Nominal DMD electrical power dissipation (W)

- CL_{2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 0.1 W. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL_{2W} is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00266 W/lm.

Sample Calculation for typical projection application:

1. $T_{CERAMIC} = 55^{\circ}C$, assumed system measurement; see [Recommended Operating Conditions](#) for specification limits.
2. SL = 300 lm
3. $Q_{ELECTRICAL} = 0.100$ W
4. $CL_{2W} = 0.00266$ W/lm
5. $Q_{ARRAY} = 0.100 + (0.00266 \times 300) = 0.898$ W
6. $T_{ARRAY} = 55^{\circ}C + (0.898 \text{ W} \times 5.4^{\circ}C/W) = 59.84^{\circ}C$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON state versus the amount of time the same micromirror is landed in the OFF state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON state 100% of the time (and in the OFF state 0% of the time), whereas 0/100 would indicate that the pixel is in the OFF state 100% of the time. Likewise, 50/50 indicates that the pixel is ON 50% of the time and OFF 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD temperature and landed duty cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical landed duty cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in [Figure 6-1](#). The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).

- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a given long-term average landed duty cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the landed duty cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 landed duty cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 landed duty cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the landed duty cycle tracks one-to-one with the grayscale value, as shown in [表 7-1](#).

表 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red_Cycle_}\% \times \text{Red_Scale_Value}) + (\text{Green_Cycle_}\% \times \text{Green_Scale_Value}) + (\text{Blue_Cycle_}\% \times \text{Blue_Scale_Value}) \quad (4)$$

where

Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_% represent the percentage of the frame time that red, green, and blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the landed duty cycle for various combinations of red, green, blue color intensities would be as shown in [表 7-2](#).

表 7-2. Example Landed Duty Cycle for Full-Color Pixels

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage	
50%	20%	30%	

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

The last factor to account for in estimating the landed duty cycle is any applied image processing. Within the DLP Controller DLPC3433/DLPC3438, the two functions which affect landed duty cycle are Gamma and IntelliBright™.

Gamma is a power function of the form $\text{Output_Level} = A \times \text{Input_Level}^{\text{Gamma}}$, where A is a scaling factor that is typically set to 1.

In the DLPC3430/DLPC3435 controller, gamma is applied to the incoming image data on a pixel-by-pixel basis. A typical gamma factor is 2.2, which transforms the incoming data as shown in [图 7-2](#).

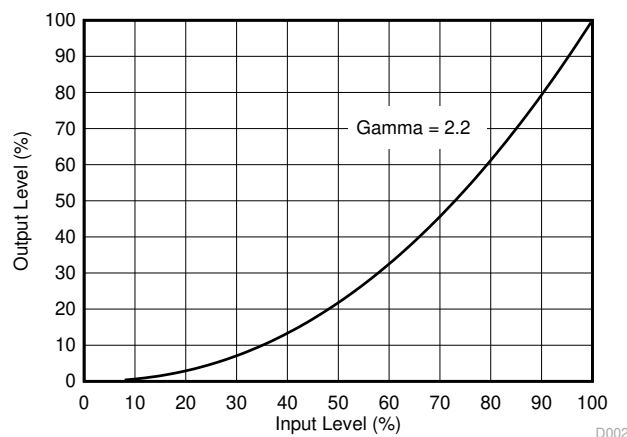


图 7-2. Example of Gamma = 2.2

From [图 7-2](#), if the grayscale value of a given input pixel is 40% (before gamma is applied), then grayscale value will be 13% after gamma is applied. Therefore, since gamma has a direct impact on displayed grayscale level of a pixel, it also has a direct impact on the landed duty cycle of a pixel.

The IntelliBright algorithms content adaptive illumination control (CAIC) and local area brightness boost (LABB) also apply transform functions on the grayscale level of each pixel.

But while amount of gamma applied to every pixel (of every frame) is constant (the exponent, γ , is constant), CAIC and LABB are both adaptive functions that can apply a different amounts of either boost or compression to every pixel of every frame.

Consideration must also be given to any image processing which occurs before the DLPC3433 or DLPC3438 controller.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

CAUTION

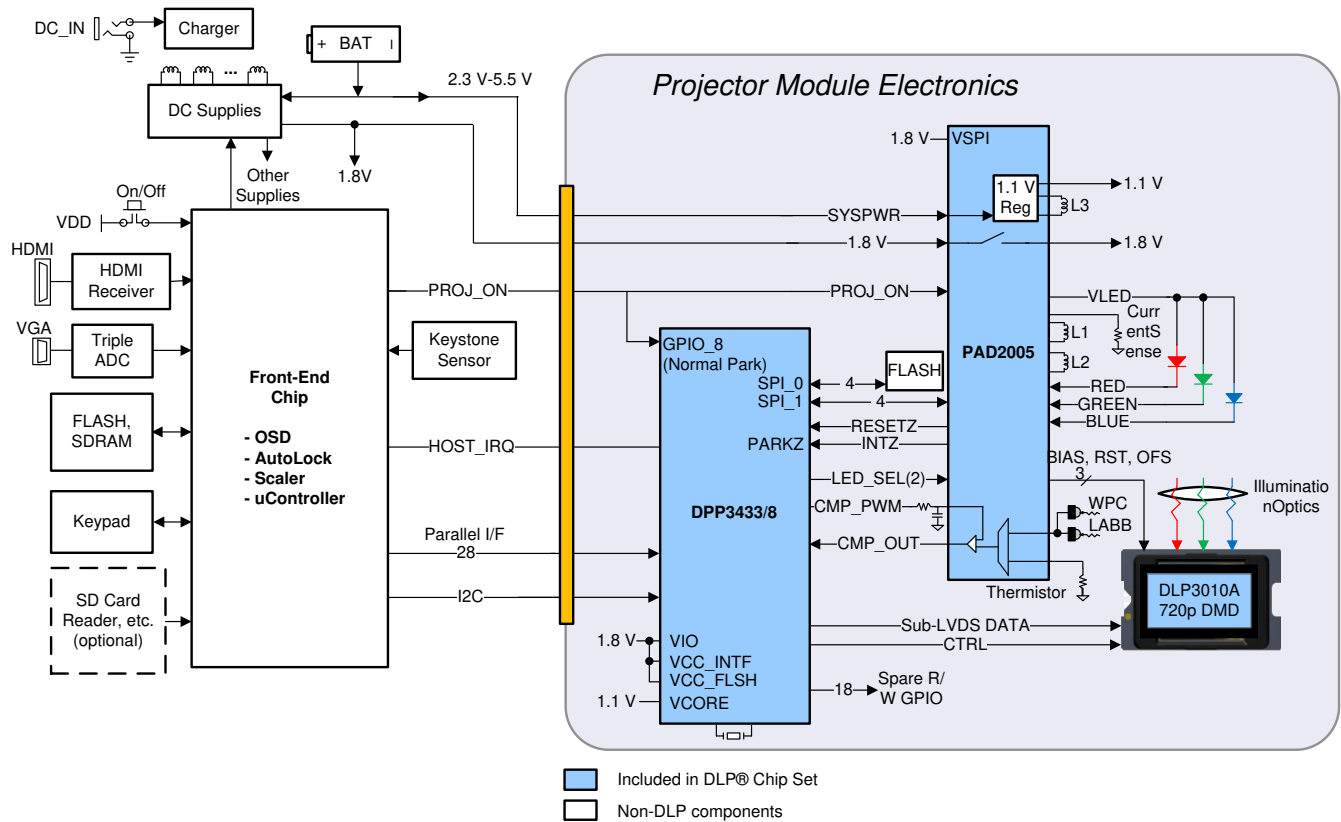
The DLP3010 DMD has mandatory software requirements. Refer to [Software Requirements for TI DLP® Pico™ TRP Digital Micromirror Devices](#) application report for additional information.

The DMDs are spatial light modulators which reflect incoming light from an illumination source to one of two directions, with the primary direction being into a projection or collection optic. Each application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3433/DLPC3438 controller. The new high tilt pixel in the side illuminated DMD increases brightness performance and enables a smaller system electronics footprint for thickness constrained applications. Applications of interest include projection embedded in display devices like smartphones, tablets, cameras, and camcorders. Other applications include wearable (near-eye) displays, battery powered mobile accessory, interactive display, low-latency gaming display, and digital signage.

DMD power-up and power-down sequencing is strictly controlled by the DLPA200x/DLPA3000. Refer to [Power Supply Recommendations](#) for power-up and power-down specifications. To ensure reliable operation, DLP3010 DMD must always be used with DLPC3433 or DLPC3438 display controller and DLPA200x/DLPA3000 PMIC/LED driver.

8.2 Typical Application

A common application when using the DLPC3433/DLPC3438 is for creating a pico-projector that can be used as an accessory to a smartphone, tablet or a laptop. The DLPC3433/DLPC3438 in the pico-projector receives images from a multimedia front end within the product as shown in the following figure.



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图 8-1. Typical Application Diagram

8.2.1 Design Requirements

A pico-projector is created by using a DLP chip set comprised of DLP3010 DMD, a DLPC3433/DLPC3438 controller and a DLPA200x/DLPA3000 PMIC/LED driver. The DLPC3433/DLPC3438 controller does the digital image processing, the DLPA200x/DLPA3000 provides the needed analog functions for the projector, and DLP3010 DMD is the display device for producing the projected image.

In addition to the three DLP chips in the chip set, other chips may be needed. At a minimum a Flash part is needed to store the software and firmware to control the DLPC3433/DLPC3438 controller.

The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the pico-projector.

For connecting the DLPC3433/DLPC3438 controller to the multimedia front end for receiving images, parallel interface is used. When the parallel interface is used, I2C should be connected to the multimedia front end for sending commands to the DLPC3433/DLPC3438 controller and configuring the DLPC3433/DLPC3438 controller for different features.

8.2.2 Detailed Design Procedure

For connecting together the DLPC3433/DLPC3438 controller, the DLPA200x/DLPA3000, and the DLP3010 DMD, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve a reliable projector.

The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents is as shown in [图 8-2](#). For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs.

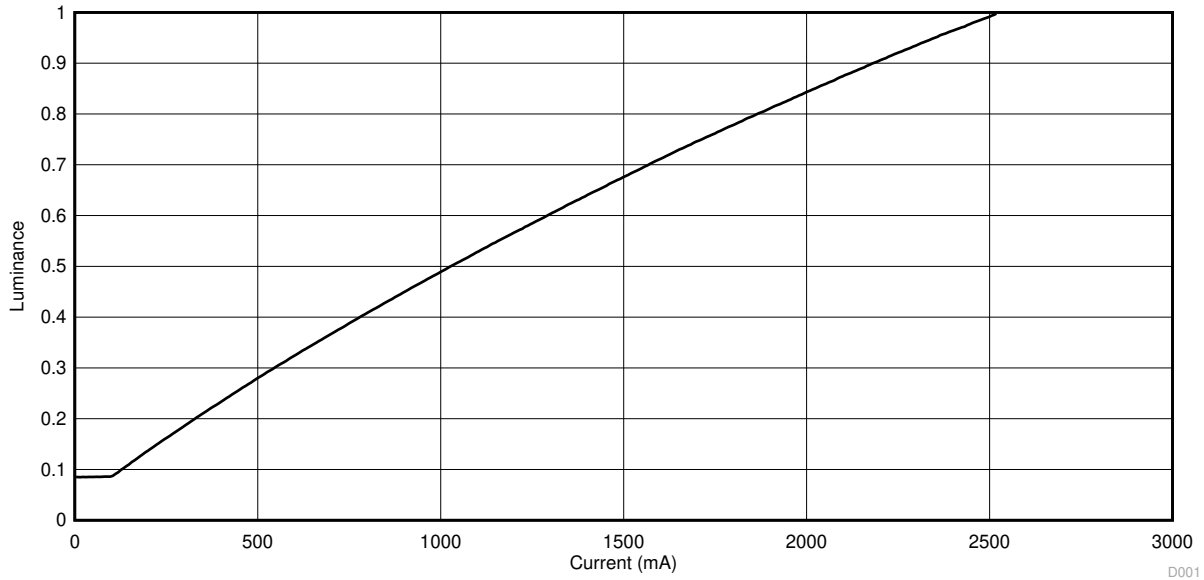


图 8-2. Luminance vs Current

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD: VSS, VDD, VDDI, VOFFSET, VBIAS, and VRESET. DMD power-up and power-down sequencing is strictly controlled by the DLP3010 devices.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

VDD, VDDI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD's reliability and lifetime. Refer to [Figure 9-2](#). VSS must also be connected.

9.1 Power Supply Power-Up Procedure

- During power-up, VDD and VDDI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in [Recommended Operating Conditions](#). Refer to [Table 9-1](#) and the [Layout Example](#) for power-up delay requirements.
- During power-up, the DMD's LPSDR input pins shall not be driven high until after VDD and VDDI have settled at operating voltage.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS. Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed previously and in [Figure 9-1](#).

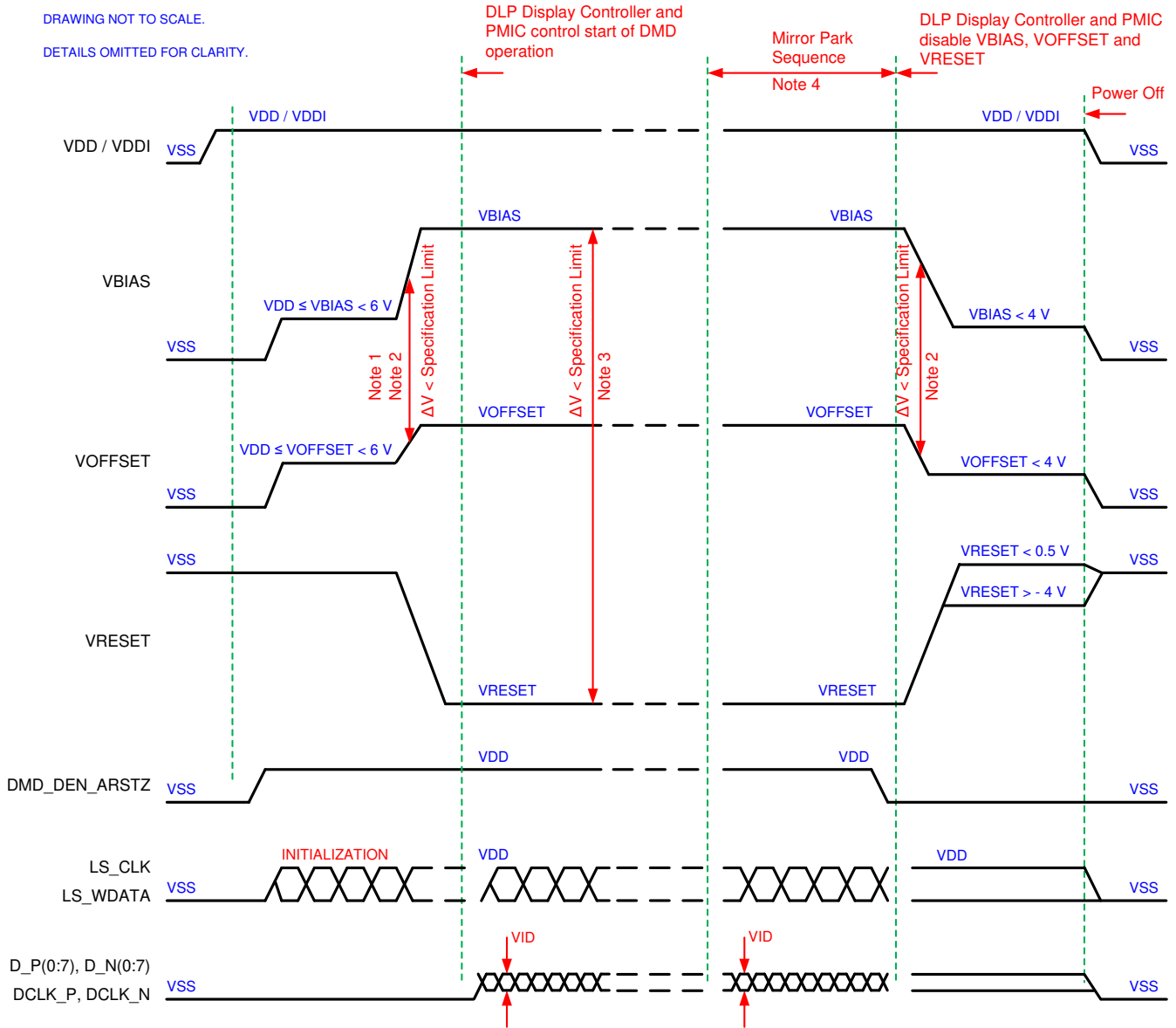
9.2 Power Supply Power-Down Procedure

- Power-down sequence is the reverse order of the previous power-up sequence. VDD and VDDI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within 4 V of ground.
- During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET, but it is a strict requirement that the delta between VBIAS and VOFFSET must be within the specified limit shown in [Recommended Operating Conditions](#) (refer to Note 2 for [Figure 9-1](#)).
- During power-down, the DMD's LPSDR input pins must be less than VDDI, the specified limit shown in [Recommended Operating Conditions](#).
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed previously and in [Figure 9-1](#).

9.3 Power Supply Sequencing Requirements

DRAWING NOT TO SCALE.

DETAILS OMITTED FOR CLARITY.

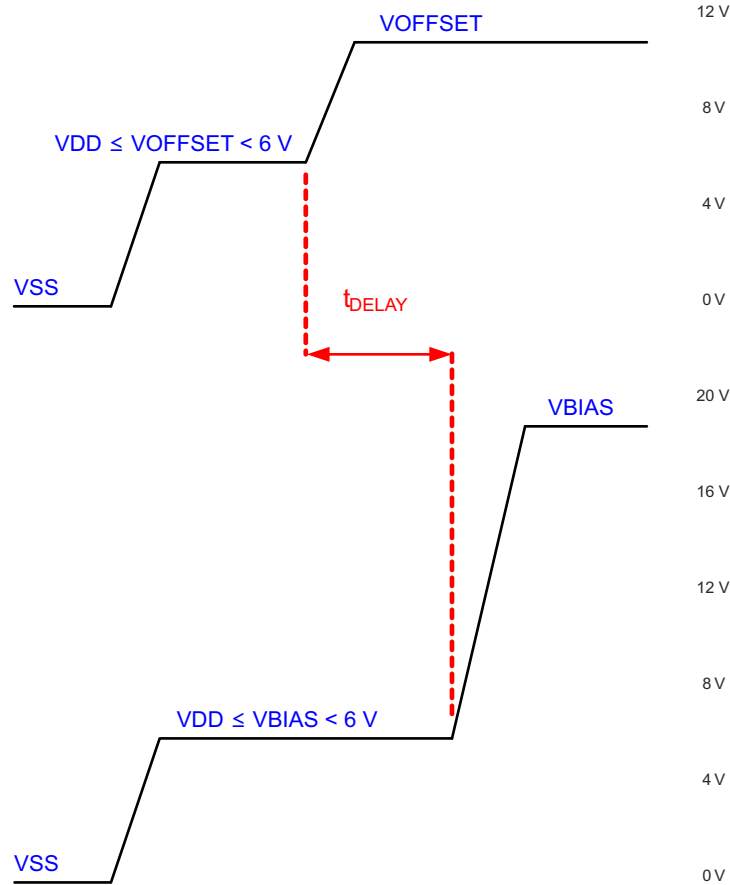


- Refer to 表 9-1 and 图 9-2 for critical power-up sequence delay requirements.
- To prevent excess current, the supply voltage delta $|VBIAS - VOFFSET|$ must be less than specified in 节 6.4. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down. Refer to 表 9-1 and 图 9-2 for power-up delay requirements.
- To prevent excess current, the supply voltage delta $|VBIAS - VRESET|$ must be less than specified limit shown in 节 6.4.
- When system power is interrupted, the DLPA200x initiates hardware power-down that disables VBIAS, VRESET and VOFFSET after the Micromirror Park Sequence.
- Drawing is not to scale and details are omitted for clarity.

图 9-1. Power Supply Sequencing Requirements (Power Up and Power Down)

表 9-1. Power-Up Sequence Delay Requirement

PARAMETER		MIN	MAX	UNIT
t_{DELAY}	Delay requirement from VOFFSET power up to VBIAS power up	2		ms
V_{OFFSET}	Supply voltage level during power - up sequence delay (see 图 9-2)		6	V
V_{BIAS}	Supply voltage level during power - up sequence delay (see 图 9-2)		6	V



A. Refer to 表 9-1 for VOFFSET and VBIAS supply voltage levels during power-up sequence delay.

图 9-2. Power-Up Sequence Delay Requirement

10 Layout

10.1 Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board to board connector to a flex cable. Flex cable provides the interface of data and CTRL signals between the DLPC343x controller and the DLP3010 DMD. For detailed layout guidelines refer to the layout design files. Some layout guideline for the flex cable interface with DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer [图 10-1](#).
- Minimum of two 100-nF decoupling capacitor close to VBIAS. Capacitor C6 and C7 in [图 10-1](#).
- Minimum of two 100-nF decoupling capacitor close to VRST. Capacitor C9 and C8 in [图 10-1](#).
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C5 and C4 in [图 10-1](#).
- Minimum of four 100-nF decoupling capacitor close to Vcci and Vcc. Capacitor C1, C2, C3 and C10 in [图 10-1](#).

10.2 Layout Example

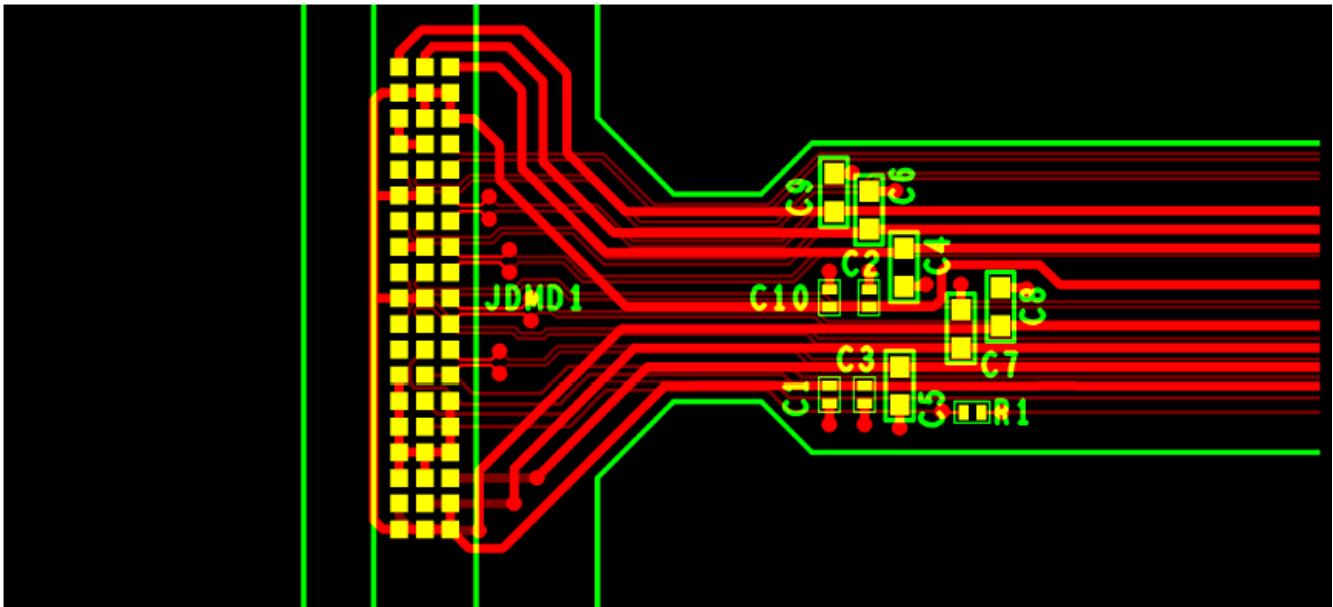


图 10-1. Power Supply Connections

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.1.2 Device Nomenclature

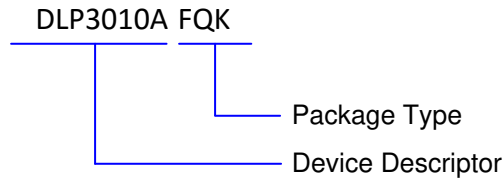


图 11-1. Part Number Description

11.1.3 Device Markings

The device marking includes the legible character string GHJJJK DLP3010AFQK. GHJJJK is the lot trace code. DLP3010AFQK is the device part number.

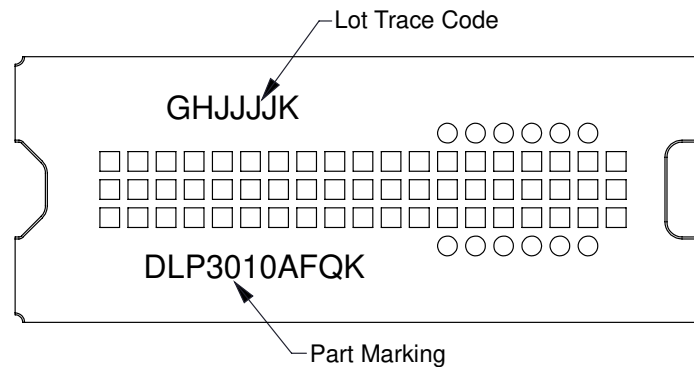


图 11-2. DMD Marking

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLP3010A	Click here	Click here	Click here	Click here	Click here
DLPC3433	Click here	Click here	Click here	Click here	Click here
DLPC3438	Click here	Click here	Click here	Click here	Click here
DLPA2005	Click here	Click here	Click here	Click here	Click here
DLPA3000	Click here	Click here	Click here	Click here	Click here

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP3010AFQK	ACTIVE	CLGA	FQK	57	120	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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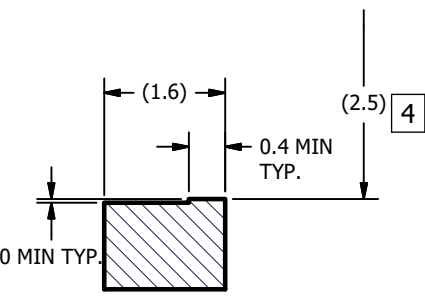
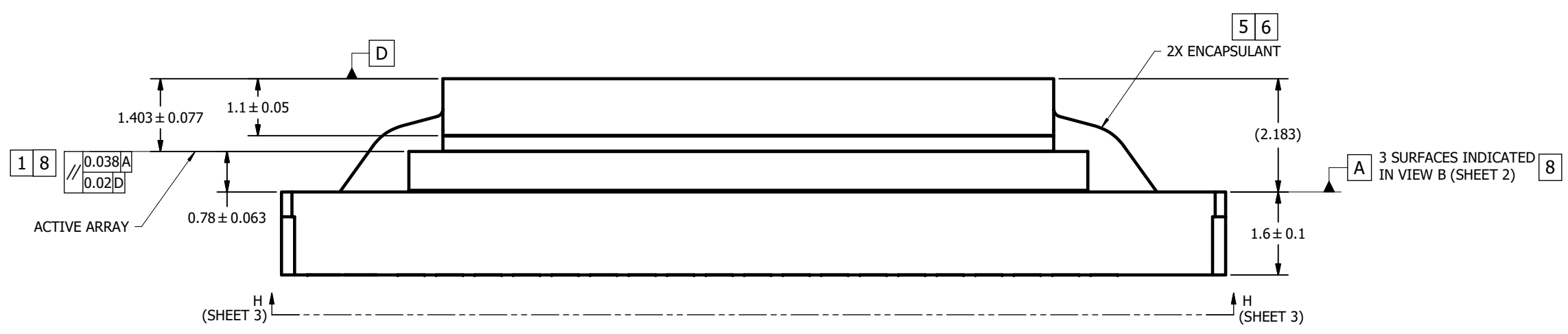
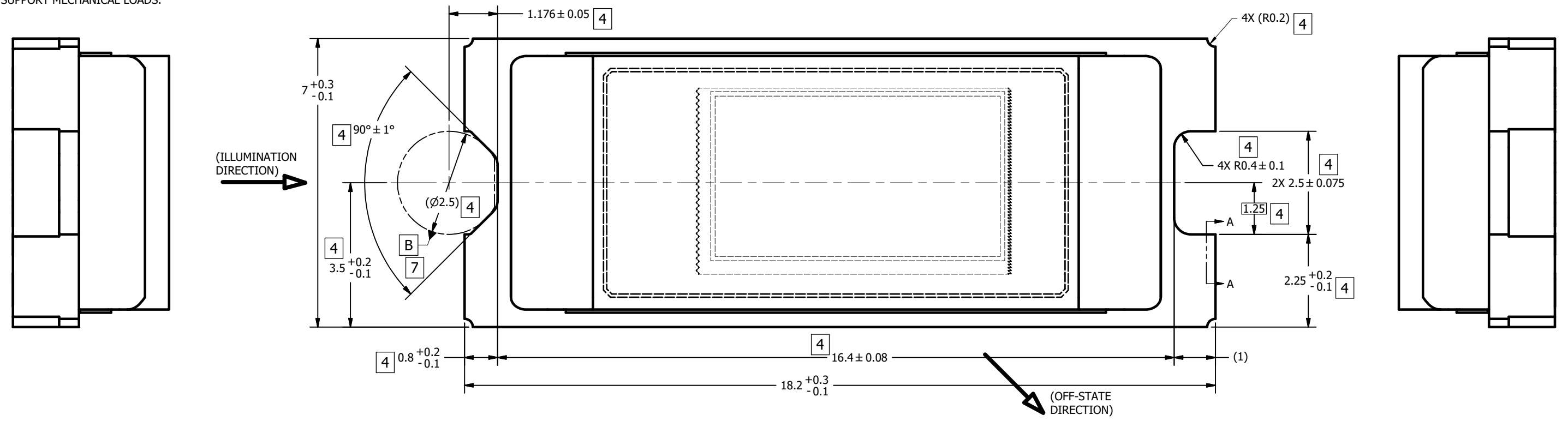
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REVISIONS			
REV	DESCRIPTION	DATE	BY
A	ECO 2133835: INITIAL RELEASE	6/6/2013	BMH
B	ECO 2134093: CORRECT WINDOW THK TOL, ZONE B6	6/17/2013	BMH
C	ECO 2186947: ADD APERTURE SLOTS PICTORIALY	4/8/2020	PPC

NOTES UNLESS OTHERWISE SPECIFIED:

- 1 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
- 2 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
- 3 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.
- 4 NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
- 5 ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW C (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
- 6 ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
- 7 DATUM B IS DEFINED BY A DIA. 2.5 PIN, WITH A FLAT ON THE SIDE FACING TOWARD THE CENTER OF THE ACTIVE ARRAY, AS SHOWN IN VIEW B (SHEET 2).
- 8 WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.



UNLESS OTHERWISE SPECIFIED

- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES:
 - ANGLES ± 1'
 - 2 PLACE DECIMALS ± 0.25
 - 1 PLACE DECIMALS ± 0.50
- DIMENSIONAL LIMITS APPLY BEFORE PROCEEDING
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994
- REMOVE ALL BURRS AND SHARP EDGES
- PARENTHETICAL INFORMATION FOR REFERENCE ONLY

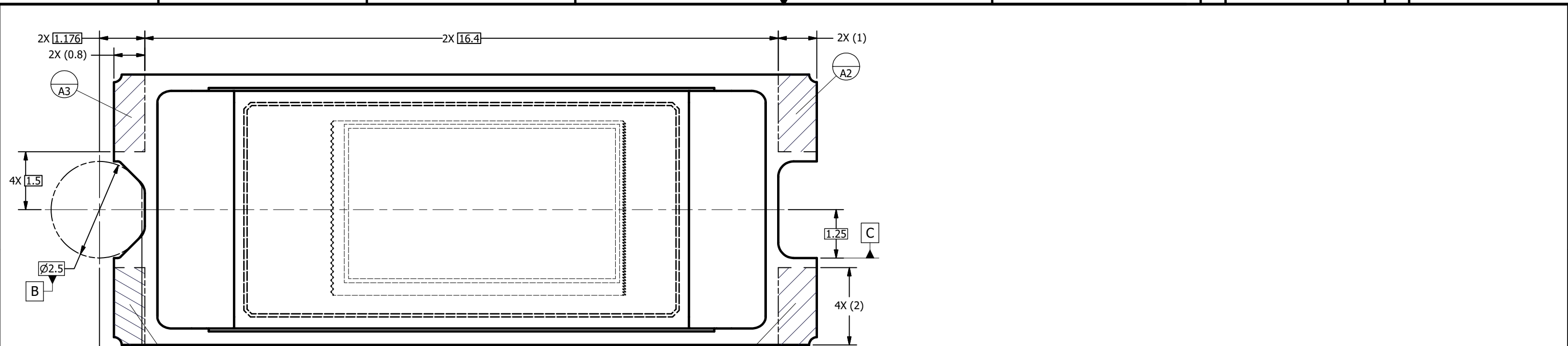
DRAWN
B. HASKETT 6/6/2013
ENGINEER
B. HASKETT 6/6/2013
QA/CE
P. KONRAD 6/7/2013
CM
S. SUSI 6/6/2013
S. CROFF 6/10/2013
APPROVED
R. LONG 6/6/2013

TEXAS INSTRUMENTS
Dallas, Texas

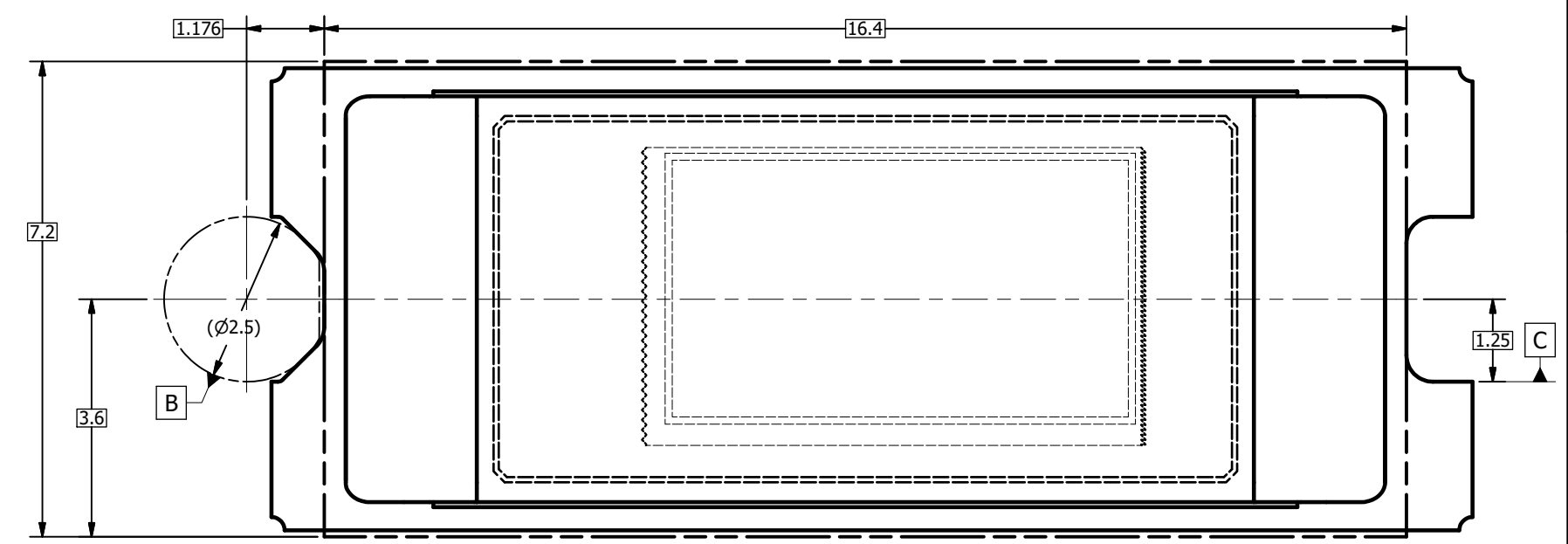
TITLE
ICD, MECHANICAL, DMD,
.3 720p SERIES 245
(FQK PACKAGE)

SIZE D SCALE 20:1 DWG NO. 2512014 SHEET 1 OF 3 REV C

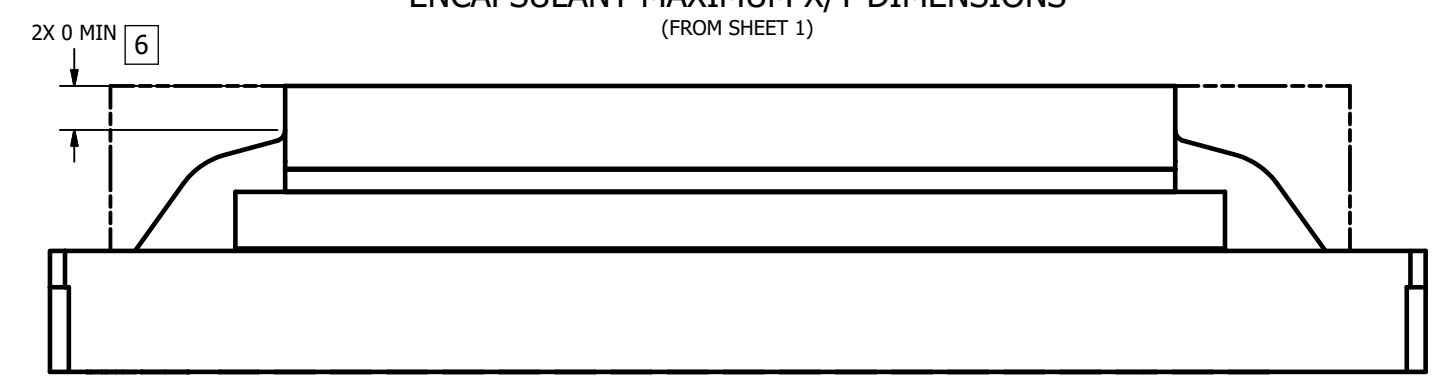
0314DA	APPLICATION
NEXT ASSY	USED ON



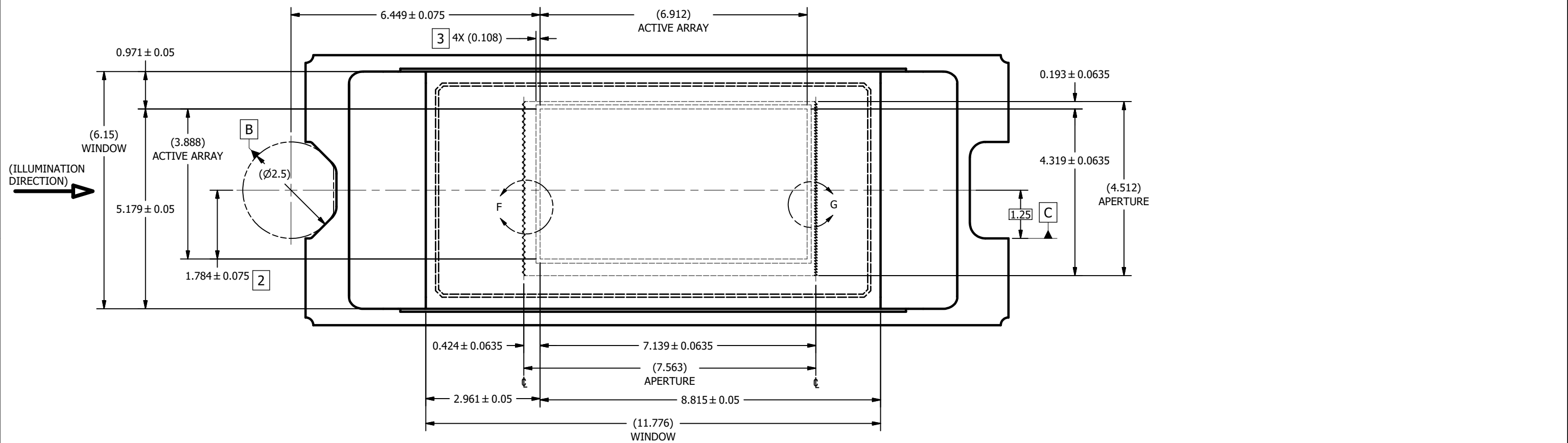
VIEW B
DATUMS A, B, C, AND E
(FROM SHEET 1)



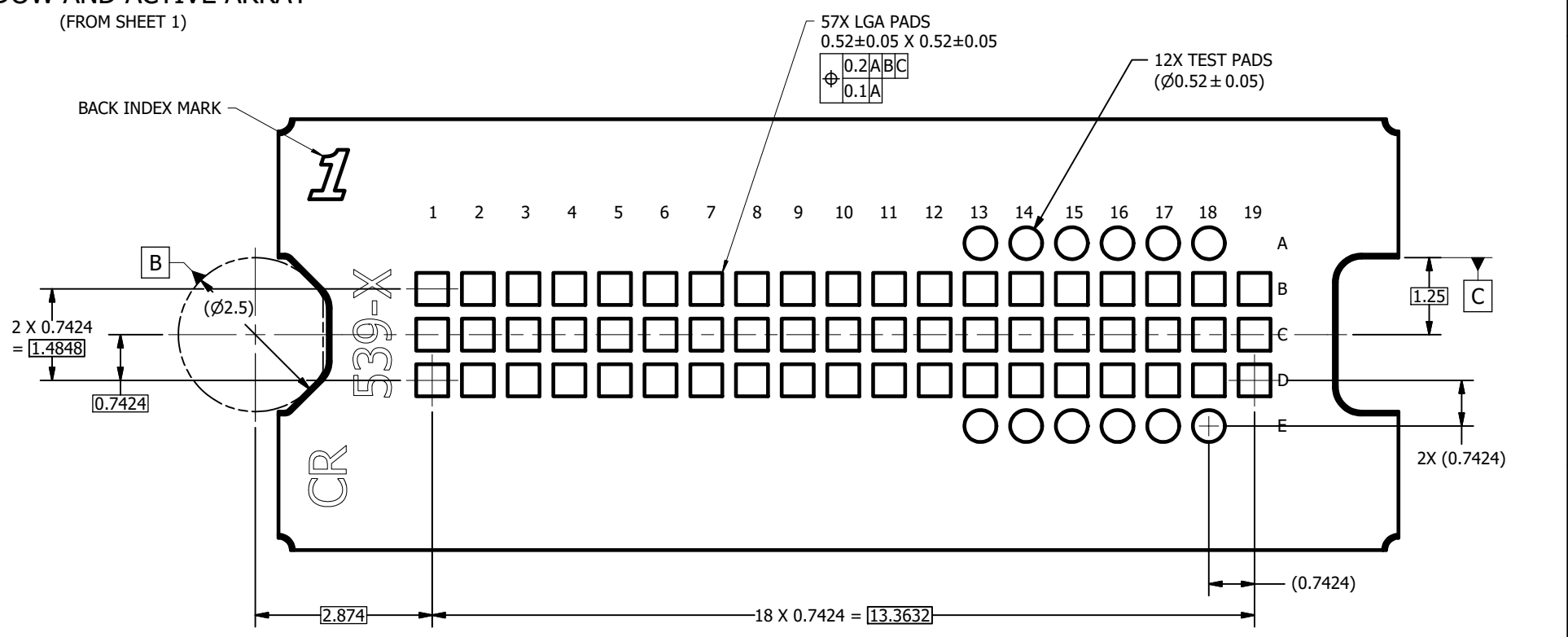
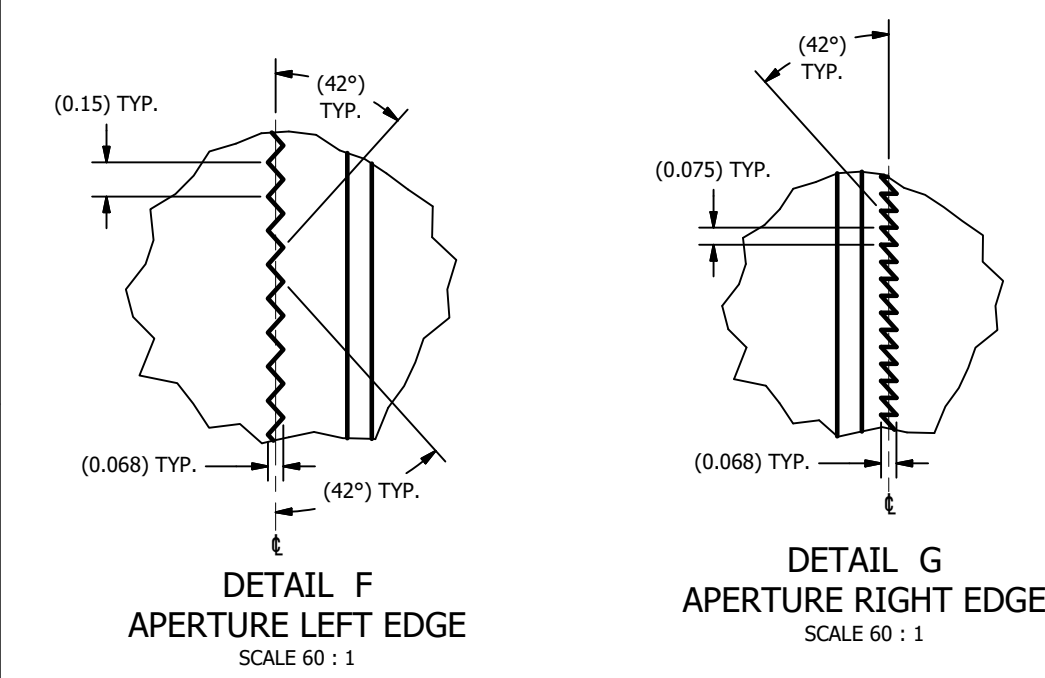
VIEW C 5
ENCAPSULANT MAXIMUM X/Y DIMENSIONS
(FROM SHEET 1)



VIEW D
ENCAPSULANT MAXIMUM HEIGHT



VIEW E
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



VIEW H-H
BACK SIDE METALLIZATION
(FROM SHEET 1)

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