DLP660TE 0.66 4K UHD 数字微镜器件

1 特性

- 0.66 英寸对角线微镜阵列
  - 系统可在屏幕上显示 4K 超高清 (UHD) 3840 × 2160 像素
  - 5.4 微米微镜间距
  - ±17° 微镜倾斜度（相对于平坦表面）
  - 底部照明
- 2xLVDS 输入数据总线
- DLP660TE 芯片组包括:
  - DLP660TE DMD
  - DLPC4420 控制器
  - DLPA100 控制器电源管理和电机驱动器 IC

2 应用

- 4K 超高清显示
- 数字标牌
- 激光电视
- 投影映射

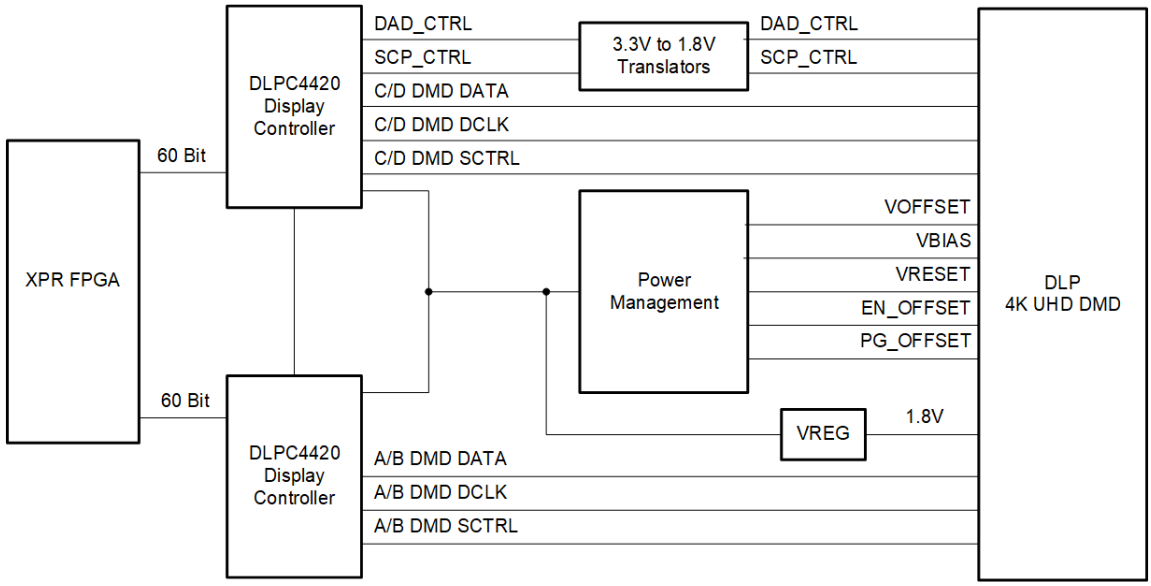
3 说明

TI DLP® DLP660TE 数字微镜器件 (DMD) 是一款数控微光机电系统 (MOEMS) 空间光调制器 (SLM)，可实现明亮、经济实惠的全 4K UHD 显示解决方案。与适当的光学系统配合使用时，DLP660TE DMD 可显示真 4K UHD 分辨率（830 万屏幕像素），并能够向各种显示介质上投射准确且清晰的图像。DLP660TE DMD 通过与 DLPC4420 显示控制器、DLPA100 控制器电源和电机驱动器配合使用，可实现高性能系统，而且非常适合 4K UHD 高亮度显示应用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DLP660TE	FYG (350)	35mm × 32mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



DLP660TE 简化应用

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (July 2022) to Revision C (February 2023)	Page
• 将控制器更改为 DLPC4420，将芯片组元件链接到产品页面	1
• 将控制器更改为 DLPC4420，更新了图	1
• Added the lamp illumination section	13
• Added the DMD efficiency specification	24
• Changed controller to DLPC4420	26
• Changed controller to DLPC4420	27
• Changed controller to DLPC4420, added a table with legacy part numbers and mechanical ICD	32
• Changed controller to DLPC4420	34
• Changed controller to DLPC4420	34
• Changed controller to DLPC4420	34
• Changed controller to DLPC4420	39
• Changed controller to DLPC4420	42

Changes from Revision A (September 2020) to Revision B (July 2022)	Page
• Changed SCP specifications to reflect 'Rise/Fall Time'	19
• Corrected 图 6-3	19
• Changed controller to DLPC4420, updated the application diagrams	32

Changes from Revision (April 2019) to Revision A (September 2020)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1

- Revised Pin Functions table to add LVDS and LVCMOS types to previously pins.....4

5 Pin Configuration and Functions

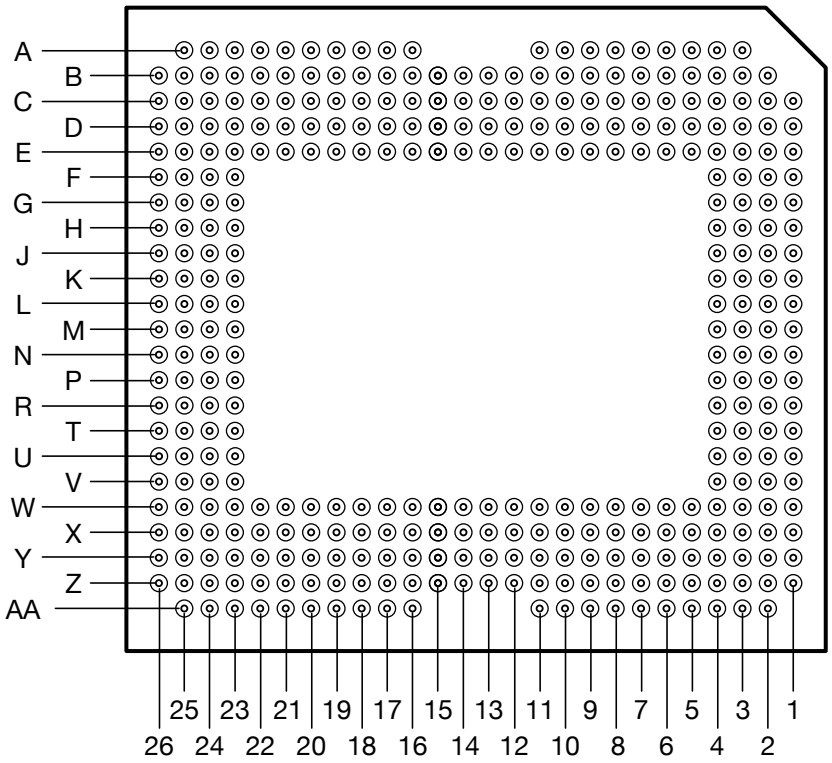


图 5-1. Series 610 350-pin FYG Bottom View

CAUTION

To ensure reliable, long-term operation of the 0.66-inch UHD S610 DMD, it is critical to properly manage the layout and operation of the signals identified in the table below. For specific details and guidelines, refer to the *PCB Design Requirements for TI DLP Standard TRP Digital Micromirror Devices* application report before designing the board.

表 5-1. Pin Functions

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
DATA INPUTS					
D_AN(0)	C7	Input	2xLVDS		LVDS pair for Data Bus A (15:0)
D_AP(0)	C8				
D_AN(1)	D4				
D_AP(1)	E4				
D_AN(2)	C5				
D_AP(2)	C4				
D_AN(3)	D6				
D_AP(3)	C6				
D_AN(4)	D8				
D_AP(4)	D7				
D_AN(5)	D3				
D_AP(5)	E3				
D_AN(6)	B3				
D_AP(6)	C3				
D_AN(7)	E11				
D_AP(7)	E10				
D_AN(8)	E6				
D_AP(8)	E5				
D_AN(9)	B10				
D_AP(9)	C10				
D_AN(10)	B8				
D_AP(10)	B9				
D_AN(11)	C13				
D_AP(11)	C14				
D_AN(12)	D15				
D_AP(12)	E15				
D_AN(13)	B12				
D_AP(13)	B13				
D_AN(14)	B15				
D_AP(14)	B16				
D_AN(15)	C16				
D_AP(15)	C17				

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_BN(0)	Y8	Input	2xLVDS		LVDS pair for Data Bus B (15:0)
D_BP(0)	Y7				
D_BN(1)	X4				
D_BP(1)	W4				
D_BN(2)	Z3				
D_BP(2)	Y3				
D_BN(3)	X6				
D_BP(3)	Y6				
D_BN(4)	X8				
D_BP(4)	X7				
D_BN(5)	X3				
D_BP(5)	W3				
D_BN(6)	W15				
D_BP(6)	X15				
D_BN(7)	W11				
D_BP(7)	W10				
D_BN(8)	W6				
D_BP(8)	W5				
D_BN(9)	AA9				
D_BP(9)	AA10				
D_BN(10)	Z8				
D_BP(10)	Z9				
D_BN(11)	Y13				
D_BP(11)	Y14				
D_BN(12)	Z10				
D_BP(12)	Y10				
D_BN(13)	Z12				
D_BP(13)	Z13				
D_BN(14)	Z15				
D_BP(14)	Z16				
D_BN(15)	Y16				
D_BP(15)	Y17				

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_CN(0)	C18	Input	2xLVDS		LVDS pair for Data Bus C (15:0)
D_CP(0)	C19				
D_CN(1)	A20				
D_CP(1)	A19				
D_CN(2)	L23				
D_CP(2)	K23				
D_CN(3)	C23				
D_CP(3)	B23				
D_CN(4)	G23				
D_CP(4)	H23				
D_CN(5)	H24				
D_CP(5)	G24				
D_CN(6)	B18				
D_CP(6)	B19				
D_CN(7)	C21				
D_CP(7)	B21				
D_CN(8)	D23				
D_CP(8)	E23				
D_CN(9)	D25				
D_CP(9)	C25				
D_CN(10)	L24				
D_CP(10)	K24				
D_CN(11)	K25				
D_CP(11)	J25				
D_CN(12)	B24				
D_CP(12)	A24				
D_CN(13)	D26				
D_CP(13)	C26				
D_CN(14)	G25				
D_CP(14)	F25				
D_CN(15)	K26				
D_CP(15)	J26				

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
D_DN(0)	Y18	Input	2xLVDS		LVDS pair for Data Bus D (15:0)
D_DP(0)	Y19				
D_DN(1)	AA20				
D_DP(1)	AA19				
D_DN(2)	N23				
D_DP(2)	P23				
D_DN(3)	Y23				
D_DP(3)	Z23				
D_DN(4)	U23				
D_DP(4)	T23				
D_DN(5)	T24				
D_DP(5)	U24				
D_DN(6)	Z18				
D_DP(6)	Z19				
D_DN(7)	Y21				
D_DP(7)	Z21				
D_DN(8)	X23				
D_DP(8)	W23				
D_DN(9)	X25				
D_DP(9)	Y25				
D_DN(10)	N24				
D_DP(10)	P24				
D_DN(11)	P25				
D_DP(11)	R25				
D_DN(12)	Z24				
D_DP(12)	AA24				
D_DN(13)	X26				
D_DP(13)	Y26				
D_DN(14)	U25				
D_DP(14)	V25				
D_DN(15)	P26				
D_DP(15)	R26				
DCLK_AN	B6	Input	LVDS		LVDS pair for Data Clock A
DCLK_AP	B5				
DCLK_BN	Z6	Input	LVDS		LVDS pair for Data Clock B
DCLK_BP	Z5				
DCLK_CN	G26	Input	LVDS		LVDS pair for Data Clock C
DCLK_CP	F26				
DCLK_DN	U26	Input	LVDS		LVDS pair for Data Clock D.
DCLK_DP	V26				
DATA CONTROL INPUTS					
SCTRL_AN	A10	Input	LVDS		LVDS pair for Serial Control (Sync) A
SCTRL_AP	A9				

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
SCTRL_BN	Y4	Input	LVDS		LVDS pair for Serial Control (Sync) B
SCTRL_BP	Y5				
SCTRL_CN	E24	Input	LVDS		LVDS pair for Serial Control (Sync) C
SCTRL_CP	D24				
SCTRL_DN	W24	Input	LVDS		LVDS pair for Serial Control (Sync) D
SCTRL_DP	X24				
DAD CONTROL INPUTS					
RESET_ADDR(0)	R3	Input	LVCMOS		Reset Driver Address Select. Bond Pad connects to an internal Pull Down circuit
RESET_ADDR(1)	R4				
RESET_ADDR(2)	T3				
RESET_ADDR(3)	U2				
RESET_MODE(0)	P4	Input	LVCMOS		Reset Driver Mode Select. Bond Pad connects to an internal Pull Down circuit
RESET_MODE(1)	V3				
RESET_OEZ	R2	Input	LVCMOS		Active Low. Output Enable signal for internal Reset Driver circuitry. Bond Pad connects to an internal Pull Up circuit
RESET_SEL(0)	P3	Input	LVCMOS		Reset Driver Level Select. Bond Pad connects to an internal Pull Down circuit
RESET_SEL(1)	V2				
RESET_STROBE	W8	Input	LVCMOS		Rising edge on RESET_STROBE latches in the control signals. Bond Pad connects to an internal Pull Down circuit
RESETZ	U4	Input	LVCMOS		Active Low. Places reset circuitry in known VOFFSET state. Bond Pad connects to an internal Pull Down circuit
SCP CONTROL					
SCPCLK	W17	Input	LVCMOS		Serial Communications Port Clock. SCPCLK is only active when SCPENZ goes low. Bond Pad connects to an internal Pull Down circuit
SCPDI	W18	Input	LVCMOS		Serial Communications Port Data. Synchronous to the Rising Edge of SCPCLK. Bond Pad connects to an internal Pull Down circuit
SCPENZ	X18	Input	LVCMOS		Active Low Serial Communications Port Enable. Bond Pad connects to an internal Pull Down circuit
SCPDO	W16	Output	LVCMOS		Serial Communications Port output
EXTERNAL REGULATOR SIGNALS					
EN_BIAS	J4	Output	LVCMOS		Active High. Enable signal for external VBIAS regulator
EN_OFFSET	H3	Output	LVCMOS		Active High. Enable signal for external VOFFSET regulator
EN_RESET	J3	Output	LVCMOS		Active High. Enable signal for external VRESET regulator
OTHER SIGNALS					
RESET_IRQZ	U3	Output	LVCMOS		Active Low. Output Interrupt to DLP controller (ASIC)
TEMP_PLUS	E16	Analog			Temperature Sensor Diode Anode.(1)
TEMP_MINUS	E17	Analog			Temperature Sensor Diode Cathode. (1)
POWER					

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
VBIAS	A5, A6, A7	Power			Power supply for Positive Bias level of micromirror reset signal
V_{CC}	A8, B2, C1, D1, D10, D12, D19, E1, E19, E20, E21, F1, K1, L1, M1, N1, P1,V1, W1, W19, W20, W21, X1, X10, X12, X19, Y1, Z1, Z2, AA2, AA8,	Power			Power supply for low voltage CMOS logic. Power supply for normal high voltage at micromirror address electrodes. Power supply for Offset level during power down sequence
V_{CCI}	A11, A16, A17, A18, A21, A22, A23, AA11, AA16, AA17, AA18, AA21, AA22, AA23,	Power			Power supply for low voltage CMOS LVDS interface
V_{OFFSET}	A3, A4, A25, B26, L26, M26, N26, Z26, AA3, AA4, AA25	Power			Power supply for high voltage CMOS logic. Power supply for stepped high voltage at micromirror address electrodes. Power supply for Offset level of MBRST(15:0)
V_{RESET}	G1, H1, J1, R1, T1, U1	Power			Power supply for Negative Reset level of micromirror reset signal
V_{SS} (Ground)	B4, B7, B11, B14, B17, B20, B22, B25, C2, C9, C20, C22, C24, D2, D5, D9, D11, D14, D18, D20, D21, D22, E2, E7, E9, E22, E25, E26, F4, F23, F24, H2, H4, H25, H26, J23, J24, K2, L2, L3, L4, L25, M2, M3, M4, M23, M24, M25, N2, N3, N25, P2,R23, R24, T2, T4, T25, T26, V4, V23, V24, W2, W7, W9, W22, W25, W26, X2, X5, X9, X11, X20, X21, X22, Y2, Y9, Y20, Y22, Y24, Z4, Z7, Z11, Z14, Z17, Z20, Z22, Z25	Ground			Common Return for all power
RESERVED SIGNALS					
RESERVED_PFE	E18	Ground			Connect to ground on the printed circuit board (PCB). Bond Pad connects to an internal Pull Down circuit
RESERVED_TM	G4	Ground			Connect to ground on the printed circuit board (PCB). Bond Pad connects to an internal Pull Down circuit
RESERVED_TP0	E8	Input			Do Not Connect on the printed circuit board (PCB)
RESERVED_TP1	J2	Input			Do Not Connect on the printed circuit board (PCB)
RESERVED_TP2	G2	Input			Do Not Connect on the printed circuit board (PCB)
RESERVED_BA	N4	Output			Do Not Connect on the printed circuit board (PCB)
RESERVED_BB	K4	Output			Do Not Connect on the printed circuit board (PCB)

表 5-1. Pin Functions (continued)

PIN		TYPE	SIGNAL	DATA RATE	DESCRIPTION
NAME	NO.				
RESERVED_BC	X17	Output			Do Not Connect on the printed circuit board (PCB)
RESERVED_BD	D17	Output			Do Not Connect on the printed circuit board (PCB)

(1) VSS must be connected for proper DMD operation.

Pin Functions - Test Pads

Pin Number	System Board
E13	Do not connect
C12	Do not connect
D13	Do not connect
C11	Do not connect
E14	Do not connect
E12	Do not connect
C15	Do not connect
D16	Do not connect
W13	Do not connect
Y12	Do not connect
X13	Do not connect
Y11	Do not connect
W14	Do not connect
W12	Do not connect
Y15	Do not connect
X16	Do not connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply Voltages				
V_{CC}	Supply voltage for LVCMOS core logic(2)	–0.5	2.3	V
V_{CCI}	Supply voltage for LVDS receivers(2)	–0.5	2.3	V
V_{OFFSET}	Supply voltage for HVCMOS and micromirror electrode(2) (3)	–0.5	11	V
V_{BIAS}	Supply voltage for micromirror electrode(2)	–0.5	19	V
V_{RESET}	Supply voltage for micromirror electrode(2)	–15	–0.3	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)(4)		0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(5)		11	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(6)		34	V
Input Voltages				
	Input voltage for all other LVCMOS input pins(2)	–0.5	V_{CC} + 0.5	V
	Input voltage for all other LVDS input pins(2) (6)	–0.5	V_{CCI} + 0.5	V
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(6)		500	mV
I_{ID}	Input differential current(7)		6.25	mA
Clocks				
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_A		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_B		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_C		400	MHz
f_{CLOCK}	Clock frequency for LVDS interface, DCLK_D		400	MHz
Environmental				
T_{ARRAY} and T_{WINDOW}	Temperature, operating(8)	0	90	°C
Temperature, non-operating(8)		–40	90	°C
$\lvert T_{DELTA} \rvert$	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 (9)		30	°C
T_{DP}	Dew Point Temperature, operating and non-operating (noncondensing)		81	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are referenced to common ground V_{SS}. V_{BIAS}, V_{CC}, V_{CCI}, V_{OFFSET}, and V_{RESET} power supplies are all required for proper DMD operation. V_{SS} must also be connected.
(3) V_{OFFSET} supply transients must fall within specified voltages.
(4) Exceeding the recommended allowable voltage difference between V_{CC} and V_{CCI} may result in excessive current draw.
(5) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{OFFSET} may result in excessive current draw.
(6) Exceeding the recommended allowable voltage difference between V_{BIAS} and V_{RESET} may result in excessive current draw.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors.
(8) The highest temperature of the active array (as calculated using 节 7.6) or of any point along the window edge as defined in 图 7-2. The locations of thermal test points TP2, TP3, TP4 and TP5 in 图 7-2 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, that point is used.
(9) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 7-2. The window test points TP2, TP3, TP4 and TP5 shown in 图 7-2 are intended to result in the worst case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point is be used.

6.2 Storage Conditions

Applicable for the DMD as a component or non-operating in a system

		MIN	MAX	UNIT
T_{stg}	DMD storage temperature	– 40	80	°C
T_{DP-AVG}	Average dew point temperature, (non-condensing) (1)		28	°C
T_{DP-MAX}	Elevated dew point temperature range , (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(2) Exposure to dew point temperatures in the elevated range during storage and operation is limited to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions . No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
Voltage Supply					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{CCI}	LVCMOS LVDS Interface supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	– 14.5	– 14	– 13.5	V
$\lvert V_{CC} - V_{CCI} \rvert$	Supply voltage delta (absolute value)(3)		0	0.3	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage delta (absolute value)(4)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage delta (absolute value)(5)			33	V
LVCMOS Interface					
$V_{IH(DC)}$	DC input high voltage(6)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(6)	– 0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(6)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(6)	– 0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse width(7)	10			ns
SCP Interface					
f_{SCPCLK}	SCP clock frequency(8)			500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising edge of SCPCLK to valid SCPDO(9)	0		900	ns
$t_{SCP\_NEG\_ENZ}$	Time between the falling edge of SCPENZ and the first rising edge of SCPCLK	2			µs
$t_{SCP\_POS\_ENZ}$	Time between the falling edge of SCPCLK and the rising edge of SCPENZ	2			µs
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling edge)(9)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling edge)(9)	900			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	2			µs
LVDS Interface					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(11)			400	MHz
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(12)	150	300	440	mV
V_{CM}	Common mode voltage(12)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(12)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions . No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
Environmental					
T_{ARRAY}	Array temperature, long-term operational(14) (15) (16) (17)	10		40 to 70(16)	°C
	Array temperature, short-term operational(15) (18)	0		10	°C
T_{WINDOW}	Window temperature—operational			85	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(19) (20)			14	°C
$T_{DP\text{-}AVG}$	Average dew point average temperature (non-condensing)(21)			28	°C
$T_{DP\text{-}MAX}$	Elevated dew point temperature range (non-condensing)(22)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	–14.5	–14	–13.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(3)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value)(4)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage(5)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(5)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(5)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(5)	–0.3		0.2 × V_{CC}	V
t_{PWRDNZ}	PWRDNZ pulse duration(6)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(7)			500	kHz
t_{SCP_PD}	Propagation delay, clock to Q, from rising-edge of SCPCLK to valid SCPDO(8)	0		900	ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			µs
$t_{SCP\_POS\_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t_{SCP_DS}	SCPDI clock setup time (before SCPCLK falling edge)(8)	800			ns
t_{SCP_DH}	SCPDI hold time (after SCPCLK falling edge)(8)	900			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse duration (high level)	2			µs
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(9)			400	MHz
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)(10)	150	300	440	mV
V_{CM}	Common mode voltage(10)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(10)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(11) (12) (13) (23)	10		40 to 70(23)	°C
	Array temperature, short-term operational(12) (15)	0		10	°C
T_{WINDOW}	Window temperature – operational(16) (17)			85	°C
$\lvert T_{DELTA} \rvert$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(18) (19)			14	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(20)			28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(21)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	months
		MIN	NOM	MAX	UNIT
VOLTAGE SUPPLY					
V_{CC}	LVCMOS logic supply voltage(1)	1.65	1.8	1.95	V
V_{OFFSET}	Mirror electrode and HVCMOS voltage(1) (2)	9.5	10	10.5	V

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions . No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
V_{BIAS}	Mirror electrode voltage(1)	17.5	18	18.5	V
V_{RESET}	Mirror electrode voltage(1)	–14.5	–14	–13.5	V
$\lvert V_{BIAS} - V_{OFFSET} \rvert$	Supply voltage difference (absolute value)(3)			10.5	V
$\lvert V_{BIAS} - V_{RESET} \rvert$	Supply voltage difference (absolute value)(4)			33	V
LVCMOS INTERFACE					
$V_{IH(DC)}$	DC input high voltage(5)	0.7 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(DC)}$	DC input low voltage(5)	–0.3		0.3 × V_{CC}	V
$V_{IH(AC)}$	AC input high voltage(5)	0.8 × V_{CC}		V_{CC} + 0.3	V
$V_{IL(AC)}$	AC input low voltage(5)	–0.3		0.2 × V_{CC}	V

6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by recommended operating conditions . No level of performance is implied when operating the device above or below the limits.

		MIN	NOM	MAX	UNIT
t_{PWRDNZ}	PWRDNZ pulse duration(6)	10			ns
SCP INTERFACE					
f_{SCPCLK}	SCP clock frequency(7)			500	kHz
t_{SCP_PD}	Propagation delay, Clock to Q, from rising-edge of SCPCLK to valid SCPDO(8)	0		900	ns
$t_{SCP\_NEG\_ENZ}$	Time between falling-edge of SCPENZ and the first rising-edge of SCPCLK	1			µs
$t_{SCP\_POS\_ENZ}$	Time between falling-edge of SCPCLK and the rising-edge of SCPENZ	1			µs
t_{SCP_DS}	SCPDI Clock setup time (before SCPCLK falling edge)(8)	800			ns
t_{SCP_DH}	SCPDI Hold time (after SCPCLK falling edge)(8)	900			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse duration (high level)	2			µs
LVDS INTERFACE					
f_{CLOCK}	Clock frequency for LVDS interface (all channels), DCLK(10)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)(11)	150	300	440	mV
V_{CM}	Common mode voltage(11)	1100	1200	1300	mV
V_{LVDS}	LVDS voltage(11)	880		1520	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			2000	ns
Z_{IN}	Internal differential termination resistance	80	100	120	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL					
T_{ARRAY}	Array temperature, long-term operational(13) (14) (16)	10		40 to 70(15)	°C
	Array temperature, short-term operational(14) (17)	0		10	°C
T_{WINDOW}	Window temperature – operational(21) (23)			85	°C
$\|T_{DELTA}\|$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1(18) (19)			14	°C
$T_{DP\text{-}AVG}$	Average dew point temperature (non-condensing)(20)			28	°C
$T_{DP\text{-}ELR}$	Elevated dew point temperature range (non-condensing)(22)	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILLUMINATION (Lamp)					
L	Operating system luminance(19)			7000	lm
ILL_{UV}	Illumination wavelengths < 395 nm(13)		0.68	2.00	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 395 nm and 800 nm		Thermally limited		mW/cm^2
ILL_{IR}	Illumination wavelengths > 800 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(23)			55	deg
ILLUMINATION (Solid State)					
L	Operating system luminance(19)			1000	lm
ILL_{UV}	Illumination wavelengths < 436 nm(13)			0.45	mW/cm^2
ILL_{VIS}	Illumination wavelengths between 436 nm and 800 nm		Thermally Limited		mW/cm^2
ILL_{IR}	Illumination wavelengths > 800 nm			10	mW/cm^2
ILL_{θ}	Illumination marginal ray angle(23)			55	deg

(1) All voltages are referenced to common ground VSS. VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies are all required for proper DMD operation. VSS must also be connected.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit. See 节 9, 图 9-1, and 表 9-1.
(4) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit. See 节 9, 图 9-1, and 表 9-1.
(5) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit. See 节 9, 图 9-1, and 表 9-1.
(6) Low-speed interface is LPSDR and adheres to the Electrical Characteristics and AC/DC Operating Conditions table in JEDEC Standard No. 209B, “Low-Power Double Data Rate (LPDDR)” JESD209B.Tester Conditions for VIH and VIL.
- Frequency = 60 MHz. Maximum Rise Time = 2.5 ns @ (20% – 80%)
- Frequency = 60 MHz. Maximum Fall Time = 2.5 ns @ (80% – 20%)

(7) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tristates the SCPDO output pin.
(8) The SCP clock is a gated clock. Duty cycle must be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(9) See 图 6-2.
(10) CP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.
(11) See LVDS Timing Requirements in 节 6.8 and 图 6-6.
(12) See 图 6-5 LVDS Waveform Requirements.
(13) Supported for video applications only
(14) Simultaneous exposure of the DMD to the maximum 节 6.4 for temperature and UV illumination will reduce device lifetime.
(15) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in 图 7-2 and the package thermal resistance 节 7.6.
(16) Per 图 6-1, the maximum operational array temperature will be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See 节 7.7 for a definition of micromirror landed duty cycle.
(17) Long-term is defined as the usable life of the device.
(18) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(19) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in 图 7-2. The window test points TP2, TP3, TP4, and TP5 shown in 图 7-2 are intended to result in the worst case delta temperature. If a particular application causes another point on the window edge to result in a larger delta temperature, that point is used.
(20) DMD is qualified at the combination of the maximum temperature and maximum lumens specified. Operation of the DMD outside of these limits has not been tested.
(21) The average over time (including storage and operating) that the device is not in the elevated dew point temperature range.
(22) Exposure to dew point temperatures in the elevated range during storage and operation will be limited to less than a total cumulative time of CT_{ELR}.
(23) The maximum marginal ray angle of the incoming illumination light at any point in the micromirror array, including Pond of Micromirrors (POM), cannot exceed 55 degrees from the normal to the device array plane. The device window aperture has not necessarily been designed to allow incoming light at higher maximum angles to pass to the micromirrors, and the device performance has not been tested nor qualified at angles exceeding this. Illumination light exceeding this angle outside the micromirror array (including POM) will contribute to thermal limitations described in this document, and may negatively affect lifetime.

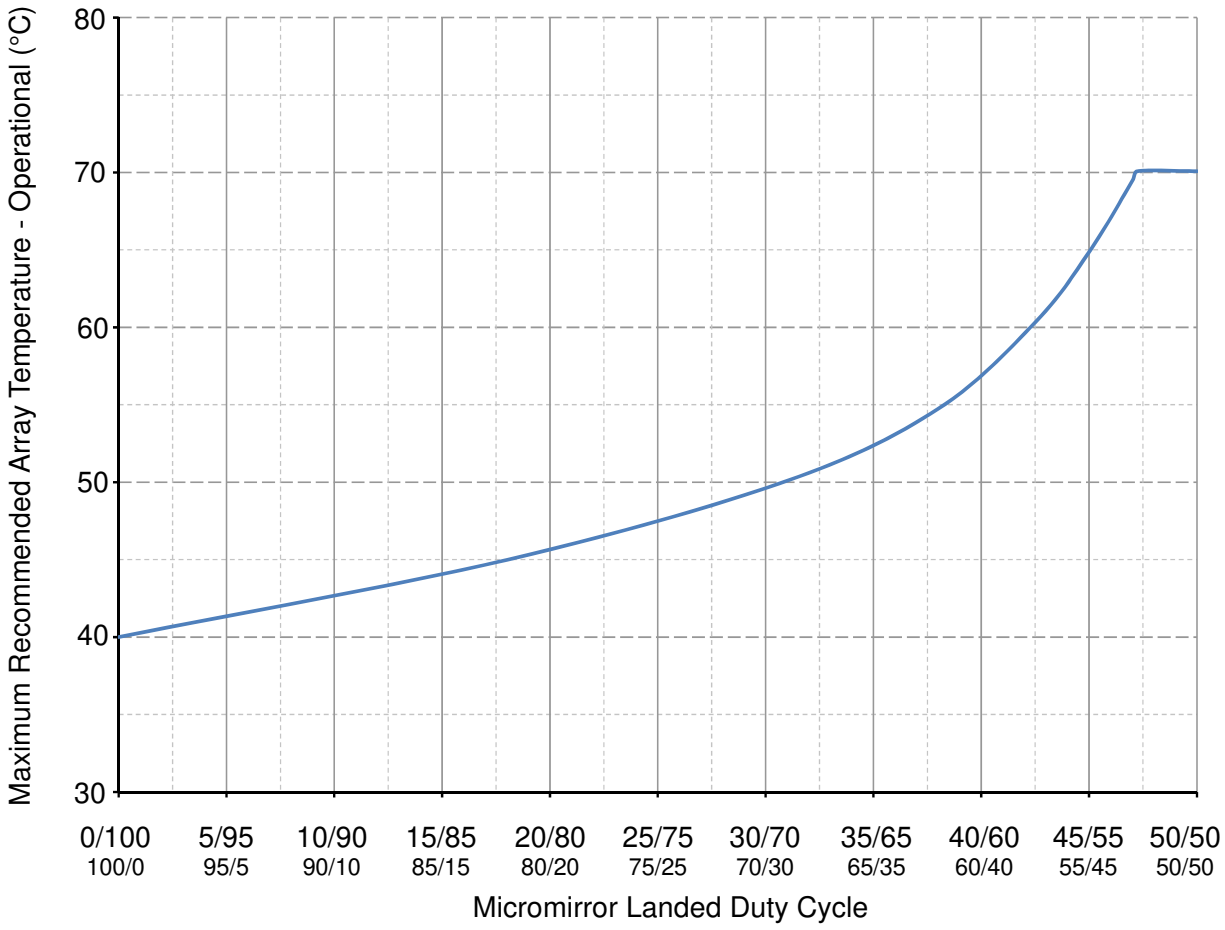


图 6-1. Max Recommended Array Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP660TE FYG Package 350 PINS	UNIT
Thermal resistance, active area to test point 1 (TP1)(1)	0.60	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the 节 6.4. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems need to be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High level output voltage	V_{CC} = 1.8 V, I_{OH} = – 2 mA	0.8 x V_{CC}			V
V_{OL}	Low level output voltage	V_{CC} = 1.95 V, I_{OL} = 2 mA			0.2 x V_{CC}	V
I_{OZ}	High impedance output current	V_{CC} = 1.95 V	-40		25	µA
I_{IL}	Low level input current	V_{CC} = 1.95 V, VI = 0	-1			µA
I_{IH}	High level input current (1)	V_{CC} = 1.95 V, VI = V_{CC}			110	µA
I_{CC}	Supply current VCC	V_{CC} = 1.95 V			1200	mA
I_{CCI}	Supply current VCCI	V_{CCI} = 1.95 V			330	mA
I_{OFFSET}	Supply current VOFFSET (2)	V_{OFFSET} = 10.5 V			13.2	mA
I_{BIAS}	Supply current VBIAS (2) (3)	V_{BIAS} = 18.5 V			-3.641	mA
I_{RESET}	Supply current VRESET (3)	V_{RESET} = – 14.5 V			9.02	mA
	Supply power dissipation Total				3320.25	mW

(1) Applies to LVCMOS pins only. Excludes LVDS pins and test pad pins.
(2) To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than the specified limit in 节 6.4.
(3) To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in 节 6.4.

6.7 Capacitance at Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{I_lvds}	LVDS Input Capacitance 2xLVDS	f = 1 MHz			20	pF
$C_{I\_nonlvds}$	Non-LVDS Input capacitance 2xLVDS	f = 1 MHz			20	pF
C_{I_tdiode}	Temp Diode Input capacitance 2xLVDS	f= 1 MHz			30	pF
C_O	Output Capacitance	f = 1 MHz			20	pF

6.8 Timing Requirements

			MIN	NOM	MAX	UNIT
SCP(1)						
t_r	Rise time	20% to 80% reference points			30	ns
t_f	Fall time	80% to 20% reference points			30	ns
LVDS(2)						
t_r	Rise slew rate	20% to 80% reference points	0.7	1		V/ns
t_f	Fall slew rate	80% to 20% reference points	0.7	1		V/ns
t_C	Clock Cycle	DCLK_A, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_B, LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_C,LVDS pair	2.5			ns
t_C	Clock Cycle	DCLK_D, LVDS pair	2.5			ns
t_W	Pulse Width	DCLK_A LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_B LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_C LVDS pair	1.19	1.25		ns
t_W	Pulse Width	DCLK_D LVDS pair	1.19	1.25		ns
t_{Su}	Setup Time	D_A(15:0) before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_B(15:0) before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_C(15:0) before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	D_D(15:0) before DCLK_D, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_A before DCLK_A, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_B before DCLK_B, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_C before DCLK_C, LVDS pair	0.325			ns
t_{Su}	Setup Time	SCTRL_D before DCLK_D, LVDS pair	0.325			ns
t_h	Hold Time	D_A(15:0) after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	D_B(15:0) after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	D_C(15:0) after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	D_D(15:0) after DCLK_D, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_A after DCLK_A, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_B after DCLK_B, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_C after DCLK_C, LVDS pair	0.145			ns
t_h	Hold Time	SCTRL_D after DCLK_D, LVDS pair	0.145			ns
LVDS(2)						
t_{SKEW}	Skew Time	Channel B relative to Channel A(3) (4), LVDS pair	– 1.25		+1.25	ns
t_{SKEW}	Skew Time	Channel D relative to Channel C(5) (6), LVDS pair	– 1.25		+1.25	ns

(1) See 图 6-3 for Rise Time and Fall Time for SCP.
(2) See 图 6-5 for Timing Requirements for LVDS.
(3) Channel A (Bus A) includes the following LVDS pairs: DCLK_AN and DCLK_AP, SCTRL_AN and SCTRL_AP, D_AN(15:0) and D_AP(15:0).
(4) Channel B (Bus B) includes the following LVDS pairs: DCLK_BN and DCLK_BP, SCTRL_BN and SCTRL_BP, D_BN(15:0) and D_BP(15:0).
(5) Channel C (Bus C) includes the following LVDS pairs: DCLK_CN and DCLK_CP, SCTRL_CN and SCTRL_CP, D_CN(15:0) and D_CP(15:0).
(6) Channel D (Bus D) includes the following LVDS pairs: DCLK_DN and DCLK_DP, SCTRL_DN and SCTRL_DP, D_DN(15:0) and D_DP(15:0).

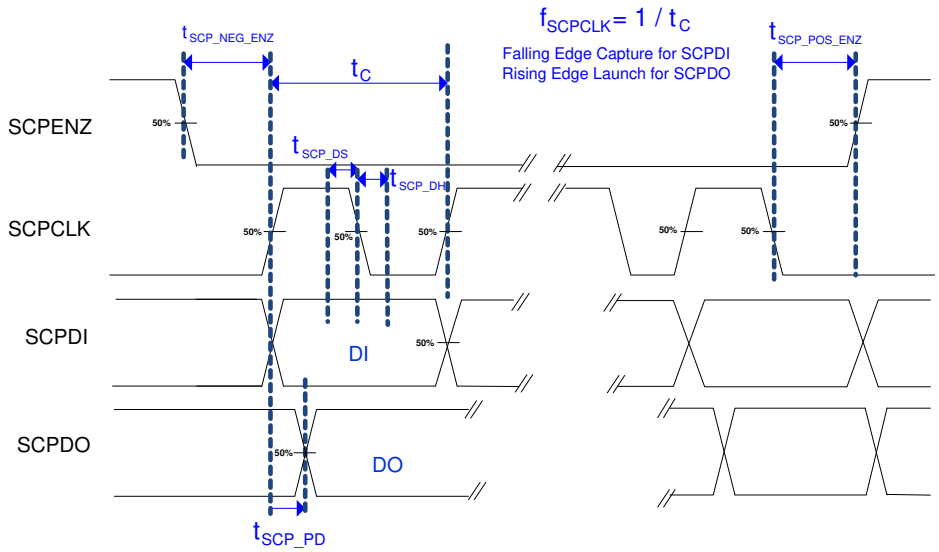


图 6-2. SCP Timing Requirements

See 节 6.4 for f_{SCPCLK}, t_{SCP_DS}, t_{SCP_DH} , and t_{SCP_PD} specifications.

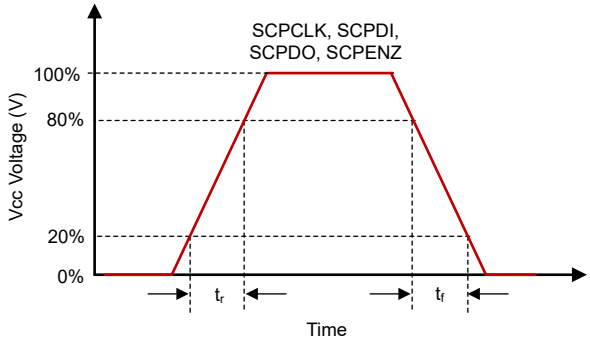


图 6-3. SCP Requirements for Rise and Fall

See 节 6.8 for t_r and t_f specifications and conditions.

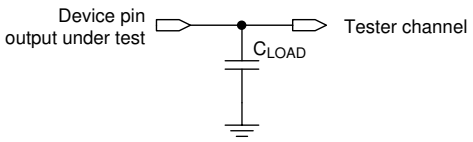


图 6-4. Test Load Circuit for Output Propagation Measurement

For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment.

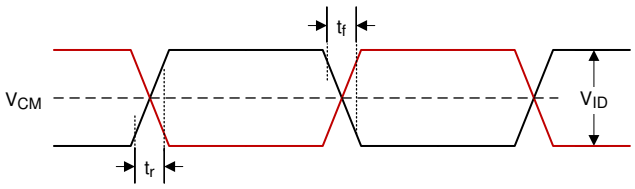


图 6-5. LVDS Waveform Requirements

A. See 方程式 1 and 方程式 2.

$$V_{LVDS\,(max)} = V_{CM\,(max)} + \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (1)$$

$$V_{LVDS\,(min)} = V_{CM\,(min)} - \left|\frac{1}{2} \times V_{ID\,(max)}\right| \quad (2)$$

See 节 6.4 for V_{CM}, V_{ID}, and V_{LVDS} specifications and conditions.

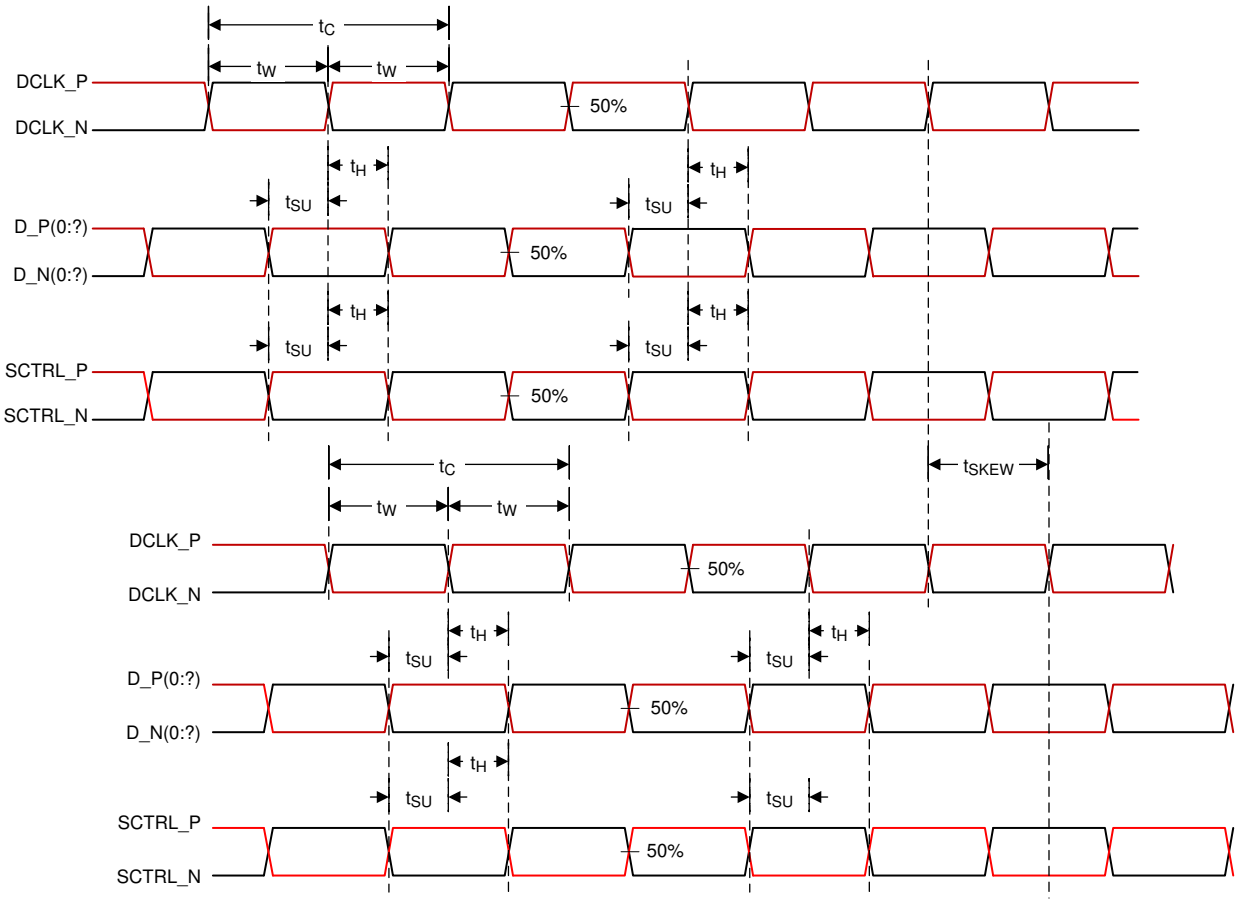


图 6-6. Timing Requirements

See 节 6.8 for timing requirements and LVDS pairs per channel (bus) defining D_P(0:?) and D_N(0:?).

6.9 System Mounting Interface Loads

表 6-1. System Mounting Interface Loads

PARAMETER		MIN	NOM	MAX	UNIT
Thermal interface area	Condition 1: Maximum load of 22.6 kg evenly distributed within each area below: (1)			11.3	kg
Electrical interface area				11.3	kg
Thermal interface area	Condition 2: Maximum load of 22.6 kg evenly distributed within each area below: (1)			0	kg
Electrical interface area				22.6	kg

(1) See 图 6-7.

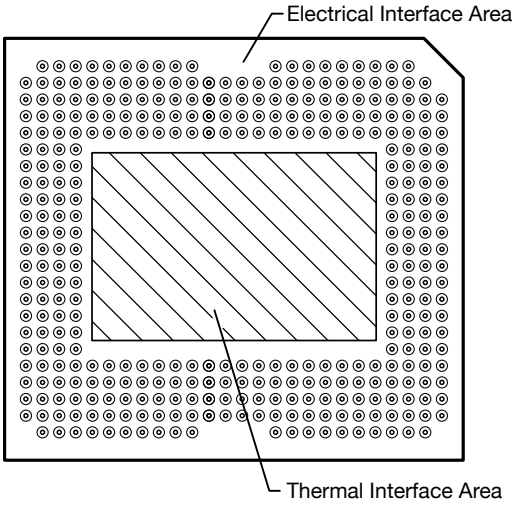


图 6-7. System Mounting Interface Loads

6.10 Micromirror Array Physical Characteristics

表 6-2. Micromirror Array Physical Characteristics

PARAMETER DESCRIPTION		VALUE	UNIT
Number of active columns (1)	M	2716	micromirrors
Number of active rows (1)	N	1528	micromirrors
Micromirror (pixel) pitch (1)	P	5.4	µm
Micromirror active array width (1)	Micromirror Pitch × number of active columns	14.67	mm
Micromirror active array height (1)	Micromirror Pitch × number of active rows	8.25	mm
Micromirror active border (Top / Bottom) (2)	Pond of micromirrors (POM)	56	micromirrors / side
Micromirror active border (Right / Left) (2)	Pond of micromirrors (POM)	20	micromirrors / side

(1) See 图 6-8.
(2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the “Pond Of Mirrors” (POM). These micromirrors are prevented from tilting toward the bright or “on” state but still require an electrical bias to tilt toward “off.”

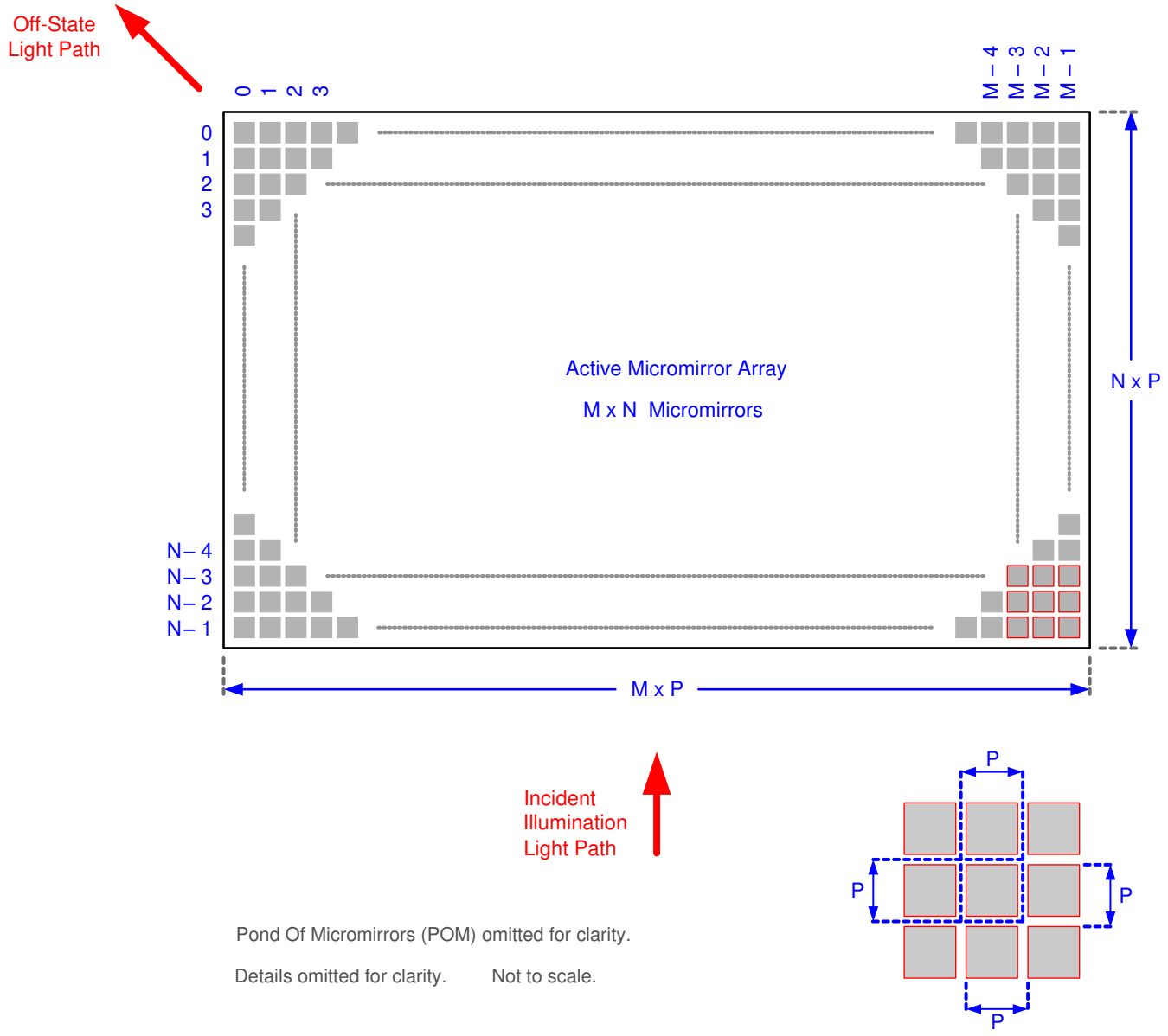


图 6-8. Micromirror Array Physical Characteristics

Refer to section *节 6.10* table for M, N, and P specifications.

6.11 Micromirror Array Optical Characteristics

表 6-3. Micromirror Array Optical Characteristics

PARAMETER		MIN	NOM	MAX	UNIT
Mirror Tilt angle, variation device to device (1) (2)		15.6	17.0	18.4	degrees
Number of out-of-specification micromirrors (3)	Adjacent micromirrors			0	micromirrors
	Non-Adjacent micromirrors			10	
DMD Efficiency (420 nm – 680 nm)			68		%

(1) Limits on variability of micromirror tilt angle are critical in the design of the accompanying optical system. Variations in tilt angle within a device may result in apparent nonuniformities, such as line pairing and image mottling, across the projected image. Variations in the average tilt angle between devices may result in colorimetric and system contrast variations.
(2) See 图 6-9.
(3) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.

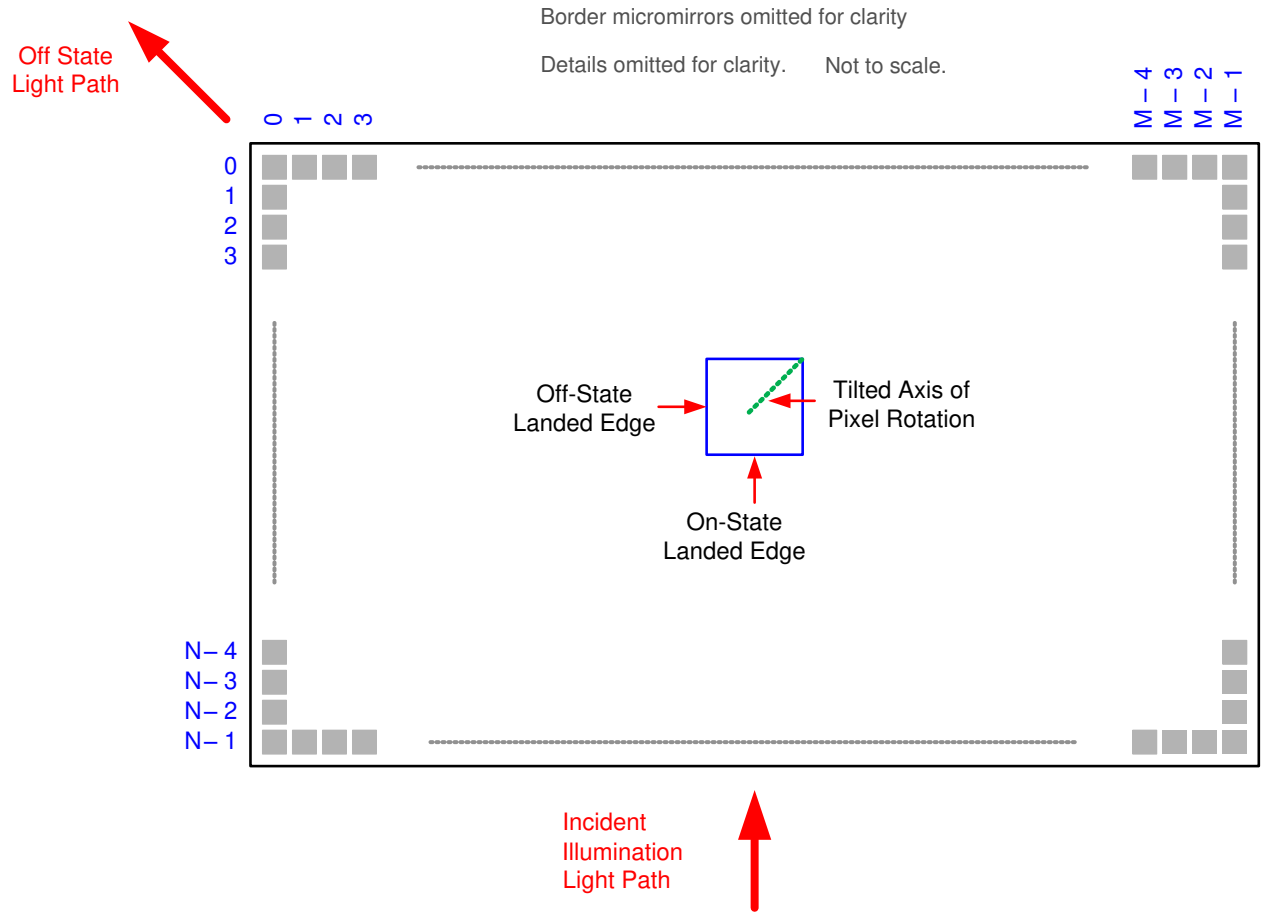


图 6-9. Micromirror Landed Orientation and Tilt

Refer to section 节 6.10 table for M, N, and P specifications.

6.12 Window Characteristics

表 6-4. DMD Window Characteristics

PARAMETER	MIN	NOM	MAX	UNIT
Window Material Designation S610		Corning Eagle XG		
Window Refractive Index at 546.1 nm		1.5119		
Window Transmittance, minimum within the wavelength range 420 – 680 nm. Applies to all angles 0 – 30° AOI. (1) (2)	97%			
Window Transmittance, average over the wavelength range 420 – 680 nm. Applies to all angles 30 – 45° AOI. (1) (2)	97%			

(1) Single-pass through both surfaces and glass.
(2) AOI – angle of incidence is the angle between an incident ray and the normal to a reflecting or refracting surface.

6.13 Chipset Component Usage Specification

Reliable function and operation of the DLP660TE DMD requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

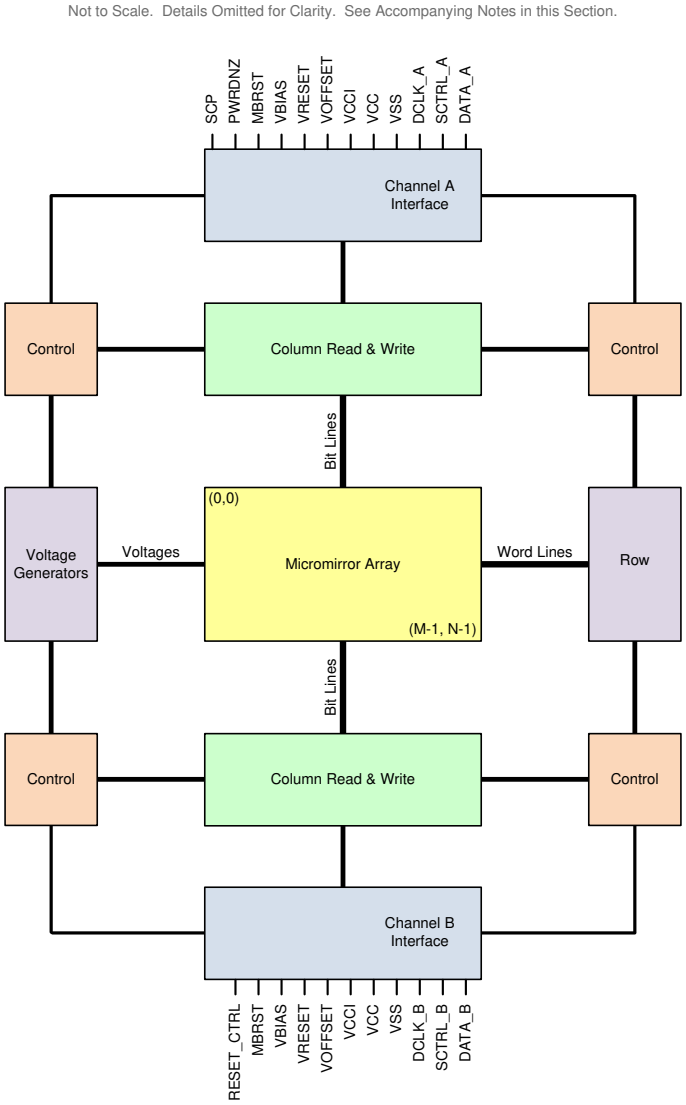
7 Detailed Description

7.1 Overview

The DMD is a 0.66-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS). The DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of M memory cell columns by N memory cell rows. Refer to the 节 7.2. The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

The DLP660TE DMD is part of the chipset comprising of the DLP660TE DMD, the DLPC4420 display controller and the DLPA100 power and motor driver. To ensure reliable operation, the DLP660TE DMD must always be used with the DLPC4420 display controller and the DLPA100 power and motor driver.

7.2 Functional Block Diagram



For pin details on Channels A, B, C, and D, refer to *Pin Configurations and Functions* 节 5 and LVDS Interface section of 节 6.8. RESET_CTRL is utilized in applications when an external reset signal is required.

图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Power Interface

The DMD requires 5 DC voltages: DMD_P3P3V, DMD_P1P8V, VOFFSET, VRESET, and VBIAS. DMD_P3P3V is created by the DLPA100 power and motor driver and is used on the DMD board to create the other 4 DMD voltages, as well as powering various peripherals (TMP411, I2C, and TI level translators). DMD_P1P8V is created by the TI PMIC LP38513S and provides the VCC voltage required by the DMD. VOFFSET (10V), VRESET (-14V), and VBIAS(18V) are made by the TI PMIC TPS65145 and are supplied to the DMD to control the micromirrors.

7.3.2 Timing

The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. 图 6-4 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. System designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4420 display controller. See the DLPC4420 display controller data sheet or contact a TI applications engineer.

7.5 Optical Interface and System Image Quality Considerations

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

7.5.1.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area are the same. This angle cannot exceed the nominal device micromirror tilt angle unless appropriate apertures are added in the illumination or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the micromirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display’s border and active area can occur.

7.5.1.2 Pupil Match

TI’s optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display’s border and active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.1.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view, and is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design he illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system’s optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

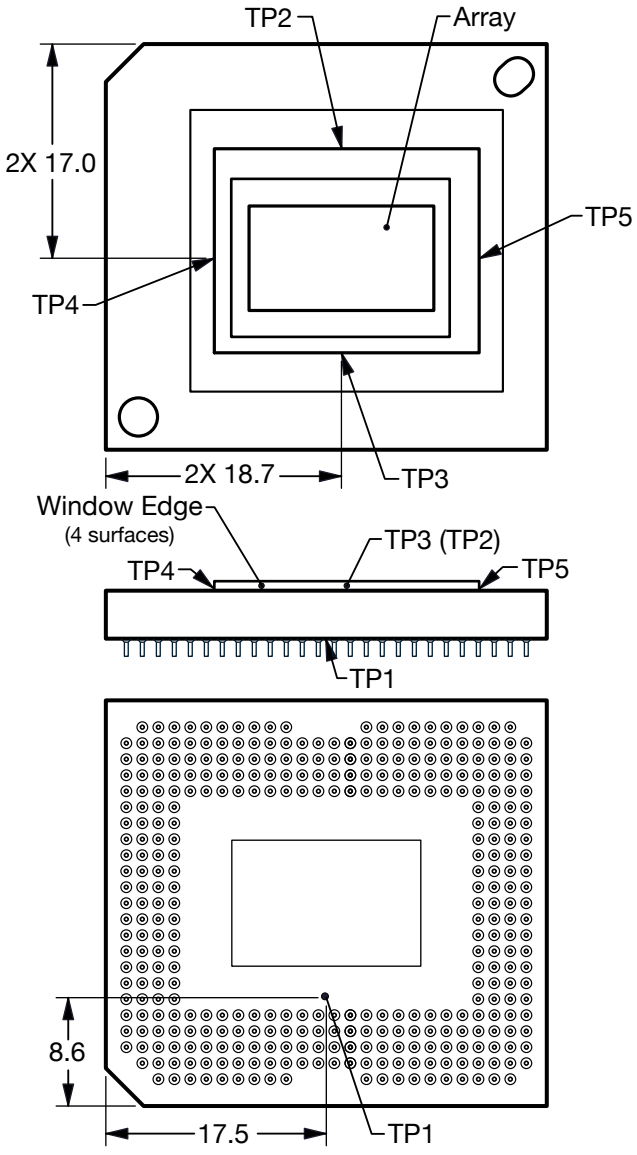


图 7-2. DMD Thermal Test Points

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{-}TO\text{-}CERAMIC})$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION}$$

where

- T_{ARRAY} = computed array temperature (°C)
- $T_{CERAMIC}$ = measured ceramic temperature (°C) (TP1 location)
- $R_{ARRAY\text{-}TO\text{-}CERAMIC}$ = thermal resistance of package from array to ceramic TP1 (°C/Watt)
- Q_{ARRAY} = Total DMD power on the array (Watts) (electrical + absorbed)
- $Q_{ELECTRICAL}$ = nominal electrical power
- $Q_{ILLUMINATION} = (C_{L2W} \times SL)$
- C_{L2W} = Conversion constant for screen lumens to power on DMD (Watts/Lumen)
- SL = measured screen lumens

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. A nominal electrical power dissipation to use when calculating array temperature is 3.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-Chip DMD system with projection efficiency from the DMD to the screen of 87%.

The conversion constant C_{L2W} is based on array characteristics. It assumes a spectral efficiency of 300 lumens/Watt for the projected light and illumination distribution of 83.7% on the active array, and 16.3% on the array border.

Sample calculations for typical projection application:

$$Q_{ELECTRICAL} = 3.0 \text{ W}$$

$$C_{L2W} = 0.00266$$

$$SL = 5000 \text{ lm}$$

$$T_{CERAMIC} = 55.0°C$$

$$Q_{ARRAY} = 3.0 \text{ W} + (0.00266 \times 5000 \text{ lm}) = 16.3 \text{ W}$$

$$T_{ARRAY} = 55.0°C + (16.3 \text{ W} \times 0.60°C/W) = 64.78°C$$

7.7 Micromirror Landed-On/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On state versus the amount of time the same micromirror is landed in the Off state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On state 100% of the time (and in the Off state 0% of the time); whereas 0/100 indicates that the pixel is in the Off state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry or asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD's usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD's usable life. This is quantified in the de-rating curve shown in 图 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD ideally will be operated at for a given long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in 表 7-1.

表 7-1. Grayscale Value and Landed Duty Cycle

Grayscale Value	Landed Duty Cycle
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_% represents the percentage of the frame time that Red displays to achieve the desired white point.
- Green_Cycle_% represents the percentage of the frame time that Green displays to achieve the desired white point.
- Blue_Cycle_% represents the percentage of the frame time that Blue displays to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities will be as shown in 表 7-2 and 表 7-3.

表 7-2. Example Landed Duty Cycle for Full-Color, Color Percentage

Red Cycle Percentage	Green Cycle Percentage	Blue Cycle Percentage
50%	20%	30%

表 7-3. Example Landed Duty Cycle for Full-Color

Red Scale Value	Green Scale Value	Blue Scale Value	Landed Duty Cycle
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). DMDs vary in resolution and size and can contain over 8-million micromirrors. Each micromirror of a DMD can represent either one or more pixels on the display and is independently controlled, synchronized with color sequential illumination, to create stunning images on any surface. DLP technology enables a wide variety of display products worldwide, from tiny projection modules embedded in smartphones to high powered digital cinema projectors, and emerging display products such as digital signage and laser TV.

The most recent class of chipsets from Texas Instruments is based on a breakthrough micromirror technology, called TRP. With a smaller pixel pitch of 5.4 µm and increased tilt angle of 17 degrees, TRP chipsets enable higher resolution in a smaller form factor and enhanced image processing features while maintaining high optical efficiency. DLP chipsets are a great fit for any system that requires high resolution and high brightness displays.

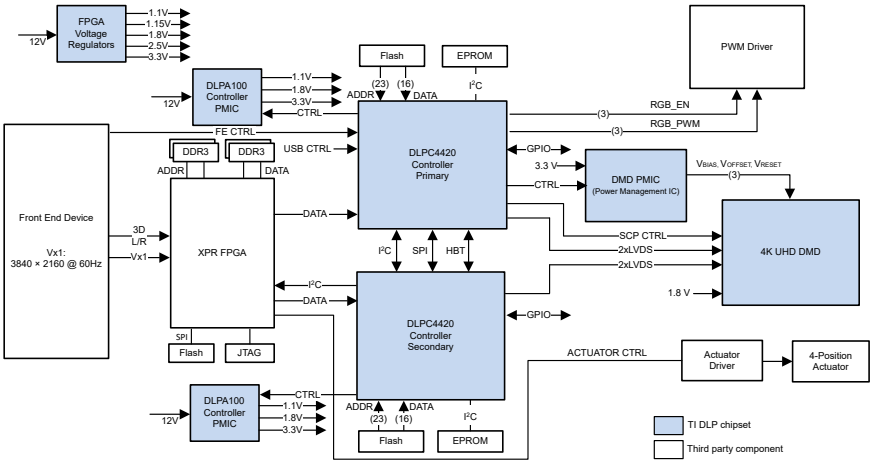
The following orderables have been replaced by the DLP660TE.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)	MECHANICAL ICD
2715-7132P	FYG (350)	35 mm × 32 mm	2514366
2715-7137P	FYG (350)	35 mm × 32 mm	2514366
2715-7139P	FYG (350)	35 mm × 32 mm	2514366
2715-713AP	FYG (350)	35 mm × 32 mm	2514366

8.2 Typical Application

The DLP660TE DMD is the first full 4K UHD DLP digital micromirror device. When combined with two display controllers (DLPC4420), an FPGA, a power management device (DLPA100), and other electrical, optical and mechanical components the chipset enables bright, affordable, full 4K UHD display solutions. 图 8-1 shows a typical 4K UHD system application using the DLP660TE DMD.



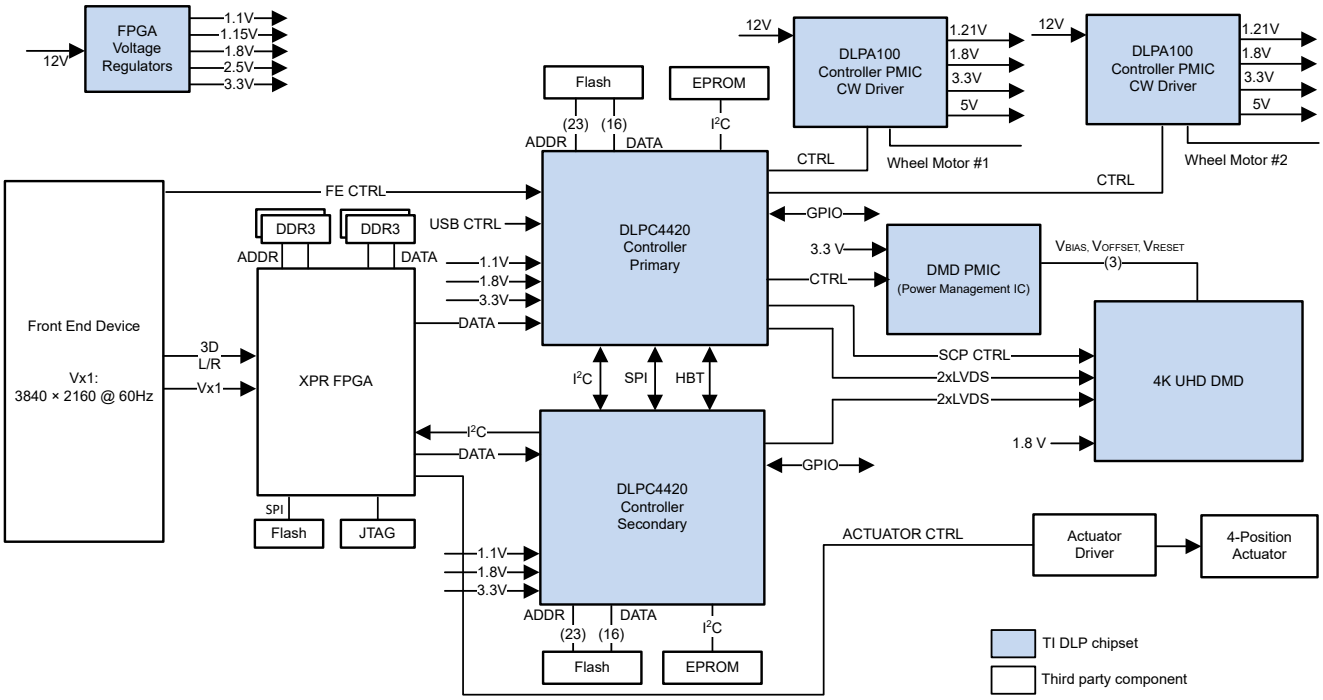


图 8-1. Typical DLPC4420 4K UHD Application (LED, Top; LPCW, Bottom)

8.2.1 Design Requirements

At the high level, DLP660TE DMD systems will include an illumination source, a light engine, electronic components, and software. The designer must first choose an illumination source and design the optical engine taking into consideration the relationship between the optics and the illumination source. The designer must then understand the electronic components of a DLP660TE DMD system, which is made up of a DMD board and formatter board. The DMD board channels image data to and powers the DMD chip. The formatter board supports the rest of the electronic components, which can include an FPGA, the DLPC4420 display controller, power supplies, and drivers for illumination sources, color wheels, fans, and dynamic optical components.

8.2.2 Detailed Design Procedure

For connecting together the DLPC4420 display controller and the DLP660TE DMD, see the reference design schematic. Layout guidelines need be followed to achieve a reliable projector. To complete the DLP system an optical module or light engine is required that contains the DLP660TE DMD, associated illumination sources, optical elements, and necessary mechanical components.

8.2.3 Application Curves

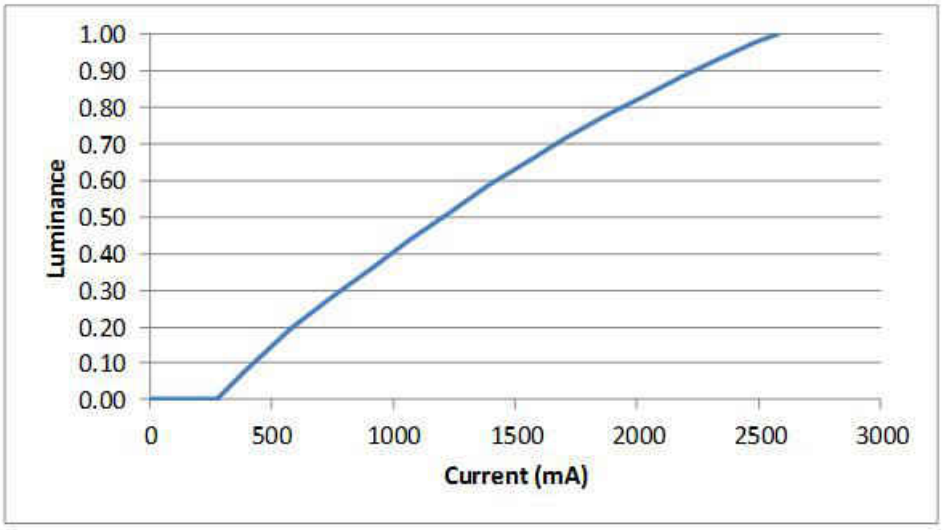
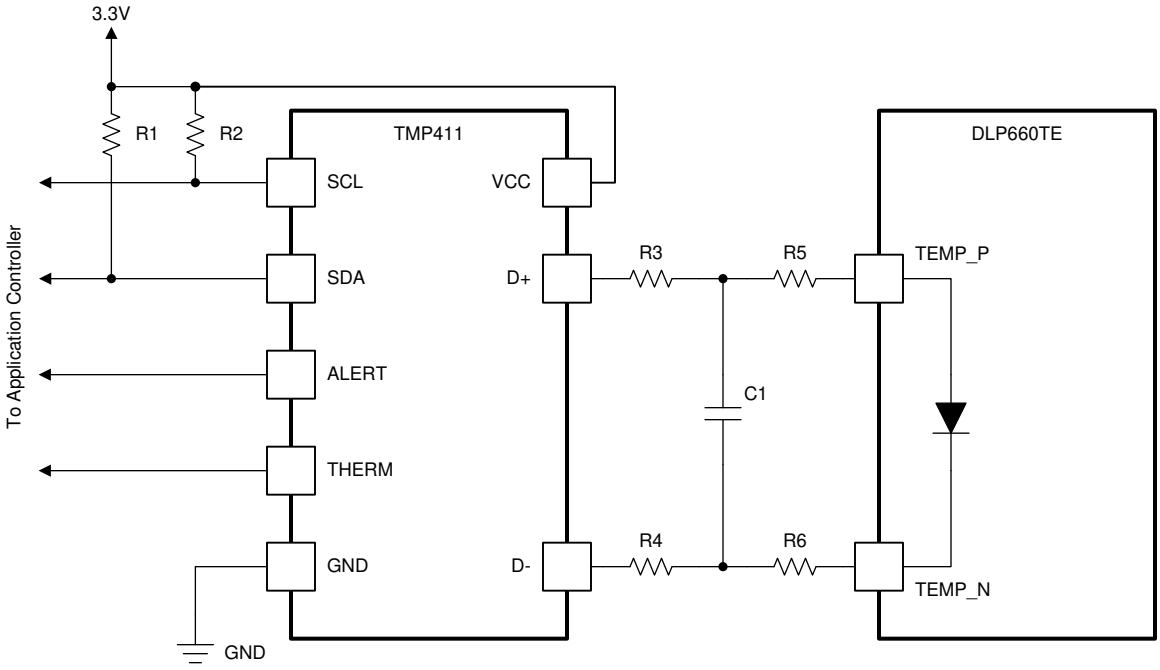


图 8-2. Luminance vs. Current

8.3 DMD Die Temperature Sensing

The DMD features a built-in thermal diode that measures the temperature at one corner of the die outside the micromirror array. The thermal diode can be interfaced with the TMP411 temperature sensor as shown in 图 8-3. The serial bus from the TMP411 can be connected to the DLPC4420 display controller to enable its temperature sensing features. See the DLPC4420 Programmers' Guide for instructions on installing the DLPC4420 controller support firmware bundle and obtaining the temperature readings.

The software application contains functions to configure the TMP411 to read the DMD temperature sensor diode. This data can be leveraged to incorporate additional functionality in the overall system design such as adjusting illumination, fan speeds, and so forth. All communication between the TMP411 and the DLPC4420 controller will be completed using the I^2C interface. The TMP411 connects to the DMD via pins E16 and E17 as outlined in 节 5.



A. Details omitted for clarity, see the TI Reference Design for connections to the DLPC4420 controller.
B. See the TMP411 data sheet for system board layout recommendation.
C. See the TMP411 data sheet and the TI reference design for suggested component values for R1, R2, R3, R4, and C1.
D. R5 = 0 Ω. R6 = 0 Ω. Zero ohm resistors need to be located close to the DMD package pins.

图 8-3. TMP411 Sample Schematic

9 Power Supply Recommendations

The following power supplies are all required to operate the DMD:

- VSS
- VCC
- VCCI
- VBIAS
- VOFFSET
- VRESET

DMD power-up and power-down sequencing is strictly controlled by the DLP display controller.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to any of the prescribed power-up and power-down requirements may affect device reliability. See 图 9-1 DMD Power Supply Sequencing Requirements.

VBIAS, VCC, VCCI, VOFFSET, and VRESET power supplies must be coordinated during power-up and power-down operations. Failure to meet any of the below requirements will result in a significant reduction in the DMD’s reliability and lifetime. Common ground VSS must also be connected.

9.1 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET plus Delay1 specified in 表 9-1, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in 节 *6.4*.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in 节 *6.1*, in 节 *6.4*, and in 图 9-1.
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in 节 *6.4*.

9.2 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. See 表 9-1.
- During power-down, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in 节 *6.4*.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in 节 *6.1*, in 节 *6.4*, and in 图 9-1.
- During power-down, LVCMOS input pins must be less than specified in 节 *6.4*.

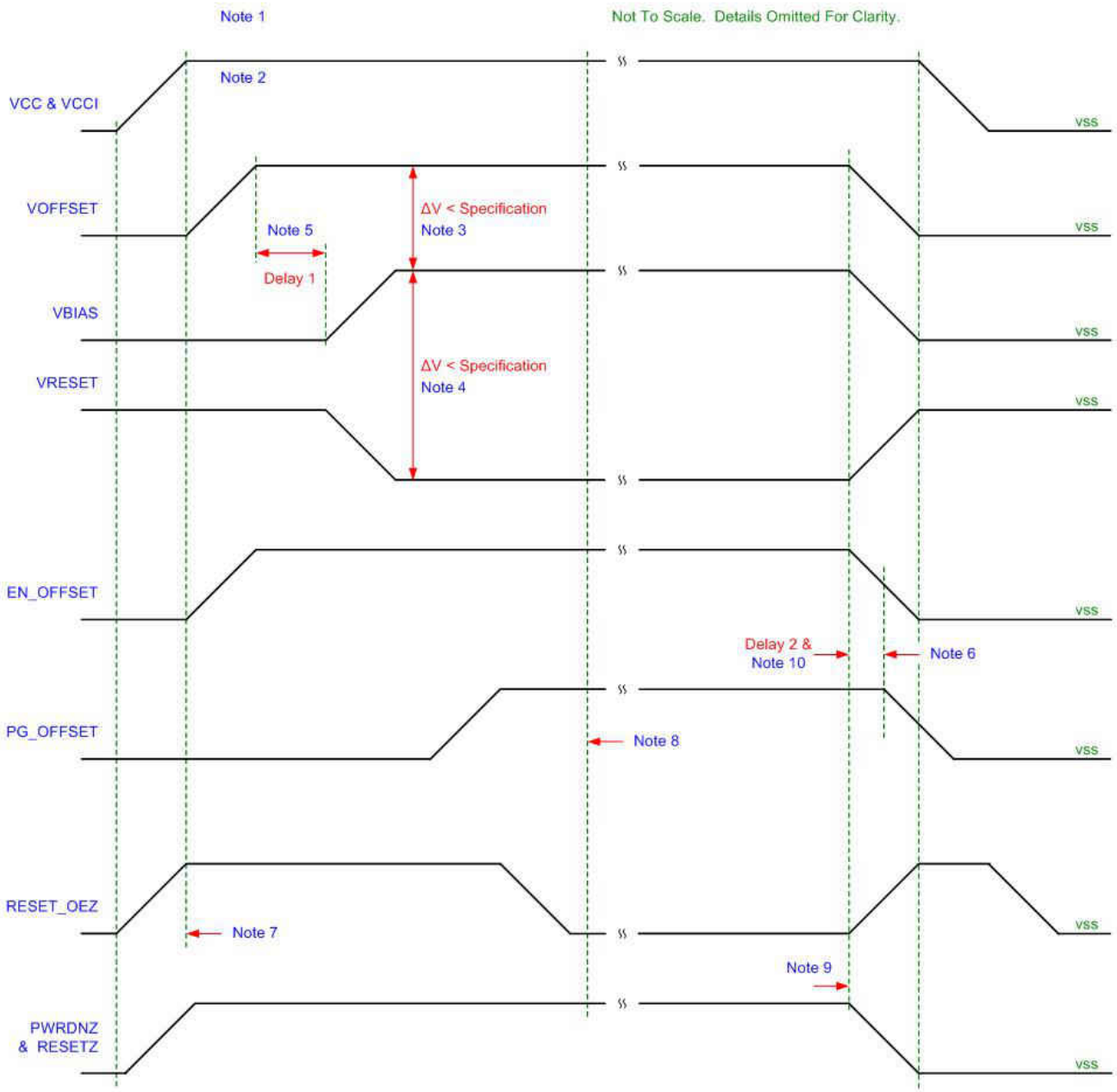


图 9-1. DMD Power Supply Requirements

1. See 节 6.4, 节 5
2. To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit in 节 6.4.
3. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified in 节 6.4.
4. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in 节 6.4.
5. VBIAS must power up after VOFFSET has powered up, per the Delay1 specification in 表 9-1.
6. PG_OFFSET must turn off after EN_OFFSET has turned off, per the Delay2 specification in 表 9-1.
7. DLP controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
8. DLP controller software initiates the global VBIAS command.

9. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET.
10. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal may go high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

表 9-1. DMD Power-Supply Requirements

Parameter	Description	Min	NOM	Max	Unit
Delay1	Delay from VOFFSET settled at recommended operating voltage to VBIAS and VRESET power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ns

10 Layout

10.1 Layout Guidelines

The DLP660TE DMD is part of a chipset that is controlled by the DLPC4420 display controller in conjunction with the DLPA100 power and motor driver. These guidelines help to design a PCB board with the DLP660TE DMD. The DLP660TE DMD board is a high-speed multilayer PCB, with primarily high-speed digital logic using dual-edge clock rates up to 400 MHz for DMD LVDS signals. The remaining traces are comprised of low speed digital LVTTL signals. TI recommends that mini power planes are used for VOFFSET, VRESET, and VBIAS. Solid planes are required for DMD_P3P3V(3.3 V), DMD_P1P8V, and Ground. The target impedance for the PCB is 50 Ω ±10% with the LVDS traces being 100-Ω ±10% differential. TI recommends using an 8-layer stack-up as described in 表 10-1.

10.2 Layout Example

10.2.1 Layers

The layer stack-up and copper weight for each layer is shown in 表 10-1. Small sub-planes are allowed on signal routing layers to connect components to major sub-planes on top or bottom layers if necessary.

表 10-1. Layer Stack-Up

LAYER NO.	LAYER NAME	COPPER WT. (oz.)	COMMENTS
1	Side A - DMD only	1.5	DMD, escapes, low frequency signals, power sub-planes.
2	Ground	1	Solid ground plane (net GND).
3	Signal	0.5	50 Ω and 100 Ω differential signals
4	Ground	1	Solid ground plane (net GND)
5	DMD_P3P3V	1	+3.3-V power plane (net DMD_P3P3V)
6	Signal	0.5	50 Ω and 100 Ω differential signals
7	Ground	1	Solid ground plane (net GND).
8	Side B - All other Components	1.5	Discrete components, low frequency signals, power sub-planes

10.2.2 Impedance Requirements

TI recommends that the board has matched impedance of 50 Ω ±10% for all signals. The exceptions are listed in 表 10-2.

表 10-2. Special Impedance Requirements

Signal Type	Signal Name	Impedance (ohms)
A channel LVDS differential pairs	D_AP(0:15), D_AN(0:15)	100 ±10% differential across each pair
	DCLKA_P, DCLKA_N	
	SCTRL_AP, SCTRL_AN	
B channel LVDS differential pairs	D_BP(0:15), D_BN(0:15)	100 ±10% differential across each pair
	DCLKB_P, DCLKB_N	
	SCTRL_BP, SCTRL_BN	
C channel LVDS differential pairs	D_CP(0:15), D_CN(0:15)	100 ±10% differential across each pair
	DCLKC_P, DCLKC_N	
	SCTRL_CP, SCTRL_CN	
D channel LVDS differential pairs	D_DP(0:15), D_DN(0:15)	100 ±10% differential across each pair
	DCLKD_P, DCLKD_N	
	SCTRL_DP, SCTRL_DN	

10.2.3 Trace Width, Spacing

Unless otherwise specified, TI recommends that all signals follow the 0.005-inch/0.005-inch design rule. Minimum trace clearance from the ground ring around the PWB has a 0.1-inch minimum. An analysis of impedance and stack-up requirements determine the actual trace widths and clearances.

10.2.3.1 Voltage Signals

表 10-3. Special Trace Widths, Spacing Requirements

SIGNAL NAME	MINIMUM TRACE WIDTH TO PINS (MIL)	LAYOUT REQUIREMENT
GND	15	Maximize trace width to connecting pin
DMD_P3P3V	15	Maximize trace width to connecting pin
DMD_P1P8V	15	Maximize trace width to connecting pin
VOFFSET	15	Create mini plane from U2 to U3
VRESET	15	Create mini plane from U2 to U3
VBIAS	15	Create mini plane from U2 to U3
All U3 control connections	10	Use 10 mil etch to connect all signals/voltages to DMD pads

11 Device and Documentation Support

11.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.2 Device Support

11.2.1 Device Nomenclature

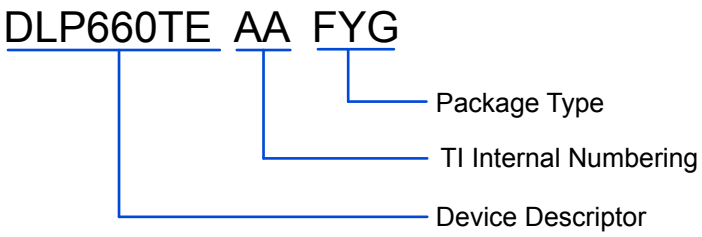


图 11-1. Part Number Description

11.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in 图 11-2. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Example: *2715-7032 GHXXXXX LLLLLLM

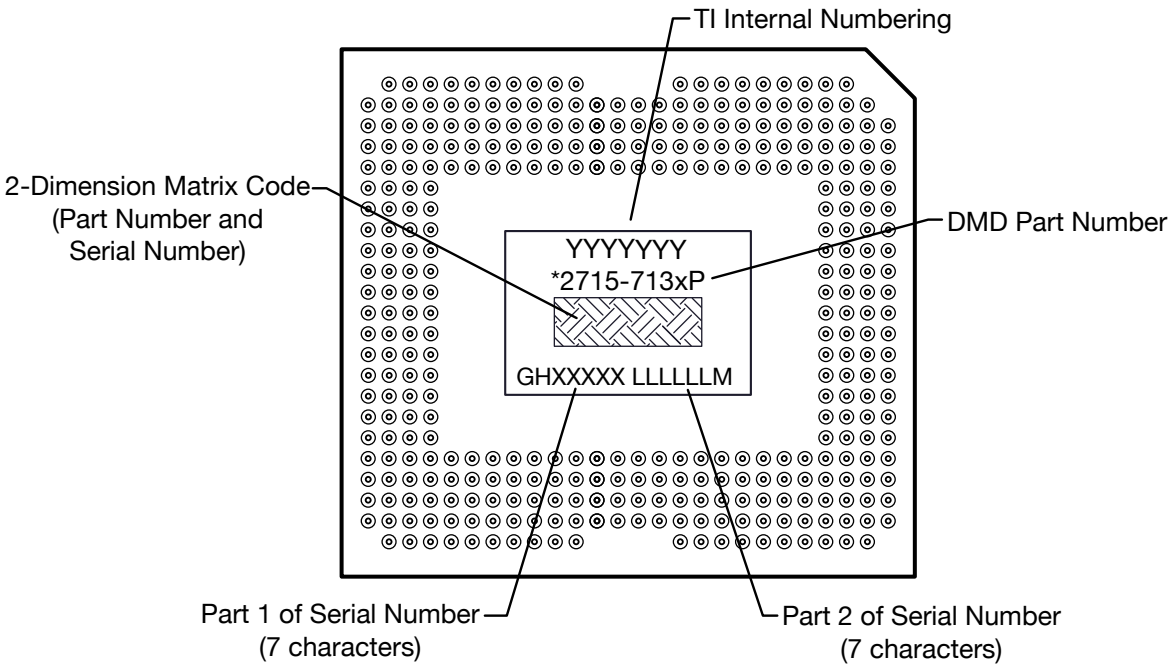


图 11-2. DMD Marking Locations

11.3 Documentation Support

11.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DLP660TE:

- *DLPC4420 Display Controller*
- *DLPA100 Power and Motor Driver Data Sheet*

11.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.6 Trademarks

TI E2E™ is a trademark of Texas Instruments.
DLP® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.7 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP660TEAAFYG	ACTIVE	CPGA	FYG	350	1	RoHS & Green	Call TI	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

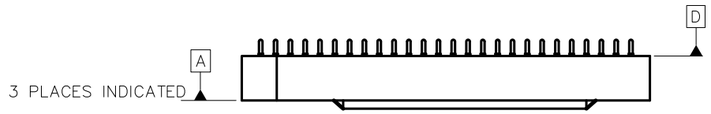
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

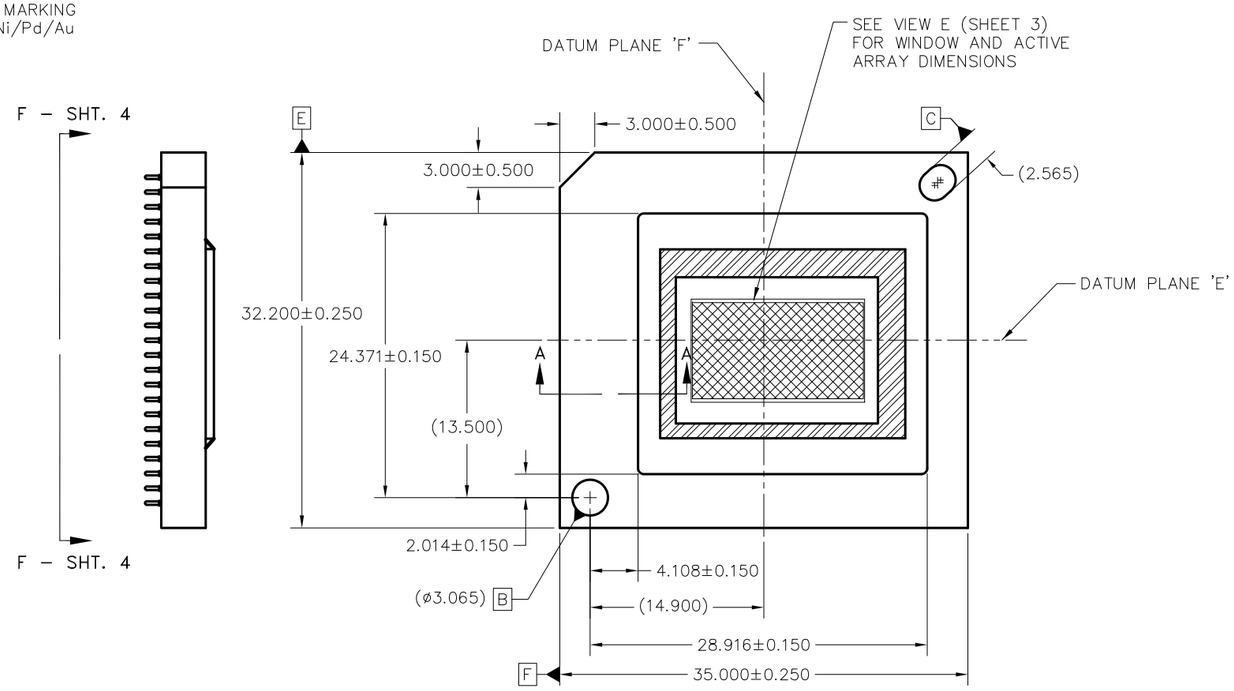
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

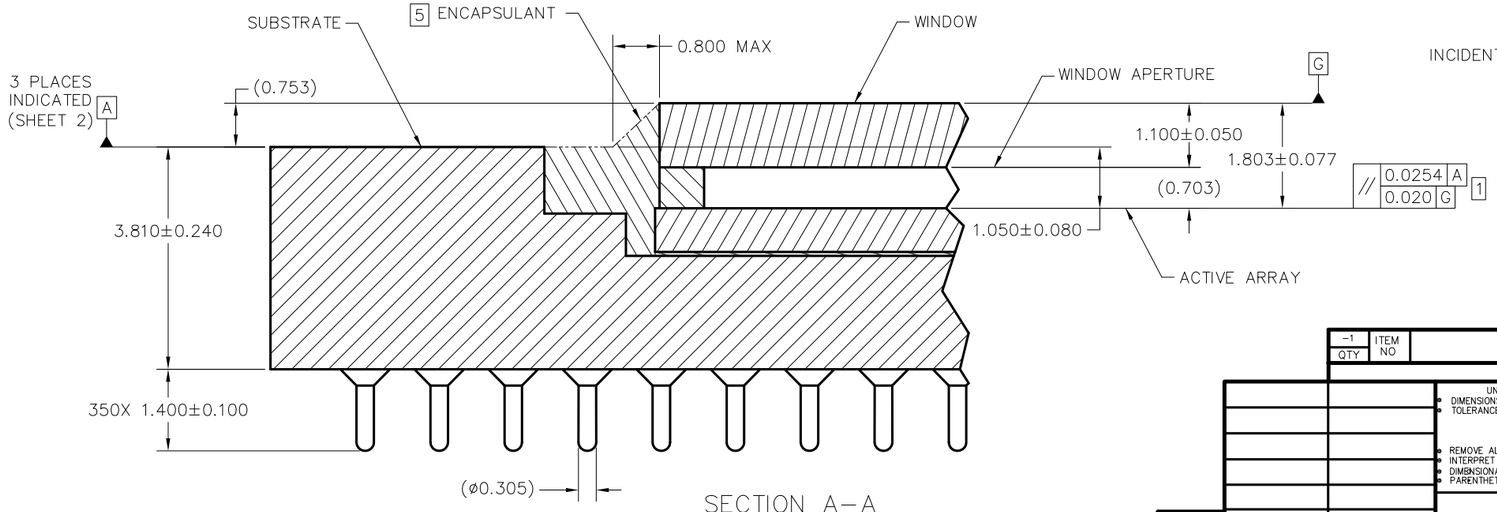
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2146754, INITIAL RELEASE	11/18/2014	M. AVERY
B	ECO 2147303, ADD GLASS DIMS	12/18/2014	F.ARMSTRONG
C	ECO 2149265, CHG ARRAY TO 1528 ROWS	03/17/2015	F.ARMSTRONG
D	ECO 2156970, CHG NUMERICAL IDENTIFIER TO 317	03/17/2016	F. ARMSTRONG

NOTES: UNLESS OTHERWISE SPECIFIED:

1. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
2. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
3. SUBSTRATE SYMBOLIZATION PAD AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
4. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
5. MAXIMUM ENCAPSULANT PROFILE SHOWN
6. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
7. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.







SECTION A–A
SCALE 20/1

–1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

DWN M. AVERY	DATE 11/18/2014	
ENGR F. ARMSTRONG	11/18/2014	
QA P. KONRAD	12/04/2014	
E. CARPENTER	12/04/2014	
CQE M. DORAK	12/04/2014	
S. SUSI	12/04/2014	

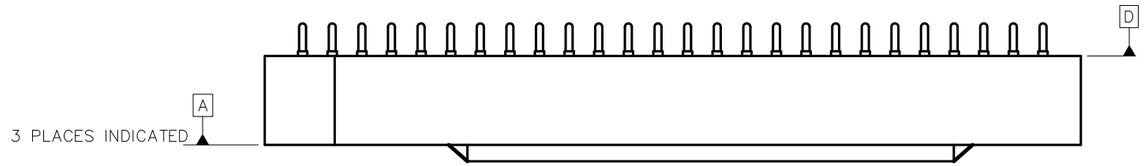
TEXAS INSTRUMENTS
Dallas, Texas

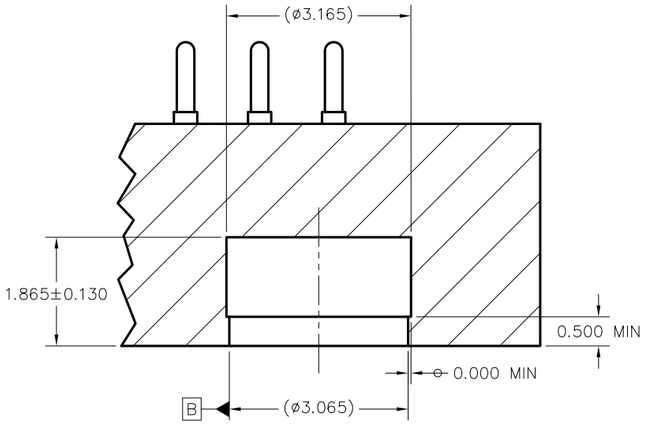
ICD, MECHANICAL, DMD
.66 UHD HB MTRP 2XLVDS
SERIES 610 (FYG PACKAGE)

SIZE D | DRAWING NO 2514366 | REV D

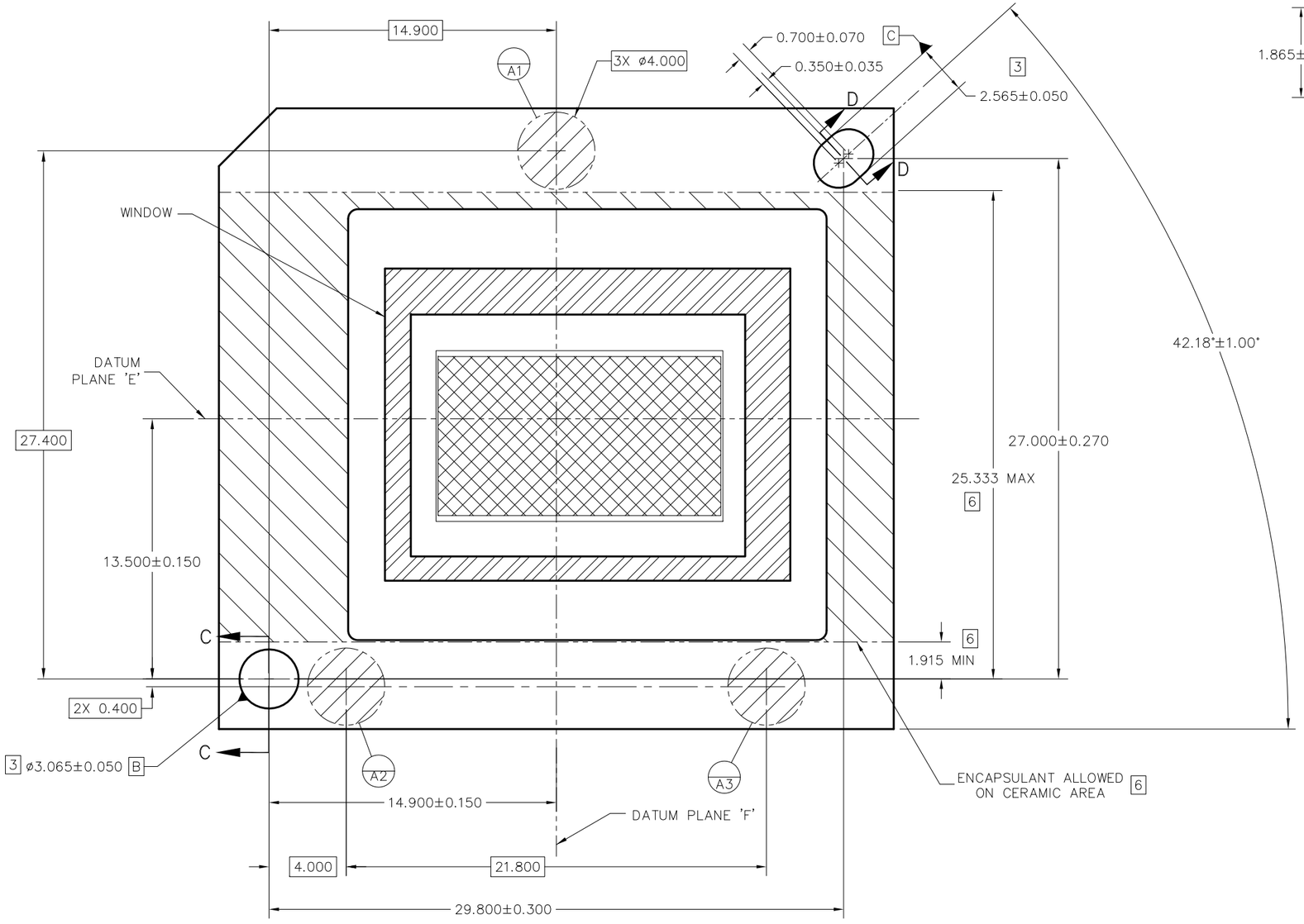
SCALE 4/1 | SHEET 1 OF 4

ACED1g

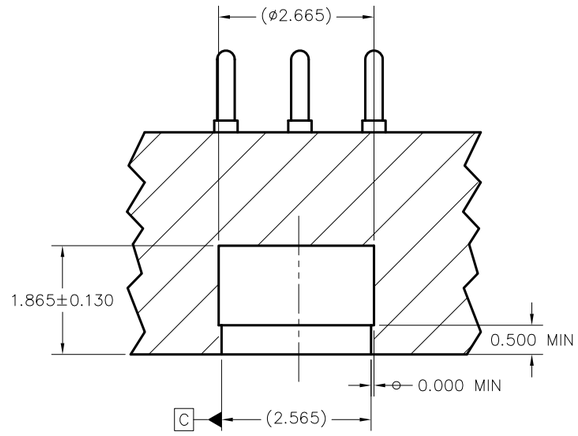




SECTION C–C
DATUM B
SCALE 16/1



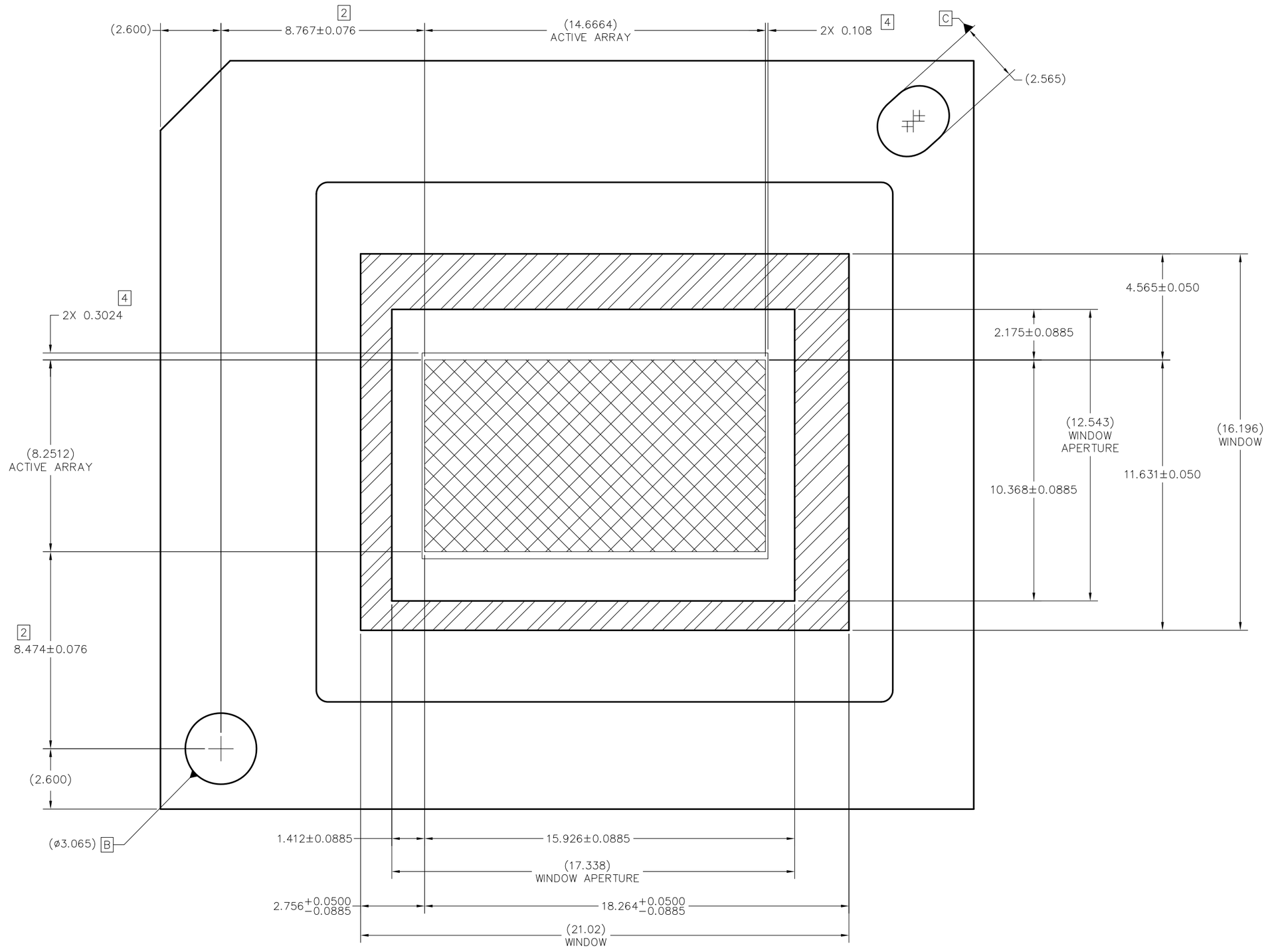
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2514366	REV D
		SCALE 4/1	SHEET 2	

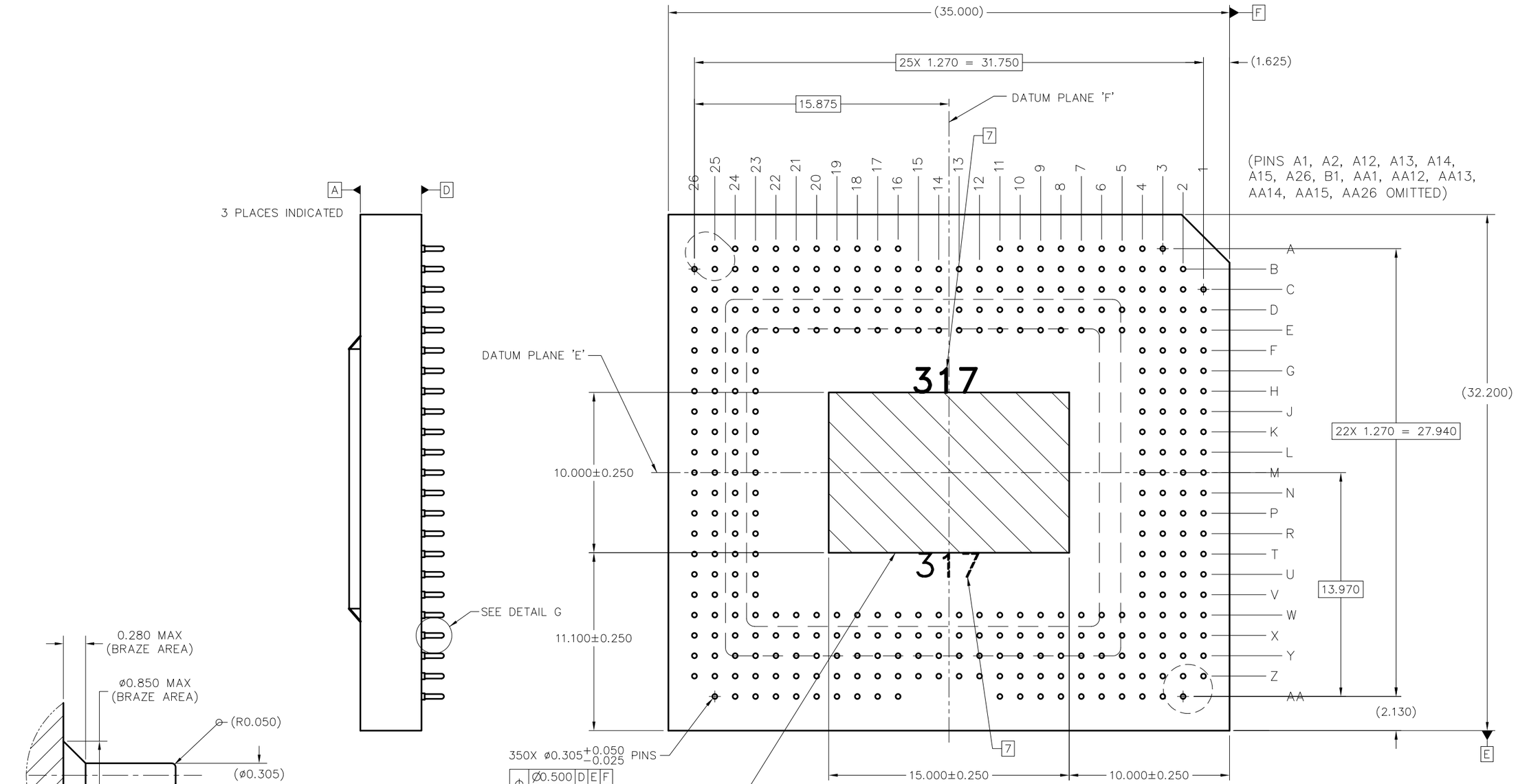
ACED2c



VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12/1

Texas Instruments, Dallas, Texas	DWN DATE	SIZE D	DRAWING NO 2514366	REV D
	ISSUE DATE	SCALE 4/1	SHEET 3	

ACED2c



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE / ISSUE DATE	SIZE D	DRAWING NO 2514366 REV D
		SCALE 4/1	SHEET 4

ACED2c

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