DLPR910 Configuration PROM

1 特性

- 预编程的 Xilinx® PROM 可配置 DLPC910 DMD 数字控制器
- I/O 引脚电压范围 1.8V 至 3.3V
- 1.8V 内核电源电压
- 工作温度范围：-40°C 至 85°C

2 应用

- 平版印刷
    - 直接成像
    - 平板显示器
    - 印刷电路板制造
- 工业
    - 3D 打印
    - 用于机器视觉的 3D 扫描仪
    - 质量控制
- 显示器
    - 3D 成像
    - 智能和自适应照明
    - 增强现实和信息覆盖

3 说明

DLPR910 器件是一款经编程的 PROM，用于正确配置 DLPC910 DLPC910ZYR 控制器，从而运行四个不同的数字微镜器件 (DMD) 选件：DLP9000X、DLP9000XUV 和 DLP6500 系列（S600 和 A 型封装）。此器件中的固件使 DLPC910 DLPC910ZYR 控制器能够提供高达 61 千兆位/秒 (Gbps)（DLP9000X 和 DLP9000XUV）以及高达 24Gbps（DLP6500 系列）的系统数据吞吐量，并提供随机行寻址和 Load4 功能选项。

查看 TI DLP® 光控制技术页面，了解如何开始使用 DLPC410ZYR。ti.com 上的 DLP 先进光控制资源可加快上市速度，这些资源包括评估模块、参考设计、光学模块制造商和 DLP 设计网络合作伙伴。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
DLPR910	DSBGA (48)	8.00mm × 9.00mm × 1.20mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 3-1. 简化版应用

English Data Sheet: DLPS065

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (September 2019) to Revision D (December 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式...1	

Changes from Revision B (November 2016) to Revision C (September 2019)	Page
• 将"三个不同 DMD 选件"更改为"四个不同 DMD 选件" 1	
• 添加了 DLP9000XUV...1	
• Updated Xilinx reference doc to revision v2.19 from v2.18...6	
• Added DLP9000XUV 7	
• Added DLP9000XUV 10	
• Added DLP9000XUV to caption of Typical Application Schematic 10	
• Added DLP9000XUV 11	
• Updated table to indicate DLP9000XUV is not compatible with DLPR910YVA 13	
• Changed Device Markings image 13	
• Added DLP9000XUV datasheet 14	

Changes from Revision A (October 2015) to Revision B (November 2016)	Page
• 更新了 *相关文档* 以包含其他受支持的 DMD。..1	
• Update document to include additional supported DMD options in *节 7*..7	
• Added typical application schematic for newly supported DMD in *节 8.2*..10	
• Updated *节 11.1.3*...13	
• Added MSL Peak Temp to *节 12.1.1* 15	

Changes from Revision * (September 2015) to Revision A (October 2015)	Page
• 将器件状态从"产品预发布"更改为"量产数据"...1	

5 Pin Configuration and Functions
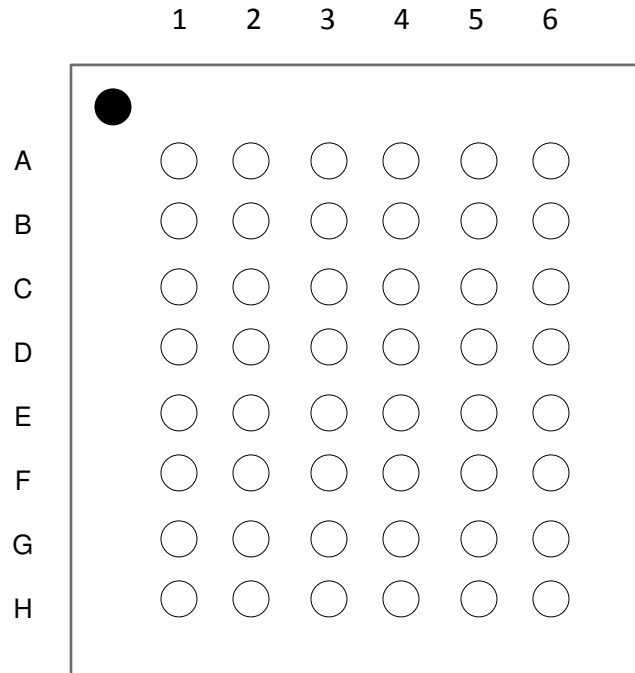
图 5-1. YVA Package 48-Pin DSBGA Top View

表 5-1. Pin Functions

| PIN | | TYPE[1] | DESCRIPTION |
NAME	NO.		
GND	A1	G	Ground
GND	A2	G	Ground
OE/ RESET	A3	I/O	Output Enable/ RESET (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM completes the internal power-on reset sequence. Polarity is not programmable. **Pin must be pulled High using an external 4.7-kΩ pull-up to V$_{CCO}$.**
DNC	A4	—	Do Not Connect. Leave unconnected.
D6	A5	—	Do Not Connect. Leave unconnected.
D7	A6	—	Do Not Connect. Leave unconnected.
V$_{CCINT}$	B1	P	Positive 1.8-V supply voltage for internal logic.
V$_{CCO}$	B2	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
CLK	B3	I	Configuration clock input. Each rising edge on the CLK input increments the internal address counter. **Pin must be pulled High and Low using an external 100-Ω pull-up to V$_{CCO}$ and an external 100-Ω pull-down to Ground. Place resistors close to pin.**
CE	B4	I	Chip Enable Input. When CE is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high impedance state. **Pin must be pulled High using an external 4.7-kΩ pull-up to V$_{CCO}$.**
D5	B5	—	Do Not Connect. Leave unconnected.
GND	B6	G	Ground
BUSY	C1	—	Do Not Connect. Leave unconnected.
CLKOUT	C2	—	Do Not Connect. Leave unconnected.
DNC	C3	—	Do Not Connect. Leave unconnected.
DNC	C4	—	Do Not Connect. Leave unconnected.

表 5-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
D4	C5	—	Do Not Connect. Leave unconnected.
V_{CCO}	C6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
$\overline{CF}$	D1	I	Configuration pin. **The $\overline{CF}$ pin must be pulled High using an external 4.7-kΩ pull-up to V_{CCO}.** Selects serial mode configuration.
$\overline{CEO}$	D2	—	Do Not Connect. Leave unconnected.
DNC	D3	—	Do Not Connect. Leave unconnected.
DNC	D4	—	Do Not Connect. Leave unconnected.
D3	D5	—	Do Not Connect. Leave unconnected.
V_{CCO}	D6	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V_{CCINT}	E1	P	Positive 1.8-V supply voltage for internal logic.
TMS	E2	I	JTAG Mode Select Input. TMS has an internal 50-kΩ resistive pull-up to V_{CCJ}.
DNC	E3	—	Do Not Connect. Leave unconnected.
DNC	E4	—	Do Not Connect. Leave unconnected.
DNC	E5	—	Do Not Connect. Leave unconnected.
TDO	E6	O	JTAG Serial Data Output. TDO has an internal 50-kΩ resistive pull-up to V_{CCJ}.
GND	F1	G	Ground
DNC	F2	—	Do Not Connect. Leave unconnected.
DNC	F3	—	Do Not Connect. Leave unconnected.
DNC	F4	—	Do Not Connect. Leave unconnected.
GND	F5	G	Ground
GND	F6	G	Ground
TDI	G1	I	JTAG Serial Data Input. TDI has an internal 50k-Ω resistive pull-up to V_{CCJ}.
DNC	G2	—	Do Not Connect. Leave unconnected.
REV_SEL0	G3	I	Revision Select [1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled. The Revision Select [1:0] inputs have an internal 50-kΩ resistive pull-up to V_{CCO}. **The REV_SEL0 pin must be pulled Low using an external 4.7-kΩ pull-down to Ground. The REV_SEL1 pin must be pulled Low using an external 4.7-kΩ pull-down to Ground.**
REV_SEL1	G4	I	
V_{CCO}	G5	P	Positive 3.3-V and 1.8-V supply voltage connected to the output voltage drivers and internal buffers.
V_{CCINT}	G6	P	Positive 1.8-V supply voltage for internal logic.
GND	H1	G	Ground
VCCJ	H2	P	Positive 3.3-V JTAG I/O supply voltage connected to the TDO output voltage driver and TCK, TMS and TDI input buffers.
TCK	H3	I	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.
$\overline{EN\_EXT\_SEL}$	H4	I	External Selection Input. $\overline{EN\_EXT\_SEL}$ has an internal 50-kΩ resistive pull- up to V_{CCO}. **The $\overline{EN\_EXT\_SEL}$ pin must be connected to Ground**.
D1	H5	—	Do Not Connect. Leave unconnected.
D0	H6	O	DATA output pin to provide data for configuring the DLPC910 in serial mode.

(1)　P = Power, G = Ground, I = Input, O = Output

6 Specifications

For complete electrical and mechanical specifications of the DLPR910, see the XCF16P product specification listed in *Related Documentation*.

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see [1] [2])

			MIN	MAX	UNIT
V_{CCINT}	Internal supply voltage	Relative to ground	– 0.5	2.7	V
V_{CCO}	I/O supply voltage	Relative to ground	– 0.5	4.0	V
V_{IN}	Input voltage with respect to ground	V_{CCO} < 2.5 V	– 0.5	3.6	V
		$V_{CCO} \geqslant$ 2.5 V	– 0.5	3.6	V
V_{TS}	Voltage applied to high-impedance output	V_{CCO} < 2.5 V	– 0.5	3.6	V
		$V_{CCO} \geqslant$ 2.5 V	– 0.5	3.6	V
T_J	Junction temperature			125	°C
T_{stg}	Storage temperature, ambient		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) Maximum DC undershoot below GND must be limited to either 0.5 V or 10 mA. During transitions, the device pins can undershoot to – 2 V or overshoot to 7 V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ [1]	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins [2]	2000	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CCINT}	Internal voltage supply		1.65	1.8	2.0	V
V_{CCO}	Supply voltage for output drivers	3.3-V operation	3.0	3.3	3.6	V
V_{IL}	Low-level input voltage	3.3-V operation	0		0.8	V
V_{IH}	High-level input voltage	3.3-V operation	2.0		3.6	V
V_O	Output voltage		0		V_{CCO}	V
t_{IN}	Input signal transition time (measured between 10% V_{CCO} and 90% V_{CCO})				500	ns
T_A	Operating ambient temperature		– 40		85	°C

6.4 Thermal Information

Refer to the XCF16P product specifications.

6.5 Electrical Characteristics

Refer to the XCF16P product specifications at www.xilinx.com.

6.6 Supply Voltage Requirements for Power-On Reset and Power-Down

(see [1])

		MIN	MAX	UNIT
t_{VCC}	V_{CCINT} rise time from 0 V to nominal voltage [2]	0.2	50	ms
V_{CCPOR}	POR threshold for V_{CCINT} supply	0.5	–	V
t_{OER}	OE/ $\overline{RESET}$ release delay following POR [3]	0.5	30	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply		0.5	V
t_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10		ms

(1) V_{CCINT}, V_{CCO}, and V_{CCJ} supplies can be applied in any order.
(2)   At power-up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified t_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Platform Flash PROM Power-Up Requirements, in the Xilinx XCF16P (v2.19) Product Specification for more information.
(3)   If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/ $\overline{RESET}$ pin is released, then the configuration data from the PROM is not available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

6.7 Timing Requirements

Refer to the XCF16P product specifications at www.xilinx.com.

7 Detailed Description

7.1 Overview

The configuration bit stream stored in the DLPR910 device supports reliable operation of the DLPC910 device with the DLP9000X and DLP9000XUV DMDs, or the DLP6500 family of DMDs. The DLPC910 digital controller loads this configuration bit stream from the DLPR910 device.
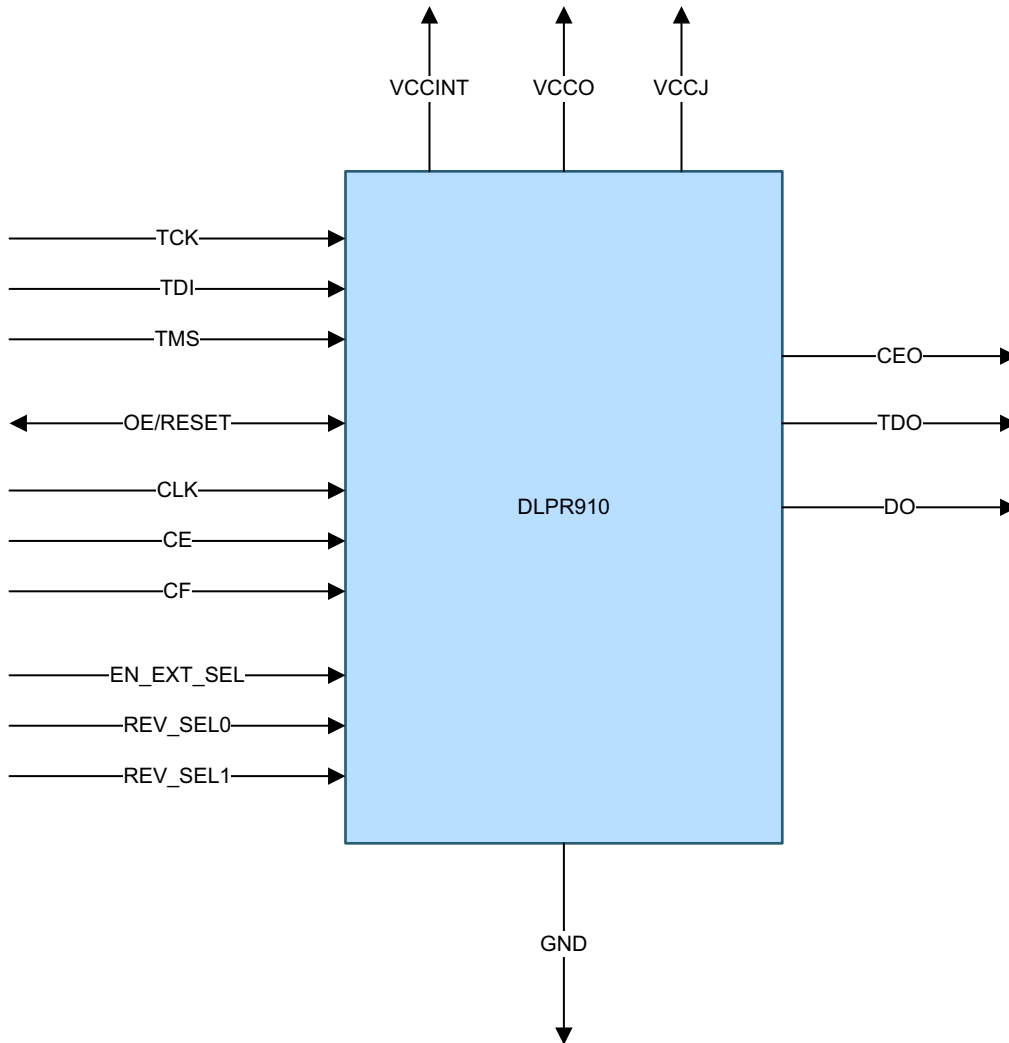
7.2 Functional Block Diagram

图 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Data Interface

7.3.1.1 Data Outputs

The DLPR910 device is configured for serial mode operation, where D0 is the data output pin. D0 output pin provides a serial connection to the DLPC910 controller, where the configuration is read out by the DLPC910 controller.

7.3.1.2 Configuration Clock Input

The configuration CLK is connected to the DLPC910 controller in Primary Serial mode, where the DLPC910 controller provides the clock pulses to read the configuration from the DLPR910 device.

Product Folder Links: *DLPR910*

7.3.1.3 Output Enable and Reset

When the OE/ $\overline{\text{RESET}}$ input is held low, the address counter is reset and the Data (D0) and CLKOUT outputs are placed in high-impedance state. **OE/ $\overline{\text{RESET}}$ must be pulled High using an external 4.7-k Ω pull-up to V$_{\text{CCO}}$.**

7.3.1.4 Chip Enable

The $\overline{\text{CE}}$ input is asserted by the DLPC910 controller to enable the Data (D0) and CLKOUT outputs. When $\overline{\text{CE}}$ is held high, the DLPR910 device address counter is reset, and the Data and CLKOUT outputs are placed in high-impedance states.

7.3.1.5 Configuration Pulse

The DLPR910 device is configured in serial mode when it holds configuration pulse pin, $\overline{\text{CF}}$, high and it enables the $\overline{\text{CE}}$ and OE pins. New data is available a short time after each rising clock edge.

7.3.1.6 Revision Selection

The device uses the REV_SEL0, REV_SEL1, and $\overline{\text{EN\_EXT\_SEL}}$ signals to select a revision to act as the default. Setting all three signals to GND defaults to revision 0 for simple DLPR910 device setup.

7.4 Device Functional Modes

To successfully program the DLPC910 controller upon power-up, the DLPR910 device must be configured and connected to the DLPC910 controller as shown in 图 7-2.
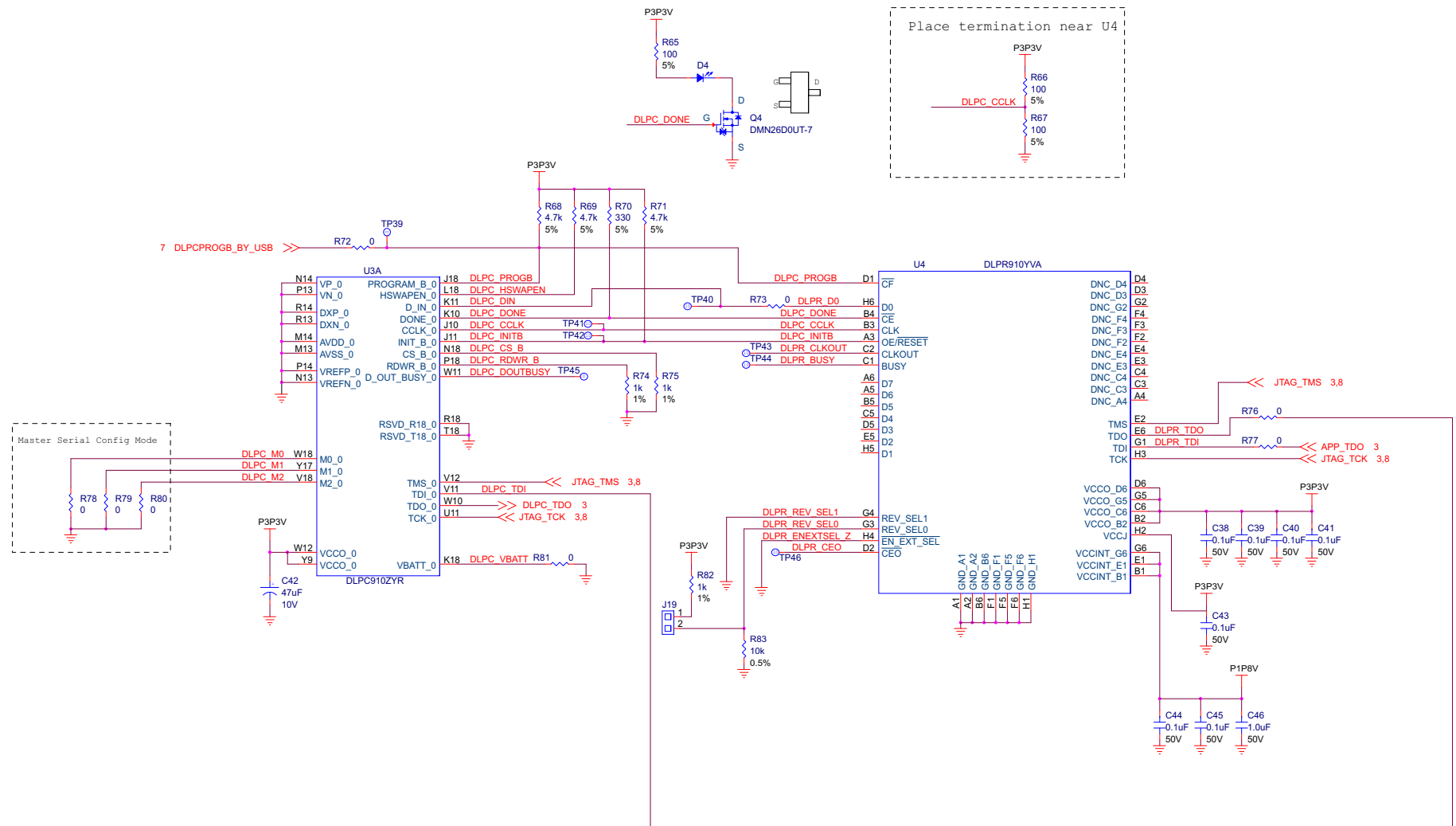
图 **7-2. DLPC910 and DLPR910 Connection Schematic**

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The DLPR910 device configuration PROM ships pre-programmed with configuration code for the DLPC910 controller. Upon power-up, the DLPC910 controller and the DLPR910 device connect to enable configuration information to be sent from the DLPR910 device to the DLPC910 controller, such that the DLPC910 controller can configure itself for proper operation within the application. Without the DLPR910 device properly connected to the DLPC910 controller in the application system, the DLPC910 controller does not boot and the system remains inoperable.

8.2 Typical Application

A typical use case for a high speed lithography application is shown in 图 8-1 and in 图 8-2. Both applications offer continuous run of printing by changing the digitally created patterns without stopping the imaging head. The DLPR910 prom configures the DLPC910 digital controller to reliably operate with the DLP9000X and DLP9000XUV DMDs, or the DLP6500 DMDs. These chipset combinations provide an ideal back-end imager that takes in digital images at 2560 × 1600 and 1920 x 1080 in resolution to achieve speeds greater than 61 Gigabits per second (Gbps) and 24 Gbps respectively. For complete details of this typical application refer to the DLPC910 data sheet listed in 节 11.2.1.
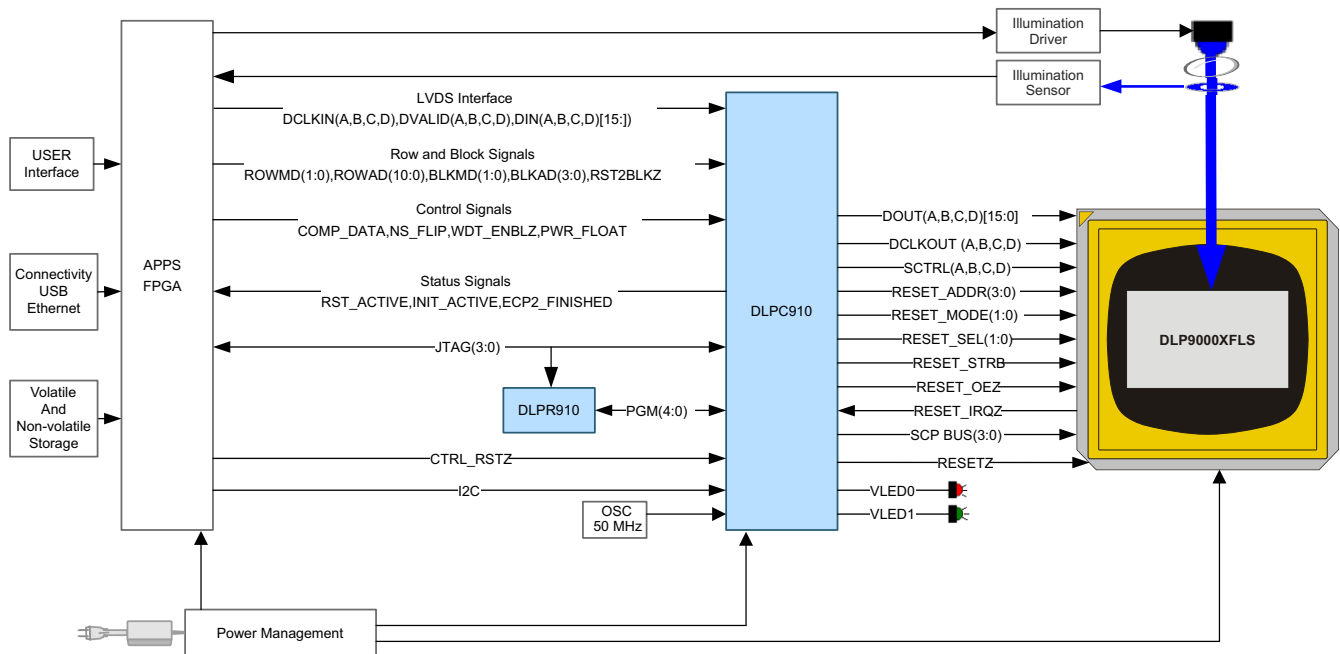

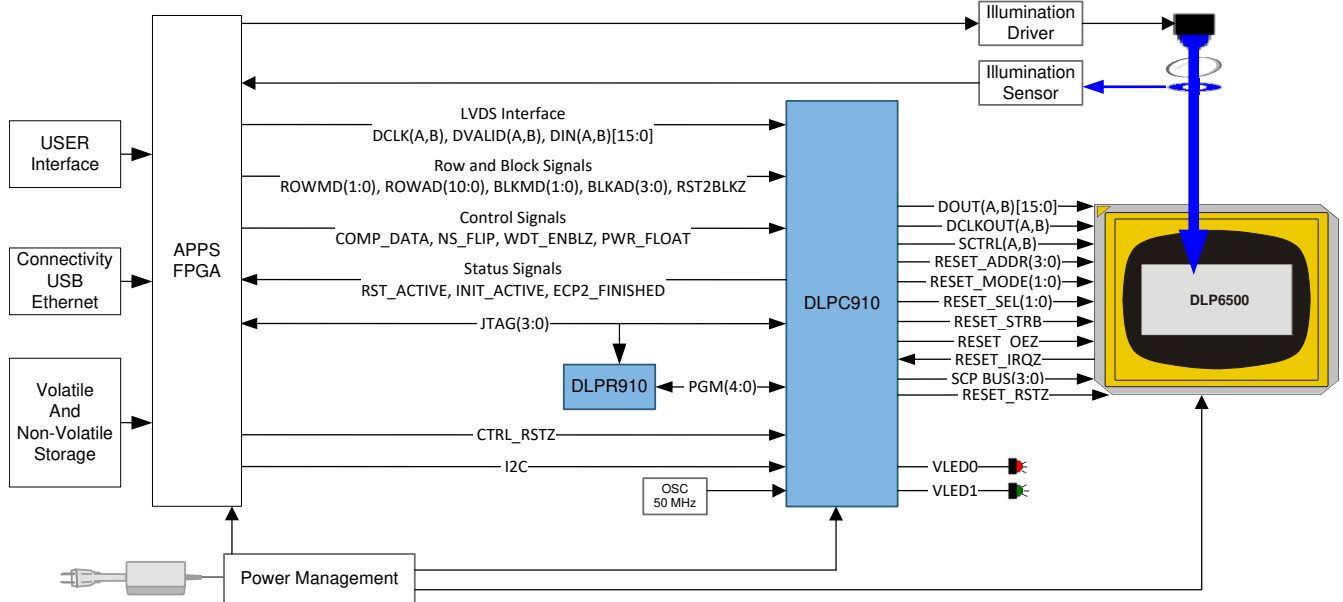图 8-1. Typical High Speed DLP9000X (or DLP9000XUV) Application Schematic

图 8-2. **Typical High Speed DLP6500 Application Schematic**

8.2.1 Design Requirements

The DLPR910 is part of a multi-chipset solution, and it is required to be coupled with the DLPC910 controller for reliable operation of the DLP9000X and DLP9000XUV DMDs, or the DLP6500 family of DMDs. For more information, refer to the DLPC910 datasheet listed in 节 11.2.1.

9 Power Supply Recommendations

The DLPR910 uses two power supply rails as shown in 表 9-1.

表 9-1. DLPR910 Power Supply Rails

SUPPLY	POWER PINS	COMMENTS
1.8 V	V_{CCINT1}, V_{CCINT2}, and V_{CCINT3}	All V_{CCINT} pins must be connected with a 0.1-μF and a 0.047-μF decoupling capacitor to GND.
3.3 V	V_{CCO1}, V_{CCO2}, V_{CCO3}, V_{CCO4}, and V_{CCJ}	All V_{CCO} and V_{CCJ} pins must be connected with a 0.1-μF and a 0.047-μF decoupling capacitor to GND.

10 Layout

10.1 Layout Guidelines

The DLPR910 is part of a multi-chipset solution. It is required to be used with the DLPC910 Controller to provide reliable control of any attached DMDs. These guidelines are targeted at designing a PCB board with the DLPR910.

Product Folder Links: DLPR910

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Compatibility

TI PART NUMBER[1]	DLP9000XFLS	DLP9000XBFLS	DLP9000XUVFLS	DLP6500FYE DLP6500FLQ	DLP6500BFYE DLP6500BFLQ
DLPR910YVA	Compatible	Not Compatible	Not Compatible	Compatible	Not Compatible
DLPR910AYVA	Compatible	Compatible	Compatible	Compatible	Compatible

(1) Refer to each individual DMD datasheet under Device and Documentation Support to determine location and revision of the DMD.

11.1.2 Device Nomenclature

表 11-1. Part Number Description

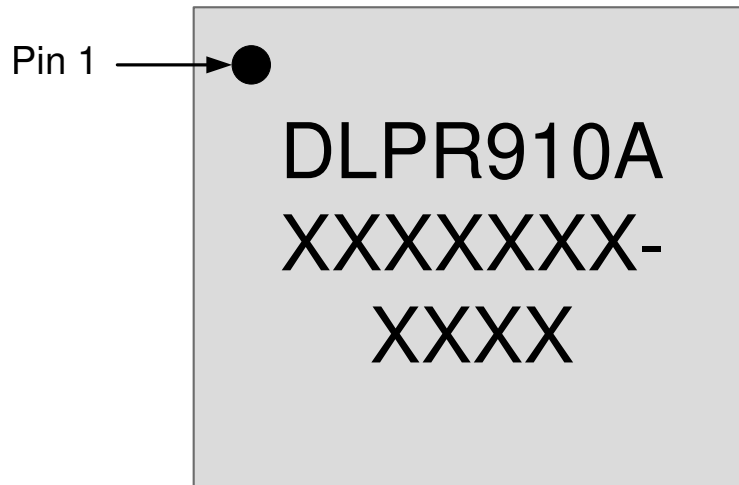| TI PART NUMBER	DESCRIPTION	REFERENCE NUMBER
DLPR910AYVA	DLPR910A Configuration PROM	2514595-0002

11.1.3 Device Markings

图 11-1. DLPR910 Device Markings

Where XXXXXXX-XXXX is the reference number located in 表 11-1.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- DLPC910 datasheet (DLPS064)
- DLP9000(X) datasheet (DLPS036)
- DLP9000XUV datasheet (DLPS158)
- DLP6500 Type A datasheet (DLPS040)
- DLP6500 S600 datasheet (DLPS053)
- XCF16P data sheet (www.xilinx.com)

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
Xilinx® is a registered trademark of Xilinx, Inc.
所有商标均为其各自所有者的财产。

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表   本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this datasheet, refer to the left-hand navigation.
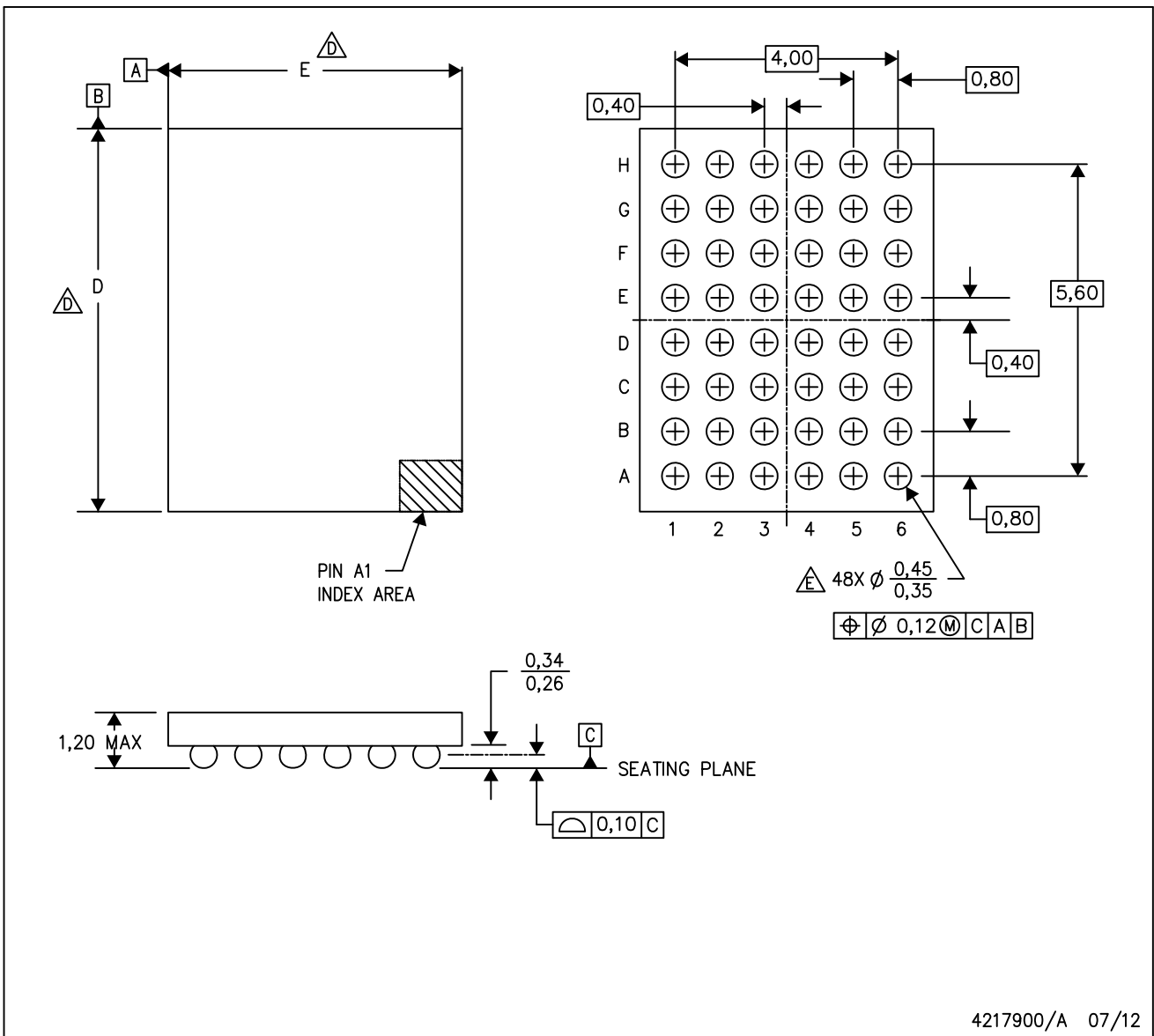
12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]	Op Temp (°C)	Device Marking[4] [5]
DLPR910AYVA	ACTIVE	DSBGA	YVA	48	1	Call TI	Call TI	Level-3-260C-168 HRS	– 40 to 85	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

YVA (R−XBGA−N48)   DIE−SIZE BALL GRID ARRAY

PIN A1
INDEX AREA

48X Ø $\frac{0,45}{0,35}$

⊕ | Ø 0,12 Ⓜ | C | A | B

$\frac{0,34}{0,26}$

1,20 MAX

SEATING PLANE

0,10 C

4217900/A   07/12

NOTES: A.   All linear dimensions are in millimeters.   Dimensioning and tolerancing per ASME Y14.5M−1994.
        B.   This drawing is subject to change without notice.
        C.   NanoFree™ package configuration.
        D.   The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version
             of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
        E.   Reference Product Data Sheet for array population.
             6 x 8 matrix pattern is shown for illustration only.
        F.   This package contains Pb−free balls.

Texas
Instruments
www.ti.com

重要声明和免责声明

TI"按原样"提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。