DS90LV011AH
ZHCSJ91C – SEPTEMBER 2005 – REVISED JULY 2021

DS90LV011AH 高温 3V LVDS 差分驱动器

1 特性

- –40°C 至 125°C 工作温度范围
- 符合 TIA/EIA-644-A 标准
- >400Mbps (200MHz) 转换速率
- 700ps（100ps 典型值）最大差动偏斜
- 1.5ns 最大传播延迟
- 3.3V 单电源
- ±350mV 差分信号传输
- 断电保护（TRI-STATE 中的输出）
- 引脚排列简化了 PCB 布局
- 低功率耗散（3.3V 典型电压下为 23mW）
- 5 引脚 SOT-23 封装
- 引脚与 SN65LVDS1 兼容

2 应用

- 板对板通信
- 测试和测量
- 电机驱动器
- LED 视频墙
- 无线基础设施
- 电信基础设施
- 多功能打印机
- NIC 卡
- 机架式服务器
- 超声波扫描仪

3 说明

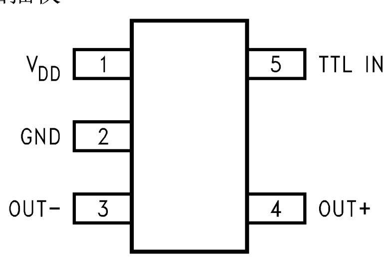
DS90LV011AH 是一款针对高数据速率和低功耗应用进行优化的 LVDS 驱动器。DS90LV011AH 是一款电流模式驱动器，即使在高频率条件下也能够保持较低的功率耗散。此外，它还能够最大限度地降低短路故障电流。该器件旨在利用低电压差分信号 (LVDS) 技术以支持超过 400Mbps (200MHz) 的数据速率。

该器件采用 5 引脚 SOT-23 封装。为简化 PCB 布局，已对 LVDS 输出进行排列。差分驱动器输出可提供低电磁干扰 (EMI)，其典型的低输出摆幅为 350mV。DS90LV011AH 可与配套的单通道线路接收器 DS90LT012AH 或任何 TI 的 LVDS 接收器搭配使用，以提供高速 LVDS 接口。

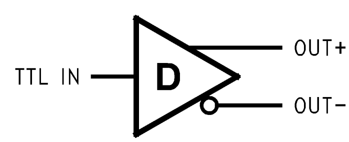
器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
DS90LV011AH	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



连接图



功能图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (January 2019) to Revision C (July 2021) — **Page**

- 更新了整个文档的表、图和交叉参考的编号格式 ... 1
- Corrected pin description table. Pin 3 should be OUT- and pin 4 should be OUT+ ... 3

Changes from Revision A (April 2013) to Revision B (January 2019) — **Page**

- 添加了*器件信息* 表、*ESD 等级* 表、*热性能信息* 表、*典型特性* 部分、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- Changed the *Absolute Maximum Ratings* tablenote ... 4
- Moved the ESD parameters in the *Absolute Maximum Ratings* table to the *ESD Ratings* table ... 4
- Changed the Temperature (T_A) parameter in the *Recommended Operating Conditions* table to Junction temperature (T_J) ... 4

Changes from Revision * (April 2013) to Revision A (April 2013) — **Page**

- 已将国家数据表的版面布局更改为 TI 格式 ... 1

5 Pin Configuration and Functions

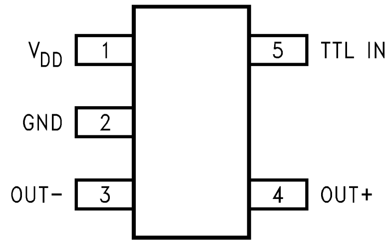


图 5-1. DBV Package 5-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Power supply pin, +3.3 V ± 0.3 V
2	GND	I	Ground pin
3	OUT-	O	Inverting driver output pin
4	OUT+	O	Noninverting driver output pin
5	TTL IN	I	LVTTL/LVCMOS driver input pins

6 Specifications

6.1 Absolute Maximum Ratings[(1)] [(2)]

		MIN	MAX	UNIT
Supply voltage (V_{DD})		−0.3	4	V
LVCMOS input voltage (TTL IN)		−0.3	3.6	V
LVDS output voltage (OUT±)		−0.3	3.9	V
LVDS output short circuit current			24	mA
Maximum package power dissipation at +25°C	DBV Package		902	mW
	Derate DBV Package (above +25°C)		7.22	mW/°C
Lead temperature range soldering (4 sec.)			260	°C
Maximum Junction Temperature			150	°C
Storage temperature, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] (1.5 kΩ, 100 pF)	9000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] (0 Ω, 0 pF)	2000	
		EIAJ (0 Ω, 200 pF)	900	
		IEC direct (330 Ω, 150 pF)	4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±9000 V may actually have higher performance.
(2) JJEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage (V_{DD})	3	3.3	3.6	V
Junction temperature (T_A)	−40	+25	+125	°C
Junction temperature (T_J)			+130	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		DS90LV011AH DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	19.3	°C/W

THERMAL METRIC(1)		DS90LV011AH DBV (SOT-23) 5 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	43.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over Supply Voltage and Operating Temperature ranges, unless otherwise specified.(1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Output Differential Voltage	R_L = 100 Ω (图 7-1 and 图 7-2)	OUT+, OUT−	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change	R_L = 100 Ω (图 7-1 and 图 7-2)	OUT+, OUT−		3	35	mV
V_{OS}	Offset Voltage	R_L = 100 Ω (图 7-1)	OUT+, OUT−	1.125	1.22	1.375	V
ΔV_{OS}	Offset Magnitude Change	R_L = 100 Ω (图 7-1)	OUT+, OUT−	0	1	25	mV
I_{OFF}	Power-off Leakage	V_{OUT} = 3.6 V or GND, V_{DD} = 0 V	OUT+, OUT−		±1	±10	μA
I_{OS}	Output Short Circuit Current(4)	V_{OUT+} and V_{OUT-} = 0 V	OUT+, OUT−		−6	−24	mA
I_{OSD}	Differential Output Short Circuit Current(4)	V_{OD} = 0 V	OUT+, OUT−		−5	−12	mA
C_{OUT}	Output Capacitance		OUT+, OUT−		3		pF
V_{IH}	Input High Voltage		TTL IN	2		V_{DD}	V
V_{IL}	Input Low Voltage		TTL IN	GND		0.8	V
I_{IH}	Input High Current	V_{IN} = 3.3 V or 2.4 V	TTL IN		±2	±10	μA
I_{IL}	Input Low Current	V_{IN} = GND or 0.5 V	TTL IN		±1	±10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	TTL IN	−1.5	−0.6		V
C_{IN}	Input Capacitance		TTL IN		3		pF
I_{DD}	Power Supply Current	No Load; V_{IN} = V_{DD} or GND	V_{DD}		5	8	mA
I_{DD}	Power Supply Current	R_L = 100 Ω; V_{IN} = V_{DD} or GND	V_{DD}		7	10	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD}.
(2) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
(3) The DS90LV011AH is a current mode device and only function with datasheet specification when a resistive load is applied to the drivers outputs.
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

6.6 Switching Characteristics

Over Supply Voltage and Operating Temperature Ranges, unless otherwise specified.(1) (2) (3) (4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential Propagation Delay High to Low	R_L = 100 Ω, C_L = 15 pF (图 7-3 and 图 7-4)	0.3	1	1.5	ns
t_{PLHD}	Differential Propagation Delay Low to High		0.3	1.1	1.5	ns
t_{SKD1}	Differential Pulse Skew $\|t_{PHLD} - t_{PLHD}\|$(5)		0	0.1	0.7	ns
t_{SKD3}	Differential Part to Part Skew(6)		0	0.2	1	ns
t_{SKD4}	Differential Part to Part Skew(7)		0	0.4	1.2	ns
t_{TLH}	Transition Low to High Time		0.2	0.5	1	ns
t_{THL}	Transition High to Low Time		0.2	0.5	1	ns
f_{MAX}	Maximum Operating Frequency(8)		200	250		MHz

(1) All typicals are given for: V_{DD} = +3.3V and T_A = +25°C.
(2) These parameters are specified by design. The limits are based on statistical analysis of the device performance over PVT (process, voltage, temperature) ranges.
(3) C_L includes probe and fixture capacitance.
(4) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, $t_r \leqslant$ 1 ns, $t_f \leqslant$ 1 ns (10%-90%).
(5) t_{SKD1}, $|t_{PHLD} - t_{PLHD}|$, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(6) t_{SKD3}, Differential Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{DD} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel to channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.

(8) f_{MAX} generator input conditions: $t_r = t_f < 1$ ns (0% to 100%), 50% duty cycle, 0V to 3V. Output criteria: duty cycle = 45%/55%, $V_{OD} >$ 250mV. The parameter is specified by design. The limit is based on the statistical analysis of the device over the PVT range by the transitions times (t_{TLH} and t_{THL}).

6.7 Typical Characteristics

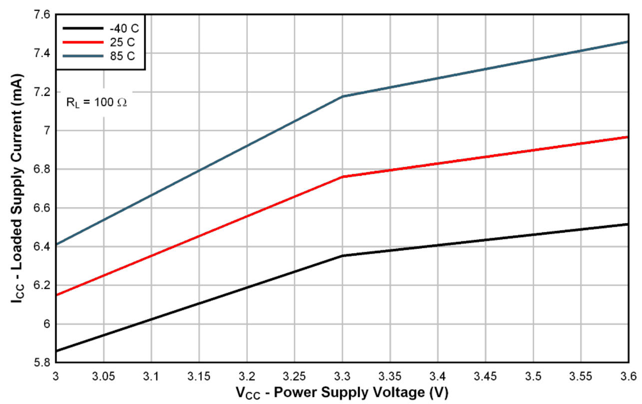


图 6-1. Loaded Supply Current vs Power Supply Voltage

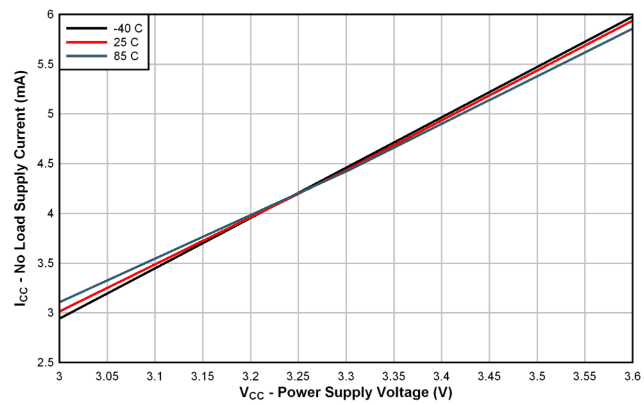


图 6-2. No Load Supply Current vs Power Supply Voltage

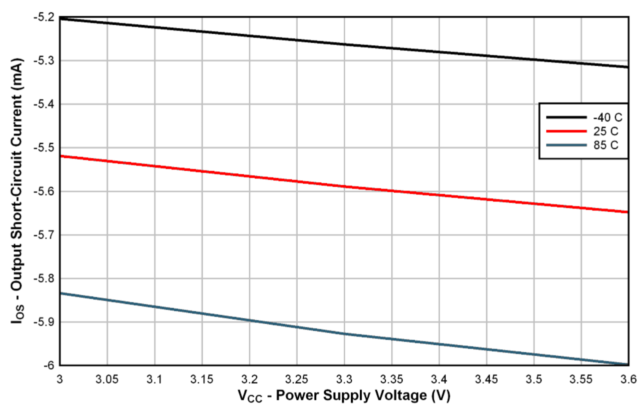


图 6-3. Output Short-Circuit Current vs Power Supply Voltage

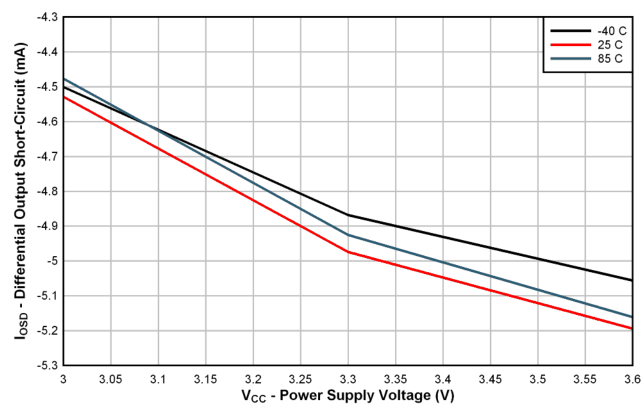


图 6-4. Differential Output Short-Circuit Current vs Power Supply Voltage

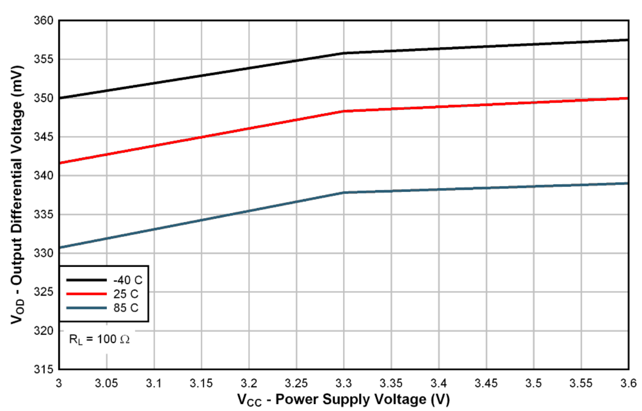


图 6-5. . Output Differential Voltage vs Power Supply Voltage

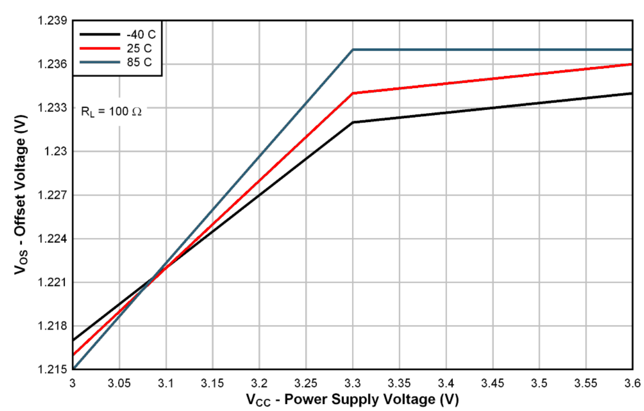


图 6-6. Offset Voltage vs Power Supply Voltage

7 Parameter Measurement Information

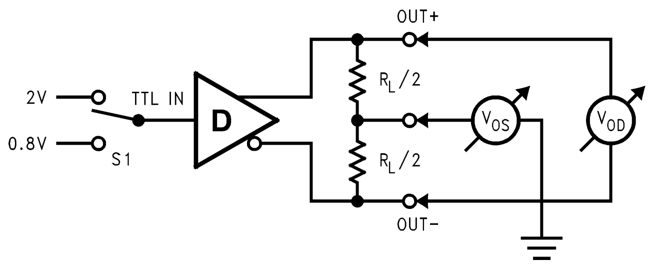


图 7-1. Differential Driver DC Test Circuit

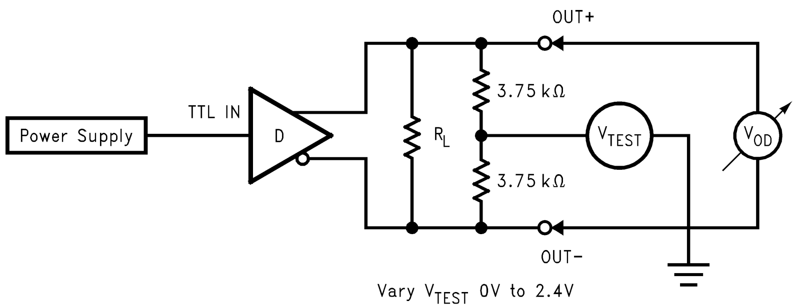


图 7-2. Differential Driver Full Load DC Test Circuit

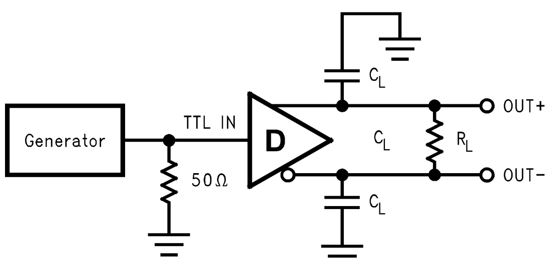


图 7-3. Differential Driver Propagation Delay and Transition Time Test Circuit

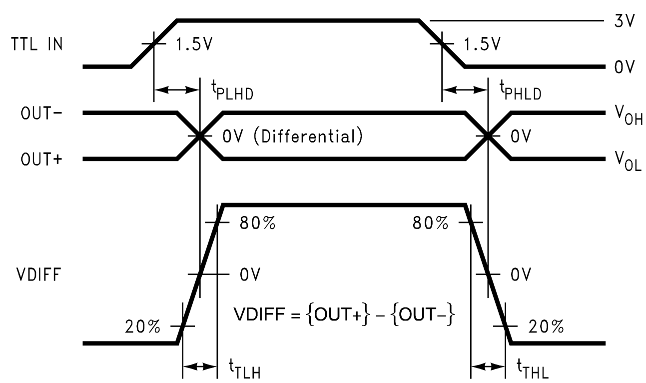


图 7-4. Differential Driver Propagation Delay and Transition Time Waveforms

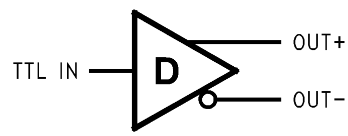
8 Detailed Description

8.1 Overview

The DS90LV011AH is a single-channel, low-voltage differential signaling (LVDS) line driver with a balanced current source design. It operates from a single supply that is nominally 3.3 V, but can be as low as 3.0 V and as high as 3.6 V. The input signal to the DS90LV011AH is an LVCMOS/LVTTL signal. The output of the device is a differential signal complying with the LVDS standard (TIA/EIA-644). The differential output signal operates with a signal level of 350 mV, nominally, at a common-mode voltage of 1.2 V. This low differential output voltage results in low electromagnetic interference (EMI). The differential nature of the output provides immunity to common-mode coupled signals that the driven signal may experience.

The DS90LV011AH is primarily used in point-to-point configurations, as seen in 图 9-1. This configuration provides a clean signaling environment for the fast edge rates of the DS90LV011AH and other LVDS drivers. The DS90LV011AH is connected through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces to a LVDS receiver. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. The DS90LV011AH device is intended to drive a 100-Ω transmission line. The 100-Ω termination resistor is selected to match the media and is located as close to the LVDS receiver input pins as possible.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DS90LV011AH Driver Functionality

As can be seen in 表 8-1, the driver signle-ended input to differential output relationship is defined. When the driver input is left open, the differential output is undefined.

表 8-1. DS90LV011AH Driver Functionality

INPUT	OUTPUTS	
LVCMOS/LVTTL IN	**OUT +**	**OUT -**
H	H	L
L	L	H
Open	?	?

8.3.2 Driver Output Voltage and Power-On Reset

The DS90LV011AH driver operates and meets all the specified performance requirements for supply voltages in the range of 3.0 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry set the driver output to a high-impedance state.

8.3.3 Driver Offset

An LVDS-compliant driver is required to maintain the common-mode output voltage at 1.2 V (±75 mV). The DS90LV011AH incorporates sense circuitry and a control loop to source common-mode current and keep the output signal within specified values. Further, the device maintains the output common-mode voltage at this set point over the full 3.0-V to 3.6-V supply range.

8.4 Device Functional Modes

The device has one mode of operation that applies when operated within 节 *6.3*.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The DS90LV011AH device is a single-channel LVDS driver. The functionality of this device is simple, yet extremely flexible, leading to its use in designs ranging from wireless base stations to desktop computers. The varied class of potential applications share features and applications discussed in the paragraphs below. The DS90LV011AH has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

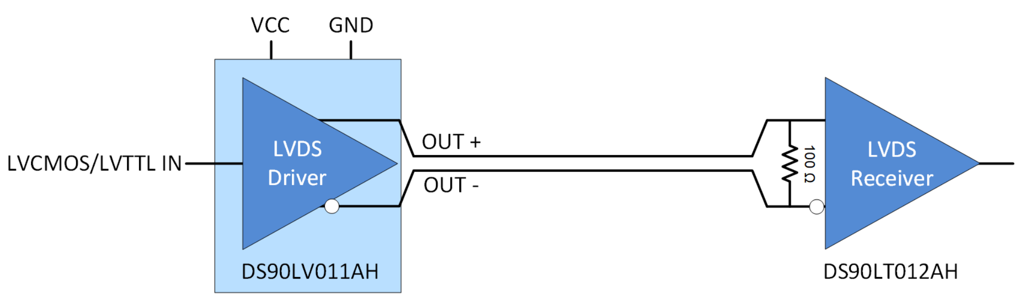


图 9-1. Point-to-Point Application

9.2.1 Design Requirements

表 9-1 lists the design parameters for this example

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{DD})	3 to 3.6 V
Driver Input Voltage	0 to V_{DD}
Signaling Rate	0 to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Number of Receiver Nodes	1
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Driver Supply Voltage

DS90LV011AH is a LVDS that is operated from a single supply. The device can support operation with a supply as low as 3.0 V and as high as 3.6 V. The driver output voltage is dependent upon the chosen supply voltage. The minimum output voltage stays within the specified LVDS limits (247 mV to 450 mV) for a 3.3-V supply. If the supply range is between 3.0 V and 3.6 V, the minimum output voltage may be as low as 150 mV. If a communication link is designed to operate with a supply within this lower range, the channel noise margin will need to be looked at carefully to ensure error-free operation.

9.2.2.2 Driver Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. Specifically, they create low-impedance paths between power and ground. At low frequencies, a good digital power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is quite often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board-level do a good job up into the kHz range. Due to their size and length of their leads, they tend to have large inductance values at the switching frequencies of modern digital circuitry. To solve this problem, one must resort to the use of smaller capacitors (nF to μF range) installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with LVDS chips can be determined by 方程式 1 and 方程式 2 according to Johnson[1] equations 8.18 to 8.21. A conservative rise time of 200 ps and a worst-case change in supply current of 1 A covers the whole range of LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 200 mV. However, this figure varies depending on the noise budget available in the design. [1]

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \tag{1}$$

$$C_{LVDS} = \left(\frac{1A}{0.2V} \right) \times 200\ \text{ps} = 0.001\ \mu F \tag{2}$$

图 9-2 lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.001 μF). TI recommends that the user place the smallest value of capacitance as close to the chip as possible.

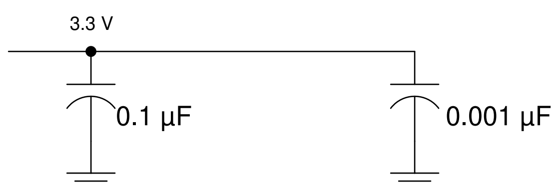


图 9-2. Recommended LVDS Bypass Capacitor Layout

9.2.2.3 Driver Input Votlage

DS90LV011AH input is designed to support a wide input voltage range. The input stage can accept signals as high as 3.6 V when the supply voltage is 3.6 V.

9.2.2.4 Driver Output Voltage

DS90LV011AH driver output has a 1.2-V common-mode voltage, with a nominal differential output signal of 350 mV. This 350 mV is the absolute value of the differential swing (VOD = |V+ – V–|). The peak-to-peak differential voltage is twice this value, or 700 mV. LVDS receiver thresholds are ±100 mV. With these receiver decision thresholds, it is clear that the disadvantage of operating the driver with a lower supply will be noise margin. With fully compliant LVDS drivers and receivers, we would expect a minimum of ~150 mV of noise margin (247-mV minimum output voltage – 100-mV maximum input requirement). If we operate the DS90LV011AH with a supply in the range of 3.0 V to 3.6 V, the minimum noise margin will drop to 150 mV.

[1] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.

9.2.2.5 Interconnecting Media

The physical communication channel between the driver and the driver may be any balanced and paired metal conductors meeting the requirements of the LVDS standard, the key points of which are included here. This media may be a twisted-pair, twinax, flat ribbon cable, or PCB traces. The nominal characteristic impedance of the interconnect media should be between 100 Ω and 120 Ω with a variation of no more than 10% (90 Ω to 132 Ω).

9.2.2.6 PCB Transmission Lines

As per the *LVDS Owner's Manual Design Guide, 4th Edition*, 图 9-3 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and return path with a uniform cross section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. 图 9-3 shows examples of edge-coupled microstrip lines, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, S is less than 2 W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

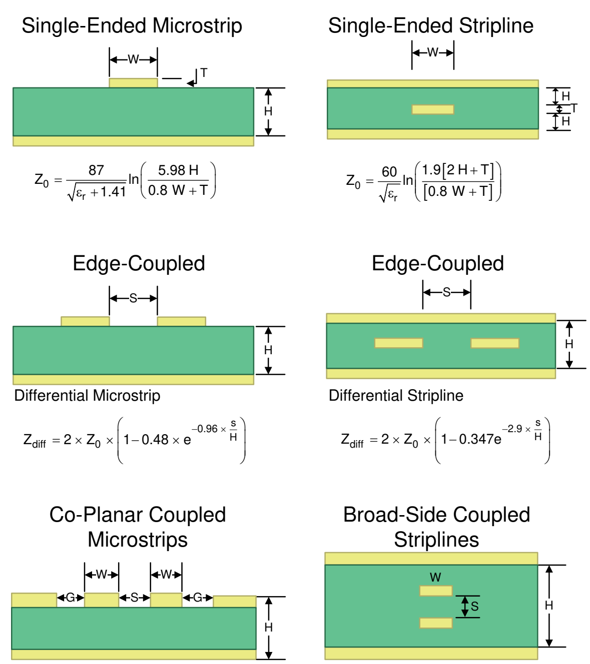


图 9-3. Controlled-Impedance Transmission Lines

9.2.3 Termination Resistor

As shown earlier, an LVDS communication channel employs a current source driving a transmission line that is terminated with a resistive load. This load serves to convert the transmitted current into a voltage at the receiver input. To ensure incident wave switching (which is necessary to operate the channel at the highest signaling rate), the termination resistance should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistance is within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistance should be between 90 Ω and 110 Ω. The line termination resistance should be placed as close to the receiver as possible to minimize the stub length from the resistor to the receiver.

9.2.4 Application Curve

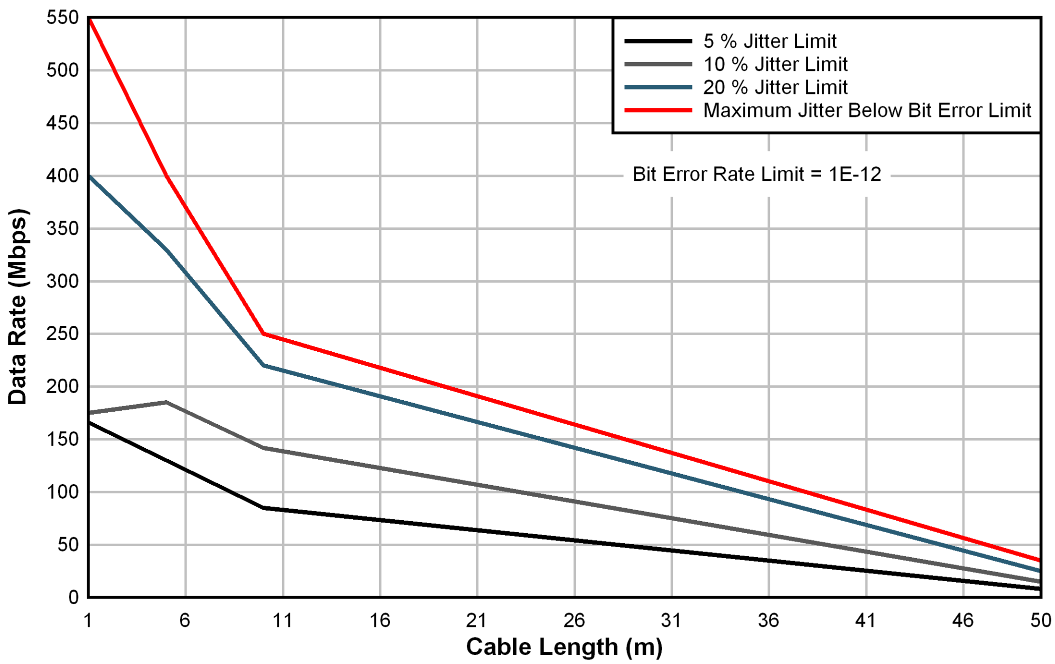


图 9-4. DS90LV011AH Performance: Data Rate vs Cable Length

10 Power Supply Recommendations

The DS90LV011AH driver is designed to operate from a single power supply with supply voltage in the range of 3.0 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the driver power supply would be less than |±1 V|. Board level and local device level bypass capacitance should be used.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per the *LVDS Application and Data Handbook*, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 图 11-1.

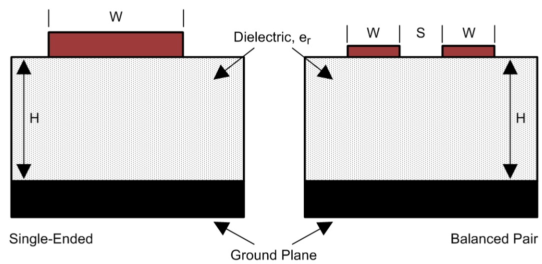


图 11-1. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing LVDS signals on microstrip transmission lines when possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[2], 2[3], and 3[4] provide formulas for Z_O and t_{PD} for differential and single-ended traces. [2] [3] [4]

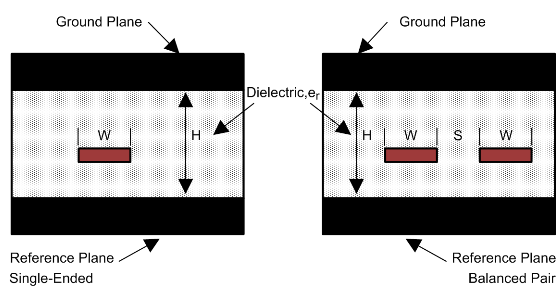


图 11-2. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with LVDS signals. If rise or fall times of LVCMOS/LVTTL signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 µm or 0.0003 in (minimum).
- Copper plating should be 25.4 µm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

[2] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
[3] Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
[4] Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, the designer must decide how many levels to use in the stack. To reduce the LVCMOS/LVTTL to LVDS crosstalk, it is good practice to have at least two separate signal planes as shown in 图 11-3.

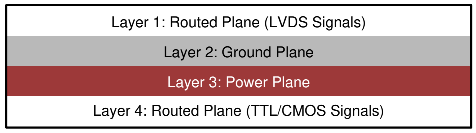


图 11-3. Four-Layer PCB Board

Note

The separation between layers 2 and 3 should be 127 µm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 图 11-4.

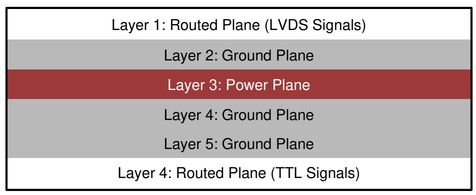


图 11-4. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity, but fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors, but the amount of coupling that can be tolerated usually dictates the actual separation. Low-noise coupling requires close coupling between the differential pair of an LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

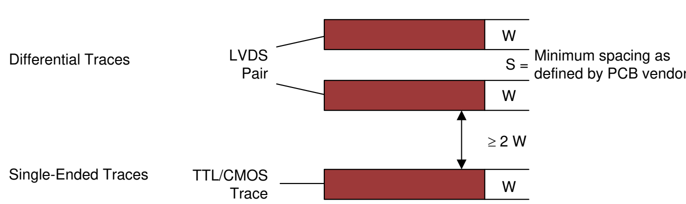


图 11-5. 3-W Rule for Single-Ended and Differential Traces (Top View)

Exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close to its originating trace as possible. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. TI recommends placing a via immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

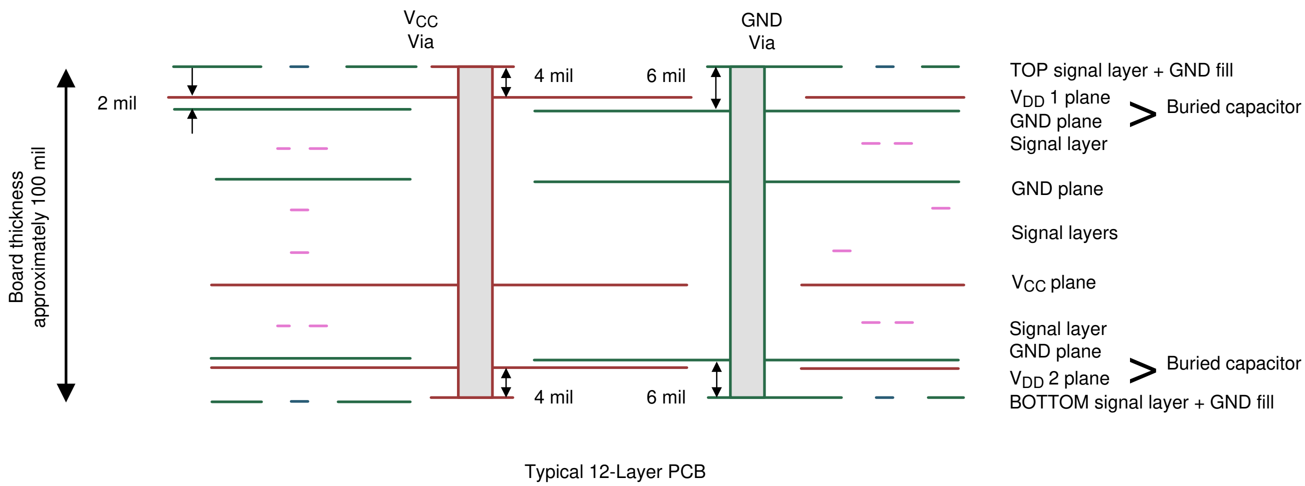


图 11-6. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402 or even 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in 图 11-7(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 µF, and 0.1 µF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Refer back to Figure 8 for some examples. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center dap must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the dap connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in 图 9-3) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature.

Multiple paths for heat transfer minimize this possibility. In many cases the GND dap that is so important for heat dissipation makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-dap spacing as shown in 图 11-7(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.

图 11-7. Typical Decoupling Capacitor Layouts

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 图 11-8.

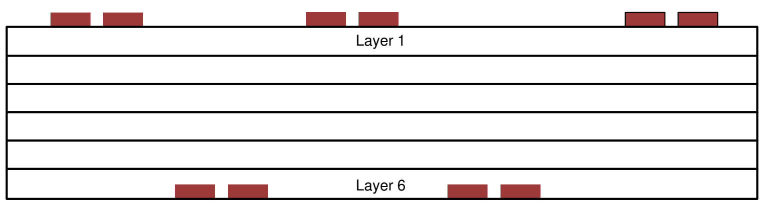


图 11-8. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers. Thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 图 11-9. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

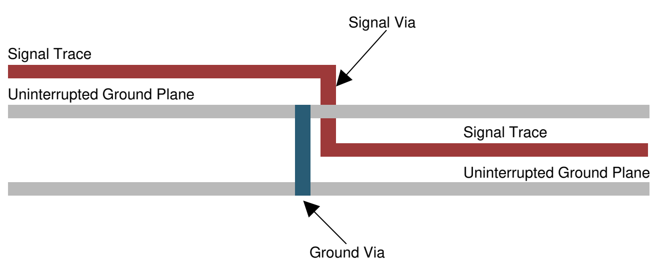


图 11-9. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

11.2 Layout Example

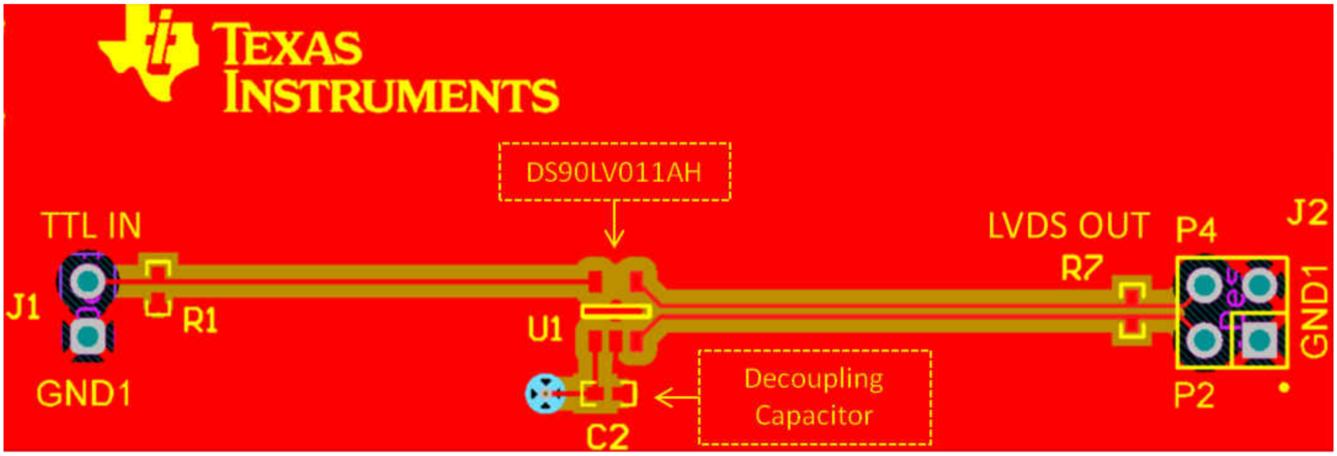


图 11-10. Example DS90LV011AH Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LVDS Owner's Manual* dseign guide
- Texas Instruments, *AN-808 Long Transmission Lines and Data Signal Quality* application note
- Texas Instruments, *AN-977 LVDS Signal Quality: Jitter Measurements Using Eye Patterns Test Report #1* application note
- Texas Instruments, *AN-971 An Overview of LVDS Technology* application note
- Texas Instruments, *AN-916 A Practical Guide to Cable Selection* application note
- Texas Instruments, *AN-805 Calculating Power Dissipation for Differential Line Drivers* application note
- Texas Instruments, *AN-903 A Comparison of Differential Termination Techniques* application note
- Texas Instruments, *AN-1194 Failsafe Biasing of LVDS Interfaces* application note

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV011AHMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	N04	Samples
DS90LV011AHMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	N04	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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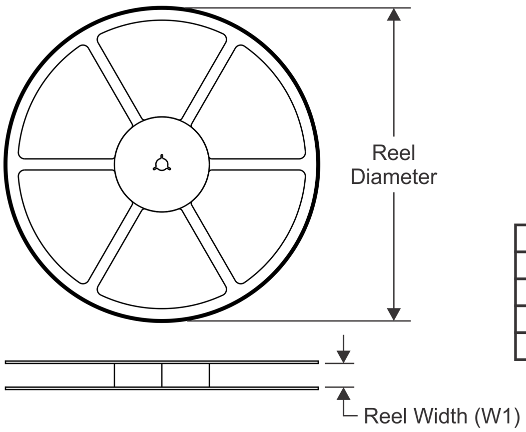
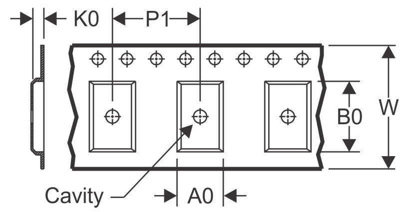
TAPE AND REEL INFORMATION

REEL DIMENSIONS

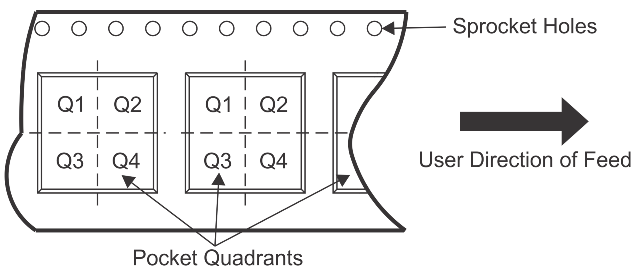


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

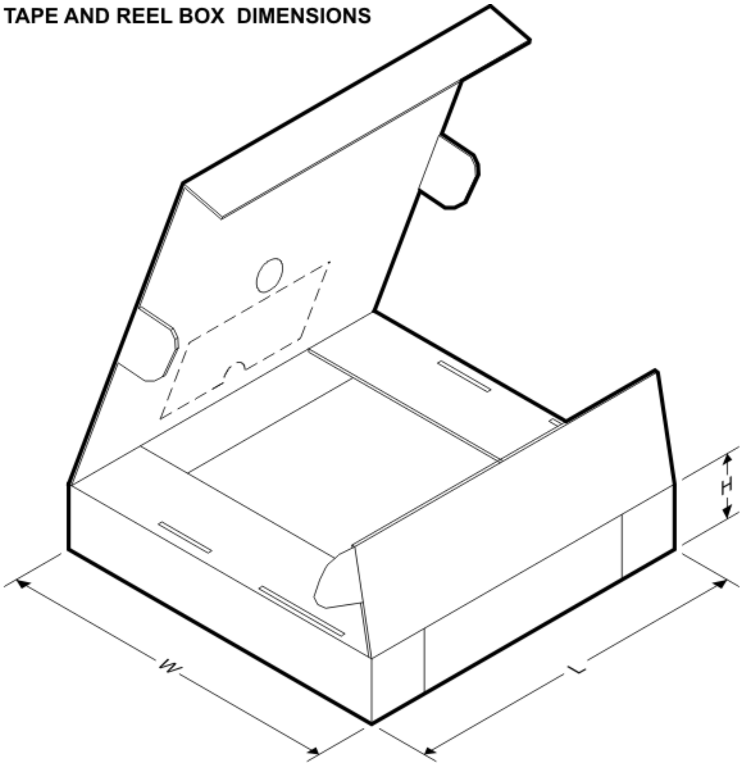
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

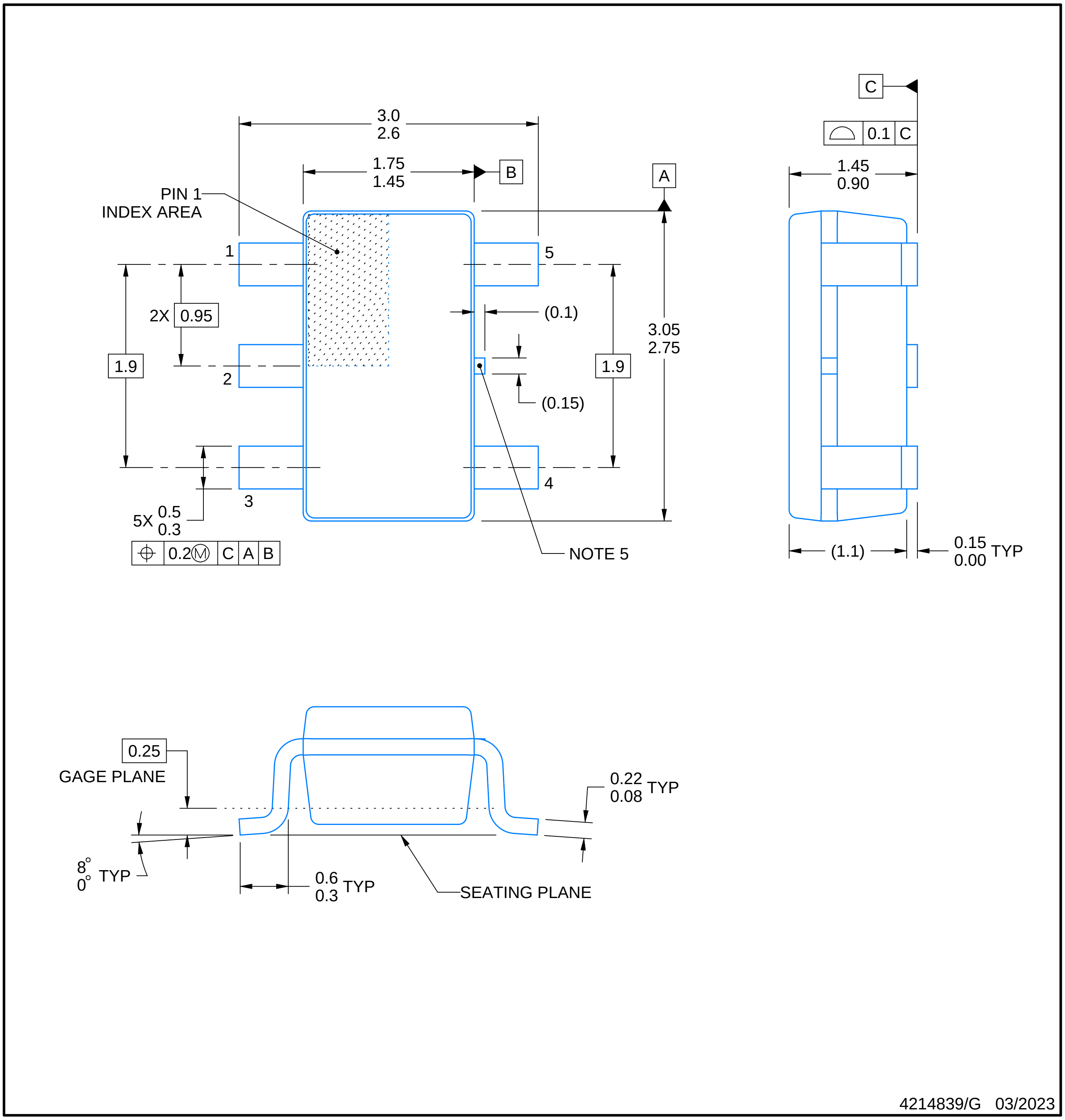
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV011AHMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DS90LV011AHMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV011AHMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
DS90LV011AHMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0



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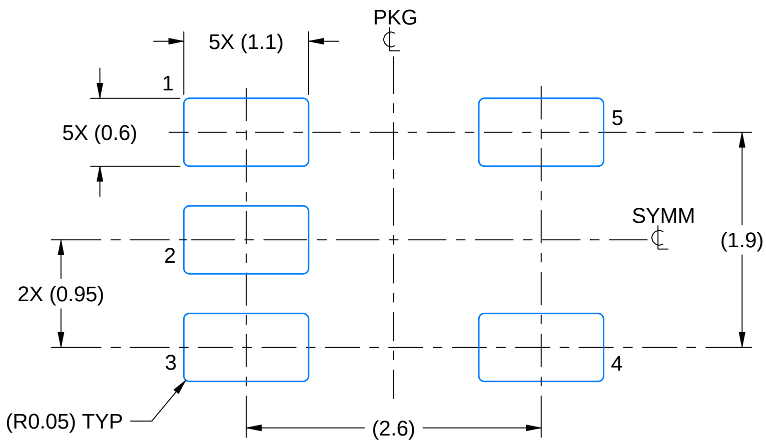
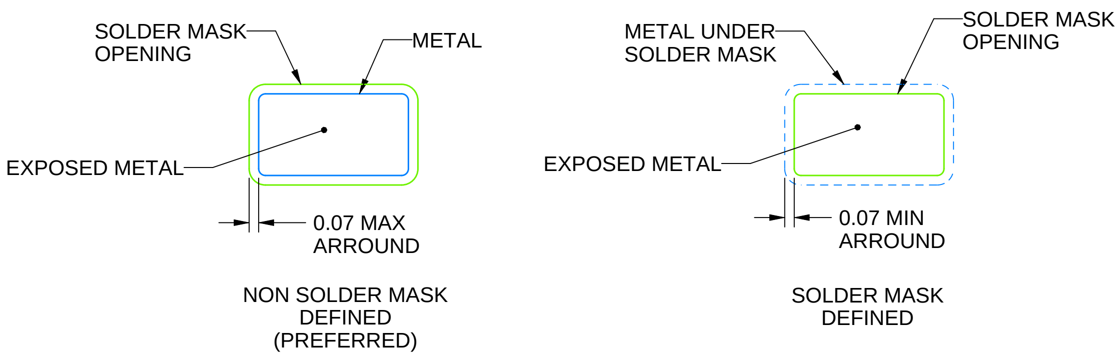
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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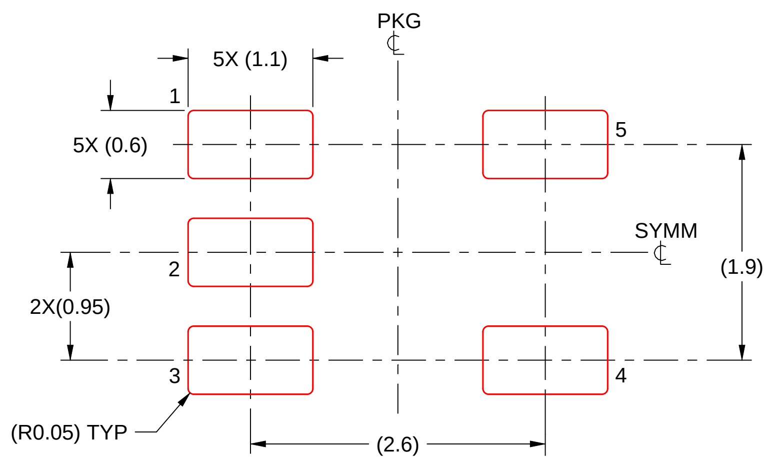
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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